

Titan S10 SOM



Hardware Manual

FPGA

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Chapter 1

Overview

This chapter provides an overview of the Titan S10 SoM Board and installation guide.

1.1 General Description

The Titan S10 SOM is a compact, production-ready FPGA module built on the Altera's Stratix® 10 SoC with 1.1M logic elements, purpose-built for compute-intensive embedded applications. Measuring just 98mm × 86mm, the SOM integrates dual 64-bit 4GB DDR4 memory, USB 3.1, and high-speed transceivers up to 12.5Gbps. This high-performance SOM is available in FMC and FMC+ interface versions, allowing customers the option to choose the configuration that best fits their system I/O requirements.

Designed for performance and versatility, the SOM offers up to a dedicated 64-bit quad-core ARM HPS subsystem with onboard eMMC storage, dual Gigabit Ethernet PHYs, and a USB-UART interface—enabling seamless hardware acceleration alongside embedded software programmability. A full featured, cost-effective SOM development kit is available for initial evaluation and early system development.



Figure 1-1 Titan S10 SOM

1.2 Board Layout

The figures below depict the layout of the board and indicate the location of the connectors and key components.

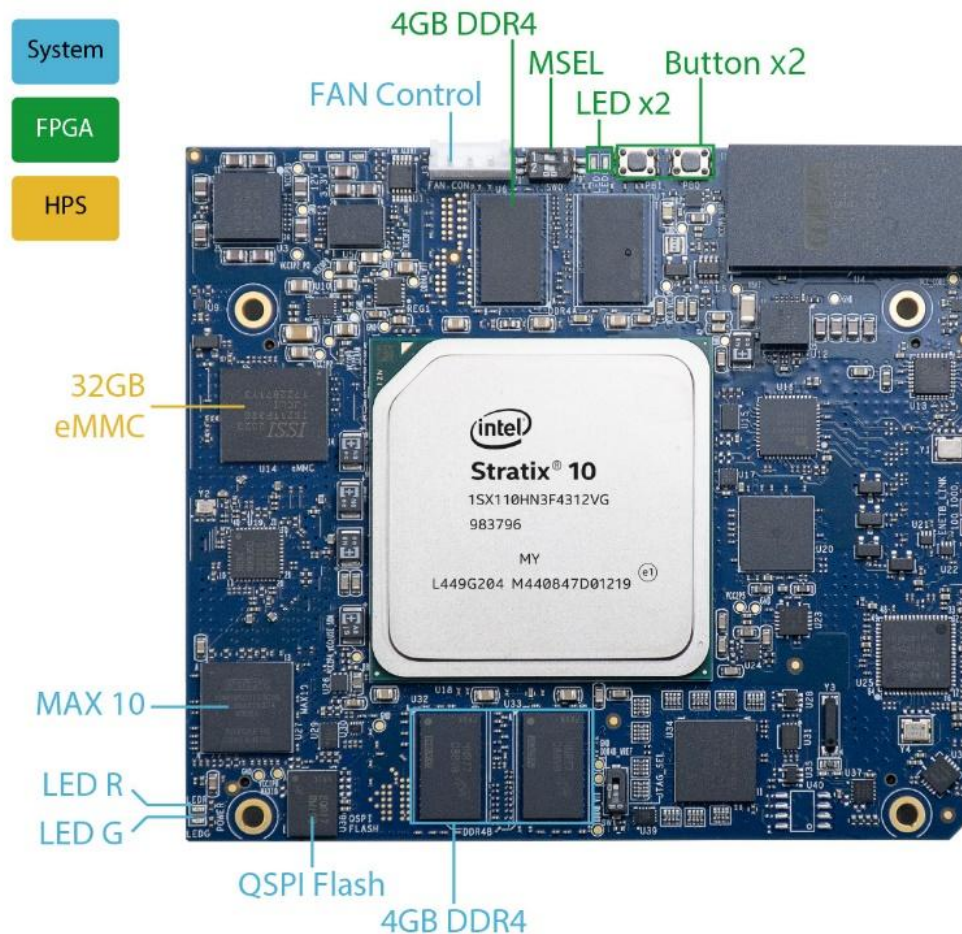


Figure 1-2 Titan S10 SOM top

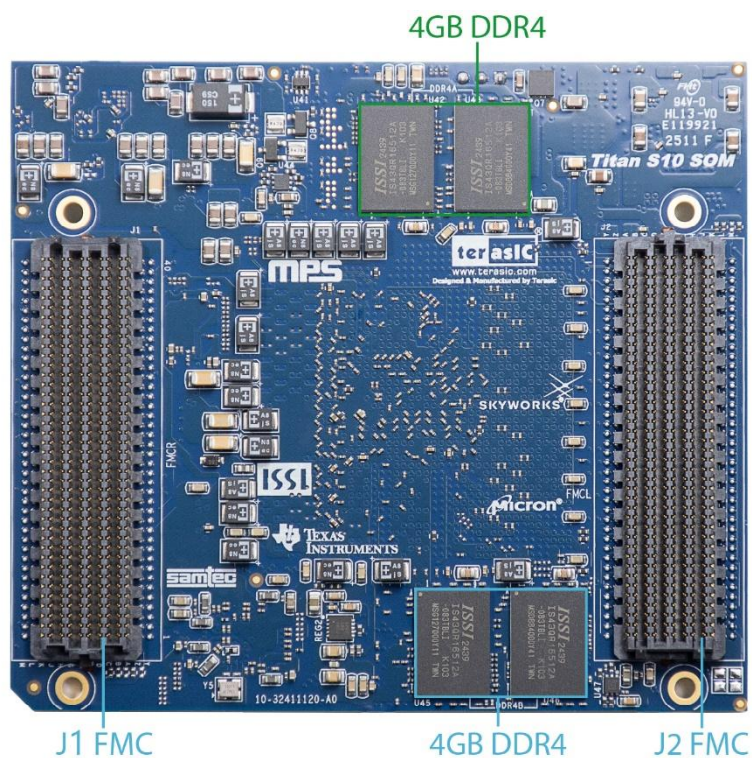
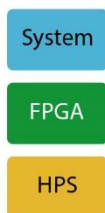


Figure 1-3 Titan S10 SOM bottom (FMC version)

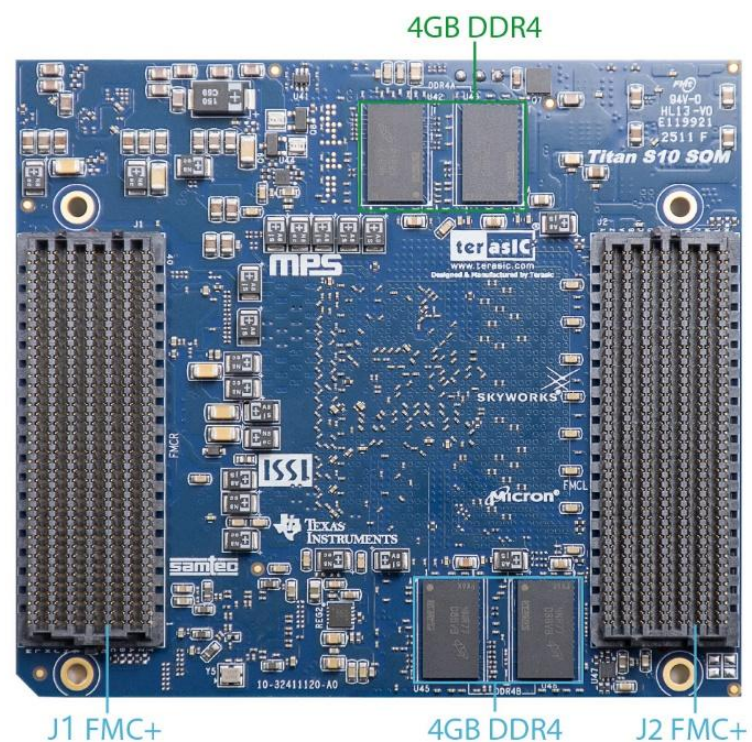
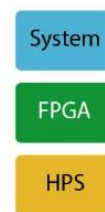


Figure 1-4 Titan S10 SOM bottom (FMC+ version)

1.3 Key Features

The following hardware is implemented on the Titan S10 SOM:

■ FPGA Device

- Altera Stratix 10 FPGA: 1SX110HN3F43I2V
 - 1100K logic elements (LEs)
 - 107 Mbits embedded memory(M20K)
 - 5184 18-bit x 19-bit multipliers

■ System

- Module Size : 98mm x 86mm
- ASx4 Mode with 512Mb QSPI Flash
- Board Management System
- Active Heatsink (12V Fan)
- Power by 12V via FMC+ Connector

■ FPGA Side

- LED x2, KEY x2, SW x2, Fixed 25 /100MHz clock
- Programmer clock generator Si5341 for XCVR REFCK
- 64-bit 4GB DDR4
- 154 LVDS connected to FMC+ (114 LVDS for FMC Edition)
- 32 XCVR TX/RX connected to FMC+. Up to 12.5Gbps per channel. (2 4 XCVR TX/RX for FMC Edition)
- USB 3.1 (Cypress FX3)
- Gigabit Ethernet PHY, co-working with HPS

■ HPS(Hard Processor System) Side

- 64-bit 4GB DDR4 (can share with FPGA)

- UART, GPIO x2, Gigabit Ethernet PHY x1, USB PHY x1
- 32GB eMMC
- RTC, Temperature Sensor and EEPROM

1.3. Block Diagram

Figure 1-5 shows the block diagram of the Titan S10 SOM. To provide maximum flexibility for the users, all key components are connected to the Stratix 10 SoC FPGA device. Thus, users can configure the FPGA to implement any system design.

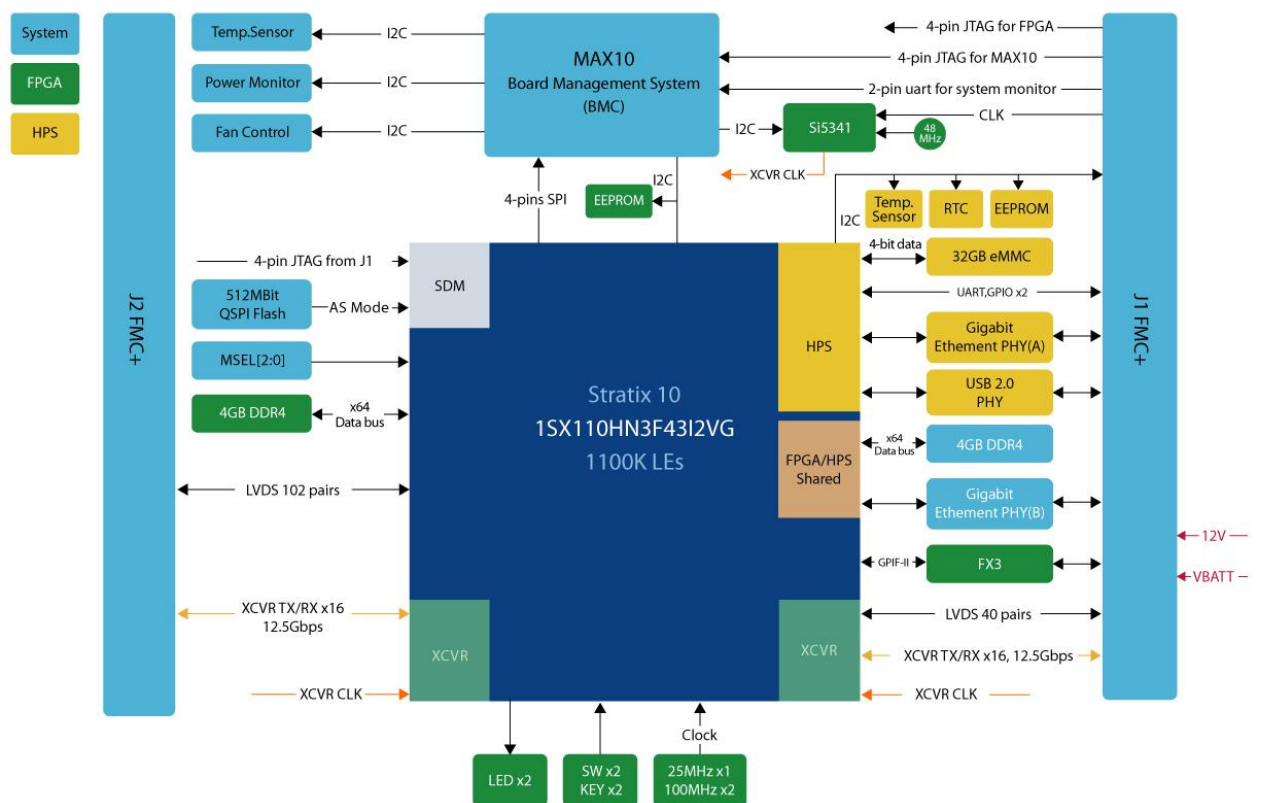


Figure 1-5 Block diagram of the Titan S10 SOM

1.4. Mechanical Specifications

Figure 1-6 shows the Mechanical Layout of Titan S10 SOM. The unit of the Mechanical Layout is millimeter (mm).

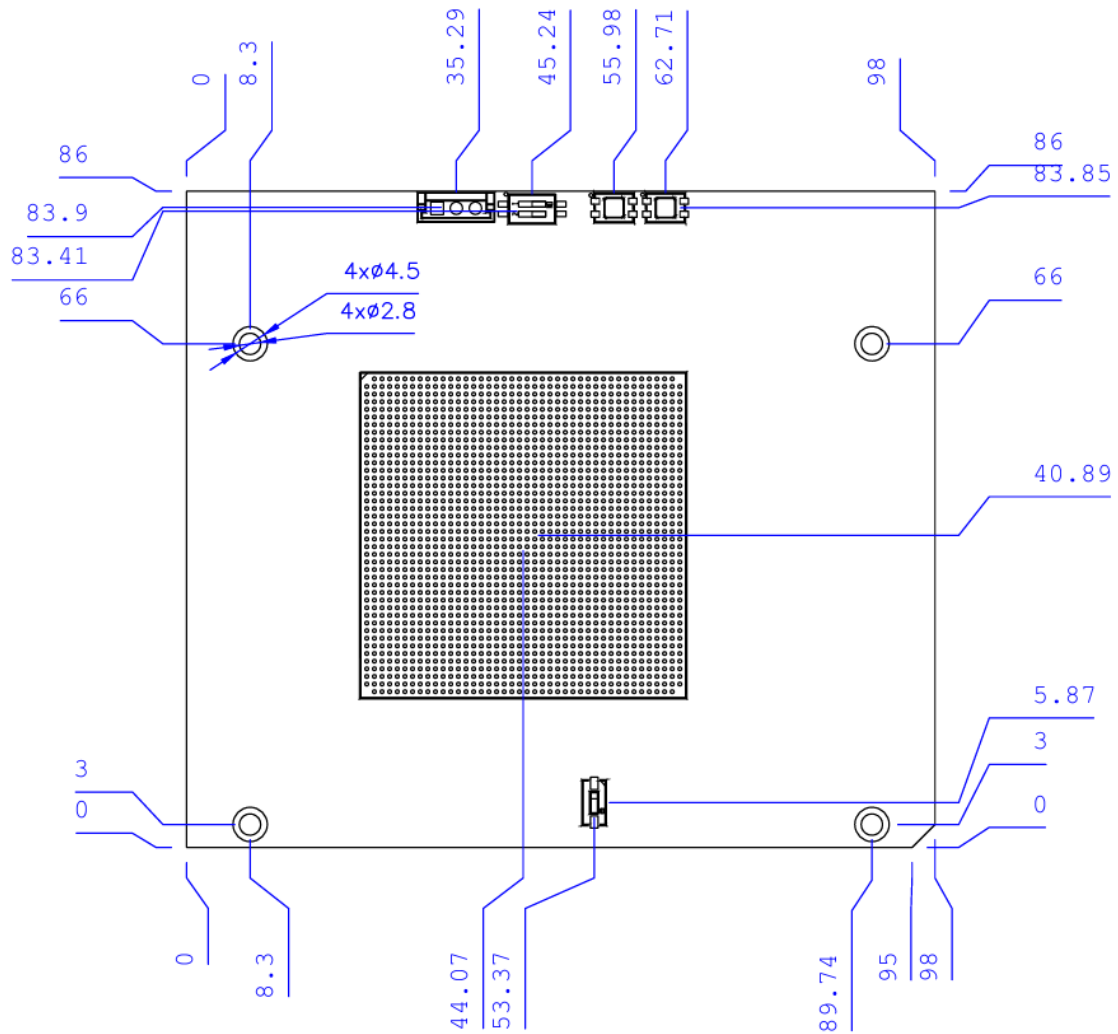


Figure 1-6 Mechanical layout (Top View)

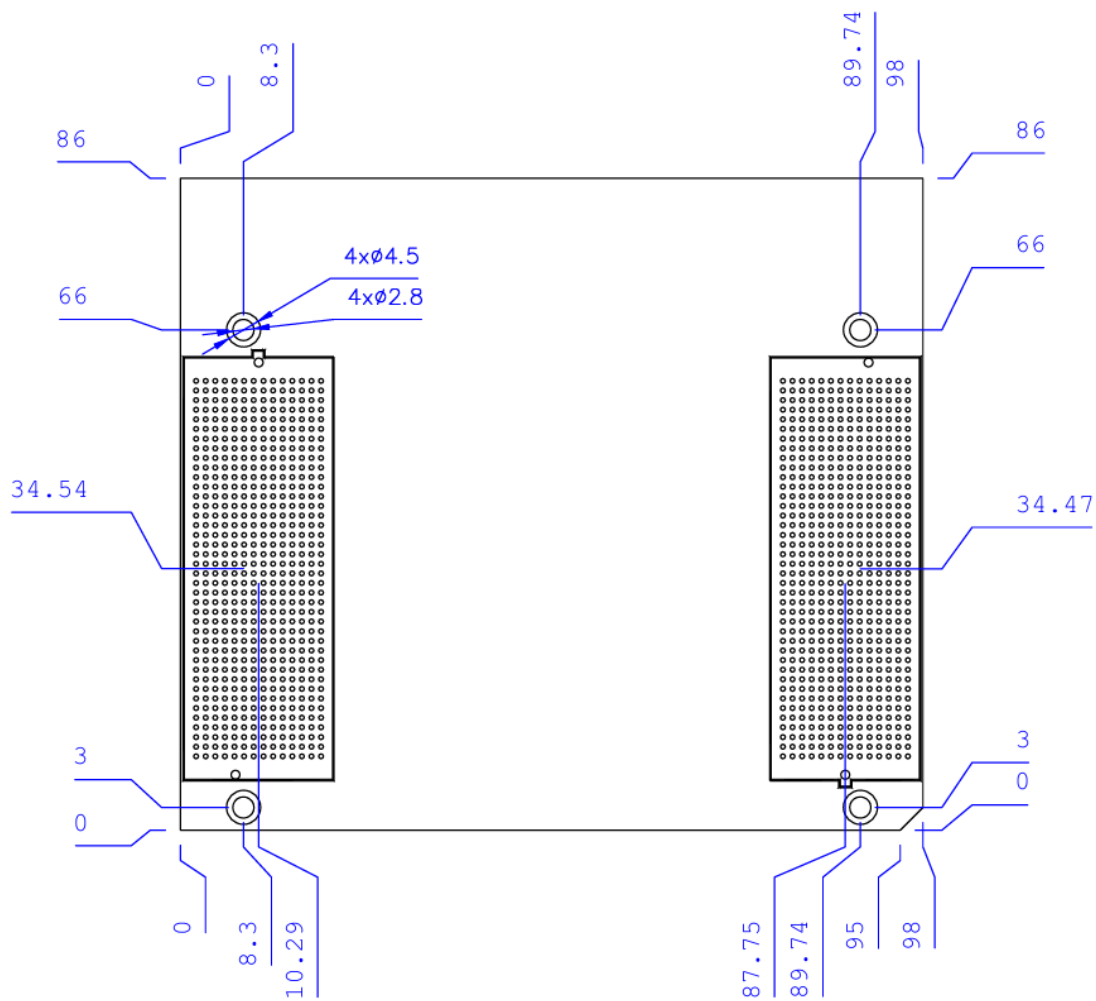


Figure 1-7 Mechanical layout (Bottom view)

1.5. Power Requirement

■ Power Consumption

Table 1-1 presents Titan S10 SOM power consumption.

Table 1-1 Power Consumption the Titan S10 SOM

Status	Power Consumption
Typical	50W
Maximum	100W

■ Power Input for the SOM

The Titan S10 SOM board receives 12V power from the carrier board via the FMCR

(J1) connector. **Table 1-2** lists the 12 power pins used.

Table 1-2 12V Power pin in FMCR Connector

Number	Signal Name in FMC Specification	FMCR (J1) Pin Number	Titan S10 SOM Schematic
1	12P0V	C35	VCC12
2	12P0V	C37	
3	3P3V	C39	
4	GA1	D35	
5	3P3V	D40	
6	VADJ	E39	
7	VADJ	F40	
8	VADJ	G39	
9	VADJ	H40	
10	VIO_B_M2C	J39	

1.6. Connectivity

The Titan S10 SOM offers FMC or FMC+ connectors for expansion. Through the FMC+/FMC connector, users can interface with the carrier board (see **Figure 1-8**) to access power delivery and multiple expansion interfaces, including USB Blaster programming, communication links, multimedia outputs, and memory peripherals.

If user wants to make their owned carrier board to connect with the Titan S10 SOM, The following table (**Table 1-3**) lists the manufacturer and manufacturer part numbers of the FMC+/FMC connector that can match with the connector of the Titan S10 SOM



Figure 1-8 Titan S10 SOM connects to the carrier board

Table 1-3 Part Number of the connector on the Titan S10 SOM

Connector	Titan S10 SOM's Part Number	Carrier Board's Part Number
FMC+	J1/J2 Samtec : ASP-188588-01	Samtec : ASP-184329-01
FMC	J1/J2 Samtec : ASP-134602-01	Samtec : ASP-134485-01

Chapter 2

Board Component

This chapter introduces all the important components on the Titan S10.

2.1 Configuration Interface

The FPGA on the Titan S10 board can use two configuration modes: JTAG and Active Serial (AS). Below, we will describe these two modes in detail:

■ JTAG Programming mode

JTAG configuration mode is one of the most common methods for programming an FPGA during development. In this mode, a configuration file with the extension .sof (SRAM Object File) is downloaded to the FPGA via a JTAG programming circuit. However, because the .sof file is loaded into the FPGA's volatile SRAM, the configuration is lost when power is turned off. As a result, the FPGA must be reprogrammed each time it is powered on.

Note 1: The Titan S10 board does not include an onboard USB Blaster circuit. Users must either provide a USB Blaster circuit or other JTAG programming interface on the carrier board.

Note 2: The Titan S10 SOM features two FPGA devices: Stratix 10 and MAX 10. The JTAG buses of both devices are switched through a multiplexer and share a common path routed to the carrier board via the FMC+ connector. Users must configure a switch to select whether the JTAG bus of the Stratix 10 or the MAX 10 is connected to the carrier board. The default setting is the JTAG bus of the Stratix 10 FPGA connected to the FMC+ connector.

■ Active Serial Fast mode

The Active Serial Fast (AS fast) mode is a non-volatile configuration scheme for altera FPGAs, utilizing an external Quad SPI (QSPI) Flash memory to store the configuration bitstream. Upon power-up, the FPGA autonomously reads this configuration data from the QSPI Flash, enabling self-contained device initialization. Because the configuration persists across power cycles, the AS fast mode is well-suited for applications demanding reliable, standalone operation without requiring configuration by an external host after initial programming.

Figure 2-1 shows the JTAG interface and configuration device of the Titan S10 SOM.

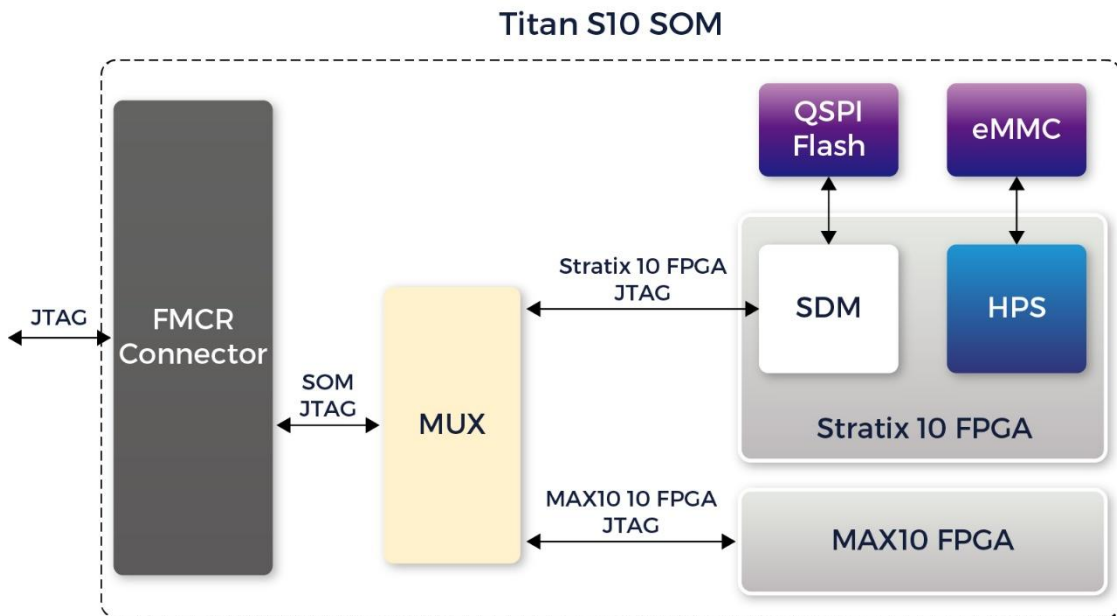


Figure 2-1 Block diagram of the JTAG interface and configuration for the board

The following content will introduce the HPS boot process within the SoC FPGA.

■ SoC FPGA boot

The boot process for Stratix 10 SoC FPGAs can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and

FPGA fabric after powering on. More details can be found in the user documentation: [Intel Stratix 10 SoC FPGA Boot User Guide](#).

The factory setting of the SoC boot of the Titan S10 board is the **HPS Boot First Mode**. The architecture is shown in the **Figure 2-2**. Two storage mediums are used. The system needs QSPI flash on Titan S10 as SDM flash for booting.

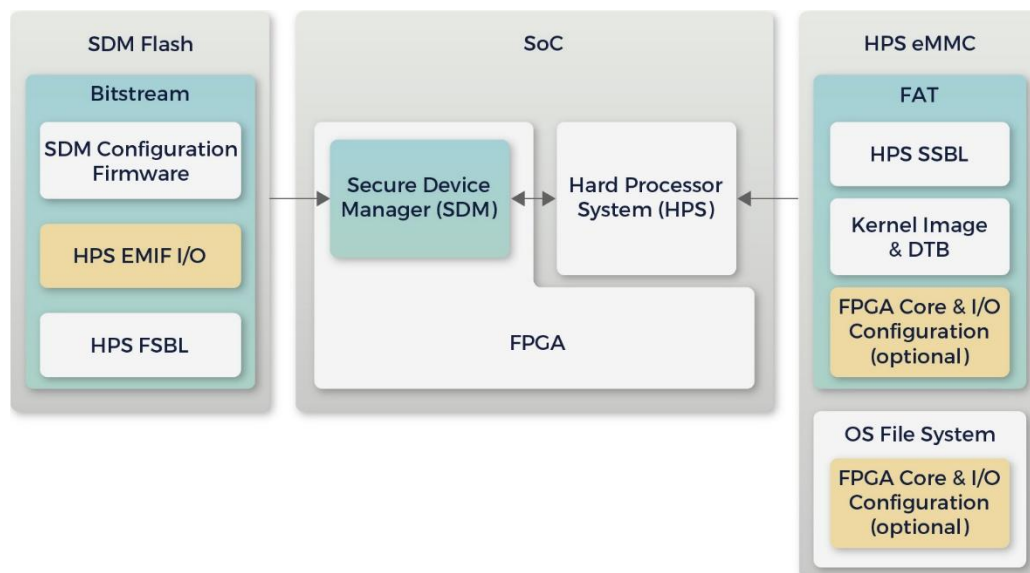


Figure 2-2 HPS boot First Dual SDM and HPS Flash

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the eMMC flash with built-in image data as HPS flash, which is used for HPS boot in the later part. The eMMC flash stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Titan S10 is summarized as follows:

When the Titan S10 board is powered on, the SDM will read the configuration firmware and complete SDM initial form the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the eMMC flash into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

2.2 Setup and Status Components

This section will introduce the use of the switch for setup on the Titan S10 board, as well as a description of the various status LEDs.

■ Status LED

The FPGA development board includes board-specific status LEDs to indicate board status. Please refer to **Table 2-1** for the description of the LED indicators. **Figure 2-3** shows the location of all these status LED.

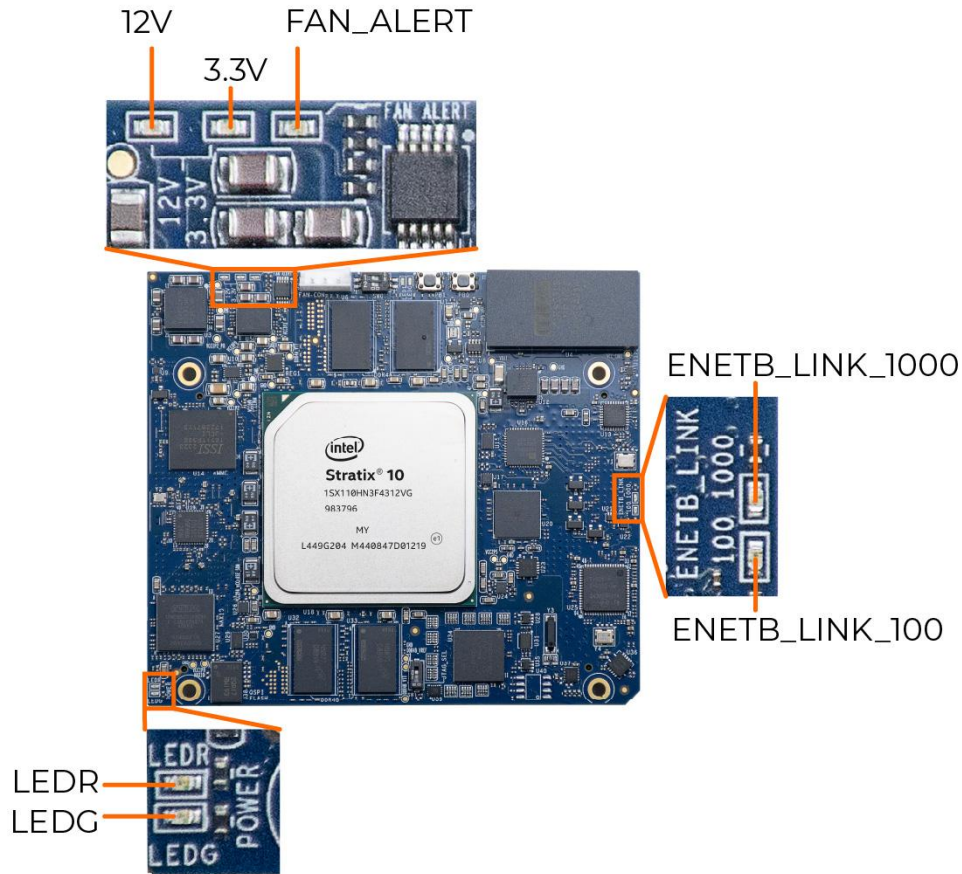


Figure 2-3 Position of the status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
D1	12V	Illuminates when 12-V power is active.
D2	3.3V	Illuminates when 3.3-V power is active.
D3	FAN_ALERT	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
D4	ENETB_LINK1000	LED_LINK1000 pin of the Ethernet Port B (88E1111 PHY)
D5	ENETB_LINK100	LED_LINK100 pin of the Ethernet Port B(88E1111 PHY)
D6	LEDG	Illuminates when the 3.3V power good and power sequence process finished.
D7	LEDR	1. Illuminates when the 3.3V power abnormal or

		<p>power sequence process failed.</p> <p>2. LED will blink when the following situations occur: (i) the FPGA temperature on the board temperature exceeds 95 degrees. (ii) the power consumption exceeds 160W. (iii) when the current of VCC_CORE exceeds 100A. Also, all the power of the FPGA will be cut off when this LED is blinking.</p>
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■ JTAG Chain Select Switch

This switch (SW1) can be used to select whether the Stratix 10 FPGA or the MAX 10 FPGA JTAG bus is connected to the FMC connector (See [Figure 2-4](#)). This allows the user to choose which FPGA to program from the carrier board via the JTAG bus. The switch is connected to the Stratix 10 FPGA by default.

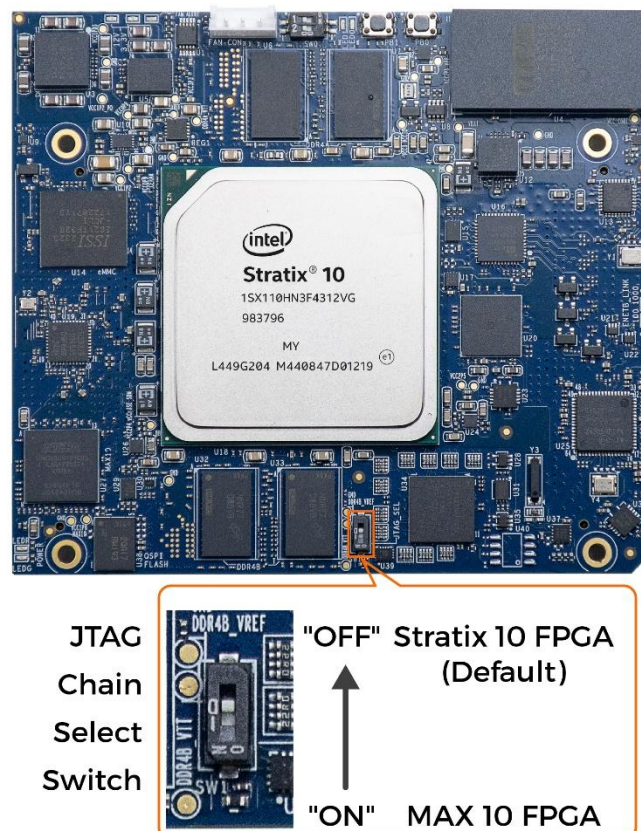


Figure 2-4 Position of slide switches SW3

Table 2-2 SW1 setting

Board Reference	Signal Name	Description	Default
SW1	JTAG_SEL	ON: Connects MAX 10 FPGA JTAG to FMCR connector OFF: Connects Stratix 10 FPGA JTAG to FMCR connector	OFF

2.3 Clock Circuit

Figure 2-5 shows the clock tree of the Titan S10 SOM board.

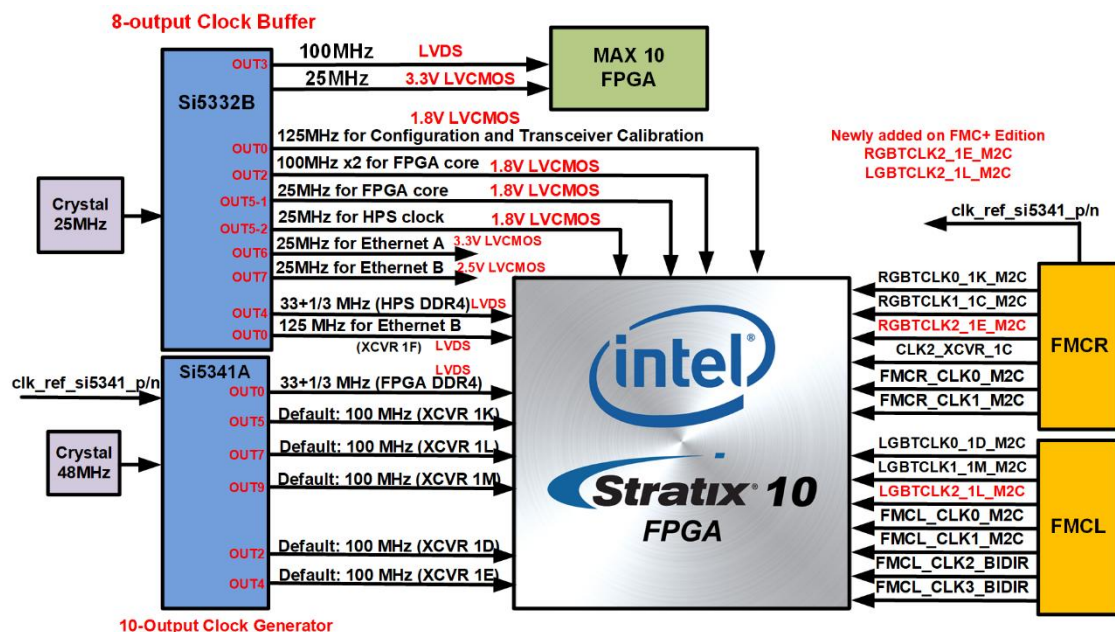


Figure 2-5 Clock tree of the FPGA Board

The primary clock sources on the board are provided by two programmable PLL clock generators (**Si5332B** and **Si5341A**).

The **Si5332B** mainly provides reference clocks for the FPGA core, HPS, two Ethernet

PHYs, and HPS DDR4. The **SI5341** mainly serves as the reference clock for transceiver applications and DDR4B.

Table 2-3 and **Table 2-4** list the clock pin assignments and default frequency for the **Si5332B** and **SI5341**, respectively.

Table 2-3 Clock Pin Assignments of the Si5332B

Clock Output Port	Schematic Signal Name	Default Frequency	I/O Standard	Connected to	Application
OUT0	ENETB_REFCLK_p	125 MHz	LVDS	Stratix 10 PIN_AD34	(Ethernet PHY 88E1111) Transmit signal reference clock for FPGA
OUT0B	ENETB_REFCLK_n		LVDS	Stratix 10 PIN_AD33	
OUT1	OSC_CLK_1	125Mhz	-	Stratix 10 PIN_AY9	User-supplied configuration clock
OUT1B	-	-	-	-	-
OUT2	CLK_100_B3A	100Mhz	1.8V	Stratix 10 PIN_AV8	User application
OUT2B	CLK_100_B3L			Stratix 10 PIN_B2	User application
OUT3	CLK_100_MAX10_p	100MHz	LVDS	MAX 10 PIN_G9	MAX 10 FPGA reference clock
OUT3B	CLK_100_MAX10_n			MAX 10 PIN_G10	
OUT4	DDR4A_REFCLK_p	33.333MHz	LVDS	Stratix 10 PIN_D27	DDR4A reference clock
OUT4B	DDR4A_REFCLK_n			Stratix 10 PIN_E27	
OUT5	HPS_OSC_CLK	25MHz	1.8V	Stratix 10	HPS

				PIN_E17	Oscillator Clock Input Pin
OUT5B	CLK_25_B3L	25MHz	1.8V	Stratix 10 PIN_B5	User application
OUT6	ENETA_CLK_25	25MHz	3.3V	KSZ9031 PHY	KSZ9031 PHY reference clock
OUT6B	CLK_25_MAX10	25MHz	3.3V	MAX 10 PIN_H6	MAX 10 FPGA Reference clock
OUT7	ENETB_CLK_25	25MHz	2.5V	88E1111 PHY	88E1111 PHY reference clock
OUT7B	-	-	-	-	-

Table 2-4 Clock Pin Assignments of the Si5341A

Clock Output Port	Schematic Signal Name	Default Frequency	I/O Standard	Connected to	Application
OUT0	DDR4B_REFCLK_p	33.333MHz	LVDS	Stratix 10 PIN_AY19	DDR4B reference clock
OUT0B	DDR4B_REFCLK_n			Stratix 10 PIN_AW19	
OUT2	XCVR_REFCLK1M_p	100Mhz	LVDS	Stratix 10 PIN_M34	Reference clock for FPGA transceiver bank 1M
OUT2B	XCVR_REFCLK1M_n			Stratix 10 PIN_M33	
OUT4	XCVR_REFCLK1L_p	100Mhz	LVDS	Stratix 10 PIN_V34	Reference clock for FPGA
OUT4B	XCVR_REFCLK1L_p			Stratix 10	

				PIN_V33	transceiver bank 1L
OUT5	XCVR_REFCLK1K_p	100MHz	LVDS	Stratix 10 PIN_AB34	Reference clock for FPGA transceiver bank 1K
OUT5B	XCVR_REFCLK1K_p			Stratix 10 PIN_AB33	
OUT7	XCVR_REFCLK1E_p	100Mhz	LVDS	Stratix 10 PIN_AH34	Reference clock for FPGA transceiver bank 1E
OUT7B	XCVR_REFCLK1E_p			Stratix 10 PIN_AH33	
OUT9	XCVR_REFCLK1D_p	100Mhz	LVDS	Stratix 10 PIN_AM34	Reference clock for FPGA transceiver bank 1D
OUT9B	XCVR_REFCLK1D_p			Stratix 10 PIN_AM33	

■ Modifying the Output Clock Frequency of the SI5341 Programmable PLL Clock Generator

Upon power-on, the MAX10 FPGA on the Titan S10 SOM board first reads the frequency configuration data stored in the EEPROM. It then configures the SI5341's output frequencies via the I2C interface.

To change the output frequency of the SI5341, users can modify the data in the EEPROM through the FPGA. This enables updating the output frequency as needed. For detailed instructions, please refer to [demonstration_manual.pdf](#).

2.4 General User I/O

This section describes the user I/O interface of the FPGA as shown in [Figure 2-6](#).



Figure 2-6 Position of all the user LEDs/Switches/Buttons

■ User Defined Push-buttons

The FPGA board includes two FPGA user defined push-buttons that allow users to interact with the Stratix 10. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. [Table 2-5](#) lists the board references, signal names and their corresponding Stratix 10 device pin numbers for the push-buttons of the FPGA.

Table 2-5 Push-button Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
PB0	BUTTON0	High Logic Level when the button is not pressed	3.0-V LVTTL	PIN_V31
PB1	BUTTON1		3.0-V LVTTL	PIN_V30

■ User-Defined Dip Switch

There are two positions dip switch (**SW0**) on the FPGA fabric to provide additional FPGA input control. When a position of dip switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Stratix 10 FPGA, respectively.

Table 2-6 lists the signal names and their corresponding Stratix 10 device pin numbers.

Table 2-6 Dip Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
SW0	SW0	High logic level when SW in the UPPER position.	1.2 V	PIN_AT21
SW1	SW1		1.2 V	PIN_AM22

■ User-Defined LEDs

The FPGA board consists of 2 FPGA user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix 10 FPGA. Each LED is driven directly by the FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in **Table 2-7**.

Table 2-7 User LEDs Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
LED0	LED0	Driving a logic 0 on the I/O port turns the LED ON.	1.2 V	PIN_AP21
LED1	LED1	Driving a logic 1 on the I/O port turns the LED OFF.		

2.5 USB 2.0 OTG PHY

The board supports USB 2.0 for HPS fabric via an SMSC USB3300 controller, which connects to the user's USB connector (carrier board) through the FMC connector. It uses a ULPI interface to communicate with the HPS USB controller and supports OTG mode for both Host and Device operations. **Figure 2-7** shows the connection between the FPGA, SMSC USB3300, and the FMC connector. **Table 2-8** lists the signal names and their corresponding Stratix 10 device pin numbers.

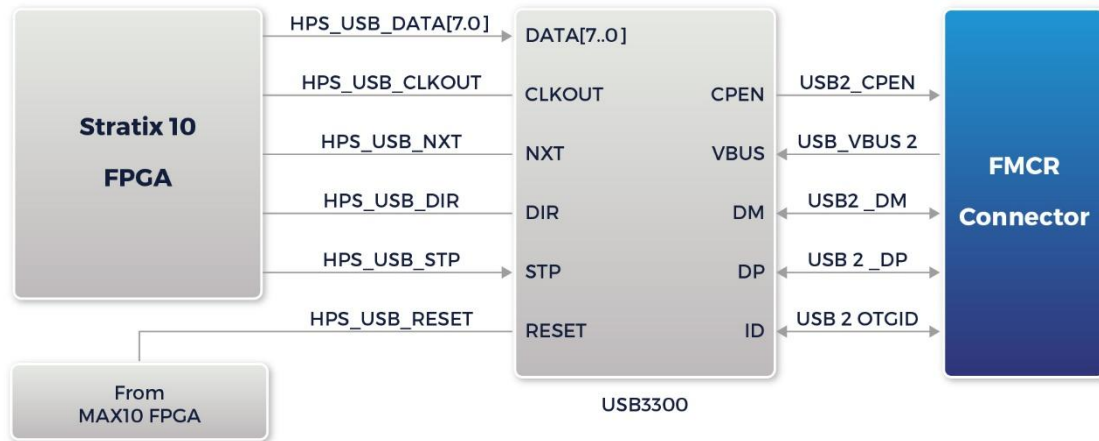


Figure 2-7 Connections between the Stratix 10 FPGA and USB controller

Table 2-8 Pin Assignment of USB OTG PHY

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_USB_CLK	60MHz Reference Clock Output	1.8V	PIN_A15
HPS_USB_DATA[0]	HPS USB_DATA[0]	1.8V	PIN_A11
HPS_USB_DATA[1]	HPS USB_DATA[1]	1.8V	PIN_B13
HPS_USB_DATA[2]	HPS USB_DATA[2]	1.8V	PIN_B14
HPS_USB_DATA[3]	HPS USB_DATA[3]	1.8V	PIN_B17
HPS_USB_DATA[4]	HPS USB_DATA[4]	1.8V	PIN_A10
HPS_USB_DATA[5]	HPS USB_DATA[5]	1.8V	PIN_A16
HPS_USB_DATA[6]	HPS USB_DATA[6]	1.8V	PIN_A12
HPS_USB_DATA[7]	HPS USB_DATA[7]	1.8V	PIN_C16
HPS_USB_DIR	Direction of the Data Bus	1.8V	PIN_C18
HPS_USB_NXT	Throttle the Data	1.8V	PIN_A14
HPS_USB_STP	Stop Data Stream on the Bus	1.8V	PIN_B15

2.6 Gigabit Ethernet

The board supports two Gigabit Ethernet connections via two external PHY chips.

■ Ethernet Port A (ENETA)

- PHY Model: Micrel KSZ9031RN (RGMII mode)
- Connection Architecture: This PHY is directly connected to the HPS (Hard Processor System) I/O pins and its built-in MAC controller.

■ Ethernet Port B (ENETB)

- PHY Model: Micrel KSZ9031MNXIC (GMII mode)
- Connection Architecture: The I/O of this PHY is directly connected to the FPGA Fabric.
- Intended Use: The primary design for this port allows the user to connect it to the HPS's second MAC controller via internal FPGA routing. The advantage of this architecture is that the user does not need to instantiate any MAC IP in the FPGA to enable the dual Ethernet port feature on the Titan S10 SOM's HPS.
- Design Reference: For details on how to connect to the HPS within the FPGA and the related HPS software configuration, please refer to our provided GHRD (Golden Hardware Reference Design) example.
- Alternative Use: Alternatively, the user can connect this PHY to a MAC IP (Soft IP) within the FPGA fabric to implement a purely FPGA-based network application.

The media interfaces for both PHYs (ENETA and ENETB) are routed to the FMC+ (FMC) connector.

Figure 2-8 illustrates the connection between the two Gigabit Ethernet PHYs, the FPGA, and the FMC connector. The pin assignments for the KSZ9031RN (ENETA) and KSZ9031MNXIC (ENETB) interfaces are provided in **Table 2-9** and **Table 2-10**, respectively.

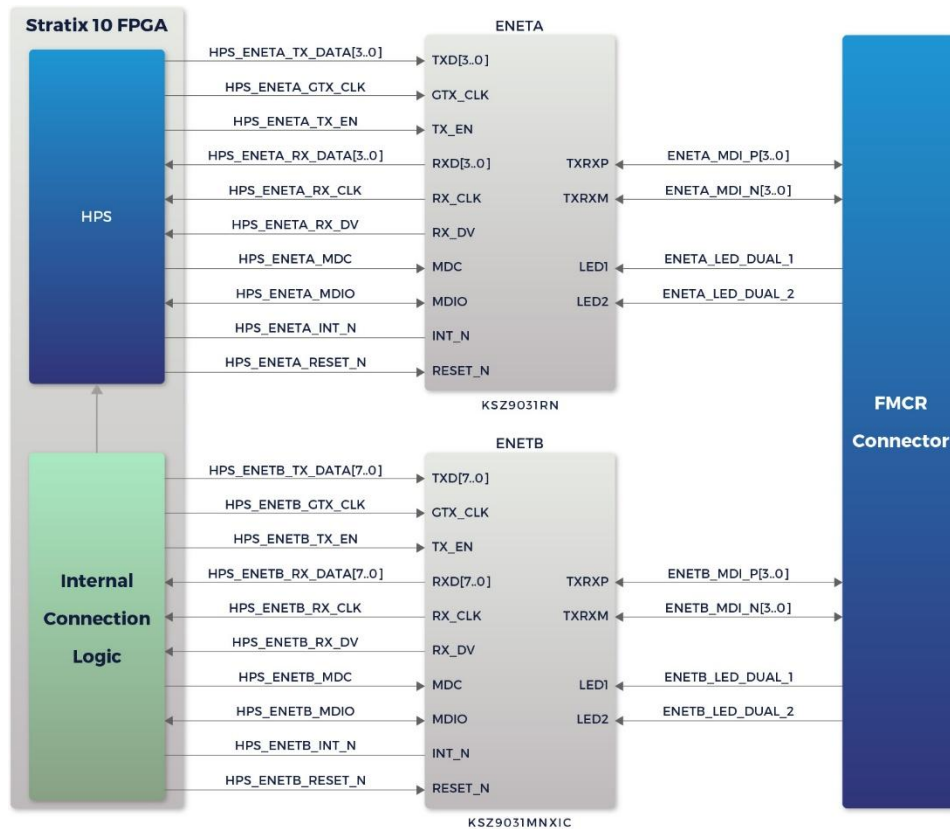


Figure 2-8 Connections between the Stratix 10 FPGA and Gigabit Ethernet PHYS

Table 2-9 Pin Assignment of KSZ9031RN PHY and FPGA

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_ENETA_TX_CTL	RGMII transmit enable	1.8V	PIN_C17
HPS_ENETA_TX_DATA[0]	RGMII transmit data[0]	1.8V	PIN_A9
HPS_ENETA_TX_DATA[1]	RGMII transmit data[1]	1.8V	PIN_B18
HPS_ENETA_TX_DATA[2]	RGMII transmit data[2]	1.8V	PIN_B12
HPS_ENETA_TX_DATA[3]	RGMII transmit data[3]	1.8V	PIN_C15
HPS_ENETA_TX_CLK	RGMII transmit clock	1.8V	PIN_A19
HPS_ENETA_RX_CTL	RGMII receive data valid	1.8V	PIN_A17
HPS_ENETA_RX_DATA[0]	RGMII receive data[0]	1.8V	PIN_B9
HPS_ENETA_RX_DATA[1]	RGMII receive data[1]	1.8V	PIN_A20
HPS_ENETA_RX_DATA[2]	RGMII receive data[2]	1.8V	PIN_B19

HPS_ENETA_RX_DATA[3]	RGMII receive data[3]	1.8V	PIN_B8
HPS_ENETA_RX_CLK	RGMII receive clock	1.8V	PIN_B10
HPS_ENETA_MDIO	Management Data	1.8V	PIN_R19
HPS_ENETA_MDC	Management Data Clock Reference	1.8V	PIN_B20

Table 2-10 Pin Assignment of KSZ9031MNX and FPGA

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
ENETB_RX_CLK	GMII receive clock	1.8V	PIN_B3
ENETB_RX_DATA[0]	GMII receive data bit 0	1.8V	PIN_E3
ENETB_RX_DATA[1]	GMII receive data bit 1	1.8V	PIN_E2
ENETB_RX_DATA[2]	GMII receive data bit 2	1.8V	PIN_G7
ENETB_RX_DATA[3]	GMII receive data bit 3	1.8V	PIN_F7
ENETB_RX_DATA[4]	GMII receive data bit 4	1.8V	PIN_D3
ENETB_RX_DATA[5]	GMII receive data bit 5	1.8V	PIN_D4
ENETB_RX_DATA[6]	GMII receive data bit 6	1.8V	PIN_E1
ENETB_RX_DATA[7]	GMII receive data bit 7	1.8V	PIN_D1
ENETB_RX_COL	GMII collision detect signal	1.8V	PIN_A4
ENETB_RX_CRS	GMII carrier sense signal	1.8V	PIN_C3
ENETB_RX_DV	GMII receive data valid signal	1.8V	PIN_C2
ENETB_RX_ER	GMII receive error indication	1.8V	PIN_D5
ENETB_GTX_CLK	GMII transmit clock generated by MAC	1.8V	PIN_B4
ENETB_TX_DATA[0]	GMII transmit data bit 0	1.8V	PIN_F5
ENETB_TX_DATA[1]	GMII transmit data bit 1	1.8V	PIN_F6
ENETB_TX_DATA[2]	GMII transmit data bit 2	1.8V	PIN_J8
ENETB_TX_DATA[3]	GMII transmit data bit 3	1.8V	PIN_J9
ENETB_TX_DATA[4]	GMII transmit data bit 4	1.8V	PIN_F4
ENETB_TX_DATA[5]	GMII transmit data bit 5	1.8V	PIN_E4
ENETB_TX_DATA[6]	GMII transmit data bit 6	1.8V	PIN_H7
ENETB_TX_DATA[7]	GMII transmit data bit 7	1.8V	PIN_H8
ENETB_TX_EN	GMII transmit enable signal	1.8V	PIN_H12

ENETB_TX_ER	GMII transmit error indication	1.8V	PIN_H11
ENETB_INT_n	Ethernet controller interrupt (active low)	1.8V	PIN_E9
ENETB_MDC	Management data clock for MDIO interface	1.8V	PIN_E8
ENETB_MDIO	Management data input/output for PHY access	1.8V	PIN_A6
ENETB_RESET_n	Ethernet PHY reset signal (active low)	1.8V	PIN_A7

2.7 I2C, UART and GPIO for HPS

This section introduces the I2C bus, UART, and GPIO interfaces connected to the HPS fabric.

■ I2C

Figure 2-9 shows the I2C bus connected to the HPS fabric and its associated devices, including a temperature sensor, RTC, EEPROM (256Kb), and FMCR connector. The HPS can access temperature and time data from the board and store data to the EEPROM. **Table 2-11** lists the signal names and their corresponding Stratix 10 device pin.

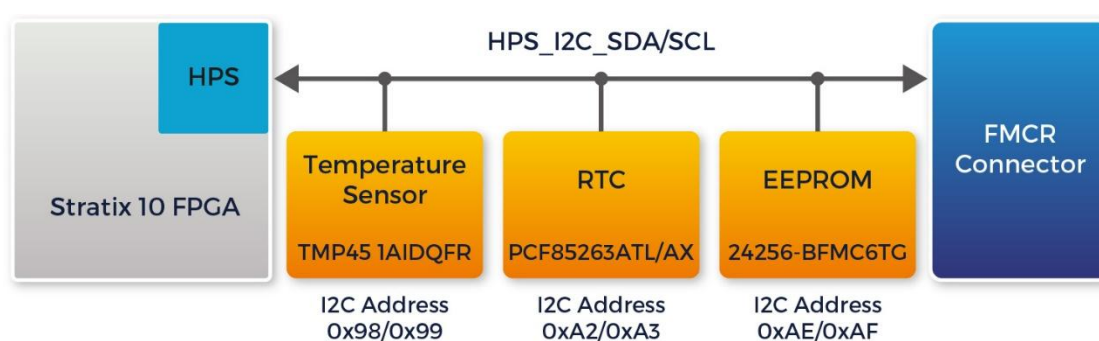


Figure 2-9 I2C interface for HPS fabric on the Titan S10 board

Table 2-11 HPS I2C Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard	FMCRC Pin Number
HPS_I2C_SDA	PIN_G18	I2C serial data line	1.8V	E37
HPS_I2C_SCL	PIN_N20	I2C serial clock line	1.8V	E36

■ UART and GPIO

A UART interface with flow control connects the HPS fabric to the FMCRC connector for communication (see **Figure 2-10**). Two HPS GPIO pins are also available for general-purpose use. **Table 2-12** lists the signal names and their corresponding Stratix 10 device pin.

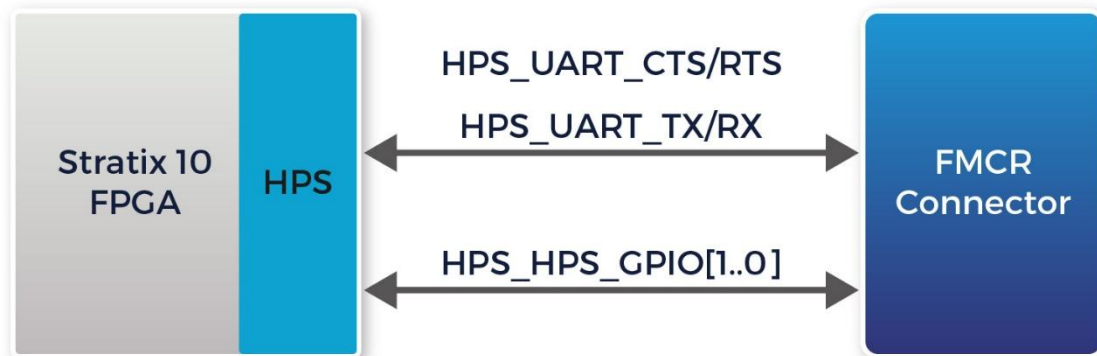


Figure 2-10 UART and GPIO interface for HPS fabric on the Titan S10 board

Table 2-12 HPS UART/GPIO Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard	FMCRC Pin Number
HPS_UART_RX	PIN_F20	HPS UART Receiver	1.8V	F35
HPS_UART_TX	PIN_D19	HPS UART Transmitter	1.8V	F34
HPS_UART_CTS	PIN_M19	HPS UART Clear To Send	1.8V	F37

HPS_UART_RTS	PIN_F19	HPS UART Request To Send	1.8V	F38
HPS_GPIO0	PIN_D18	HPS GPIO 0	1.8V	J14
HPS_GPIO1	PIN_D20	HPS GPIO 1	1.8V	J15

2.8 DDR4 SDRAM

The development board supports two independent banks of DDR4 SDRAM (**DDR4A**, and **DDR4B**). Each DDR4 bank can support 4GB DDR4-2400 with 64-bit data bus. The I/O bank hosting DDR4A supports the Intel Stratix 10 EMIF IP in conjunction with the Hard Processor System (HPS). If HPS EMIF is not utilized, the DDR4A bank can instead be used by the FPGA for EMIF implementation. Figure 2-11 shows the connections between the DDR4 SDRAM bank and Stratix 10 FPGA.

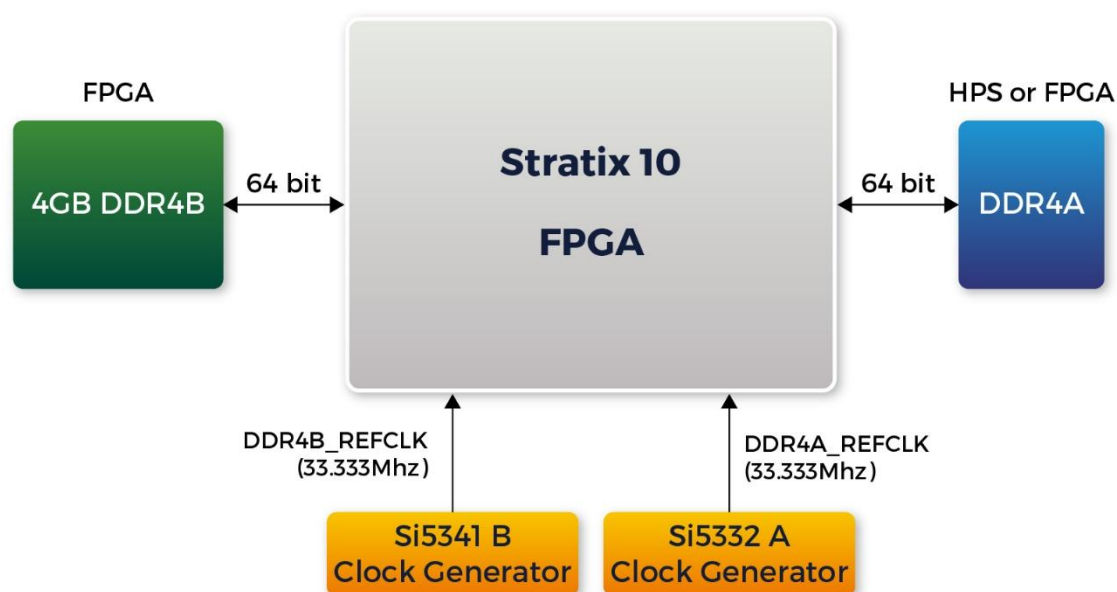


Figure 2-11 Connection between the DDR4 and Stratix 10 FPGA

The pin assignments for DDR4 SDRAM Bank A and Bank B are listed in [Table 2-13](#) and [Table 2-14](#) respectively.

Table 2-13 DDR4A Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Stratix 10 Pin Number
DDR4A_DQ0	Data [0]	1.2-V POD	PIN_F24
DDR4A_DQ1	Data [1]	1.2-V POD	PIN_B22
DDR4A_DQ2	Data [2]	1.2-V POD	PIN_E24
DDR4A_DQ3	Data [3]	1.2-V POD	PIN_D23
DDR4A_DQ4	Data [4]	1.2-V POD	PIN_D24
DDR4A_DQ5	Data [5]	1.2-V POD	PIN_A22
DDR4A_DQ6	Data [6]	1.2-V POD	PIN_E23
DDR4A_DQ7	Data [7]	1.2-V POD	PIN_A21
DDR4A_DQ8	Data [8]	1.2-V POD	PIN_J25
DDR4A_DQ9	Data [9]	1.2-V POD	PIN_G25
DDR4A_DQ10	Data [10]	1.2-V POD	PIN_L25
DDR4A_DQ11	Data [11]	1.2-V POD	PIN_J24
DDR4A_DQ12	Data [12]	1.2-V POD	PIN_L24
DDR4A_DQ13	Data [13]	1.2-V POD	PIN_H26
DDR4A_DQ14	Data [14]	1.2-V POD	PIN_M25
DDR4A_DQ15	Data [15]	1.2-V POD	PIN_K24
DDR4A_DQ16	Data [16]	1.2-V POD	PIN_K22
DDR4A_DQ17	Data [17]	1.2-V POD	PIN_L22
DDR4A_DQ18	Data [18]	1.2-V POD	PIN_K23
DDR4A_DQ19	Data [19]	1.2-V POD	PIN_M22
DDR4A_DQ20	Data [20]	1.2-V POD	PIN_M23
DDR4A_DQ21	Data [21]	1.2-V POD	PIN_N22
DDR4A_DQ22	Data [22]	1.2-V POD	PIN_P23
DDR4A_DQ23	Data [23]	1.2-V POD	PIN_N23
DDR4A_DQ24	Data [24]	1.2-V POD	PIN_F21
DDR4A_DQ25	Data [25]	1.2-V POD	PIN_F22
DDR4A_DQ26	Data [26]	1.2-V POD	PIN_E21
DDR4A_DQ27	Data [27]	1.2-V POD	PIN_D21
DDR4A_DQ28	Data [28]	1.2-V POD	PIN_H21
DDR4A_DQ29	Data [29]	1.2-V POD	PIN_G22
DDR4A_DQ30	Data [30]	1.2-V POD	PIN_E22
DDR4A_DQ31	Data [31]	1.2-V POD	PIN_J21

DDR4A_DQ32	Data [32]	1.2-V POD	PIN_D11
DDR4A_DQ33	Data [33]	1.2-V POD	PIN_E11
DDR4A_DQ34	Data [34]	1.2-V POD	PIN_D10
DDR4A_DQ35	Data [35]	1.2-V POD	PIN_F12
DDR4A_DQ36	Data [36]	1.2-V POD	PIN_F11
DDR4A_DQ37	Data [37]	1.2-V POD	PIN_G12
DDR4A_DQ38	Data [38]	1.2-V POD	PIN_C10
DDR4A_DQ39	Data [39]	1.2-V POD	PIN_C11
DDR4A_DQ40	Data [40]	1.2-V POD	PIN_G14
DDR4A_DQ41	Data [41]	1.2-V POD	PIN_D15
DDR4A_DQ42	Data [42]	1.2-V POD	PIN_E13
DDR4A_DQ43	Data [43]	1.2-V POD	PIN_D14
DDR4A_DQ44	Data [44]	1.2-V POD	PIN_G13
DDR4A_DQ45	Data [45]	1.2-V POD	PIN_G15
DDR4A_DQ46	Data [46]	1.2-V POD	PIN_J15
DDR4A_DQ47	Data [47]	1.2-V POD	PIN_H15
DDR4A_DQ48	Data [48]	1.2-V POD	PIN_J16
DDR4A_DQ49	Data [49]	1.2-V POD	PIN_N16
DDR4A_DQ50	Data [50]	1.2-V POD	PIN_K16
DDR4A_DQ51	Data [51]	1.2-V POD	PIN_N15
DDR4A_DQ52	Data [52]	1.2-V POD	PIN_L16
DDR4A_DQ53	Data [53]	1.2-V POD	PIN_P16
DDR4A_DQ54	Data [54]	1.2-V POD	PIN_M15
DDR4A_DQ55	Data [55]	1.2-V POD	PIN_P15
DDR4A_DQ56	Data [56]	1.2-V POD	PIN_M18
DDR4A_DQ57	Data [57]	1.2-V POD	PIN_E16
DDR4A_DQ58	Data [58]	1.2-V POD	PIN_F17
DDR4A_DQ59	Data [59]	1.2-V POD	PIN_G17
DDR4A_DQ60	Data [60]	1.2-V POD	PIN_N18
DDR4A_DQ61	Data [61]	1.2-V POD	PIN_H17
DDR4A_DQ62	Data [62]	1.2-V POD	PIN_L17
DDR4A_DQ63	Data [63]	1.2-V POD	PIN_K17
DDR4A_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_C23

DDR4A_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-V POD	PIN_C22
DDR4A_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_N25
DDR4A_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_P25
DDR4A_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V POD	PIN_T23
DDR4A_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_R24
DDR4A_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V POD	PIN_J23
DDR4A_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_H23
DDR4A_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2-V POD	PIN_D8
DDR4A_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2-V POD	PIN_C8
DDR4A_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2-V POD	PIN_E14
DDR4A_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2-V POD	PIN_F14
DDR4A_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2-V POD	PIN_R17
DDR4A_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2-V POD	PIN_P18
DDR4A_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2-V POD	PIN_N17
DDR4A_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2-V POD	PIN_M17
DDR4A_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_G23
DDR4A_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_G24
DDR4A_DBI_n2	Data Bus	1.2-V POD	PIN_P24

	Inversion [2]		
DDR4A_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_H22
DDR4A_DBI_n4	Data Bus Inversion [4]	1.2-V POD	PIN_E12
DDR4A_DBI_n5	Data Bus Inversion [5]	1.2-V POD	PIN_F15
DDR4A_DBI_n6	Data Bus Inversion [6]	1.2-V POD	PIN_L15
DDR4A_DBI_n7	Data Bus Inversion [7]	1.2-V POD	PIN_H16
DDR4A_A0	Address [0]	SSTL-12	PIN_M28
DDR4A_A1	Address [1]	SSTL-12	PIN_N28
DDR4A_A2	Address [2]	SSTL-12	PIN_R26
DDR4A_A3	Address [3]	SSTL-12	PIN_P26
DDR4A_A4	Address [4]	SSTL-12	PIN_P28
DDR4A_A5	Address [5]	SSTL-12	PIN_R27
DDR4A_A6	Address [6]	SSTL-12	PIN_K26
DDR4A_A7	Address [7]	SSTL-12	PIN_K27
DDR4A_A8	Address [8]	SSTL-12	PIN_N26
DDR4A_A9	Address [9]	SSTL-12	PIN_N27
DDR4A_A10	Address [10]	SSTL-12	PIN_L27
DDR4A_A11	Address [11]	SSTL-12	PIN_M27
DDR4A_A12	Address [12]	SSTL-12	PIN_J29
DDR4A_A13	Address [13]	SSTL-12	PIN_J28
DDR4A_A14	Address [14]/ WE_n	SSTL-12	PIN_K28
DDR4A_A15	Address [15]/ CAS_n	SSTL-12	PIN_H31
DDR4A_A16	Address [16]/ RAS_n	SSTL-12	PIN_H30
DDR4A_BA0	Bank Select [0]	SSTL-12	PIN_H27
DDR4A_BA1	Bank Select [1]	SSTL-12	PIN_G27
DDR4A_BG0	Bank Group	SSTL-12	PIN_F27

	Select [0]		
DDR4A_BG1	Bank Group Select [1]	SSTL-12	PIN_N30
DDR4A_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_K31
DDR4A_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_L30
DDR4A_CKE	Clock Enable pin	SSTL-12	PIN_M30
DDR4A_ODT	On Die Termination	SSTL-12	PIN_K30
DDR4A_CS_n	Chip Select	SSTL-12	PIN_M29
DDR4A_PAR	Command and Address Parity Input	SSTL-12	PIN_P29
DDR4A_ALERT_n	Register ALERT_n output	1.2 V	PIN_B23
DDR4A_ACT_n	Activation Command Input	SSTL-12	PIN_L29
DDR4A_RESET_n	Chip Reset	1.2 V	PIN_P31
DDR4A_REFCLK_p	DDR4 A port Reference Clock p	LVDS	PIN_D27
DDR4A_REFCLK_n	DDR4 A port Reference Clock n	LVDS	PIN_E27
DDR4A_RZQ	External precision resistor	1.2 V	PIN_J30

Table 2-14 DDR4B Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Stratix 10 Pin Number
DDR4B_DQ0	Data [0]	1.2-V POD	PIN_AV25
DDR4B_DQ1	Data [1]	1.2-V POD	PIN_AW24
DDR4B_DQ2	Data [2]	1.2-V POD	PIN_AW25
DDR4B_DQ3	Data [3]	1.2-V POD	PIN_AY24
DDR4B_DQ4	Data [4]	1.2-V POD	PIN_AT26

DDR4B_DQ5	Data [5]	1.2-V POD	PIN_AT24
DDR4B_DQ6	Data [6]	1.2-V POD	PIN_AR27
DDR4B_DQ7	Data [7]	1.2-V POD	PIN_AU25
DDR4B_DQ8	Data [8]	1.2-V POD	PIN_BA26
DDR4B_DQ9	Data [9]	1.2-V POD	PIN_AY26
DDR4B_DQ10	Data [10]	1.2-V POD	PIN_AY27
DDR4B_DQ11	Data [11]	1.2-V POD	PIN_BA24
DDR4B_DQ12	Data [12]	1.2-V POD	PIN_BB27
DDR4B_DQ13	Data [13]	1.2-V POD	PIN_AW26
DDR4B_DQ14	Data [14]	1.2-V POD	PIN_AV27
DDR4B_DQ15	Data [15]	1.2-V POD	PIN_BA27
DDR4B_DQ16	Data [16]	1.2-V POD	PIN_AP28
DDR4B_DQ17	Data [17]	1.2-V POD	PIN_AT29
DDR4B_DQ18	Data [18]	1.2-V POD	PIN_AP30
DDR4B_DQ19	Data [19]	1.2-V POD	PIN_AM30
DDR4B_DQ20	Data [20]	1.2-V POD	PIN_AR28
DDR4B_DQ21	Data [21]	1.2-V POD	PIN_AT30
DDR4B_DQ22	Data [22]	1.2-V POD	PIN_AN30
DDR4B_DQ23	Data [23]	1.2-V POD	PIN_AL30
DDR4B_DQ24	Data [24]	1.2-V POD	PIN_AM28
DDR4B_DQ25	Data [25]	1.2-V POD	PIN_AP26
DDR4B_DQ26	Data [26]	1.2-V POD	PIN_AK29
DDR4B_DQ27	Data [27]	1.2-V POD	PIN_AN27
DDR4B_DQ28	Data [28]	1.2-V POD	PIN_AL29
DDR4B_DQ29	Data [29]	1.2-V POD	PIN_AM27
DDR4B_DQ30	Data [30]	1.2-V POD	PIN_AK30
DDR4B_DQ31	Data [31]	1.2-V POD	PIN_AN28
DDR4B_DQ32	Data [32]	1.2-V POD	PIN_AV18
DDR4B_DQ33	Data [33]	1.2-V POD	PIN_BA17
DDR4B_DQ34	Data [34]	1.2-V POD	PIN_AW16
DDR4B_DQ35	Data [35]	1.2-V POD	PIN_AY16
DDR4B_DQ36	Data [36]	1.2-V POD	PIN_AV16
DDR4B_DQ37	Data [37]	1.2-V POD	PIN_AW18
DDR4B_DQ38	Data [38]	1.2-V POD	PIN_AU18

DDR4B_DQ39	Data [39]	1.2-V POD	PIN_AV17
DDR4B_DQ40	Data [40]	1.2-V POD	PIN_AR17
DDR4B_DQ41	Data [41]	1.2-V POD	PIN_AT19
DDR4B_DQ42	Data [42]	1.2-V POD	PIN_AR19
DDR4B_DQ43	Data [43]	1.2-V POD	PIN_AT17
DDR4B_DQ44	Data [44]	1.2-V POD	PIN_AP19
DDR4B_DQ45	Data [45]	1.2-V POD	PIN_AR18
DDR4B_DQ46	Data [46]	1.2-V POD	PIN_AR16
DDR4B_DQ47	Data [47]	1.2-V POD	PIN_AT16
DDR4B_DQ48	Data [48]	1.2-V POD	PIN_AK23
DDR4B_DQ49	Data [49]	1.2-V POD	PIN_AJ23
DDR4B_DQ50	Data [50]	1.2-V POD	PIN_AL22
DDR4B_DQ51	Data [51]	1.2-V POD	PIN_AL20
DDR4B_DQ52	Data [52]	1.2-V POD	PIN_AJ24
DDR4B_DQ53	Data [53]	1.2-V POD	PIN_AL21
DDR4B_DQ54	Data [54]	1.2-V POD	PIN_AJ25
DDR4B_DQ55	Data [55]	1.2-V POD	PIN_AK24
DDR4B_DQ56	Data [56]	1.2-V POD	PIN_AK19
DDR4B_DQ57	Data [57]	1.2-V POD	PIN_AK17
DDR4B_DQ58	Data [58]	1.2-V POD	PIN_AL19
DDR4B_DQ59	Data [59]	1.2-V POD	PIN_AK18
DDR4B_DQ60	Data [60]	1.2-V POD	PIN_AM20
DDR4B_DQ61	Data [61]	1.2-V POD	PIN_AJ19
DDR4B_DQ62	Data [62]	1.2-V POD	PIN_AM19
DDR4B_DQ63	Data [63]	1.2-V POD	PIN_AM17
DDR4B_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_AT27
DDR4B_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-V POD	PIN_AU27
DDR4B_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_BB25
DDR4B_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_BA25
DDR4B_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V	PIN_AP29

		POD	
DDR4B_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_AR30
DDR4B_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V POD	PIN_AK28
DDR4B_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_AK27
DDR4B_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2-V POD	PIN_BB18
DDR4B_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2-V POD	PIN_BB17
DDR4B_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2-V POD	PIN_AM18
DDR4B_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2-V POD	PIN_AN18
DDR4B_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2-V POD	PIN_AK22
DDR4B_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2-V POD	PIN_AK21
DDR4B_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2-V POD	PIN_AH18
DDR4B_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2-V POD	PIN_AJ18
DDR4B_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_AU24
DDR4B_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_AV26
DDR4B_DBI_n2	Data Bus Inversion [2]	1.2-V POD	PIN_AT21
DDR4B_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_AT31
DDR4B_DBI_n4	Data Bus Inversion [4]	1.2-V POD	PIN_AY18
DDR4B_DBI_n5	Data Bus Inversion [5]	1.2-V POD	PIN_AP18

DDR4B_DBI_n6	Data Bus Inversion [6]	1.2-V POD	PIN_AH24
DDR4B_DBI_n7	Data Bus Inversion [7]	1.2-V POD	PIN_AN17
DDR4B_A0	Address [0]	SSTL-12	PIN_AM25
DDR4B_A1	Address [1]	SSTL-12	PIN_AN25
DDR4B_A2	Address [2]	SSTL-12	PIN_AP24
DDR4B_A3	Address [3]	SSTL-12	PIN_AP25
DDR4B_A4	Address [4]	SSTL-12	PIN_AL24
DDR4B_A5	Address [5]	SSTL-12	PIN_AM24
DDR4B_A6	Address [6]	SSTL-12	PIN_AL26
DDR4B_A7	Address [7]	SSTL-12	PIN_AL25
DDR4B_A8	Address [8]	SSTL-12	PIN_AP23
DDR4B_A9	Address [9]	SSTL-12	PIN_AN23
DDR4B_A10	Address [10]	SSTL-12	PIN_AR23
DDR4B_A11	Address [11]	SSTL-12	PIN_AR24
DDR4B_A12	Address [12]	SSTL-12	PIN_AY21
DDR4B_A13	Address [13]	SSTL-12	PIN_BB19
DDR4B_A14	Address [14]/ WE_n	SSTL-12	PIN_BA19
DDR4B_A15	Address [15]/ CAS_n	SSTL-12	PIN_AW21
DDR4B_A16	Address [16]/ RAS_n	SSTL-12	PIN_AV21
DDR4B_BA0	Bank Select [0]	SSTL-12	PIN_BA20
DDR4B_BA1	Bank Select [1]	SSTL-12	PIN_AW20
DDR4B_BG0	Bank Group Select [0]	SSTL-12	PIN_AV20
DDR4B_BG1	Bank Group Select [1]	SSTL-12	PIN_BA22
DDR4B_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_AU22
DDR4B_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_AV22

DDR4B_CKE	Clock Enable pin	SSTL-12	PIN_AV23
DDR4B_ODT	On Die Termination	SSTL-12	PIN_BB23
DDR4B_CS_n	Chip Select	SSTL-12	PIN_AT22
DDR4B_PAR	Command and Address Parity Input	SSTL-12	PIN_AW23
DDR4B_ALERT_n	Register ALERT_n output	1.2 V	PIN_AT25
DDR4B_ACT_n	Activation Command Input	SSTL-12	PIN_AR22
DDR4B_RESET_n	Chip Reset	1.2 V	PIN_AY22
DDR4B_REFCLK_p	DDR4 B port Reference Clock p	LVDS	PIN_AY19
DDR4B_REFCLK_n	DDR4 B port Reference Clock n	LVDS	PIN_AW19
DDR4B_RZQ	External precision resistor	1.2 V	PIN_BA21

2.9 Infineon(Cypress) FX3 USB

Controller

The Titan S10 SOM board includes an Infineon(Cypress) FX3 USB Controller (CYUSB3014) for USB 3.0 connectivity. The USB controller interfaces with the FPGA through a **32-bit GPIF II** data bus.

On the board, the FX3 controller's PMODE[2:0] pins are connected to the MAX10 FPGA for boot mode control. By default, the PMODE[2:0] setting is “**SPI; on failure, USB boot enabled.**” Upon power-up, the FX3 attempts to load firmware from a 4Mb serial SPI Flash, which handles USB communication and high-speed data transfer via GPIF II.

As shown in **Figure 2-12**, users can configure PMODE[2:0] through the **USBFX3_USB_MODE** pin between the MAX10 and the FPGA.

- When **USBFX3_USB_MODE** is logic high (1), FX3 boots from SPI Flash.
- When it is logic low (0), FX3 enters USB boot mode, allowing firmware updates via the USB interface from a PC.

For details on the update procedure, please refer to the demonstration manual.

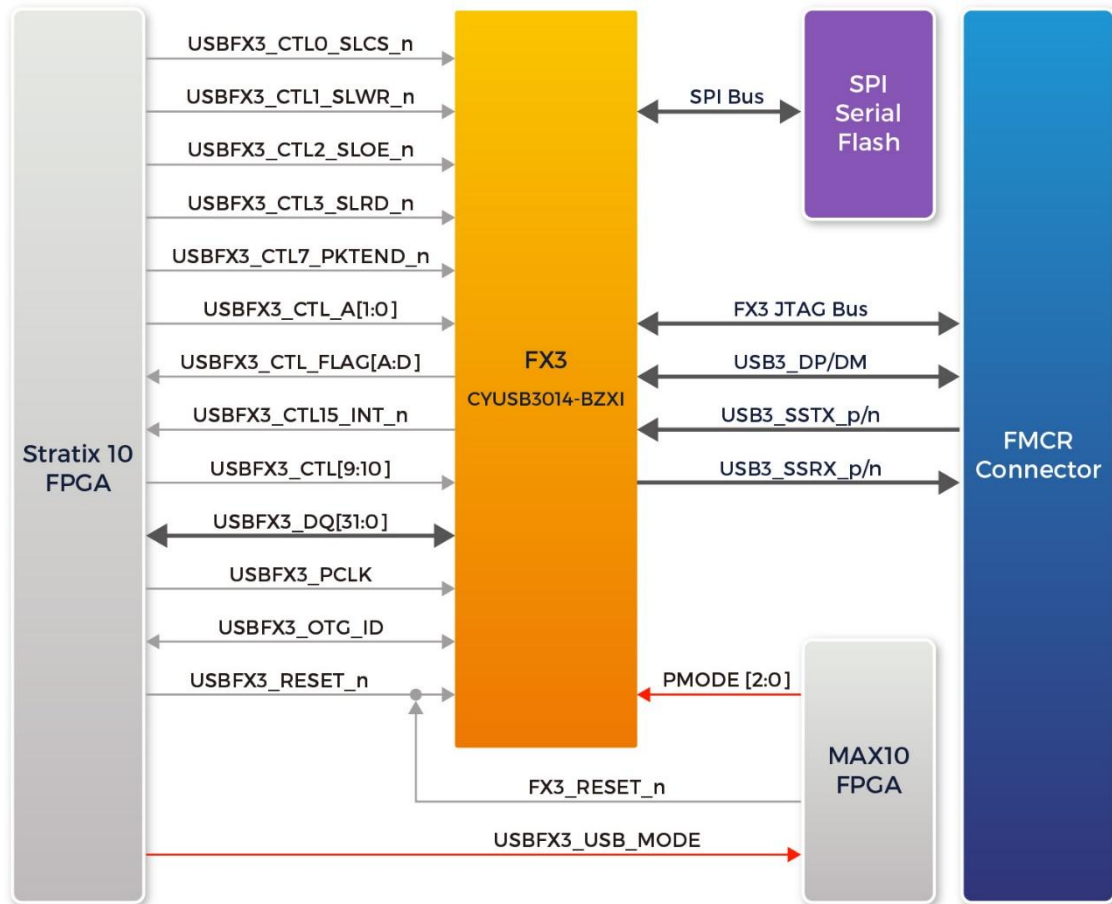


Figure 2-12 FX3 controller interface overview on the board

Table 2-15 DDR4B Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
USBFX3_RESET_n	FX3 reset	1.8 V	PIN_AW11
USBFX3_PCLK	Slave FIFO interface clock.	1.8 V	PIN_AV6
USBFX3_UART_TX	USB to UART	1.8 V	PIN_AW1

	transmitter		
USBFX3_UART_RX	USB to UART receiver	1.8 V	PIN_AU2
USBFX3_CTL0_SLCS_n	GPIF II Control Bus 0	1.8 V	PIN_AR3
USBFX3_CTL1_SLWR_n	GPIF II Control Bus 1	1.8 V	PIN_AW9
USBFX3_CTL2_SLOE_n	GPIF II Control Bus 2	1.8 V	PIN_AV7
USBFX3_CTL3_SLRD_n	GPIF II Control Bus 3	1.8 V	PIN_AV10
USBFX3_CTL4_FLAGA	GPIF II Control Bus 4	1.8 V	PIN_AR4
USBFX3_CTL5_FLAGB	GPIF II Control Bus 5	1.8 V	PIN_AV2
USBFX3_CTL6_FLAGC	GPIF II Control Bus 6	1.8 V	PIN_AU3
USBFX3_CTL7_PKTEND_n	GPIF II Control Bus 7	1.8 V	PIN_AV3
USBFX3_CTL8_FLAGD	GPIF II Control Bus 8	1.8 V	PIN_AW10
USBFX3_CTL9	GPIF II Control Bus 9	1.8 V	PIN_AU10
USBFX3_CTL10	GPIF II Control Bus 10	1.8 V	PIN_AV11
USBFX3_CTL11_A1	GPIF II Control Bus 11	1.8 V	PIN_AV12
USBFX3_CTL12_A0	GPIF II Control Bus 12	1.8 V	PIN_AV5
USBFX3_CTL15_INT_n	GPIF II Control Bus 15	1.8 V	PIN_AP4
USBFX3_DQ[0]	GPIF II Data Bus 0	1.8 V	PIN_BA5
USBFX3_DQ[1]	GPIF II Data Bus 1	1.8 V	PIN_BB5
USBFX3_DQ[2]	GPIF II Data Bus 2	1.8 V	PIN_BA4
USBFX3_DQ[3]	GPIF II Data Bus 3	1.8 V	PIN_BB4
USBFX3_DQ[4]	GPIF II Data Bus 4	1.8 V	PIN_AW5
USBFX3_DQ[5]	GPIF II Data Bus 5	1.8 V	PIN_AU5
USBFX3_DQ[6]	GPIF II Data Bus 6	1.8 V	PIN_AY4
USBFX3_DQ[7]	GPIF II Data Bus 7	1.8 V	PIN_AW4
USBFX3_DQ[8]	GPIF II Data Bus 8	1.8 V	PIN_AW3
USBFX3_DQ[9]	GPIF II Data Bus 9	1.8 V	PIN_AY3
USBFX3_DQ[10]	GPIF II Data Bus 10	1.8 V	PIN_AY6
USBFX3_DQ[11]	GPIF II Data Bus 11	1.8 V	PIN_AY7
USBFX3_DQ[12]	GPIF II Data Bus 12	1.8 V	PIN_AU4
USBFX3_DQ[13]	GPIF II Data Bus 13	1.8 V	PIN_BA2
USBFX3_DQ[14]	GPIF II Data Bus 14	1.8 V	PIN_AY2
USBFX3_DQ[15]	GPIF II Data Bus 15	1.8 V	PIN_AV1
USBFX3_DQ[16]	GPIF II Data Bus 16	1.8 V	PIN_AW8
USBFX3_DQ[17]	GPIF II Data Bus 17	1.8 V	PIN_AT7

USBFX3_DQ[18]	GPIF II Data Bus 18	1.8 V	PIN_AU7
USBFX3_DQ[19]	GPIF II Data Bus 19	1.8 V	PIN_AW6
USBFX3_DQ[20]	GPIF II Data Bus 20	1.8 V	PIN_AT9
USBFX3_DQ[21]	GPIF II Data Bus 21	1.8 V	PIN_AU9
USBFX3_DQ[22]	GPIF II Data Bus 22	1.8 V	PIN_AU8
USBFX3_DQ[23]	GPIF II Data Bus 23	1.8 V	PIN_AT10
USBFX3_DQ[24]	GPIF II Data Bus 24	1.8 V	PIN_AT11
USBFX3_DQ[25]	GPIF II Data Bus 25	1.8 V	PIN_AT12
USBFX3_DQ[26]	GPIF II Data Bus 26	1.8 V	PIN_AR11
USBFX3_DQ[27]	GPIF II Data Bus 27	1.8 V	PIN_AR12
USBFX3_DQ[28]	GPIF II Data Bus 28	1.8 V	PIN_AR13
USBFX3_DQ[29]	GPIF II Data Bus 29	1.8 V	PIN_AP13
USBFX3_DQ[30]	GPIF II Data Bus 30	1.8 V	PIN_AU12
USBFX3_DQ[31]	GPIF II Data Bus 31	1.8 V	PIN_AU13
USBFX3_OTG_ID	OTG ID pin	1.8 V	OTG ID pin
USBFX3_USB_MODE	FX3 boot mode setting pin	1.8 V	<ul style="list-style-type: none"> ● Logic low (0) FX3 in USB boot mode ● Logic high (1) FX3 in SPI boot mode (default)

2.10 FMC/FMC+ Connector

This section provides an overview of the interfaces connected through these two FMC or FMC+ connectors. As shown in **Figure 2-14** and **Figure 2-14**, the Titan S10 SOM board includes two FMC (or FMC+) connectors, named FMCR (J1) and FMCL (J2). These connectors serve as the primary interface for connecting the SOM to various peripherals and FPGA I/Os, and deliver power to the SOM.

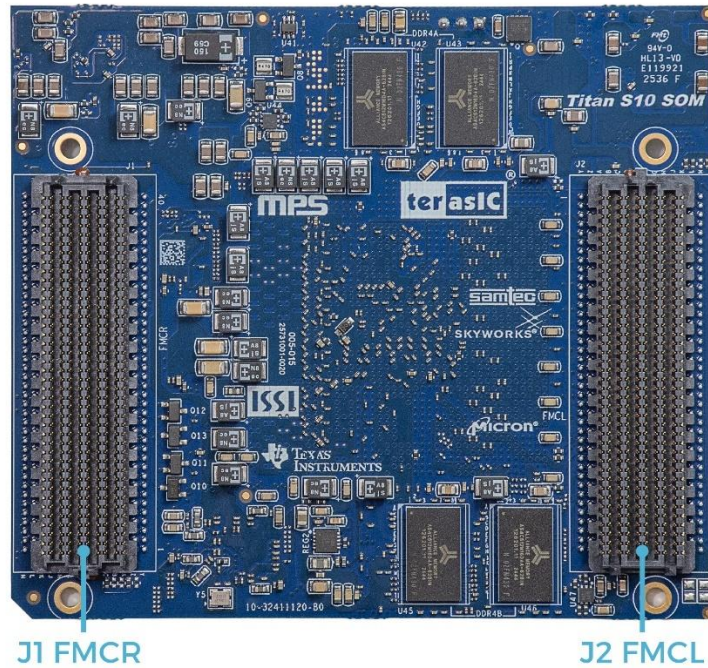


Figure 2-13 FMC connectors on Titan S10 SoM board

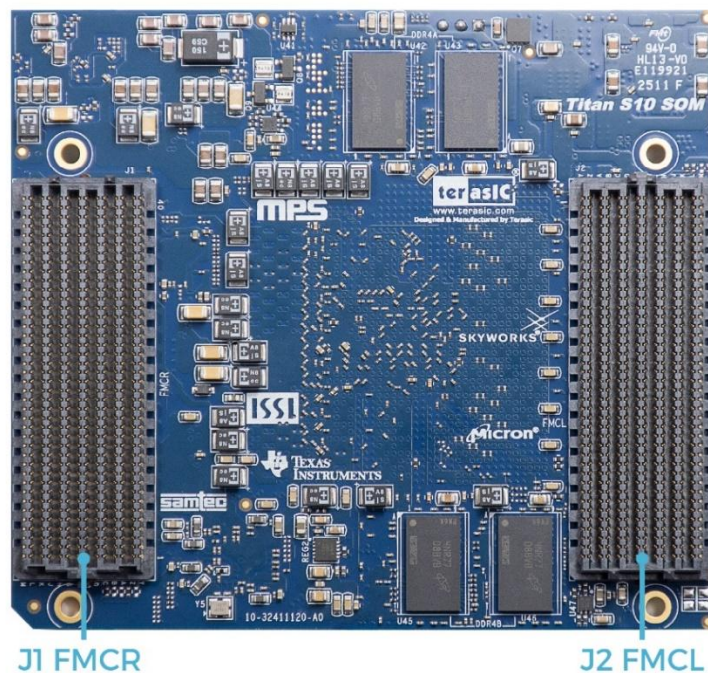


Figure 2-14 FMC+ connectors on Titan S10 SoM board

Below we will introduce according to the individual functions of FMC and FMC+ connector.

■ FMCR

Figure 2-15 illustrates the interfaces connected through the FMCR connector. For detailed information on net names, pin assignments, and signal descriptions, please refer to the Excel file: [Titan_S10_SOM_FMC_pinout.xlsx](#) included in the Resource Package.

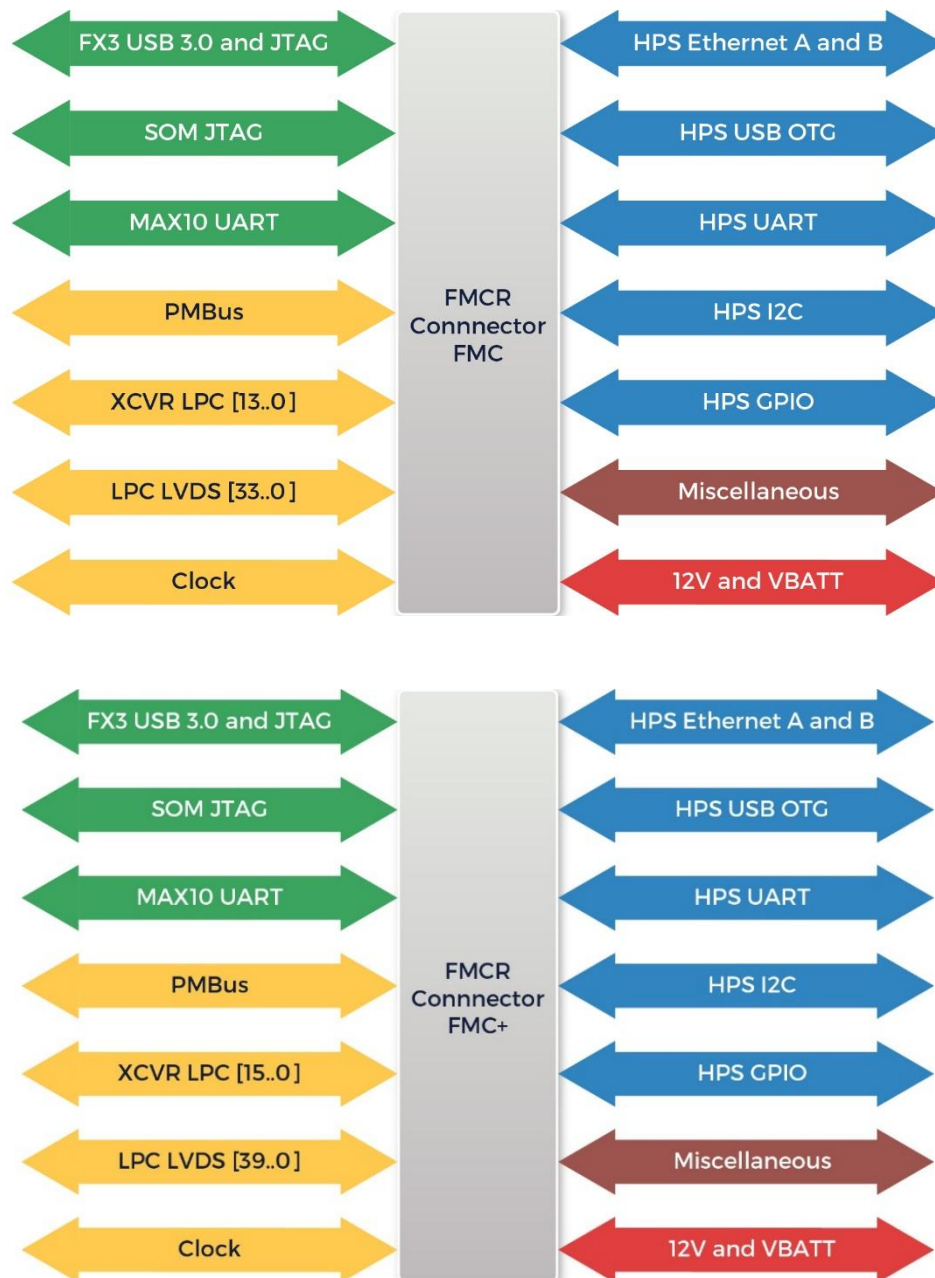


Figure 2-15 Interfaces connected through the FMCR connector

The main interfaces connected to FMCR are as follows:

- **Power**

- Supplies 12V and VBAT power to the SOM.

- **HPS Interface**

All interfaces connected to the HPS (Hard Processor System) of the Stratix 10 FPGA are routed to the FMCR connector and used for connections to carrier board peripherals, including:

- Ethernet A and B
- HPS UART
- USB 2.0 OTG
- HPS I²C
- HPS GPIO

- **JTAG**

- SOM JTAG: Connects to the JTAG interface of the Stratix 10 or MAX10 FPGA on the SOM.
- FX3 JTAG: Connects to the JTAG interface of the onboard FX3 controller.

- **User I/O**

- FMC: 34 pairs of LVDS I/O (LA00–LA33);
FMC+: 40 pairs of LVDS I/O (LA00–LA33, HC00–HC05)
- 2 pairs of LVDS clock to FPGA
- FMC: 14 pairs of 12.5 Gbps transceivers (DP0–DP13, including 4 pairs in the K column);
FMC+: 16 pairs of 12.5 Gbps transceivers (DP0–DP15, including 4 pairs in the K column)
- 3 pairs of transceiver clocks to FPGA

- **PMBus**

- Connects to the FPGA core power IC

- **MAX10 UART**

- UART interface for power monitor communication from the MAX10 FPGA

- **Clock**

- Reference clock input from the carrier board for the onboard programmable PLL clock generator (Si5341A)
- Signal name: CLK_REF_Si5341_P/N

- **Miscellaneous**

- Configuration Status: SOM_CG_M2C, SOM_CG_C2M
- Connection Status: SOM_PRSNT_N
- Board Temperature Status: TEMP_FAULT
- Reset Signals:
 - Carrier to SOM reset: SOM_RST_C2M
 - SOM to Carrier reset: SOM_RST_M2C
 - PCIe Hard IP reset: PCIE_NPERSTL0
- Power Status:
 - Power-good from SOM: SOM_PG
 - Power-good from carrier to SOM: SOM_CG_C2M
- I²C Bus to power IC on SOM: MAX_MPM_SCL / MAX_MPM_SDA
- Reserved Signals:
 - Carrier_Tester_ID: Leave unconnected or pull high. Do not pull low.
 - MPS_DONG_EN_N, PMBUS_DONG_EN_N

■ FMCL

The FMCL connector primarily provides high-speed transceivers and FPGA I/O directly connected to the Stratix 10 device. **Figure 2-16** illustrates the interfaces connected through the FMCL connector.

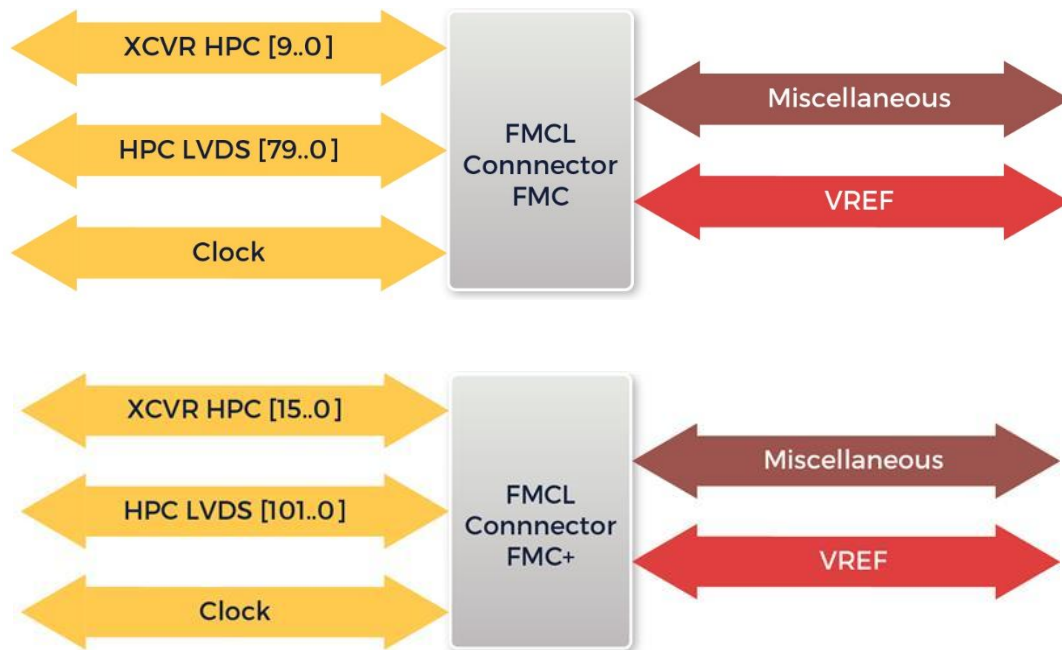


Figure 2-16 Interfaces connected through the FMCL connector

For detailed information on net names, pin assignments, and signal descriptions, please refer to the Excel file: [Titan_S10_SOM_FMC_pinout.xlsx](#) included in the Resource Package.

The main interfaces connected to FMCL are as follows:

- **User I/O**

- FMC: 80 pairs of LVDS FPGA I/O:
 - LA01–LA33, HA00–HA23, HB00–HB22
- FMC+: 102 pairs of LVDS FPGA I/O:
 - LA01–LA33, HA00–HA23, HB00–HB22, HD00–HD21
- FMC: 10 pairs of 12.5 Gbps transceivers (DP0–DP9)
- FMC+: 16 pairs of 12.5 Gbps transceivers (DP0–DP15)
- 3 pairs of transceiver clocks
- One I²C interface: SDA, SCL, GA0, GA1

- **Miscellaneous**

- Configuration Status: SOM_CG_M2C, SOM_CG_C2M
- Connection Status: SOM_PRSNT_N
- Reset: Connected to the reset signal from PCIe edge connector

- **Power**

- Provides voltage reference for Stratix 10 FPGA banks 3C and 3J:
MCL_VREF_A_M2C, MCL_VREF_B_M2C

Chapter 3

Additional Information

3.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Titan S10 Web: agilex-som.terasic.com

■ Revision History

Date	Version	Changes
2025.05	First publication	
2025.10	V1.1	Modify section 2.6 ENETB PHY and section 2.10 for FMC+ descriptions
2025.11	V1.2	Modify section 1.1 overview