



Titan S10 SOM Evaluation Kit



Getting Start Guide

FPGA

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Chapter 1

Overview

This manual serves as a quick start guide for the Titan S10 SOM Evaluation Kit, outlining the essential hardware setup, software installation, and basic knowledge required for initial operation.

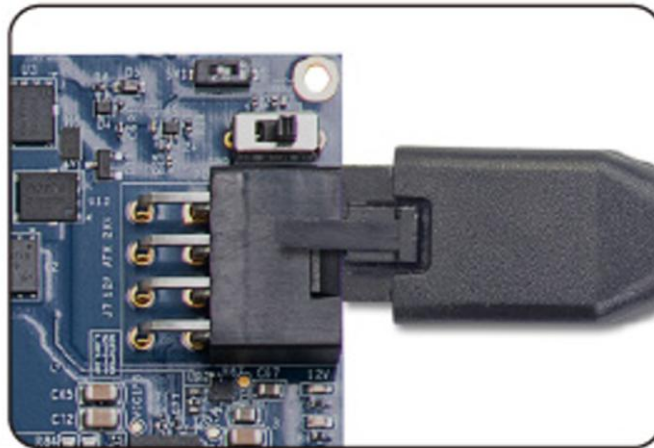
This guide includes the following topics:

- Powering on the board
- Using USB Blaster III on Windows/Linux
- Installing the UART driver
- Programming the FPGA configuration into QSPI flash

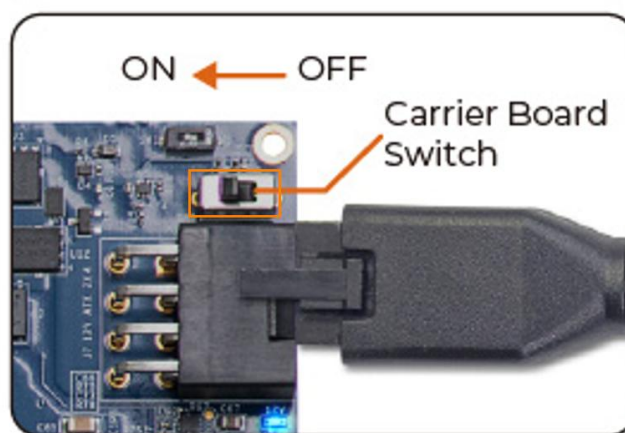
Chapter 2

Power On the Board

1. Connect the power adapter to the 2x4 power connector on the board.



2. Power on the kit by turning the power switch on the carrier board to **ON** position



Chapter 3

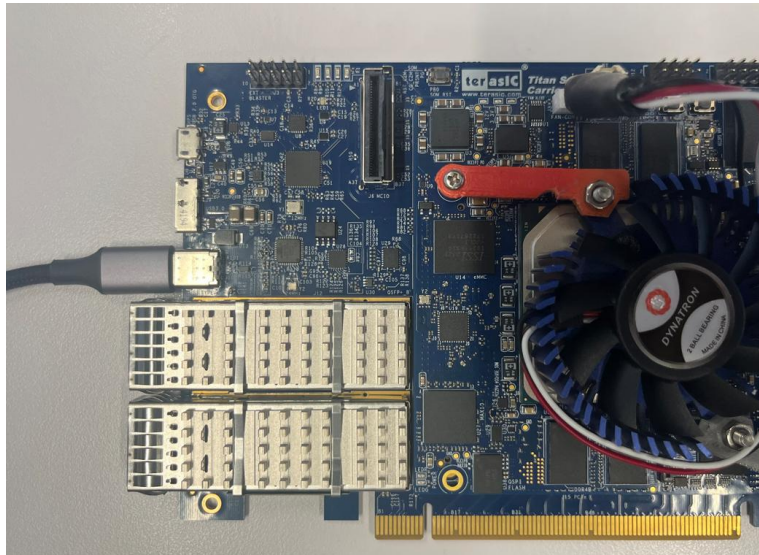
Using the USB Blaster III

Under Windows

The Titan S10 Evaluation Kit includes Altera's latest **USB Blaster III** circuitry. This guide explains how to enable and use this feature..

3.1 Hardware Connection

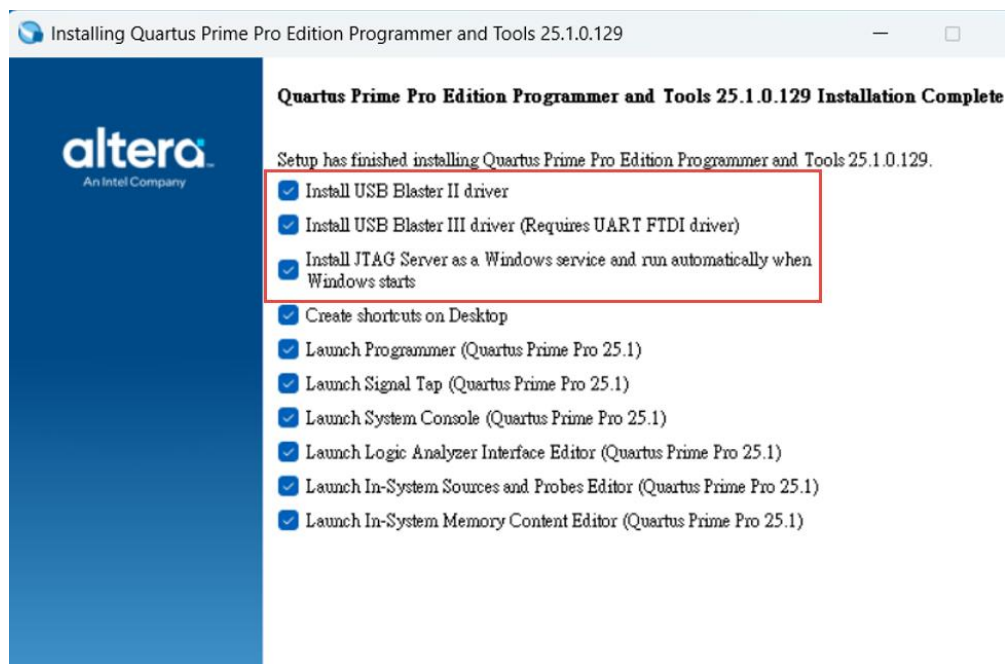
Connect the **Type-C port** on the Titan S10 Evaluation Kit to your **host PC** using a USB cable, then power on the board.



3.2 For Quartus Pro 25.1 Users

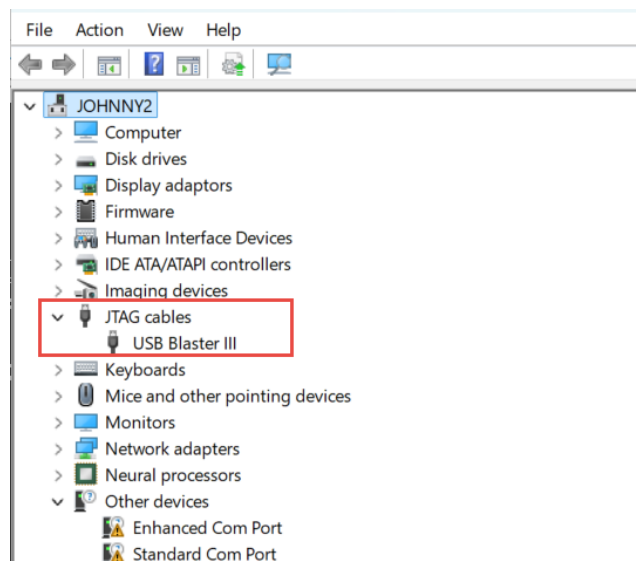
Starting with Quartus Pro 25.1, **USB Blaster III** is supported. When installing Quartus, ensure the following options are selected:

- Install USB Blaster III driver
- Install USB Blaster III driver (Requires UART FTDI driver)
- Install JTAG server as a Windows service and run automatically when windows starts

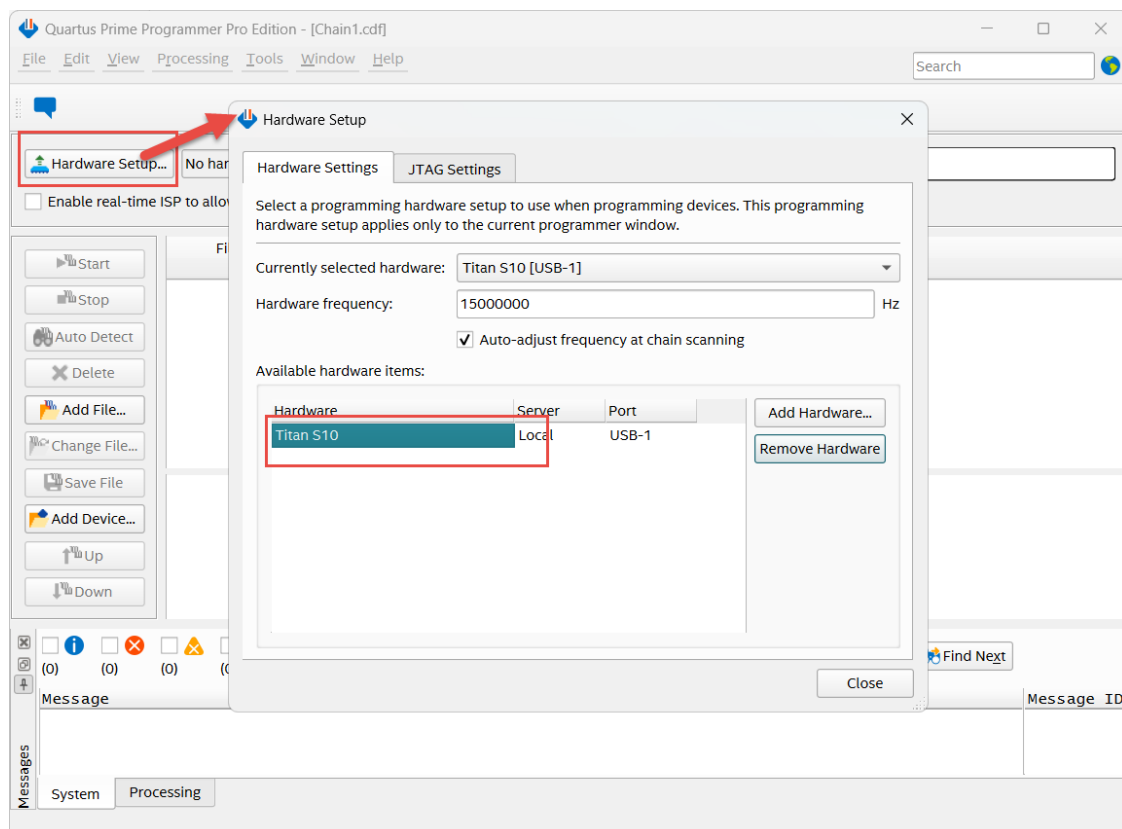


After installation:

- **Device Manager** should display USB Blaster III in JTAG cables tab.



- Quartus Programmer 25.1 should list USB Blaster III as an available option



3.3 For Non-Quartus Pro 25.1 Users (e.g., Quartus 24.3)

If you are using a version earlier than 25.1, follow these steps:

i. Install Quartus Pro 25.1 Programmer

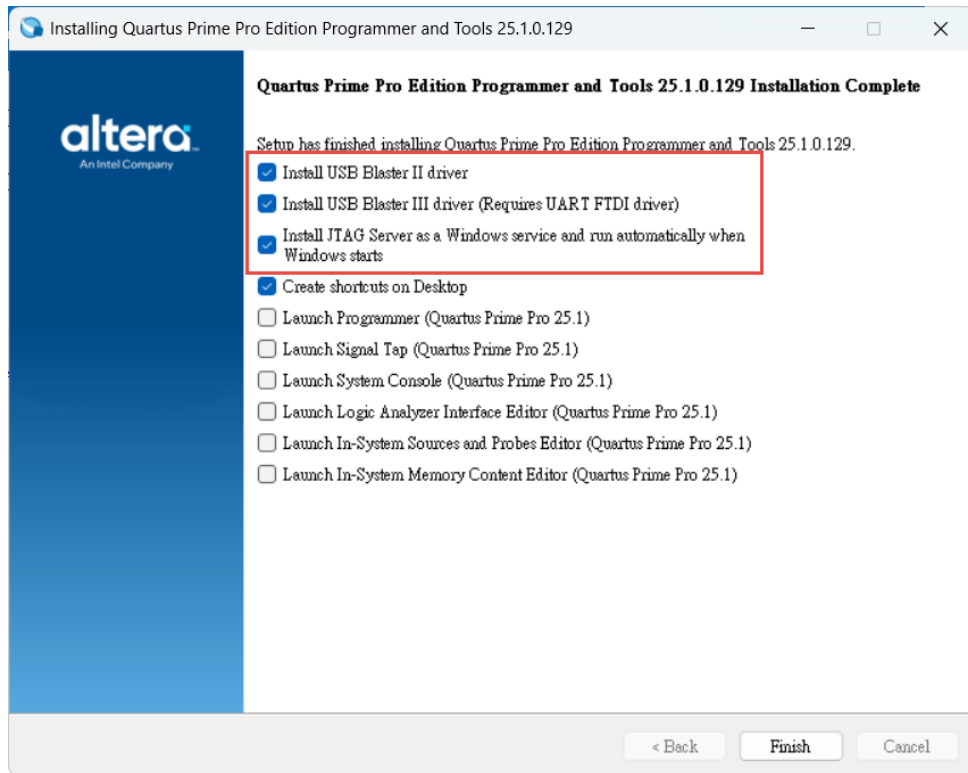
- Download from the link below:

[Intel Quartus Pro 25.1 Programmer Download](#)

- Go to the Individual Files tab, find **Quartus® Prime Pro Edition Programmer and Tools**, and download it.

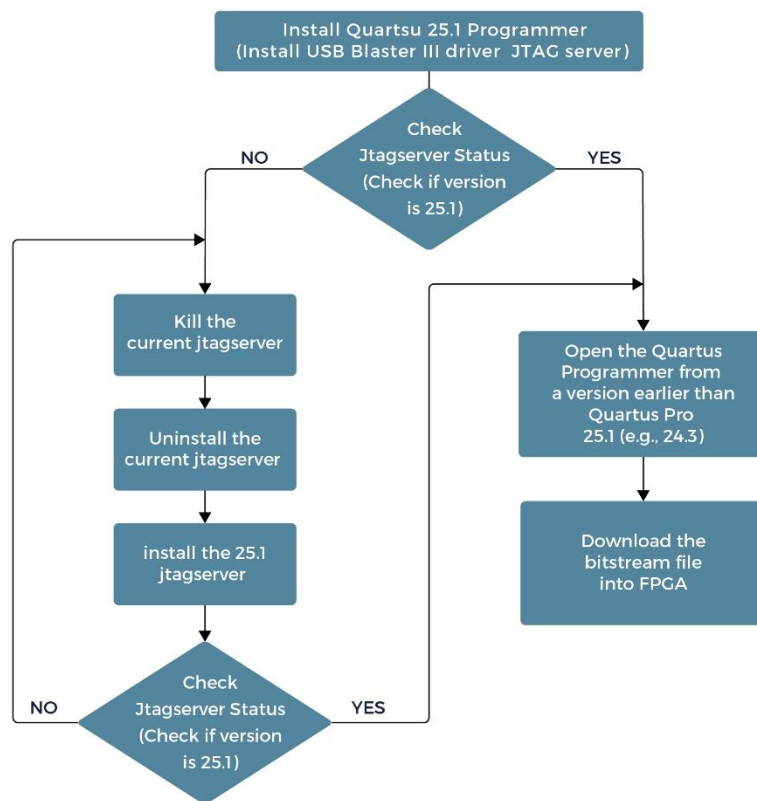


- During installation, ensure the following are selected:
 - Install USB Blaster III driver
 - Install USB Blaster III driver (Requires UART FTDI driver)
 - Install JTAG server as a Windows service and run automatically when windows starts



ii. Workflow for setting USB blaster III

- After completing Step i, follow the flow shown in the figure below.



To allow Quartus 24.3 Programmer to recognize the USB Blaster III circuit, the user must ensure that **the JTAG Server running on the host is version 25.1**.

- If the running JTAG Server is version 25.1, Quartus 24.3 Programmer should be able to detect and use the USB Blaster III directly.
- If the running JTAG Server is **not** version 25.1, some additional commands are required to switch it to version 25.1.

iii. Check Running JTAG Server Version

1. Open Command Prompt as **Administrator**.
2. Run the following command:

```
powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"
```

- If the path points to Quartus 25.1 Programmer, the correct version is running. Proceed to **Step v**.

```
C:\Windows\System32>powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"
ProcessName Path
-----
jtagserver D:\altera_pro\25.1\qprogrammer\quartus\bin64\jtagserver.exe
C:\Windows\System32>
```

- If it shows Quartus 24.3, continue to **Step iv** to switch the version of the JTAG Server.

```
Administrator: Command Prompt
Microsoft Windows [Version 10.0.26100.2314]
(c) Microsoft Corporation. All rights reserved.

C:\Windows\System32>powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"
ProcessName Path
-----
jtagserver D:\intelFPGA_pro\24.3\quartus\bin64\jtagserver.exe
C:\Windows\System32>
```

iv. Switch JTAG Server to Version 25.1

- Terminate the current JTAG Server process.

```
taskkill /f /im jtagserver.exe
```

```
Administrator: Command Prompt
Microsoft Windows [Version 10.0.26100.2314]
(c) Microsoft Corporation. All rights reserved.

C:\Windows\System32>powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"
ProcessName Path
-----
jtagserver D:\intelFPGA_pro\24.3\quartus\bin64\jtagserver.exe

C:\Windows\System32>taskkill /f /im jtagserver.exe
SUCCESS: The process "jtagserver.exe" with PID 11556 has been terminated.
C:\Windows\System32>
```

- Uninstall the current JTAG Server.

<Quartus 25.1 programmer install path>\quartus\bin64\jtagserver.exe --uninstall

```
Administrator: Command Prompt
Microsoft Windows [Version 10.0.26100.2314]
(c) Microsoft Corporation. All rights reserved.

C:\Windows\System32>powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"

ProcessName Path
-----
jtagserver D:\intelFPGA_pro\24.3\quartus\bin64\jtagserver.exe

C:\Windows\System32>taskkill /f /im jtagserver.exe
SUCCESS: The process "jtagserver.exe" with PID 11556 has been terminated.

C:\Windows\System32>D:\altera_pro\25.1\qprogrammer\quartus\bin64\jtagserver.exe --uninstall
C:\Windows\System32>
```

- Install the 25.1 JTAG Server:

<Quartus 25.1 programmer install path>\quartus\bin64\jtagserver.exe --install

```
Administrator: Command Prompt
Microsoft Windows [Version 10.0.26100.2314]
(c) Microsoft Corporation. All rights reserved.

C:\Windows\System32>powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"

ProcessName Path
-----
jtagserver D:\intelFPGA_pro\24.3\quartus\bin64\jtagserver.exe

C:\Windows\System32>taskkill /f /im jtagserver.exe
SUCCESS: The process "jtagserver.exe" with PID 11556 has been terminated.

C:\Windows\System32>D:\altera_pro\25.1\qprogrammer\quartus\bin64\jtagserver.exe --uninstall
C:\Windows\System32>D:\altera_pro\25.1\qprogrammer\quartus\bin64\jtagserver.exe --install
C:\Windows\System32>
```

- Run the PowerShell command from Step iii again to verify the version is now 25.1.

powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"

- If confirmed, proceed to Step v. If not, check previous steps for any omissions.


```
Administrator: Command Prompt
Microsoft Windows [Version 10.0.26100.2314]
(c) Microsoft Corporation. All rights reserved.

C:\Windows\System32>powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"

ProcessName Path
-----
jtagserver  D:\intelFPGA_pro\24.3\quartus\bin64\jtagserver.exe

C:\Windows\System32>taskkill /f /im jtagserver.exe
SUCCESS: The process "jtagserver.exe" with PID 11556 has been terminated.

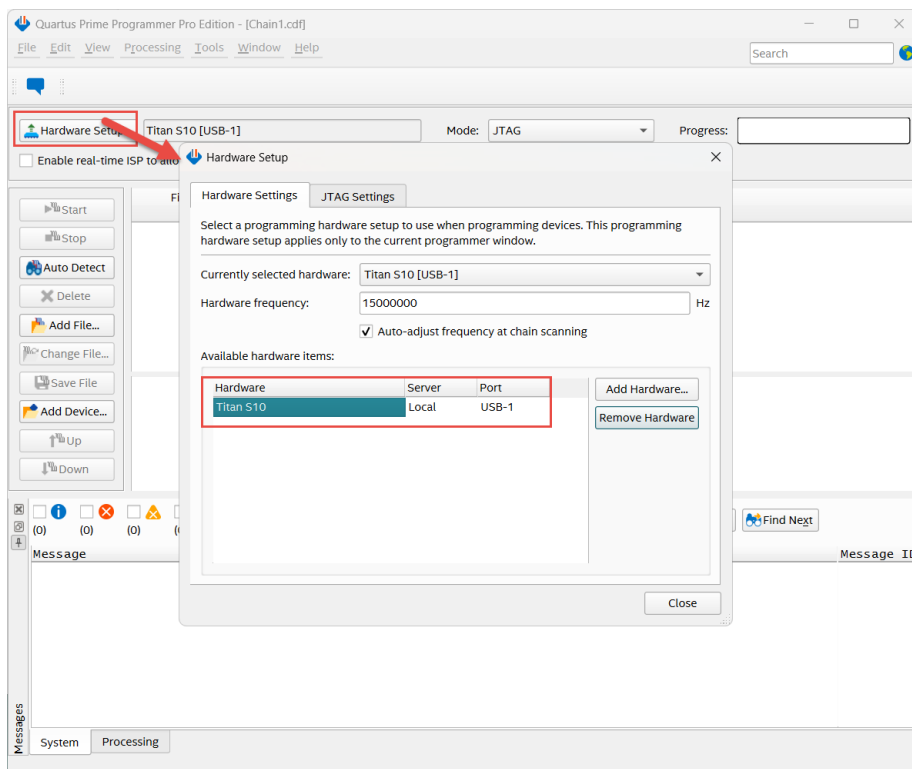
C:\Windows\System32>D:\altera_pro\25.1\qprogrammer\quartus\bin64\jtagserver.exe --uninstall
C:\Windows\System32>D:\altera_pro\25.1\qprogrammer\quartus\bin64\jtagserver.exe --install
C:\Windows\System32>powershell.exe -Command "Get-Process -Name jtagserver | Select-Object ProcessName, Path"

ProcessName Path
-----
jtagserver  D:\altera_pro\25.1\qprogrammer\quartus\bin64\jtagserver.exe

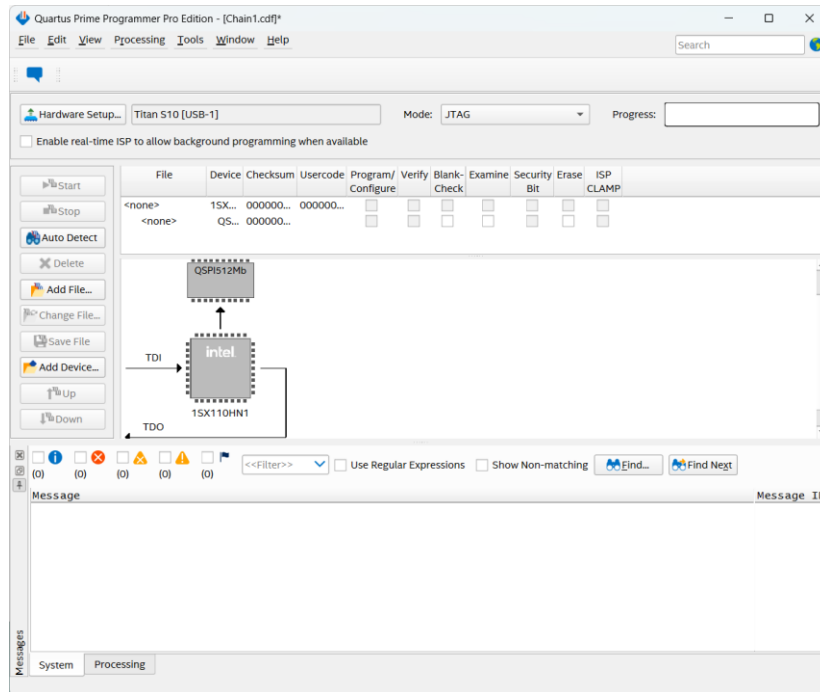
C:\Windows\System32>
```

v. Configure Quartus Programmer

1. Launch Quartus 24.3 Programmer..
2. Select USB Blaster III as the programming hardware.



3. Click Auto Detect to ensure the FPGA is recognized.



Chapter 4

Using the USB Blaster III

Under Linux

This chapter will explain how to use the **USB Blaster III** under a **Linux** environment.

4.1 Driver Setup

Add the following lines to the `/etc/udev/rules.d/51-usbblaster.rules` file in user's linux system.

```
# USB-Blaster
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6001", MODE="0666"
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6002", MODE="0666"
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6003", MODE="0666"

# USB-Blaster II
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6010", MODE="0666"
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6810", MODE="0666"

# USB-Blaster III
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6020", MODE="0666"
```

4.2 Hardware Connection

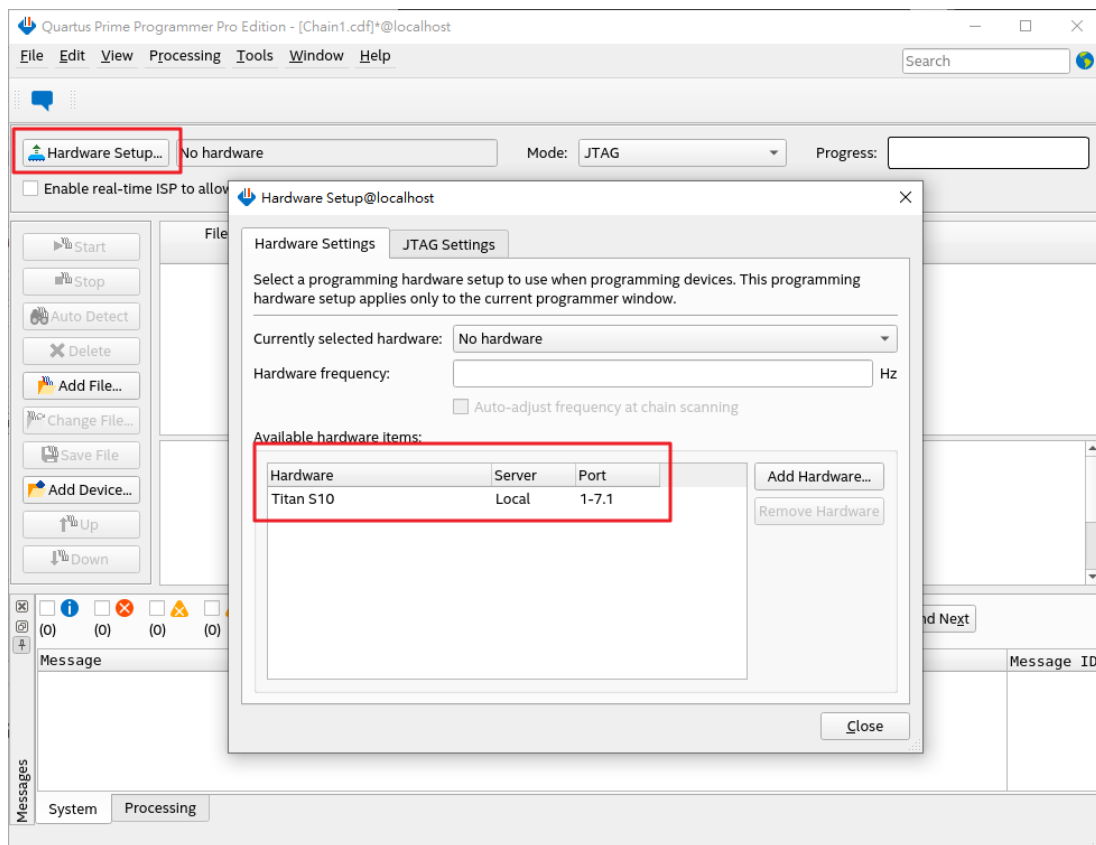
Connect the **Type-C port** on the Titan S10 Evaluation Kit to your **host PC** using a USB cable, then power on the board.



4.3 For Quartus Pro 25.1 Users

Starting with Quartus Pro 25.1, **USB Blaster III** is supported.

Please open the Quartus Programmer 25.1 and it should list USB Blaster III as an available option



4.4 For Non-Quartus Pro 25.1 Users (e.g., Quartus 24.3)

If you are using a version earlier than 25.1, follow these steps:

i. Install Quartus Pro 25.1 Programmer

- Download from the link below:

[Intel Quartus Pro 25.1 Programmer Download](#)

- Go to the Individual Files tab, find **Quartus® Prime Pro Edition Programmer and Tools**, and download it.

Quartus® Prime Pro Edition Programmer and Tools

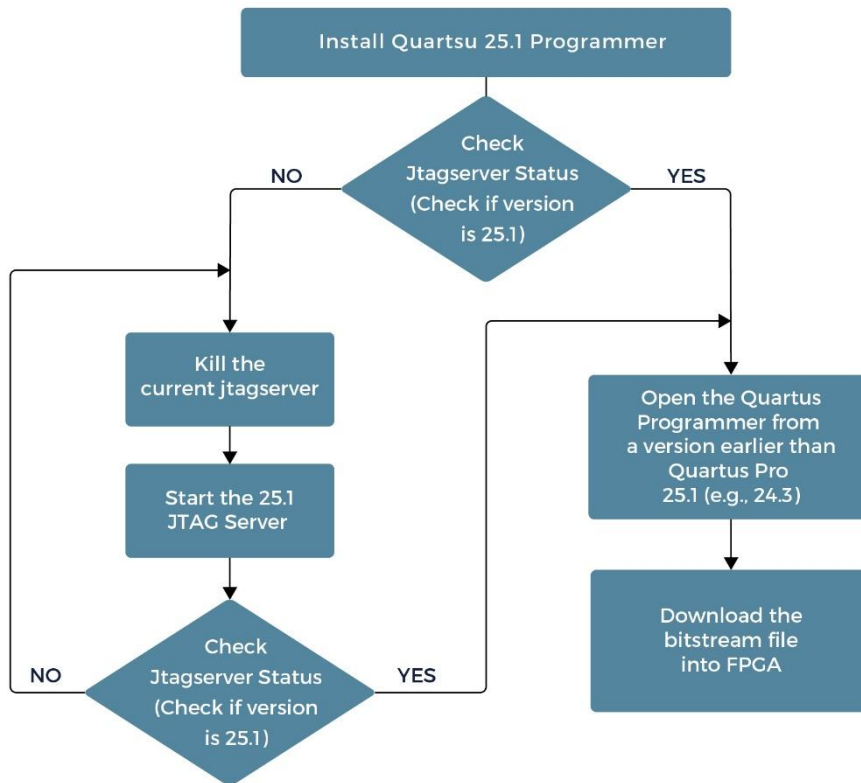
Download
QuartusProProgrammerSetup-25.1.0.129-linux.run

Size: 1.5 GB

SHA1: a80f03fa51b274d2f439004f9f9120f1b867d2ac

ii. Workflow for setting USB blaster III

- After completing Step i, follow the flow shown in the figure below.



To allow Quartus 24.3 Programmer to recognize the USB Blaster III circuit, the user must ensure that **the JTAG Server running on the host is version 25.1**.

- If the running JTAG Server is version 25.1, Quartus 24.3 Programmer should be able to detect and use the USB Blaster III directly.
- If the running JTAG Server is **not** version 25.1, some additional commands are required to switch it to version 25.1.

iii. Check Running JTAG Server Version

- Open Terminal
- Run the following command:

```
ls -l | grep jtagd || echo 0 | grep txt
```

```
user@localhost:~$ lsof -p `pgrep jtagd` | echo 0` | grep txt
jtagd  4696 user  txt      REG  8,18   2007208 6601351 /home/user/altera_pro/25.1/qprogrammer/quartus/linux64/jtagd
user@localhost:~$
```

- If the **path** points to Quartus 25.1 Programmer, the correct version is running. Proceed to **Step v**.
- If it shows Quartus 24.3, continue to **Step iv** to switch the version of the JTAG Server.

```
user@localhost:~$ lsof -p `pgrep jtagd` | echo 0` | grep txt
jtagd  5070 user  txt      REG  8,18   689280 8268673 /home/user/intelFPGA_pro/24.3/qprogrammer/quartus/linux64/jtagd
user@localhost:~$
```

iv. Switch JTAG Server to Version 25.1

- Terminate the current JTAG Server process.

```
killall -9 jtagd
```

```
user@localhost:~$ killall -9 jtagd
user@localhost:~$
```

- Start the 25.1 JTAG Server:

```
<Quartus 25.1 programmer install path>/quartus/bin/jtagd
```

```
user@localhost:~$ /home/user/altera_pro/25.1/qprogrammer/quartus/linux64/jtagd
user@localhost:~$
```

- Run the command from Step iii again to verify the version is now 25.1.

```
lsof -p `pgrep jtagd` | echo 0` | grep txt
```

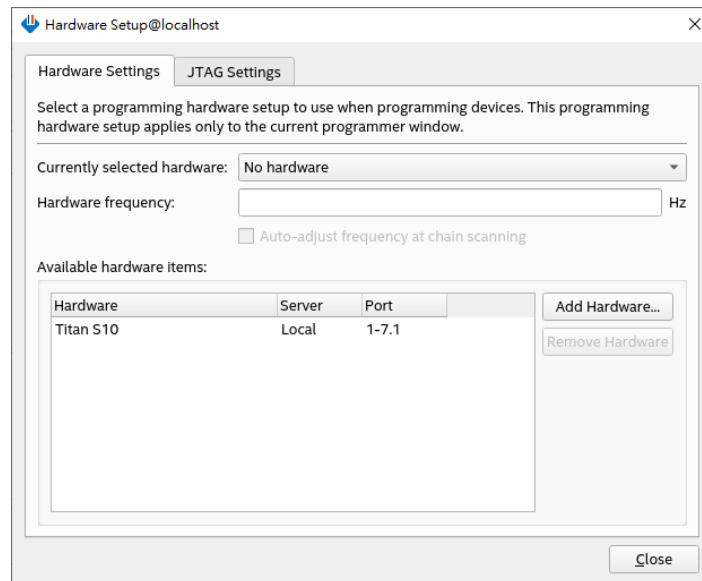
```
user@localhost:~$ lsof -p `pgrep jtagd` | echo 0` | grep txt
jtagd  5083 user  txt      REG  8,18   2007208 6601351 /home/user/altera_pro/25.1/qprogrammer/quartus/linux64/jtagd
user@localhost:~$
```

- If confirmed, proceed to Step v. If not, check previous steps for any omissions.

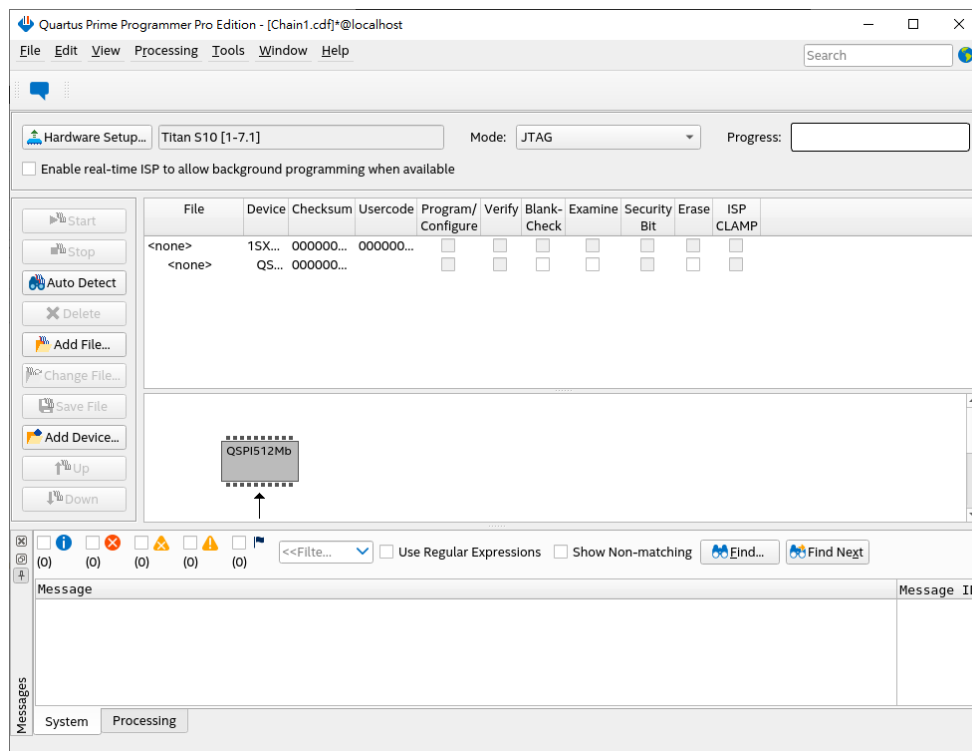
v. Configure Quartus Programmer

1. Launch Quartus 24.3 Programmer.

2. Select USB Blaster III as the programming hardware.



3. Click Auto Detect to ensure the FPGA is recognized.

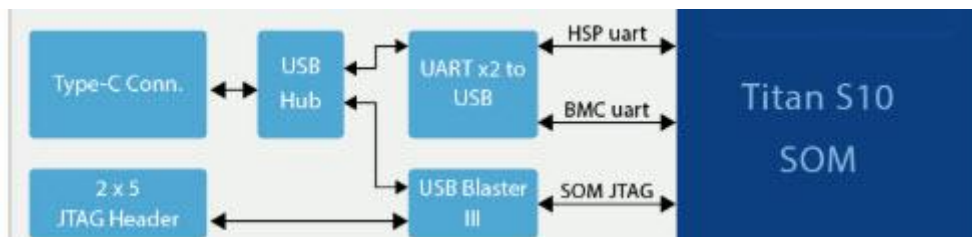


Chapter 5

Install UART Driver

This chapter explains how to install the UART interface driver for the Titan S10 EVK.

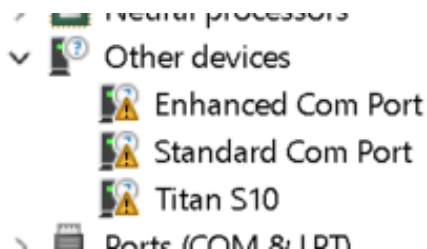
As shown in the diagram, the USB Type-C connector on the Titan S10 EVK supports three functions:



- USB Blaster III
- HPS UART
- BMC UART

For USB Blaster III driver installation, refer to Chapter 3.

The HPS and BMC UART interfaces are supported by a Silicon Labs CP2105 USB-to-Dual-UART Bridge Controller. When the USB Type-C connector is connected to the host PC, Windows Device Manager will detect three UART devices.



One is the USB Blaster III UART, which is currently unused and can be ignored. The remaining two are the HPS and BMC UART ports. Please follow the link below

for the driver installation instructions : [The CP2105 \(USB to UART\) Driver Installation Instructions](#)

Once installed successfully, Device Manager should display the following:

- Enhanced Port corresponds to HPS UART
- Standard Port corresponds to BMC UART

Make sure to check the COM port numbers to match your intended connection (HPS or BMC).

Chapter 6

Programming FPGA

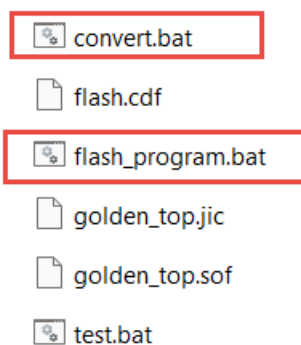
Configuration into QSPI Flash

This chapter explains how to program the user's .sof file into QSPI flash, allowing users to boot the FPGA in AS Fast mode.

6.1 Programming .sof File into QSPI Flash

For FPGA-only designs, users can convert and program their .sof file into QSPI flash using the provided Terasic demo batch file. Follow these steps:

1. Download the Titan S10 SOM EVK CD-ROM to your host PC.
2. Navigate to the folder: /Demonstration/FPGA/LED_Blink/demo_batch/.



3. Rename your target .sof file to `golden_top.sof`, replacing the existing file in the above directory.

4. Execute `convert.bat` within the `demo_batch` folder to convert `golden_top.sof` into `golden_top.jic`.

```
C:\Windows\system32\cmd.exe
FPGA Configure...
Info: *****
Info: Running Quartus Prime Programming File Generator
Info: Version 24.3.0 Build 212 11/18/2024 SC Pro Edition
Info: Copyright (C) 2024 Intel Corporation. All rights reserved.
Info: Your use of Intel Corporation's design tools, logic functions
Info: and other software and tools, and any partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Intel Program License
Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
Info: the Intel FPGA IP License Agreement, or other applicable license
Info: agreement, including, without limitation, that your use is for
Info: the sole purpose of programming logic devices manufactured by
Info: Intel and sold by Intel or its authorized distributors. Please
Info: refer to the Intel FPGA Software License Subscription Agreements
Info: on the Quartus Prime software download page.
Info: Processing started: Mon Jun 2 13:19:08 2025
Info: System process ID: 19376
Info: Command: quartus_pfg -c golden_top.sof golden_top.jic -o device=MT25QU512 -o flash_loader=15X110HN3F43I2VG -o mode
-A5X4
Info (19848): Regular SEU info => 53 sector(s), 4 thread(s), 1000000 interval time in microsecond(s)
Info (19848): IO hash is C8588DD7D8E255F95DF0E6BA02FD7880116E1815B6F26408D7085B0955E8A0
Info (19848): Keyed hash is 3F711913286C78C1A67E32D85E227B5C2808E4DC311ED3391F9E07082D81F041
Info (19848): Design hash is 347A58374F4AF52344E01580A8124AAF51D3EF625F8A5482BD45B8BDFD408B87
Info (19848): IO hash is C8588DD7D8E255F95DF0E6BA02FD7880116E1815B6F26408D7085B0955E8A0
Info (19848): Keyed hash is 6DE339E0DAE1D5118413F8DD4CCA741FB52808F973047DA798DD885454D09E4D9
Info: Quartus Prime Programming File Generator was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 1109 megabytes
Info: Processing ended: Mon Jun 2 13:19:16 2025
Info: Elapsed time: 00:00:08
Info: System process ID: 19376
```

5. Connect the Titan S10 SOM EVK board to your host PC using a USB Type-C cable and power on the board.
6. Run `flash_program.bat` to program `golden_top.jic` into the QSPI flash.

```
C:\Windows\system32\cmd.exe
FPGA Configure...
Info: *****
Info: Running Quartus Prime Programmer
Info: Version 24.3.0 Build 212 11/18/2024 SC Pro Edition
Info: Copyright (C) 2024 Intel Corporation. All rights reserved.
Info: Your use of Intel Corporation's design tools, logic functions
Info: and other software and tools, and any partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Intel Program License
Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
Info: the Intel FPGA IP License Agreement, or other applicable license
Info: agreement, including, without limitation, that your use is for
Info: the sole purpose of programming logic devices manufactured by
Info: Intel and sold by Intel or its authorized distributors. Please
Info: refer to the Intel FPGA Software License Subscription Agreements
Info: on the Quartus Prime software download page.
Info: Processing started: Mon Jun 2 13:21:38 2025
Info: System process ID: 24940
Info: Command: quartus_pgm -m jtag -c 1 -o pvi:golden_top.jic
Info (213045): Using programming cable "Titan S10 [USB-1]"
Info (213011): Using programming file golden_top.jic with checksum 0xDE0BD01A for device 15X110HN3@1
Info (209060): Started Programmer operation at Mon Jun 2 13:21:41 2025
Info (18942): Configuring device index 1
Info (18943): Configuration succeeded at device index 1
Info (19094): Erasing flash chip select 0 at device index 1
Info (19096): Programming flash chip select 0 at device index 1
Info (19097): Verifying flash chip select 0 at device index 1
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Mon Jun 2 13:22:19 2025
Info: Quartus Prime Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 1359 megabytes
Info: Processing ended: Mon Jun 2 13:22:19 2025
Info: Elapsed time: 00:00:41
Info: System process ID: 24940
```

6.2 Restoring Factory Image into QSPI Flash

The Titan S10 SOM QSPI flash contains a factory image with the first-stage bootloader for HPS. The following steps restore the factory image to the QSPI flash:

1. Navigate to the folder:
 /Demonstration/SoC_FPGA/GHRD/output_files/program_qspi_flash/.
2. Connect the Titan S10 SOM EVK board to your host PC using a USB Type-C cable and power on the board.
3. Execute `flash_erase_hps.bat` to erase existing data from the flash.
4. Execute `flash_program_hps.bat` to program the factory image (`golden_top_hps.hps.jic`) located in the parent directory into the flash.

Chapter 7

Assembling and Disassembling the SOM and Carrier Board

This chapter explains how to assemble and disassemble the Titan S10 SOM and Terasic carrier board. Users can refer to the video below for step-by-step guidance, including the required tools for the process.

<https://www.youtube.com/watch?v=RbhVenAc4ps>



Chapter 8

Additional Information

8.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Agilex 7 FPGA Starter Kit Web: A7SK.terasic.com

Revision History

Date	Version	Changes
2023.05	First publication	
2023.07	V1.1	Update section 2.4 and 2.5
2023.08	V1.2	Update PCIe demo path
2023.11	V1.3	Add Section 2.2 Clock controller
2024.04	V1.4	Add section 2.7 HDMI TX