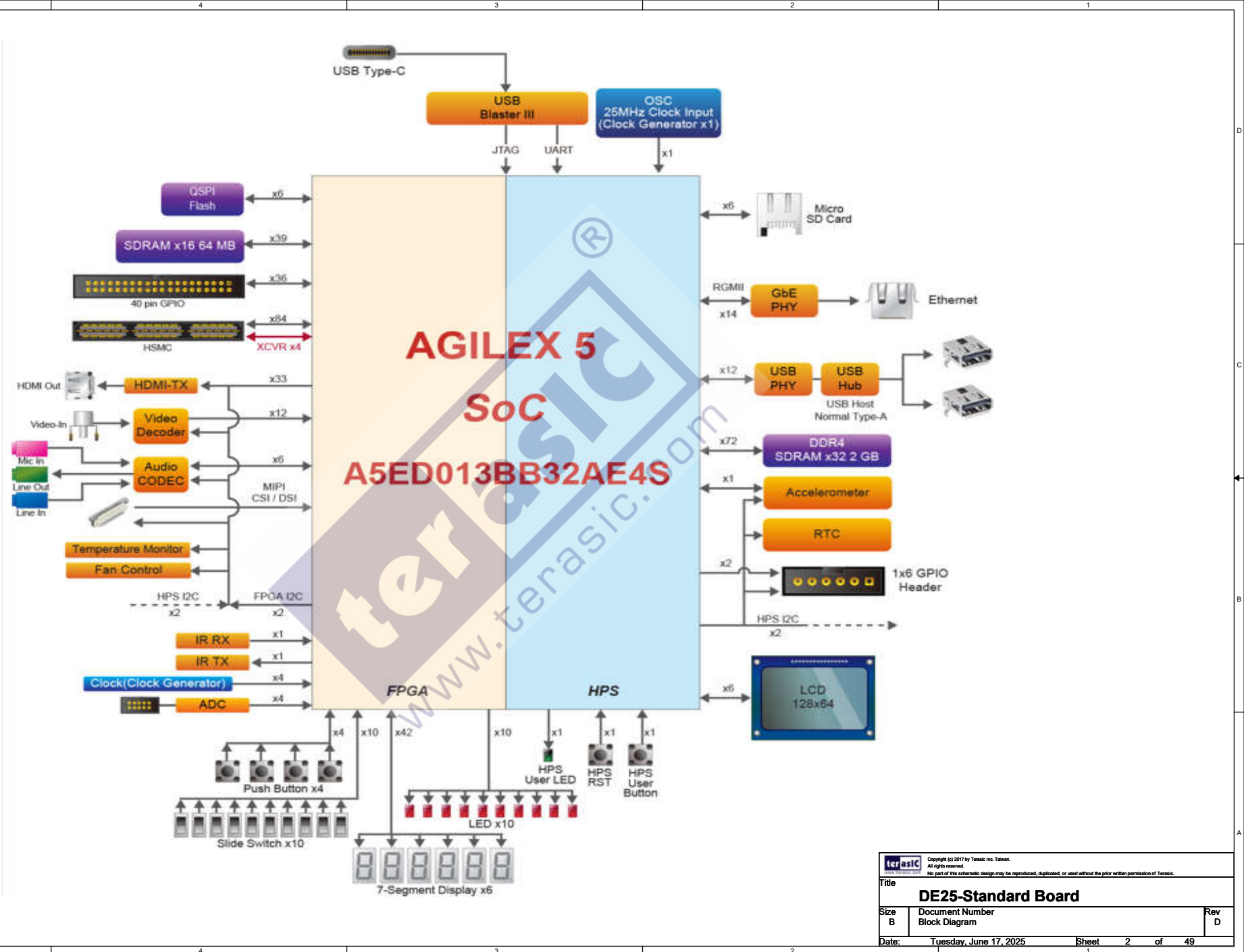
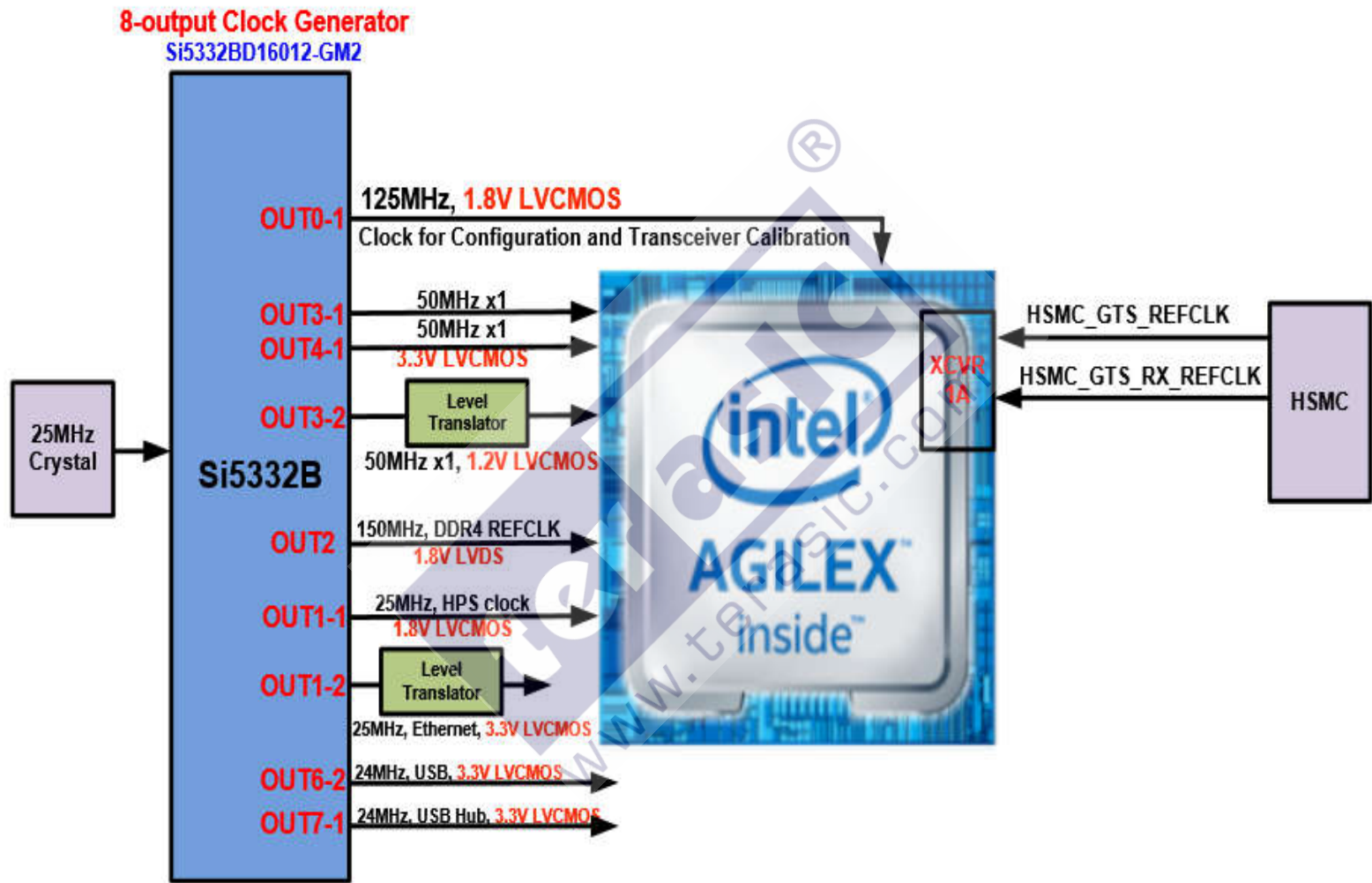


Block Diagram



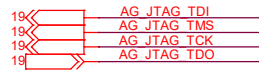
Clock Tree



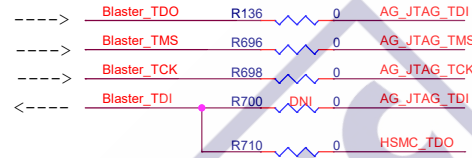
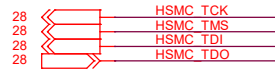
### USB Blaster III



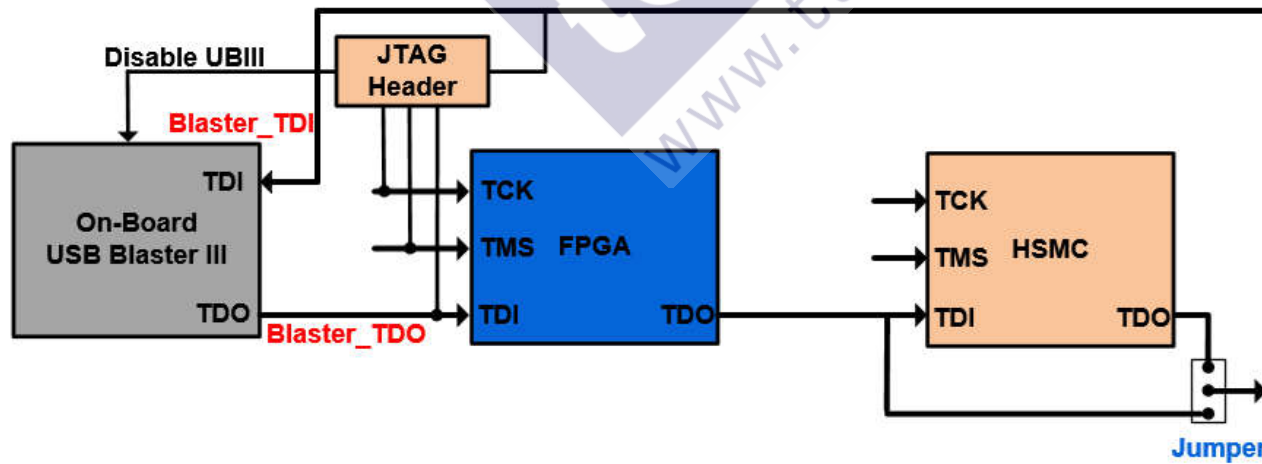
### FPGA JTAG INTERFACE



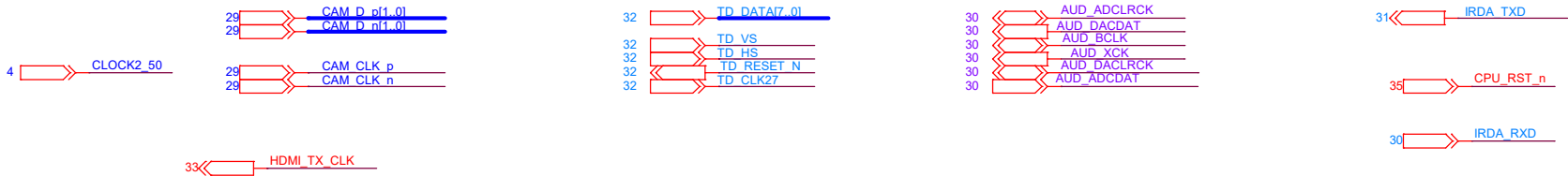
### HSMC JTAG INTERFACE



## JTAG Chain



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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	JTAG Chain	D
Date:	Tuesday, June 17, 2025	Sheet 6 of 49



U30C

VCCIO = 1.2V

HDMI\_TX\_CLK CH59  
SW7 CF59  
HEX56 CH62  
LEDR6 CF62  
LEDR5 CC62  
LEDR4 CA62  
LEDR3 CF69  
LEDR2 CH69  
LEDR8 CA71  
LEDR0 CC71  
KEY3 CH71  
KEY2 CF71  
KEY1 CA59  
KEY0 BW59  
SW9 BR59  
SW8 BU59  
LEDR9 BR62  
SW6 BU62  
CAM\_CLK\_n CA69  
CAM\_CLK\_p BW69  
CAM\_D\_n1 BU71  
CAM\_D\_p1 BR71  
CAM\_D\_n0 BU69  
CAM\_D\_p0 BR69  
SW5 BK59  
SW4 BM59  
SW3 BH59  
SW2 BH62  
SW1 BP62  
SW0 BM62  
HEX52 BK69  
LEDR7 BM69  
HEX55 BH71  
CAM\_RZQ1 BH69  
HEX53 BP71  
CLOCK2\_50 BM71  
TD\_DATA0 BF72  
TD\_CLK27 BF75  
TD\_DATA1 BE75  
TD\_DATA2 BE79  
TD\_DATA3 BF83  
TD\_DATA4 BE83  
TD\_DATA5 BE86  
TD\_DATA6 BF86  
TD\_DATA7 BF90  
TD\_RESET\_N BF93  
TD\_HS BE93  
TD\_VS BE96

BANK 2AT

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

BANK 2AB

I/O Lane 3

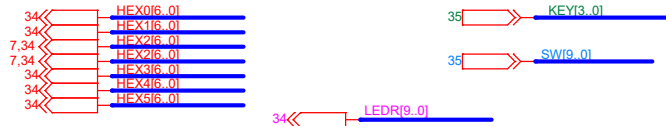
I/O Lane 2


I/O Lane 1

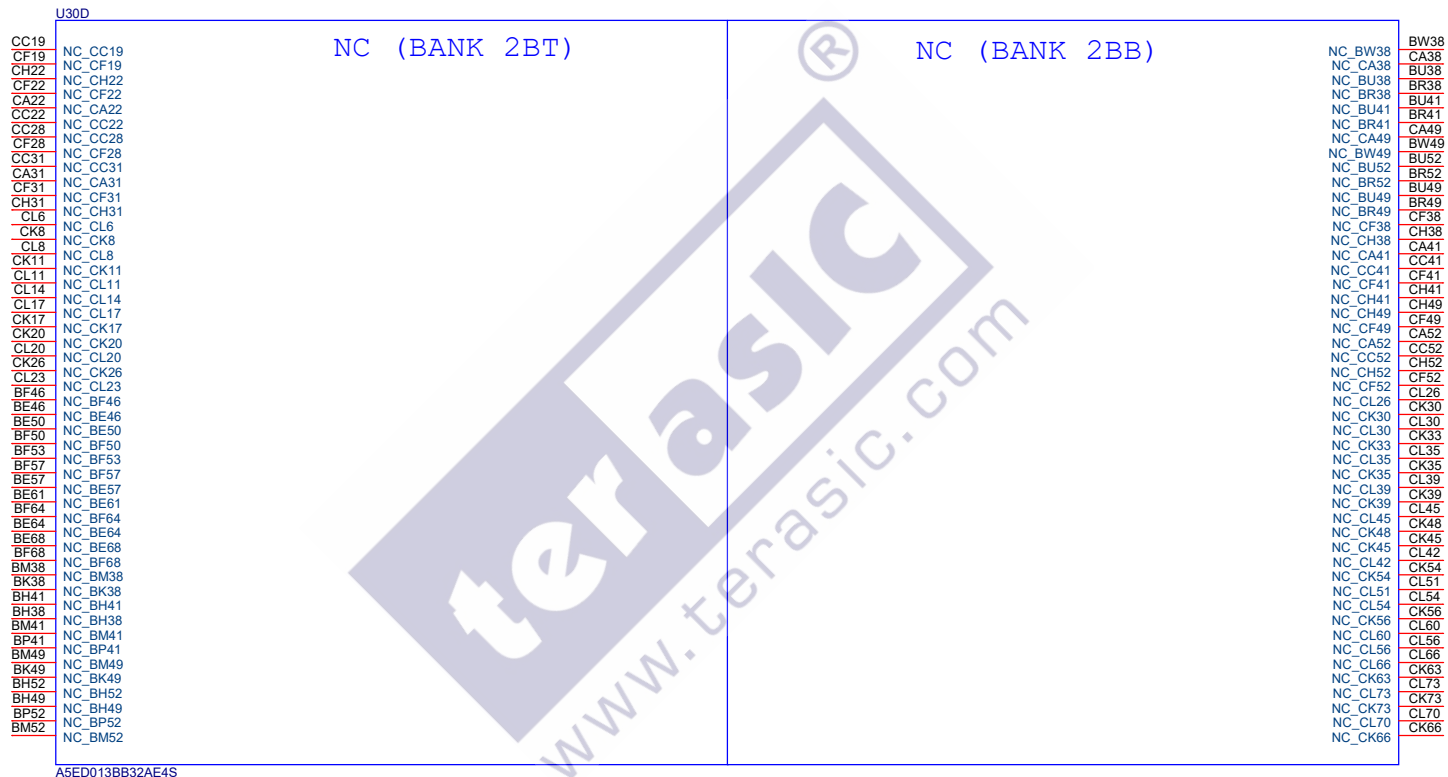
I/O Lane 0

IOB\_CDR\_DIFF\_IO\_2A\_B1N, DQ4  
IOB\_CDR\_DIFF\_IO\_2A\_B1P, DQ4  
IOB\_DIFF\_IO\_2A\_B2N, DQ4  
IOB\_DIFF\_IO\_2A\_B2P, DQ4  
IOB\_DIFF\_IO\_2A\_B3N, DQ4  
IOB\_DIFF\_IO\_2A\_B3P, DQ4  
IOB\_PLL\_2A\_B\_CLKOUT1N, DIFF\_IO\_2A\_B4N, DQSN4  
IOB\_PLL\_2A\_B\_CLKOUT1P, PLL\_2A\_B\_CLKOUT1, PLL\_2A\_B\_FB1, DIFF\_IO\_2A\_B4P, DQSN4  
IOB\_CDR\_DIFF\_IO\_2A\_B5N, DQ4  
IOB\_RZQ\_B\_2A, CDR\_DIFF\_IO\_2A\_B5P, DQ4  
IOB\_CLK\_B\_2A\_1N, DIFF\_IO\_2A\_B6N, DQ4  
IOB\_CLK\_B\_2A\_1P, DIFF\_IO\_2A\_B6P, DQ4  
IOB\_CLK\_B\_2A\_0N, CDR\_DIFF\_IO\_2A\_B7P, DQ5  
IOB\_CLK\_B\_2A\_0P, CDR\_DIFF\_IO\_2A\_B8P, DQ5  
IOB\_DIFF\_IO\_2A\_B8N, DQ5  
IOB\_DIFF\_IO\_2A\_B8P, DQ5  
IOB\_PLL\_2A\_B\_CLKOUT0N, DIFF\_IO\_2A\_B9N, DQ5  
IOB\_PLL\_2A\_B\_CLKOUT0P, PLL\_2A\_B\_CLKOUT0, PLL\_2A\_B\_FB0, DIFF\_IO\_2A\_B9P, DQ5  
IOB\_DIFF\_IO\_2A\_B10N, DQSN5  
IOB\_DIFF\_IO\_2A\_B10P, DQSN5  
IOB\_CDR\_DIFF\_IO\_2A\_B11N, DQ5  
IOB\_CDR\_DIFF\_IO\_2A\_B11P, DQ5  
IOB\_DIFF\_IO\_2A\_B12N, DQ5  
IOB\_DIFF\_IO\_2A\_B12P, DQ5  
IOB\_CDR\_DIFF\_IO\_2A\_B13N, DQ6  
IOB\_CDR\_DIFF\_IO\_2A\_B13P, DQ6  
IOB\_DIFF\_IO\_2A\_B14N, DQ6  
IOB\_DIFF\_IO\_2A\_B14P, DQ6  
IOB\_DIFF\_IO\_2A\_B15N, DQ6  
IOB\_DIFF\_IO\_2A\_B15P, DQ6  
IOB\_DIFF\_IO\_2A\_B16N, DQSN6  
IOB\_DIFF\_IO\_2A\_B16P, DQSN6  
IOB\_CDR\_DIFF\_IO\_2A\_B17N, DQ6  
IOB\_CDR\_DIFF\_IO\_2A\_B17P, DQ6  
IOB\_DIFF\_IO\_2A\_B18N, DQ6  
IOB\_DIFF\_IO\_2A\_B18P, DQ6  
IOB\_CDR\_DIFF\_IO\_2A\_B19N, DQ7  
IOB\_CDR\_DIFF\_IO\_2A\_B19P, DQ7  
IOB\_DIFF\_IO\_2A\_B20N, DQ7  
IOB\_DIFF\_IO\_2A\_B20P, DQ7  
IOB\_DIFF\_IO\_2A\_B21N, DQ7  
IOB\_DIFF\_IO\_2A\_B21P, DQ7  
IOB\_DIFF\_IO\_2A\_B22N, DQSN7  
IOB\_DIFF\_IO\_2A\_B22P, DQSN7  
IOB\_CDR\_DIFF\_IO\_2A\_B23N, DQ7  
IOB\_CDR\_DIFF\_IO\_2A\_B23P, DQ7  
IOB\_DIFF\_IO\_2A\_B24N, DQ7  
IOB\_DIFF\_IO\_2A\_B24P, DQ7


BK78 IRDA\_TXD  
BM78 CPU\_RST\_n  
BH78 LEDR1  
BH81 IRDA\_RXD  
BP81 HEX00  
BM81 HEX01  
BM89 HEX02  
BK89 HEX03  
BH89 HEX04  
BH89 HEX05  
BM92 HEX06  
CA78 HEX10  
BW78 HEX11  
BU78 HEX12  
BR78 HEX13  
BU81 HEX14  
BR81 HEX15  
CA89 HEX16  
BW89 HEX20  
BU89 HEX21  
BR92 HEX22  
BU89 HEX23  
BR89 HEX24  
CF78 HEX25  
CH78 HEX26  
CC81 HEX30  
CA81 HEX31  
CH81 HEX32  
CF81 HEX33  
CF89 HEX34  
CH89 HEX35  
CH92 HEX36  
CF92 HEX40  
CA92 HEX41  
CC92 HEX42  
CL76 HEX43  
CK76 HEX44  
CL82 HEX45  
CK80 HEX46  
CL85 HEX50  
CK85 HEX51  
CK88 AUD\_ADCLCK  
CL88 AUD\_DACDAT  
CL97 AUD\_BCLK  
CK97 AUD\_XCLK  
CK94 AUD\_DACLCK  
CL91 AUD\_ADCDATA



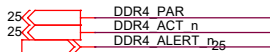
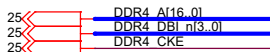
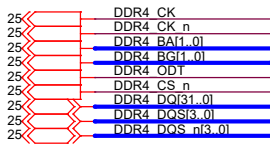
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Title <b>DE25-Standard Board</b>		
Size B	Document Number FPGA Bank 2A	Rev D
Date:	Tuesday, June 17, 2025	Sheet 7 of 49



A5ED013BB32AE4S

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Title <b>DE25-Standard Board</b>		
Size <b>B</b>	Document Number <b>FPGA NC (2B)</b>	Rev <b>D</b>
Date: <b>Tuesday, June 17, 2025</b>	Sheet <b>8</b>	of <b>49</b>

## DDR4



RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14

DDR4_DQ25	D84
DDR4_DQ29	F84
DDR4_DQ31	M87
DDR4_DQ27	K87
DDR4_DBI_n3	F87
DDR4_DQS_n3	H87
DDR4_DQS3	D95
DDR4_DQ26	F95
DDR4_DQ24	M98
DDR4_DQ28	F98
DDR4_DQ30	H98
DDR4_DQ23	P84
DDR4_DQ22	T84
DDR4_DQ19	M84
DDR4_DQ17	K84
DDR4_DBI_n2	T87
DDR4_DQS_n2	V87
DDR4_DQS2	K95
DDR4_DQ16	T95
DDR4_DQ18	P95
DDR4_DQ20	T98
DDR4_DQ21	V98
DDR4_DQ15	Y84
DDR4_DQ13	Y87
DDR4_DQ11	Y95
DDR4_DQ9	Y98
DDR4_DBI_n1	AC86
DDR4_DQS_n1	AC90
DDR4_DQS1	AC93
DDR4_DQ12	AC96
DDR4_DQ14	AC100
DDR4_DQ10	AG104
DDR4_DQ8	AG100

U30E

## BANK 3AT

A91	IOB, DIFF_IO_3A_T1N, DQ16
B88	IOB, DIFF_IO_3A_T1P, DQ16
A94	IOB, DIFF_IO_3A_T2N, DQ16
B91	IOB, DIFF_IO_3A_T2P, DQ16
A97	IOB, DIFF_IO_3A_T3N, DQ16
B97	IOB, DIFF_IO_3A_T3P, DQ16
B101	IOB, DIFF_IO_3A_T3P, DQ16, AVST_READY
A101	IOB, DIFF_IO_3A_T4N, DQSN16
A110	IOB, DIFF_IO_3A_T4P, DQSN16
B106	IOB, CDR, DIFF_IO_3A_T5N, DQ16
B103	IOB, CDR, DIFF_IO_3A_T5P, DQ16
A106	IOB, DIFF_IO_3A_T6N, DQ16
D84	IOB, DIFF_IO_3A_T6P, DQ16
F84	IOB, DIFF_IO_3A_T7N, DQ17, AVST_DATA10
M87	IOB, DIFF_IO_3A_T7P, DQ17, AVST_DATA9
K87	IOB, DIFF_IO_3A_T8N, DQ17, AVST_DATA8
F87	IOB, DIFF_IO_3A_T8P, DQ17, AVST_VALID
H87	IOB, DIFF_IO_3A_T9N, DQ17, AVST_DATA7
D95	IOB, DIFF_IO_3A_T9P, DQ17, AVST_DATA6
F95	IOB, DIFF_IO_3A_T10N, DQSN17, AVST_DATA5
K98	IOB, DIFF_IO_3A_T10P, DQSN17, AVST_DATA4
M98	IOB, CDR, DIFF_IO_3A_T11N, DQ17, AVST_DATA3
F98	IOB, CDR, DIFF_IO_3A_T11P, DQ17, AVST_DATA2
H98	IOB, DIFF_IO_3A_T12N, DQ17, AVST_DATA1
P84	IOB, DIFF_IO_3A_T12P, DQ17, AVST_DATA0
T84	IOB, DIFF_IO_3A_T13N, DQ18
M84	IOB, DIFF_IO_3A_T13P, DQ18
K84	IOB, DIFF_IO_3A_T14N, DQ18
T87	IOB, DIFF_IO_3A_T14P, DQ18
V87	IOB, DIFF_IO_3A_T15N, DQ18
M95	IOB, DIFF_IO_3A_T15P, DQ18
K95	IOB, PLL_3A_T_CLKOUT1N, DIFF_IO_3A_T16N, DQSN18
T95	IOB, PLL_3A_T_CLKOUT1P, PLL_3A_T_CLKOUT1, PLL_3A_T_FB1, DIFF_IO_3A_T16P, DQSN18
P95	IOB, CDR, DIFF_IO_3A_T17N, DQ18
T98	IOB, RZQ_T_3A, CDR, DIFF_IO_3A_T17P, DQ18
V98	IOB, CLK_T_3A_1N, DIFF_IO_3A_T18N, DQ18
Y84	IOB, CLK_T_3A_1P, DIFF_IO_3A_T18P, DQ18
Y87	IOB, CLK_T_3A_0N, DIFF_IO_3A_T19N, DQ19
Y95	IOB, CLK_T_3A_0P, DIFF_IO_3A_T19P, DQ19
Y98	IOB, DIFF_IO_3A_T20N, DQ19
AC86	IOB, DIFF_IO_3A_T20P, DQ19
AC90	IOB, PLL_3A_T_CLKOUT0N, DIFF_IO_3A_T21N, DQ19
AC93	IOB, PLL_3A_T_CLKOUT0P, PLL_3A_T_CLKOUT0, PLL_3A_T_FB0, DIFF_IO_3A_T21P, DQ19
AC96	IOB, DIFF_IO_3A_T22N, DQSN19, AVST_CLK
AC96	IOB, DIFF_IO_3A_T22P, DQSN19, AVST_DATA15
AC100	IOB, CDR, DIFF_IO_3A_T23N, DQ19, AVST_DATA14
AG104	IOB, CDR, DIFF_IO_3A_T23P, DQ19, AVST_DATA13
AG100	IOB, DIFF_IO_3A_T24N, DQ19, AVST_DATA12
	IOB, DIFF_IO_3A_T24P, DQ19, AVST_DATA11

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

VCCIO = 1.2V

## BANK 3AB

IOB, CDR, DIFF_IO_3A_B1N, DQ20
IOB, CDR, DIFF_IO_3A_B1P, DQ20
IOB, DIFF_IO_3A_B2N, DQ20
IOB, DIFF_IO_3A_B2P, DQ20
IOB, DIFF_IO_3A_B3N, DQ20
IOB, DIFF_IO_3A_B3P, DQ20
IOB, PLL_3A_B_CLKOUT1N, DIFF_IO_3A_B4N, DQSN20
IOB, PLL_3A_B_CLKOUT1P, PLL_3A_B_CLKOUT1, PLL_3A_B_FB1, DIFF_IO_3A_B4P, DQSN20
IOB, CDR, DIFF_IO_3A_B5N, DQ20
IOB, RZQ_B_3A, CDR, DIFF_IO_3A_B5P, DQ20
IOB, CLK_B_3A_1N, DIFF_IO_3A_B6N, DQ20
IOB, CLK_B_3A_1P, DIFF_IO_3A_B6P, DQ20
IOB, DIFF_IO_3A_B7N, DQ21
IOB, CLK_B_3A_0N, CDR, DIFF_IO_3A_B7P, DQ21
IOB, CLK_B_3A_0P, CDR, DIFF_IO_3A_B7P, DQ21
IOB, DIFF_IO_3A_B8N, DQ21
IOB, DIFF_IO_3A_B8P, DQ21
IOB, PLL_3A_B_CLKOUT0N, DIFF_IO_3A_B9N, DQ21
IOB, PLL_3A_B_CLKOUT0P, PLL_3A_B_CLKOUT0, PLL_3A_B_FB0, DIFF_IO_3A_B9P, DQ21
IOB, DIFF_IO_3A_B10N, DQSN21
IOB, DIFF_IO_3A_B10P, DQSN21
IOB, CDR, DIFF_IO_3A_B11N, DQ21
IOB, CDR, DIFF_IO_3A_B11P, DQ21
IOB, DIFF_IO_3A_B12N, DQ21
IOB, DIFF_IO_3A_B12P, DQ21
IOB, CDR, DIFF_IO_3A_B13N, DQ22
IOB, CDR, DIFF_IO_3A_B13P, DQ22
IOB, DIFF_IO_3A_B14N, DQ22
IOB, DIFF_IO_3A_B14P, DQ22
IOB, DIFF_IO_3A_B15N, DQ22
IOB, DIFF_IO_3A_B15P, DQ22
IOB, DIFF_IO_3A_B16N, DQSN22
IOB, DIFF_IO_3A_B16P, DQSN22
IOB, CDR, DIFF_IO_3A_B17N, DQ22
IOB, CDR, DIFF_IO_3A_B17P, DQ22
IOB, DIFF_IO_3A_B18N, DQ22
IOB, DIFF_IO_3A_B18P, DQ22
IOB, CDR, DIFF_IO_3A_B19N, DQ23
IOB, CDR, DIFF_IO_3A_B19P, DQ23
IOB, DIFF_IO_3A_B20N, DQ23
IOB, DIFF_IO_3A_B20P, DQ23
IOB, DIFF_IO_3A_B21N, DQ23
IOB, DIFF_IO_3A_B21P, DQ23
IOB, DIFF_IO_3A_B22N, DQSN23
IOB, DIFF_IO_3A_B22P, DQSN23
IOB, CDR, DIFF_IO_3A_B23N, DQ23
IOB, CDR, DIFF_IO_3A_B23P, DQ23
IOB, DIFF_IO_3A_B24N, DQ23
IOB, DIFF_IO_3A_B24P, DQ23

I/O Lane 3


I/O Lane 2

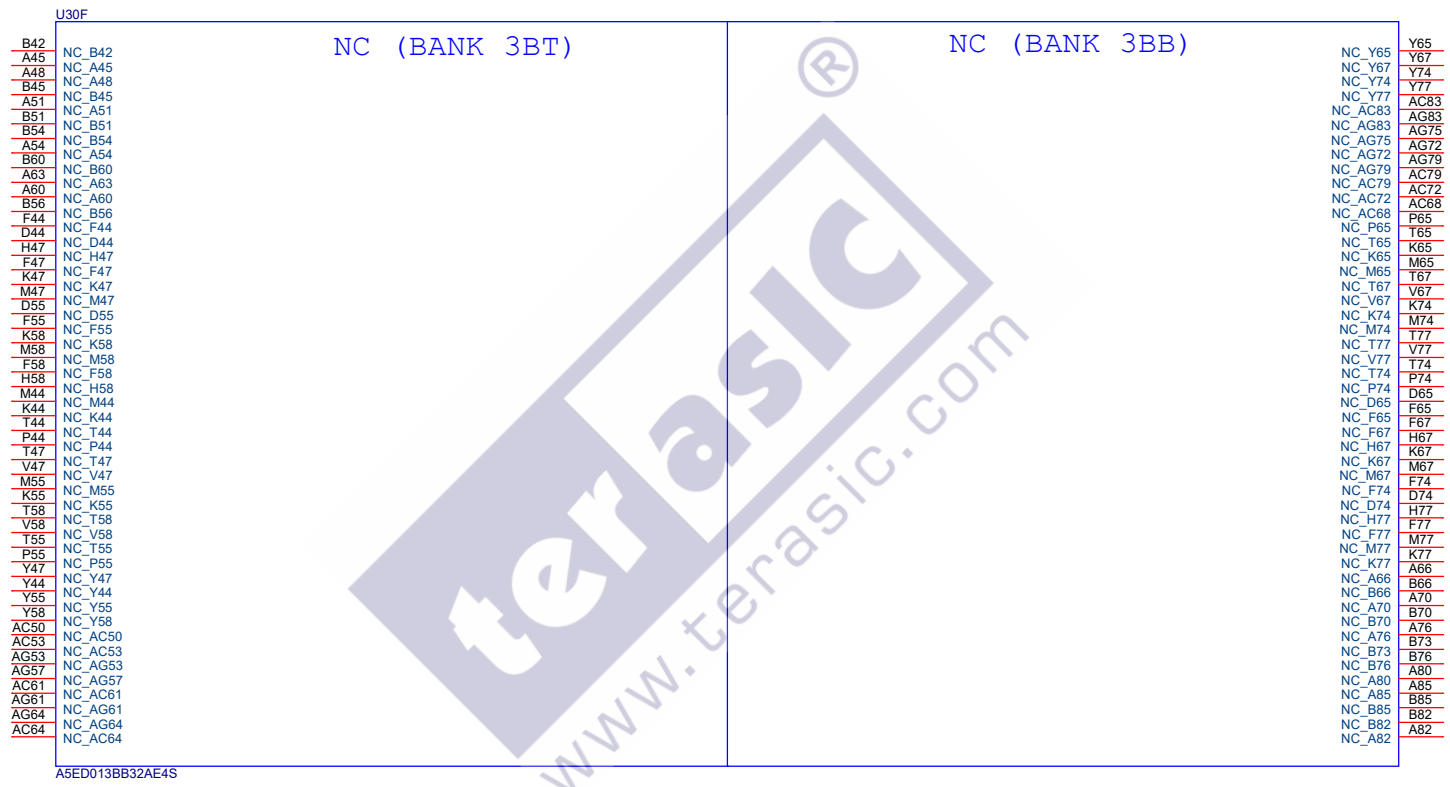
I/O Lane 1

I/O Lane 0

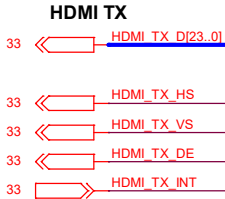
AB105	DDR4_BG0
Y105	DDR4_BA1
AB108	DDR4_BA0
Y108	DDR4_ALERT_n
AK104	DDR4_A16
AK107	DDR4_A15
AB114	DDR4_A14
Y114	DDR4_A13
AG111	DDR4_A12
AK111	RZQ_B_3A_R418
Y117	DDR4_REFCLK_n
AB117	DDR4_REFCLK_p
K105	DDR4_A11
M105	DDR4_A10
P105	DDR4_A9
T105	DDR4_A8
T108	DDR4_A7
V108	DDR4_A6
K114	DDR4_A5
M114	DDR4_A4
T117	DDR4_A3
P114	DDR4_A2
T114	DDR4_A1
K108	DDR4_PAR
M108	
F108	DDR4_CK_n
H108	DDR4_CK
D105	
F105	DDR4_CKE
D114	
F114	DDR4_ODT
M117	DDR4_ACT_n
K117	DDR4_CS_n
H117	DDR4_RESET_n
F117	DDR4_BG1
A113	DDR4_DQ7
B113	DDR4_DQ5
A116	DDR4_DQ1
B116	DDR4_DQ3
A122	
B119	DDR4_DBI_n0
A125	DDR4_DQS_n0
B122	DDR4_DQS0
A130	DDR4_DQ6
B130	DDR4_DQ4
A128	DDR4_DQ2
B128	DDR4_DQ0



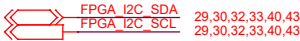
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Title <b>DE25-Standard Board</b>		
Size B	Document Number FPGA Bank 3A	Rev D
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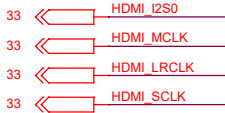




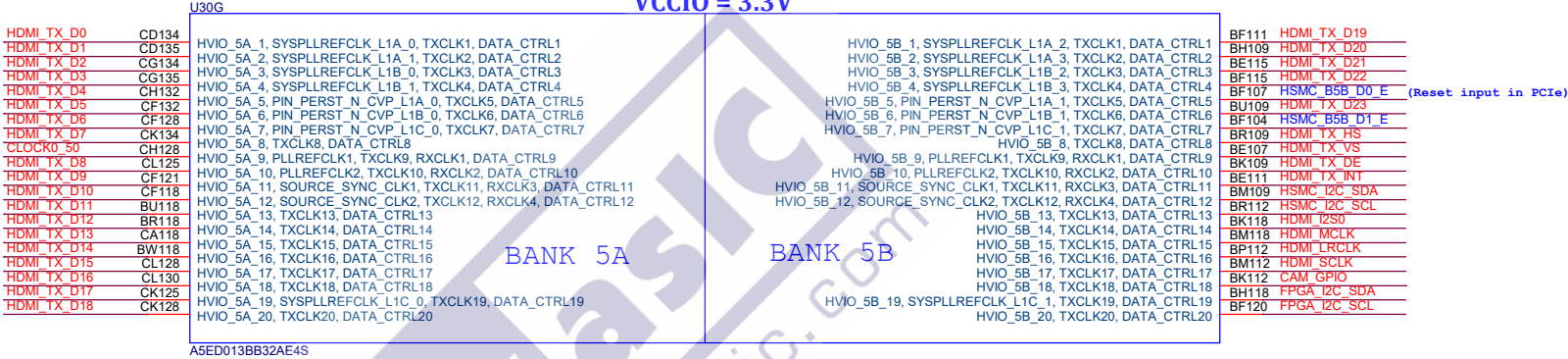
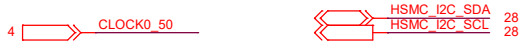
FPGA I2C Interface



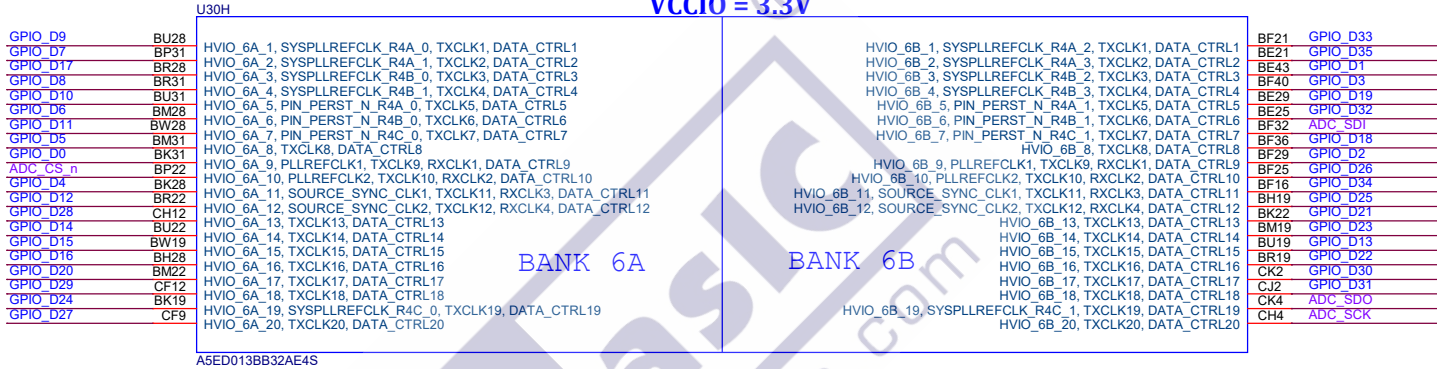
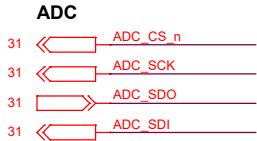
HDMI Audio Interface



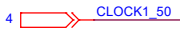
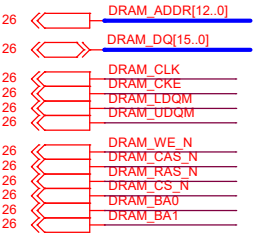
HSMC I2C Interface



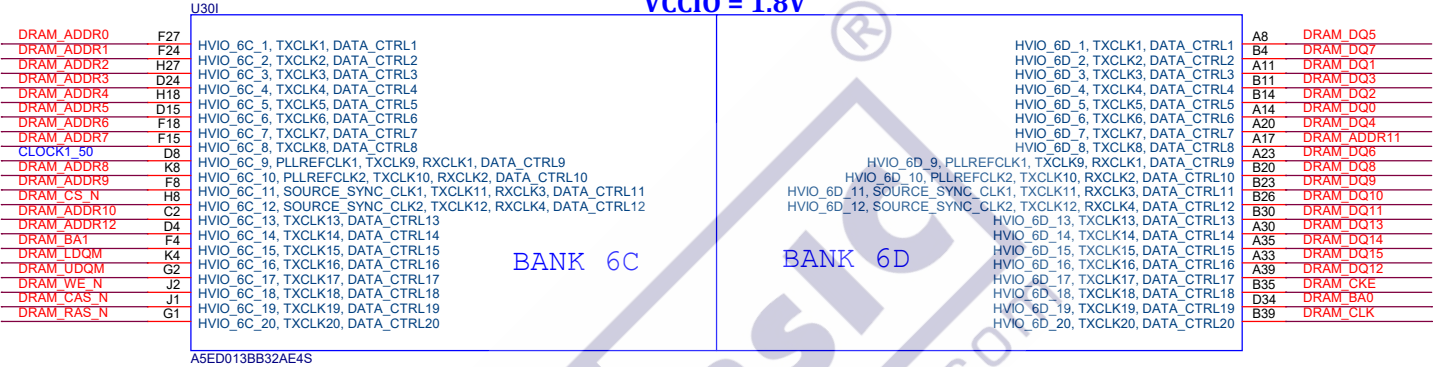




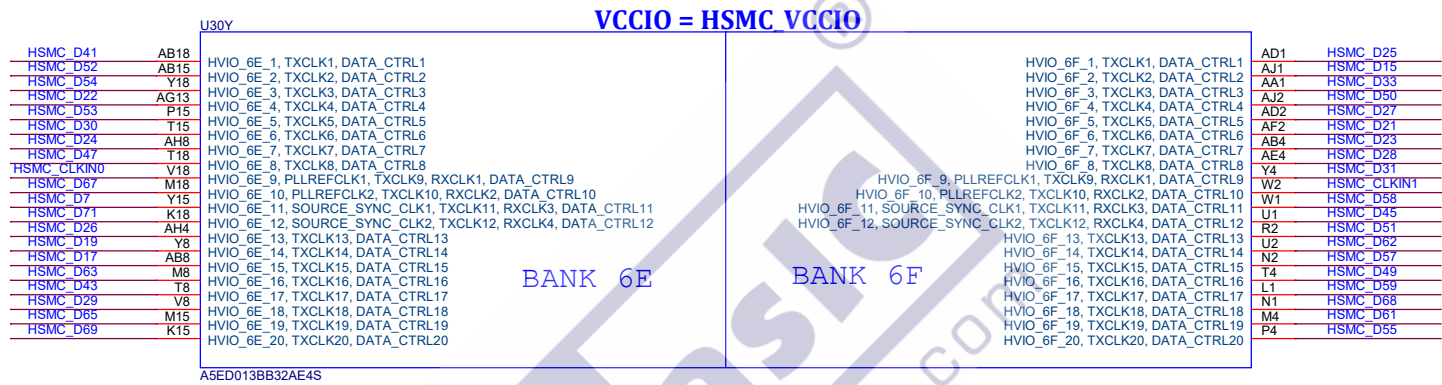
SDRAM




VCCIO = 1.8V

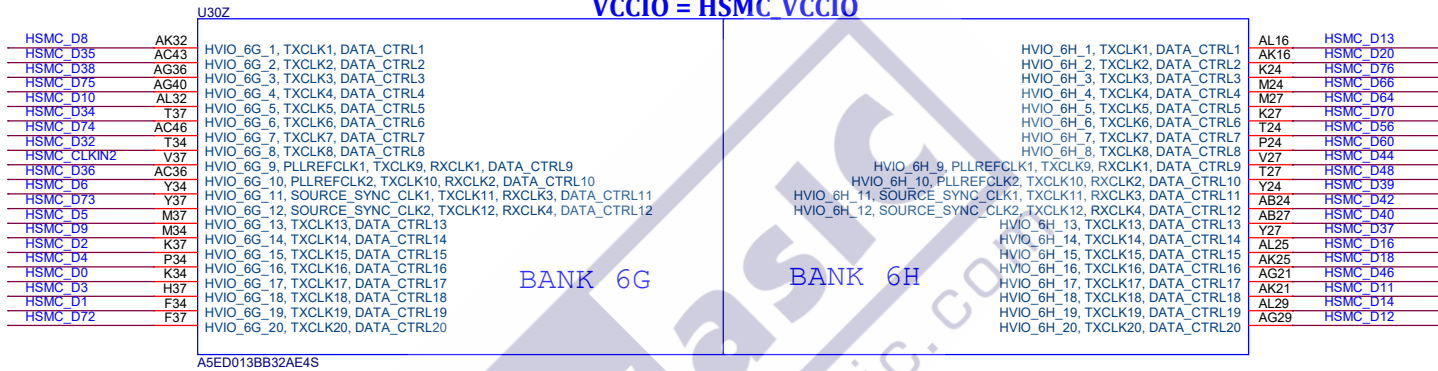


15,28 <<>> HSMC\_D[76..0]  
15,28 <<>> HSMC\_CLKIN[2..0]

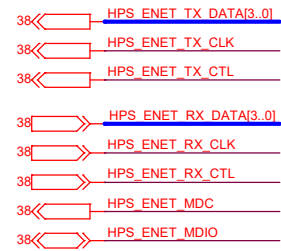


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Title	
DE25-Standard Board	
Size	Document Number
B	FPGA Bank 6E - 6F
Date:	Tuesday, June 17, 2025
Sheet	14 of 49
Rev	D

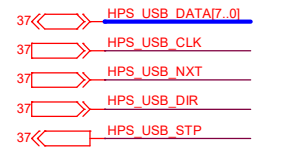
14,28 << HSMC\_D[76..0]  
14,28 << HSMC\_CLKIN[2..0]



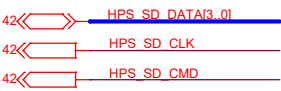
Ethernet PHY Interface (RGMII)



UBS PHY Interface (ULPI)



SD Card



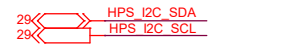
HPS 25MHz Clock



HPS GPIO



HPS I2C Interface



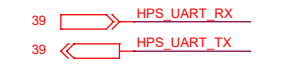
HPS User Button



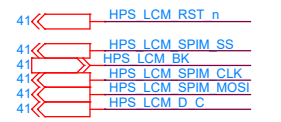
HPS User LED



UART Interface



HPS LCD



HPS_USB_CLK	W135
HPS_USB_STP	U135
HPS_USB_DIR	W134
HPS_USB_DATA0	AK115
HPS_USB_DATA1	U134
HPS_USB_NXT	AL120
HPS_USB_DATA2	R134
HPS_USB_DATA3	AG115
HPS_USB_DATA4	N135
HPS_USB_DATA5	AK120
HPS_USB_DATA6	N134
HPS_USB_DATA7	T132
HPS_ENET_TX_CTL	P132
HPS_ENET_TX_CLK	L135
HPS_ENET_RX_CLK	J135
HPS_ENET_RX_CTL	AD135
HPS_ENET_TX_DATA0	M132
HPS_ENET_TX_DATA1	AD134
HPS_ENET_RX_DATA0	K132
HPS_ENET_RX_DATA1	AG129
HPS_ENET_TX_DATA2	J134
HPS_ENET_TX_DATA3	AG120
HPS_ENET_RX_DATA2	G134
HPS_ENET_RX_DATA3	G135

HPS_SD_DATA0	E135
HPS_SD_DATA1	F132
HPS_SD_CLK	D132
HPS_CLK_25	AG123
HPS_GSENSOR_INT	B134
HPS_SD_DATA2	AA135
HPS_SD_DATA3	V127
HPS_SD_CMD	AB132
HPS_GPIO0	T127
HPS_LCM_RST_n	T124
HPS_LCM_D_C	P124
HPS_I2C_SDA	M127
HPS_I2C_SCL	K127
HPS_UART_TX	M124
HPS_UART_RX	AB127
HPS_KEY	K124
HPS_LED	Y127
HPS_LCM_BK	H127
HPS_LCM_SPIM_SS	AB124
HPS_LCM_SPIM_CLK	F127
HPS_LCM_SPIM_MOSI	Y124
HPS_ENET_MDIO	F124
HPS_ENET_MDC	D124


U30B

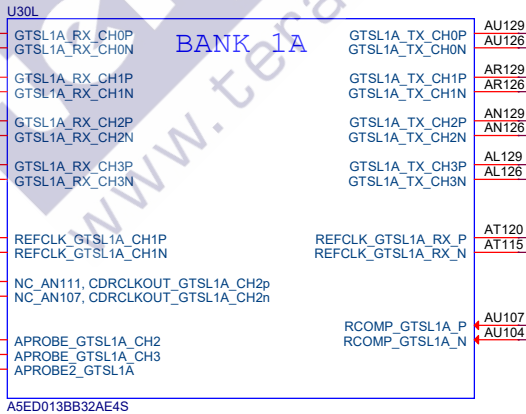
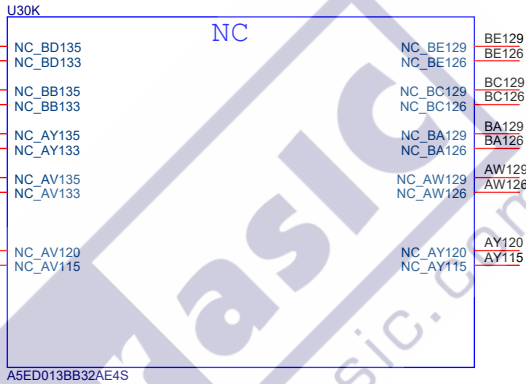
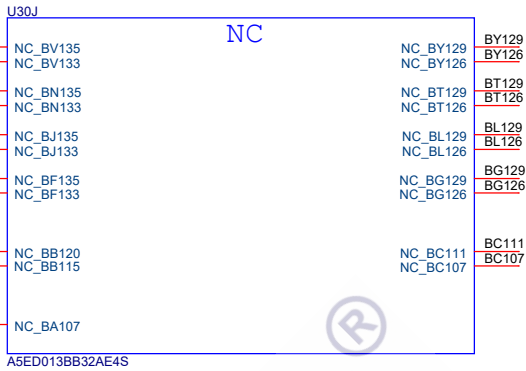
HPS\_IOA\_1, GPIO0\_IO0, SPIM0\_SS1\_N, SPIS0\_CLK, UART0\_CTS\_N, NAND\_ADQ0, SDMMC\_DATA0, USB0\_CLK, EMAC0\_PPS0, TRACE\_D10  
HPS\_IOA\_2, GPIO0\_IO1, SPIM1\_SS1\_N, SPIS0\_MOSI, UART0\_RTS\_N, NAND\_ADQ1, SDMMC\_DATA1, USB0\_STP, EMAC0\_PPSTRIG0, TRACE\_D9  
HPS\_IOA\_3, GPIO0\_IO2, SPIS0\_SS0\_N, UART0\_TX, I2C1\_SDA, NAND\_WE\_N, SDMMC\_CLK, USB0\_DIR, EMAC1\_PPS1, TRACE\_D8  
HPS\_IOA\_4, GPIO0\_IO3, SPIS0\_MISO, UART0\_RX, I2C1\_SCL, NAND\_RE\_N, USB0\_DATA0, EMAC1\_PPSTRIG1, TRACE\_D7  
HPS\_IOA\_5, GPIO0\_IO4, SPIM0\_CLK, UART1\_CTS\_N, I2C0\_SDA, NAND\_WP\_N, SDMMC\_WRITE\_PROTECT, USB0\_DATA1, EMAC2\_PPS2, TRACE\_D6  
HPS\_IOA\_6, GPIO0\_IO5, SPIM0\_MOSI, UART1\_RTS\_N, I2C0\_SCL, NAND\_ADQ2, SDMMC\_DATA2, USB0\_NXT, EMAC2\_PPSTRIG2, TRACE\_D5  
HPS\_IOA\_7, GPIO0\_IO6, SPIM0\_MISO, MDIO2\_MDIO, UART1\_TX, I2C\_EMAC2\_SDA, NAND\_ADQ3, SDMMC\_DATA3, USB0\_DATA2, TRACE\_D4  
HPS\_IOA\_8, GPIO0\_IO7, SPIM0\_SS0\_N, MDIO2\_MDC, UART1\_RX, I2C\_EMAC2\_SCL, NAND\_CLE, SDMMC\_CMD, USB0\_DATA3, TRACE\_D15  
HPS\_IOA\_9, GPIO0\_IO8, SPIM1\_CLK, SPIS1\_CLK, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ4, SDMMC\_DATA4, USB0\_DATA4, I3C1\_SDA, TRACE\_D14  
HPS\_IOA\_10, GPIO0\_IO9, SPIM1\_MOSI, SPIS1\_MOSI, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ5, SDMMC\_DATA5, USB0\_DATA5, I3C1\_SCL, TRACE\_D13  
HPS\_IOA\_11, GPIO0\_IO10, SPIM1\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, SDMMC\_DATA6, USB0\_DATA6, I3C0\_SDA, TRACE\_D12  
HPS\_IOA\_12, GPIO0\_IO11, SPIM1\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ7, SDMMC\_DATA7, USB0\_DATA7, I3C0\_SCL, TRACE\_D11  
HPS\_IOA\_13, GPIO0\_IO12, NAND\_ALE, SDMMC\_PU\_PD\_DATA2, USB1\_CLK, EMAC0\_TX\_CLK, TRACE\_D10  
HPS\_IOA\_14, GPIO0\_IO13, NAND\_RB\_N, SDMMC\_BUS\_PWR, USB1\_STP, EMAC0\_TX\_CTL, TRACE\_D9  
HPS\_IOA\_15, GPIO0\_IO14, NAND\_CE\_N, USB1\_DIR, EMAC0\_RX\_CLK, TRACE\_D8  
HPS\_IOA\_16, GPIO0\_IO15, NAND\_DQS, SDMMC\_DATA\_STROBE, USB1\_DATA0, EMAC0\_RX\_CTL, TRACE\_D7  
HPS\_IOA\_17, GPIO0\_IO16, I3C1\_SDA, NAND\_ADQ8, USB1\_DATA1, EMAC0\_TXD0, TRACE\_D6  
HPS\_IOA\_18, GPIO0\_IO17, I3C1\_SCL, NAND\_ADQ9, USB1\_NXT, EMAC0\_TXD1, TRACE\_D5  
HPS\_IOA\_19, GPIO0\_IO18, I3C0\_SDA, NAND\_ADQ10, USB1\_DATA2, EMAC0\_RXD0, TRACE\_D4  
HPS\_IOA\_20, GPIO0\_IO19, SPIM1\_SS1\_N, I3C0\_SCL, NAND\_ADQ11, USB1\_DATA3, EMAC0\_RXD1, TRACE\_CLK  
HPS\_IOA\_21, GPIO0\_IO20, SPIM1\_CLK, SPIS0\_CLK, UART0\_CTS\_N, I2C1\_SDA, NAND\_ADQ12, USB1\_DATA4, EMAC0\_TXD2, TRACE\_D0  
HPS\_IOA\_22, GPIO0\_IO21, SPIM1\_MOSI, SPIS0\_MOSI, UART0\_RTS\_N, I2C1\_SCL, NAND\_ADQ13, USB1\_DATA5, EMAC0\_TXD3, TRACE\_D1  
HPS\_IOA\_23, GPIO0\_IO22, SPIM1\_MISO, SPIS0\_SS0\_N, UART0\_TX, I2C0\_SDA, NAND\_ADQ14, USB1\_DATA6, EMAC0\_RXD2, TRACE\_D2  
HPS\_IOA\_24, GPIO0\_IO23, SPIM1\_SS0\_N, SPIS0\_MISO, UART0\_RX, I2C0\_SCL, NAND\_ADQ15, USB1\_DATA7, EMAC0\_RXD3, TRACE\_D3

HPS\_IOB\_1, GPIO1\_IO0, SPIM1\_CLK, CM\_PLL\_CLK0, UART0\_CTS\_N, EMAC0\_PPS0, NAND\_ADQ0, SDMMC\_DATA0, EMAC1\_TX\_CLK, TRACE\_D10  
HPS\_IOB\_2, GPIO1\_IO1, SPIM1\_MOSI, CM\_PLL\_CLK1, UART0\_RTS\_N, EMAC0\_PPSTRIG0, NAND\_ADQ1, SDMMC\_DATA1, EMAC1\_TX\_CTL, TRACE\_D9  
HPS\_IOB\_3, GPIO1\_IO2, SPIM1\_MISO, CM\_PLL\_CLK2, UART0\_TX, I2C0\_SDA, NAND\_WE\_N, SDMMC\_CLK, EMAC1\_RX\_CLK, TRACE\_D8  
HPS\_IOB\_4, GPIO1\_IO3, SPIM1\_SS0\_N, CM\_PLL\_CLK3, UART0\_RX, I2C0\_SCL, NAND\_RE\_N, EMAC1\_RX\_CTL, TRACE\_D7  
HPS\_IOB\_5, GPIO1\_IO4, SPIM1\_SS1\_N, SPIS1\_CLK, UART1\_CTS\_N, EMAC2\_PPS2, NAND\_WP\_N, SDMMC\_WRITE\_PROTECT, I3C1\_SDA, EMAC1\_TXD0, TRACE\_D6  
HPS\_IOB\_6, GPIO1\_IO5, SPIS1\_MOSI, UART1\_RTS\_N, EMAC2\_PPSTRIG2, NAND\_ADQ2, SDMMC\_DATA2, I3C1\_SCL, EMAC1\_TXD1, TRACE\_D5  
HPS\_IOB\_7, GPIO1\_IO6, SPIS1\_SS0\_N, I3C1\_SDA, NAND\_ADQ3, SDMMC\_DATA3, I3C0\_SDA, EMAC1\_RXD0, TRACE\_D4  
HPS\_IOB\_8, GPIO1\_IO7, SPIS1\_MISO, UART1\_RX, I2C1\_SCL, NAND\_CLE, SDMMC\_CMD, I3C0\_SCL, EMAC1\_RXD1, TRACE\_D15  
HPS\_IOB\_9, GPIO1\_IO8, JTAG\_TCK, SPIS0\_CLK, MDIO2\_MDIO, I2C\_EMAC2\_SDA, NAND\_ADQ4, SDMMC\_DATA4, EMAC1\_TXD2, TRACE\_D14  
HPS\_IOB\_10, GPIO1\_IO9, JTAG\_TMS, SPIS0\_MOSI, MDIO2\_MDC, I2C\_EMAC2\_SCL, NAND\_ADQ5, SDMMC\_DATA5, EMAC1\_TXD3, TRACE\_D13  
HPS\_IOB\_11, GPIO1\_IO10, JTAG\_TDO, SPIS0\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, SDMMC\_DATA6, EMAC1\_RXD2, TRACE\_D12  
HPS\_IOB\_12, GPIO1\_IO11, JTAG\_TDI, SPIS0\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ7, SDMMC\_DATA7, EMAC1\_RXD3, TRACE\_D11  
HPS\_IOB\_13, GPIO1\_IO12, I2C1\_SDA, NAND\_ALE, SDMMC\_PU\_PD\_DATA2, EMAC2\_TX\_CLK, TRACE\_D10  
HPS\_IOB\_14, GPIO1\_IO13, I2C1\_SCL, NAND\_RB\_N, SDMMC\_BUS\_PWR, EMAC2\_TX\_CTL, TRACE\_D9  
HPS\_IOB\_15, GPIO1\_IO14, UART1\_TX, NAND\_CE\_N, I3C1\_SDA, EMAC2\_RX\_CLK, TRACE\_D8  
HPS\_IOB\_16, GPIO1\_IO15, UART1\_RX, NAND\_DQS, SDMMC\_DATA\_STROBE, I3C1\_SCL, EMAC2\_RX\_CTL, TRACE\_D7  
HPS\_IOB\_17, GPIO1\_IO16, UART1\_CTS\_N, NAND\_ADQ8, I3C0\_SDA, EMAC2\_TXD0, TRACE\_D6  
HPS\_IOB\_18, GPIO1\_IO17, SPIM0\_SS1\_N, UART1\_RTS\_N, NAND\_ADQ9, I3C0\_SCL, EMAC2\_TXD1, TRACE\_D5  
HPS\_IOB\_19, GPIO1\_IO18, SPIM0\_MISO, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ10, EMAC2\_RXD0, TRACE\_D4  
HPS\_IOB\_20, GPIO1\_IO19, SPIM0\_SS0\_N, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ11, EMAC2\_RXD1, TRACE\_CLK  
HPS\_IOB\_21, GPIO1\_IO20, SPIM0\_CLK, SPIS1\_CLK, I2C\_EMAC2\_SDA, NAND\_ADQ12, EMAC2\_TXD2, TRACE\_D0  
HPS\_IOB\_22, GPIO1\_IO21, SPIM0\_MOSI, SPIS1\_MOSI, I2C\_EMAC2\_SCL, NAND\_ADQ13, EMAC2\_TXD3, TRACE\_D1  
HPS\_IOB\_23, GPIO1\_IO22, SPIM0\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ14, EMAC2\_RXD2, TRACE\_D2  
HPS\_IOB\_24, GPIO1\_IO23, SPIM0\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ15, EMAC2\_RXD3, TRACE\_D3

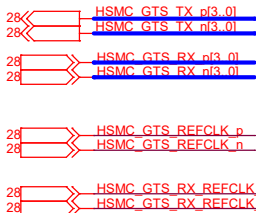
HPS


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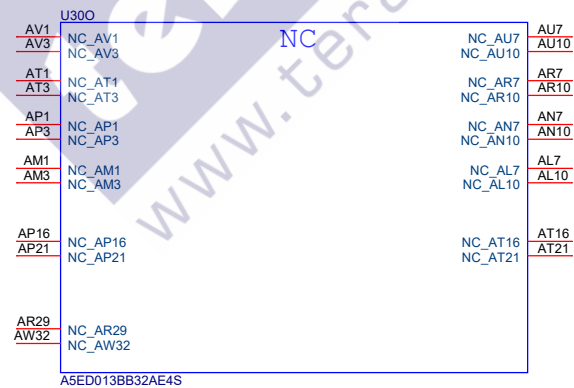
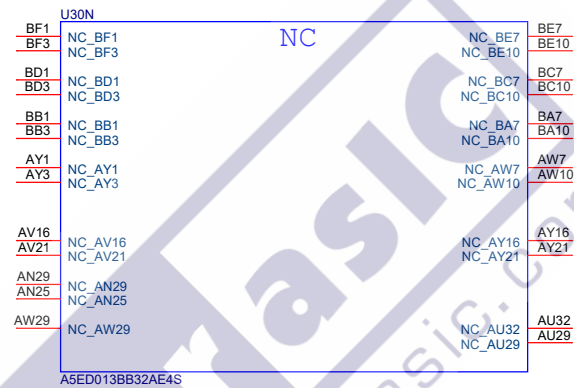
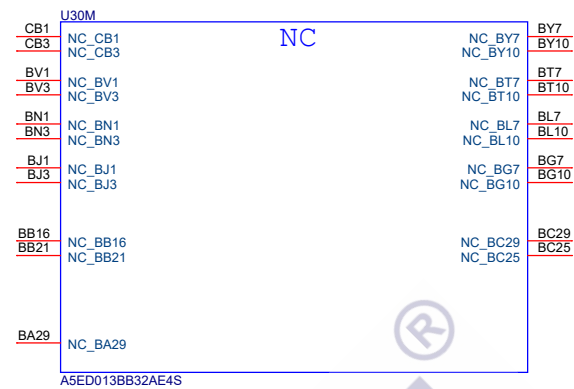
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Title			
DE25-Standard Board			
Size	Document Number		Rev
B	FPGA Bank HPS		D
Date:	Tuesday, June 17, 2025		Sheet 16 of 49



### HSMC Transceivers

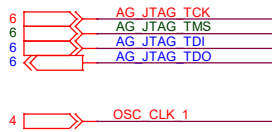


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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	FPGA XCVR Bank 1A, NC (1B1C)	D
Date:	Tuesday, June 17, 2025	Sheet 17 of 49





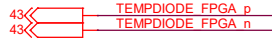
## Agilex JTAG Interface



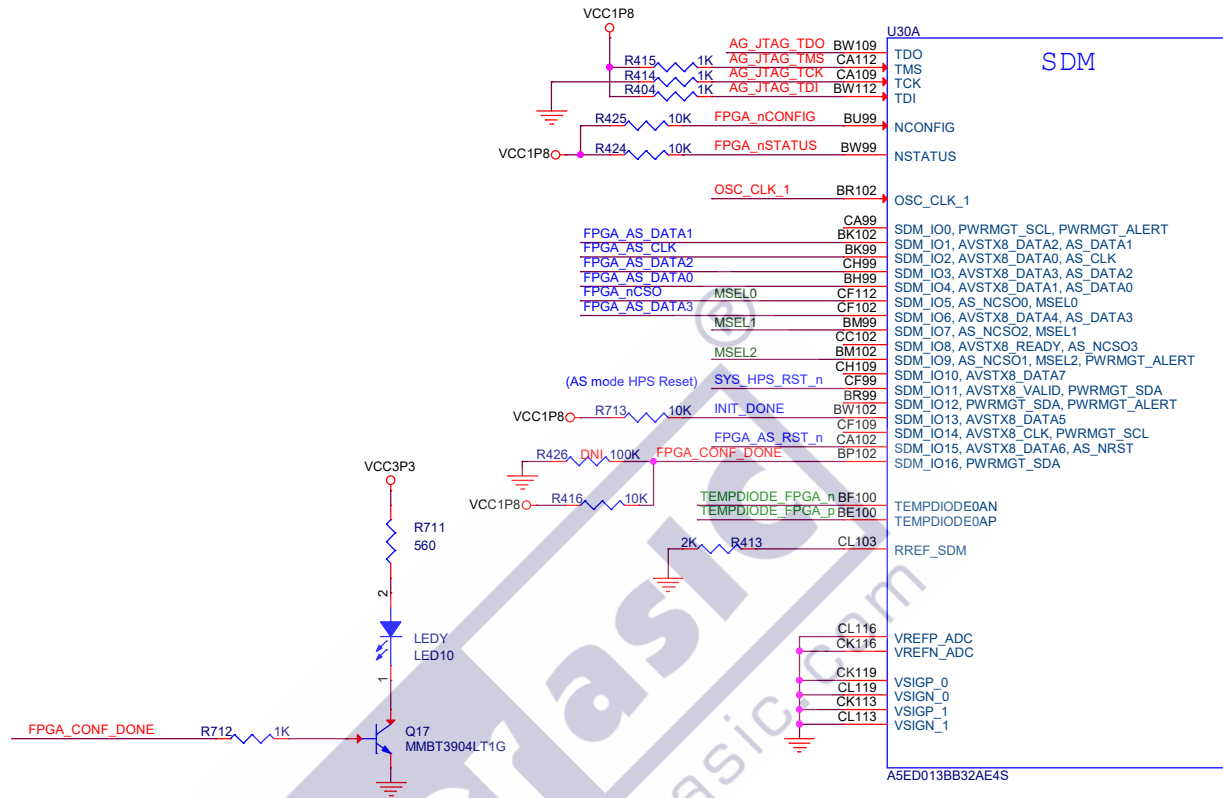
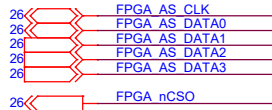
SYS HPS\_RST\_n 36,37,38,42

FPGA\_AS\_RST\_n

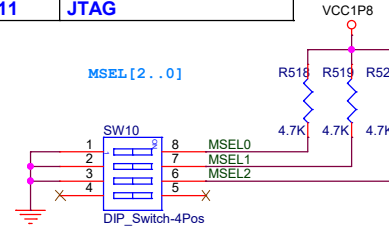
## FPGA Temperature diode



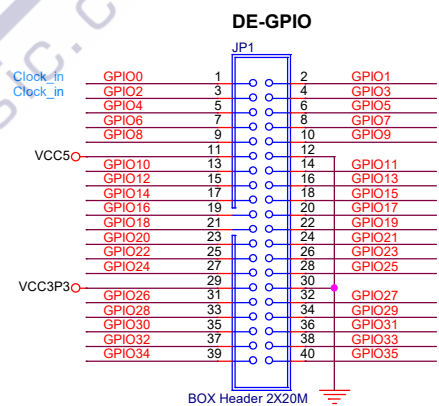
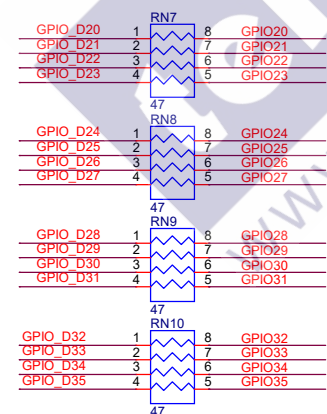
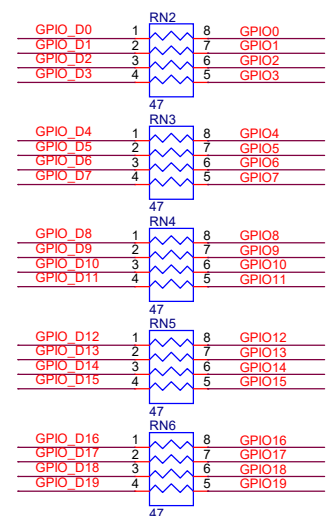
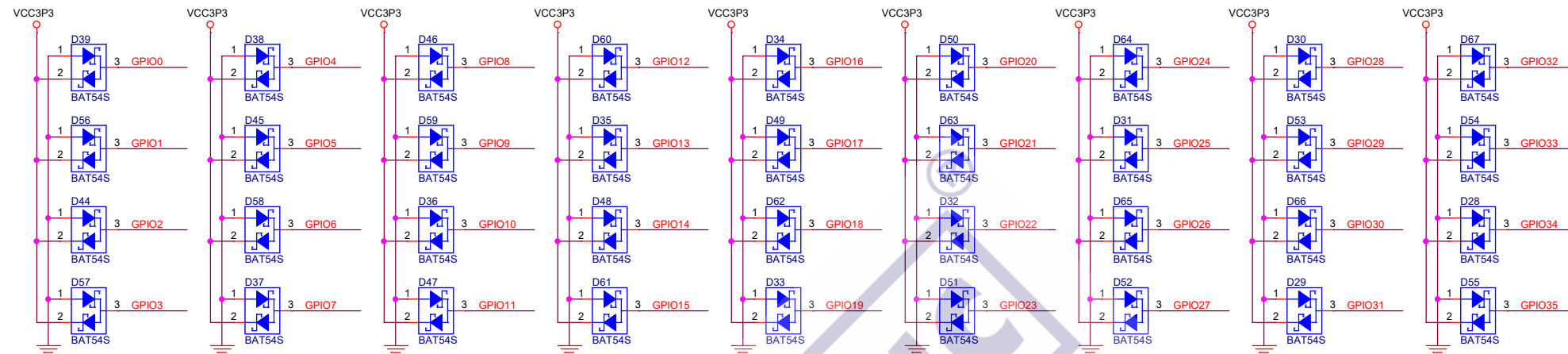
## FPGA AS Configuration

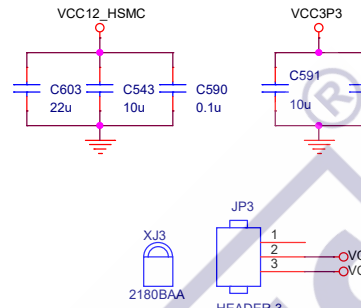
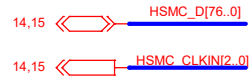
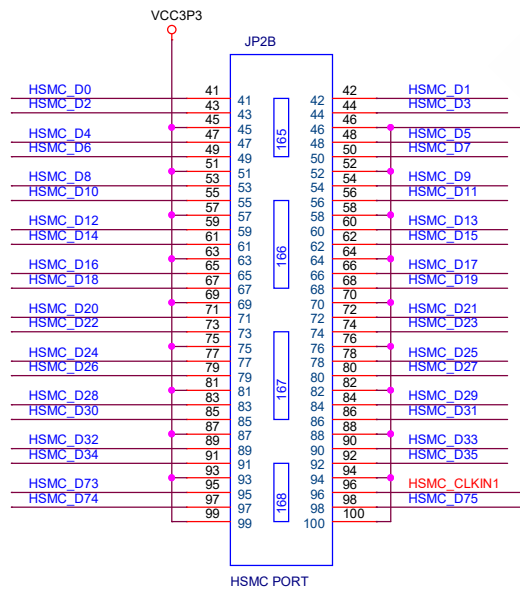
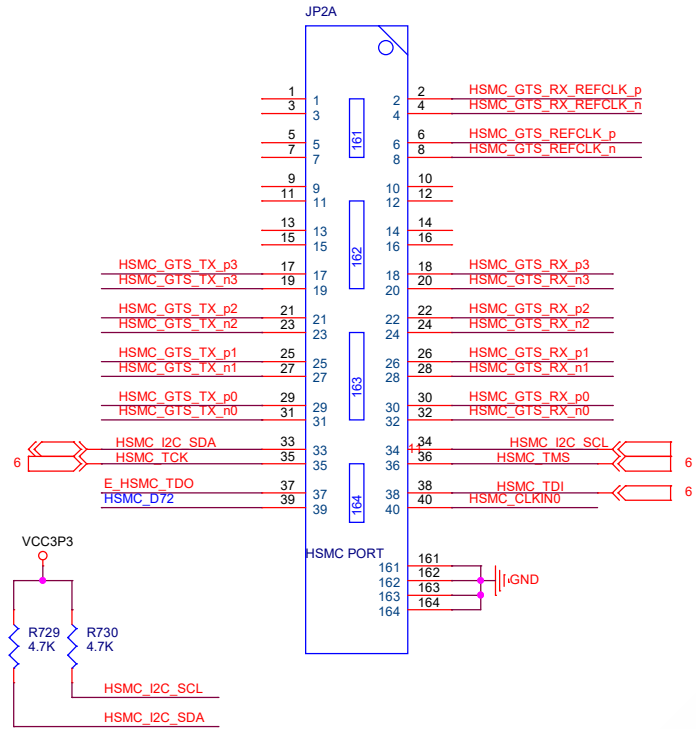


MSEL[2:0]	Configuration Mode
001	AS - Fast (Default Setting)
111	JTAG

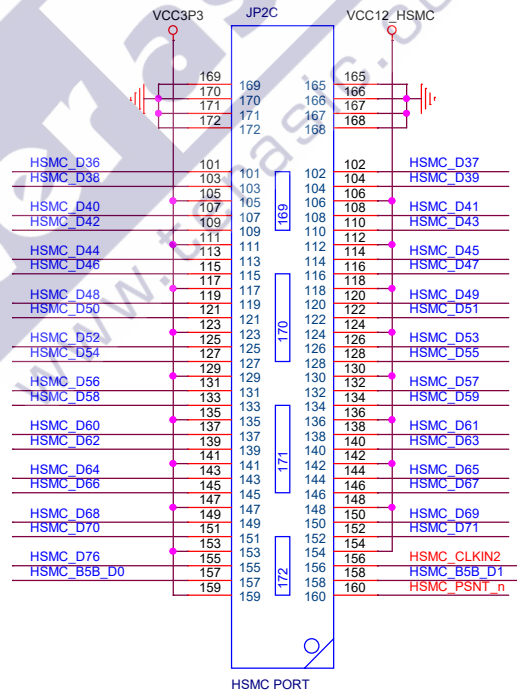


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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	FPGA Configuration	D
Date:	Tuesday, June 17, 2025	Sheet 19 of 49

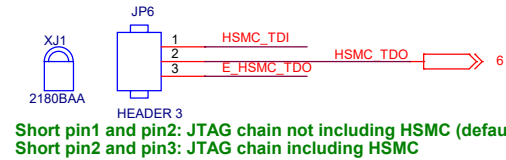
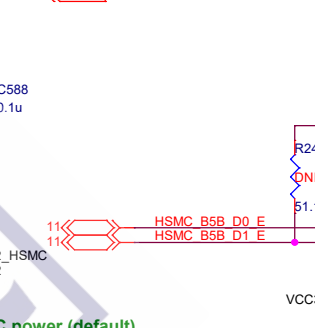
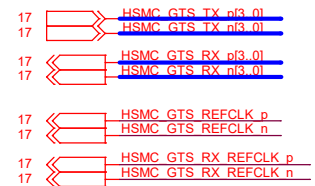




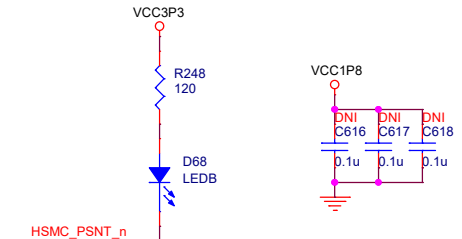
Short pin1 and pin2: Disable VCC12\_HSMC power (default)  
Short pin2 and pin3: Enable VCC12\_HSMC power

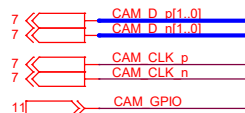


# HSMC Transceivers



Short pin1 and pin2: JTAG chain not including HSMC (default)  
Short pin2 and pin3: JTAG chain including HSMC

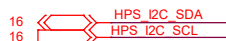




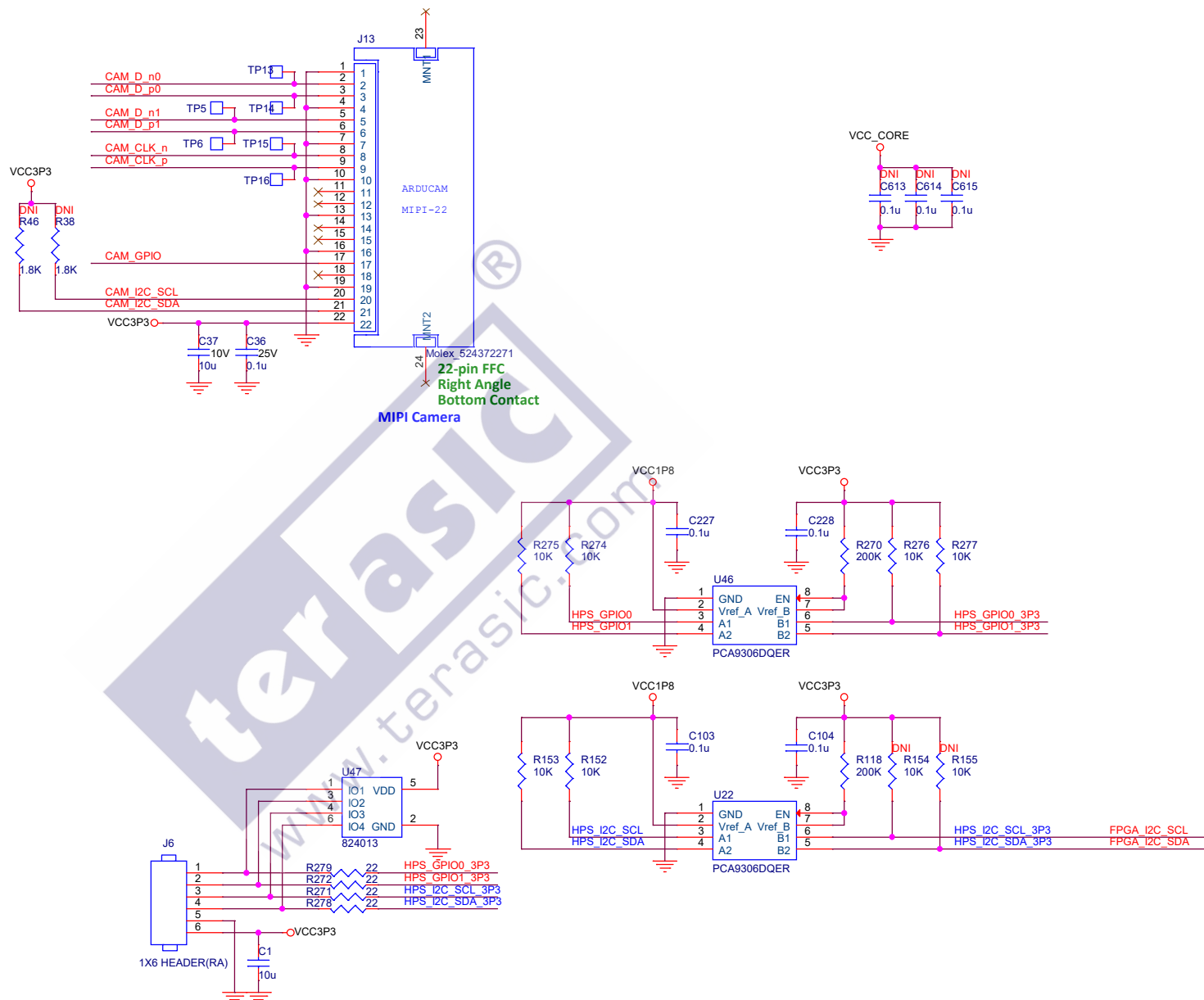
### FPGA I2C Interface



### HPS I2C Interface



### HPS GPIO



### HPS 1x6 GPIO Header

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Title <b>DE25-Standard Board</b>		
Size B	Document Number MIPI Connectors, HPS 1x6 GPIO	Rev D
Date: Tuesday, June 17, 2025	Sheet 29	of 49

