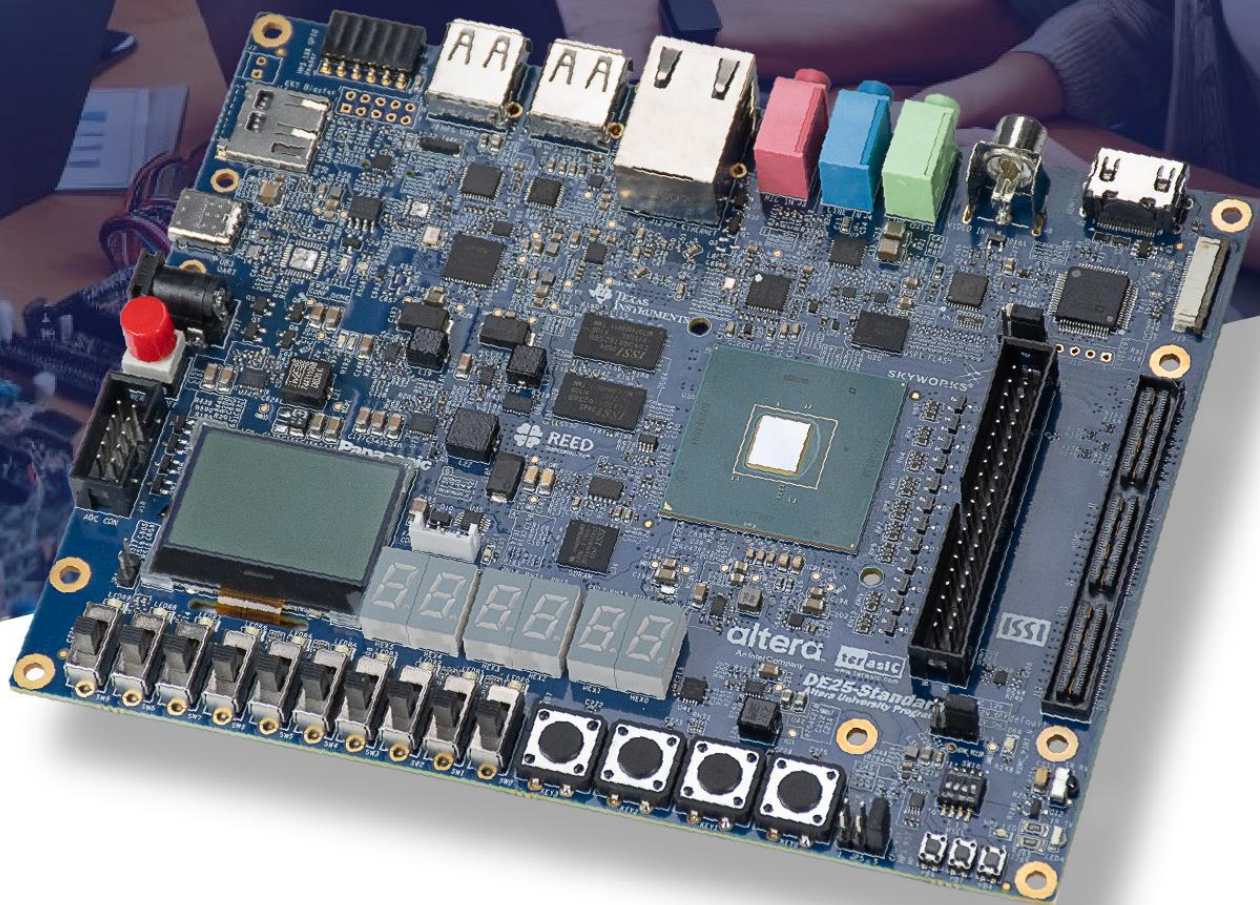


DE25-Standard Development Kit



**Powering next-level performance for
digital logic and embedded applications !**

User Manual

CONTENTS

Chapter 1	DE25-Standard Development Kit.....	3
1.1	Package Contents.....	4
1.2	DE25-Standard Resource Package	4
1.3	Getting Help	5
Chapter 2	Introduction to the DE25-Standard Board.....	6
2.1	Layout and Components.....	6
2.2	Block Diagram of the DE25-Standard Board.....	8
Chapter 3	Using the DE25-Standard Board.....	11
3.1	Settings of FPGA Configuration Mode	11
3.2	Configuration of Agilex 5 SoC FPGA on DE25-Standard	12
3.3	Board Setup Elements	17
3.4	Board Status Elements.....	21
3.5	Board Reset Elements.....	22
3.6	Clock Circuitry	23
3.7	I2C Bus.....	24
3.8	Peripherals Connected to the FPGA.....	25
3.8.1	User Push-buttons, Switches and LEDs.....	25
3.8.2	7-segment Displays.....	28
3.8.3	2x20 GPIO Expansion Header	30
3.8.4	HSMC Connector.....	31
3.8.5	24-bit Audio CODEC	35
3.8.6	HDMI Output	36
3.8.7	Color Composite Video Decoder	38
3.8.8	IR Receiver	39

3.8.9	IR Emitter LED	40
3.8.10	DDR4 Memory	40
3.8.11	SDRAM Memory	43
3.8.12	A/D Converter and 2x5 Header	45
3.8.13	MIPI Connector	46
3.9	Peripherals Connected to the Hard Processor System (HPS)	48
3.9.1	User Push-buttons and LEDs	48
3.9.2	Gigabit Ethernet	48
3.9.3	UART to USB	50
3.9.4	Micro SD Card Socket	50
3.9.5	2-port USB Host	51
3.9.6	Accelerometer (G-sensor)	52
3.9.7	1×6 Header	53
3.9.8	128×64 Pixel LCD	54
3.9.9	Real-Time Clock (RTC)	55
Chapter 4	DE25-Standard System Builder	57
4.1	Introduction	57
4.2	Design Flow	57
4.3	Using DE25-Standard System Builder	58
Chapter 5	Appendix	65
5.1	Revision History	65
5.2	Copyright Statement	65

Chapter 1

DE25-Standard Development Kit

The DE25-Standard Development Kit presents a robust hardware design platform built around the Agilex 5 SoC FPGA, which combines the ARM 2xA55 and 2xA76 embedded cores with industry-leading programmable logic for ultimate design flexibility. Users can now leverage the power of tremendous reconfigurability paired with a high-performance, low-power processor system. Intel's SoC integrates an ARM-based hard processor system (HPS) consisting of processor, peripherals and memory interfaces tied seamlessly with the FPGA fabric using a high-bandwidth interconnect backbone. The DE25-Standard development board is equipped with high-speed DDR4 memory, video and audio capabilities, Ethernet networking, MIPI interface and much more that promise many exciting applications.

The DE25-Standard Development Kit contains all the tools needed to use the board in conjunction with a computer that runs the Microsoft Windows 10.

1.1 Package Contents

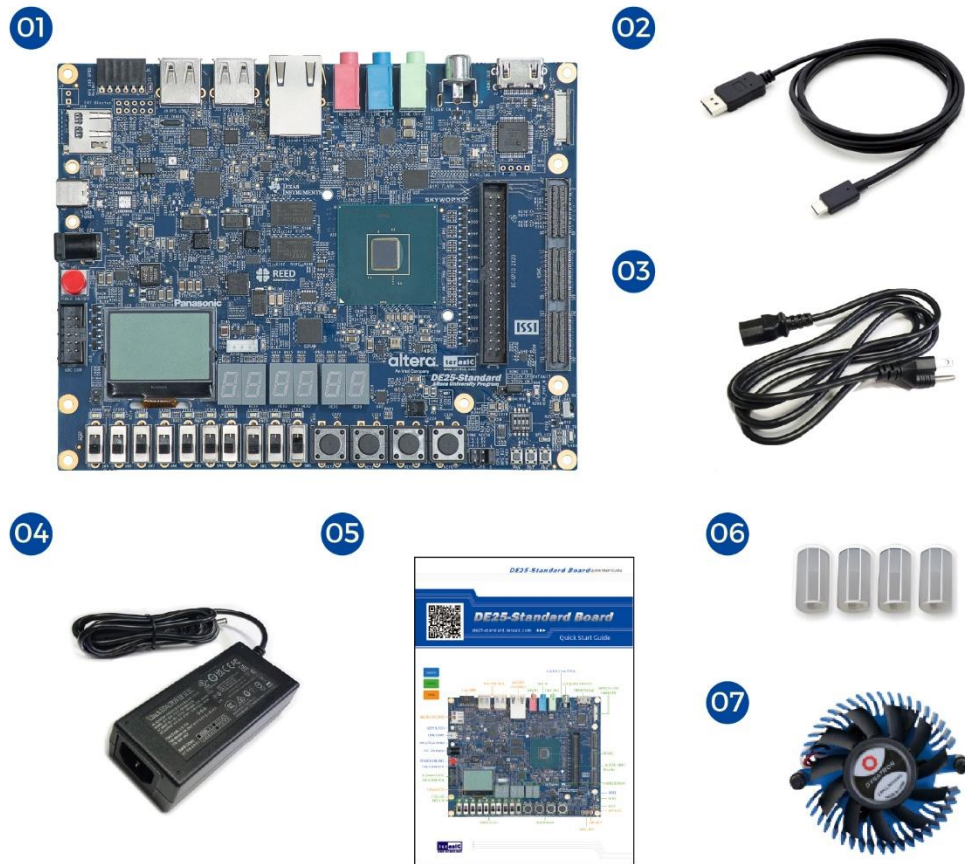


Figure 1-1 The DE25-Standard package contents

The DE25-Standard package includes:

1. DE25-Standard Board
2. Type-C USB Cable
3. AC Power Cord
4. 12V Power Supply
5. Quick Start Guide
6. Four Silicon Footstands
7. Fan (Installed)

1.2 DE25-Standard Resource Package

The DE25-Standard Resource Package contains all the documents and supporting materials associated with DE25-Standard, including the user manual, system builder, reference designs, and device datasheets. Users can download this Resource Package from the link: <http://DE25->

standard.terasic.com/cd/.

The developers can create their Quartus project based on the **golden_top** Quartus project included in this CD. The **golde_top** Quartus project is placed in the folder: *Demonstration/FPGA/golden_top* .

1.3 Getting Help

Here are the addresses where you can get help if you encounter any problems:

- Terasic Technologies
- No.80, Fenggong Rd., Hukou Township, Hsinchu County, 303035 Taiwan

Email: support@terasic.com

Tel.: +886-3-575-0880

Website: DE25-standard.terasic.com

Chapter 2

Introduction to the DE25-Standard Board

This chapter provides an introduction to the design and features of the board.

2.1 Layout and Components

Figure 2-1 shows a photograph of the board that illustrates its layout and the location of connectors and key components.

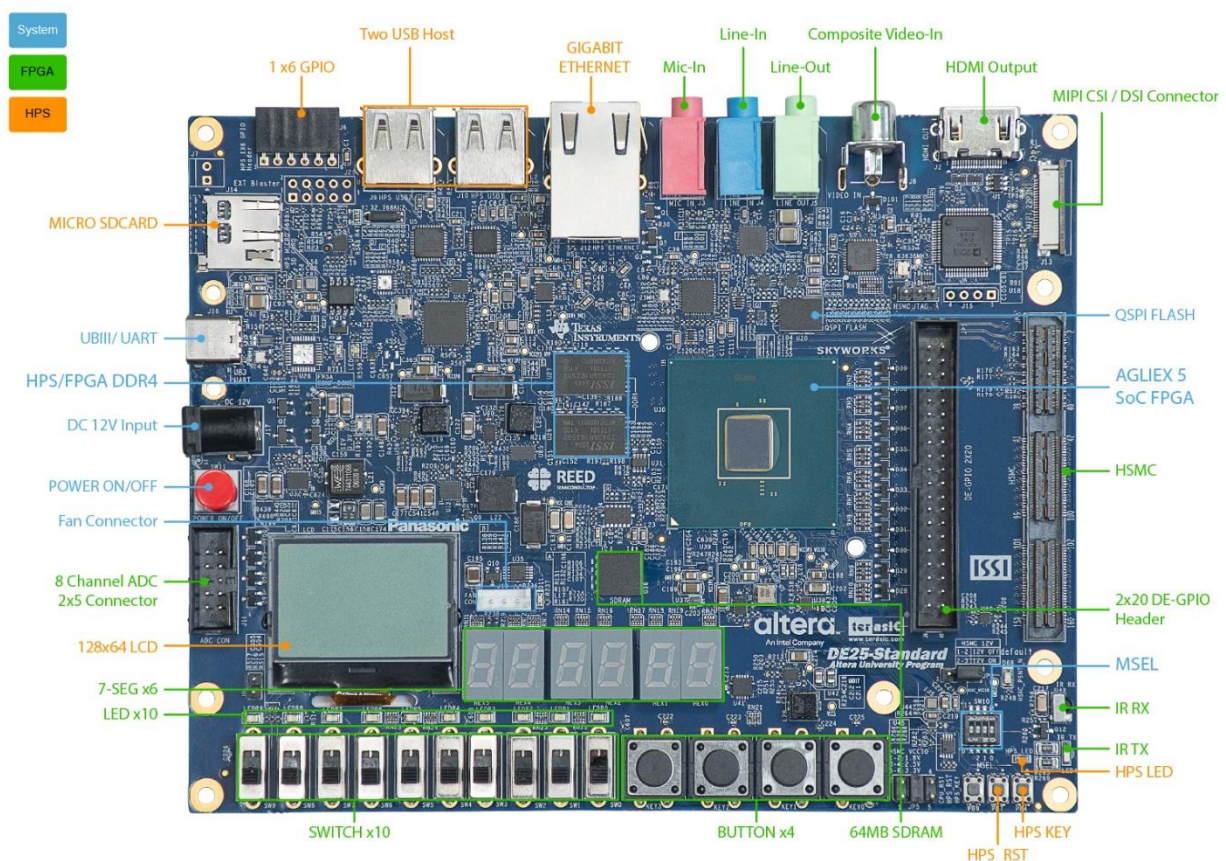


Figure 2-1 DE25-Standard development board (top view)

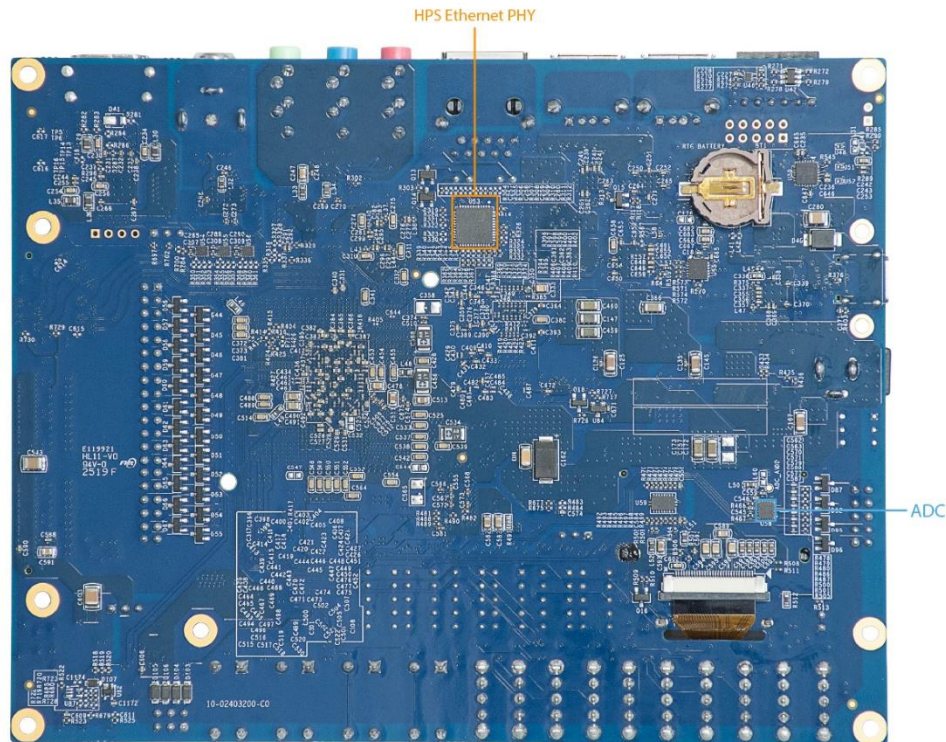


Figure 2-2 DE25-Standard development board (bottom view)

The DE25-Standard board has many features that allow users to implement a wide range of designed circuits, from simple circuits to multimedia projects.

The following hardware is provided on the board:

■ FPGA

- Agilex 5 SoC FPGA : A5ED013BB32AE4SCS (130K LEs)
- ASx4 128 Mbit QSPI Flash
- USB-Blaster III onboard for programming; JTAG Mode
- 64MB SDRAM (16-bit data bus)
- 1GB DDR4 SDRAM (32-bit data bus) share with HPS
- 4 push-buttons
- 10 slide switches
- 10 red user LEDs
- Six 7-segment displays
- Four 50 MHz clock sources from the clock generator
- 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
- HDMI 2.0 Output Port (Support 1080P)
- Composite color video decoder (NTSC/PAL/SECAM) and composite-video-in connector
- IR receiver and IR emitter

- One HSMC connector with 4 transceivers
- One 40-pin expansion header with diode protection
- A/D converter, 4-pin SPI interface with FPGA
- One 2-lane MIPI Connector for Camera/Display

■ HPS (Hard Processor System)

- ARM Cortex Processor with 2× A55 and 2× A76 cores
- 1 Gigabit Ethernet PHY with RJ45 connector
- 2-port USB host with two Type-A USB connectors
- Micro SD card socket
- Accelerometer (I2C interface + interrupt)
- UART to USB, Type-C USB connector
- Cold reset button
- One user button and one user LED
- One 3.3V 1×6 GPIO Header
- 128×64 pixel LCD module with backlight

2.2 Block Diagram of the DE25-Standard Board

Figure 2-3 is the block diagram of the board. All the connections are established through the Agilex 5 SoC FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

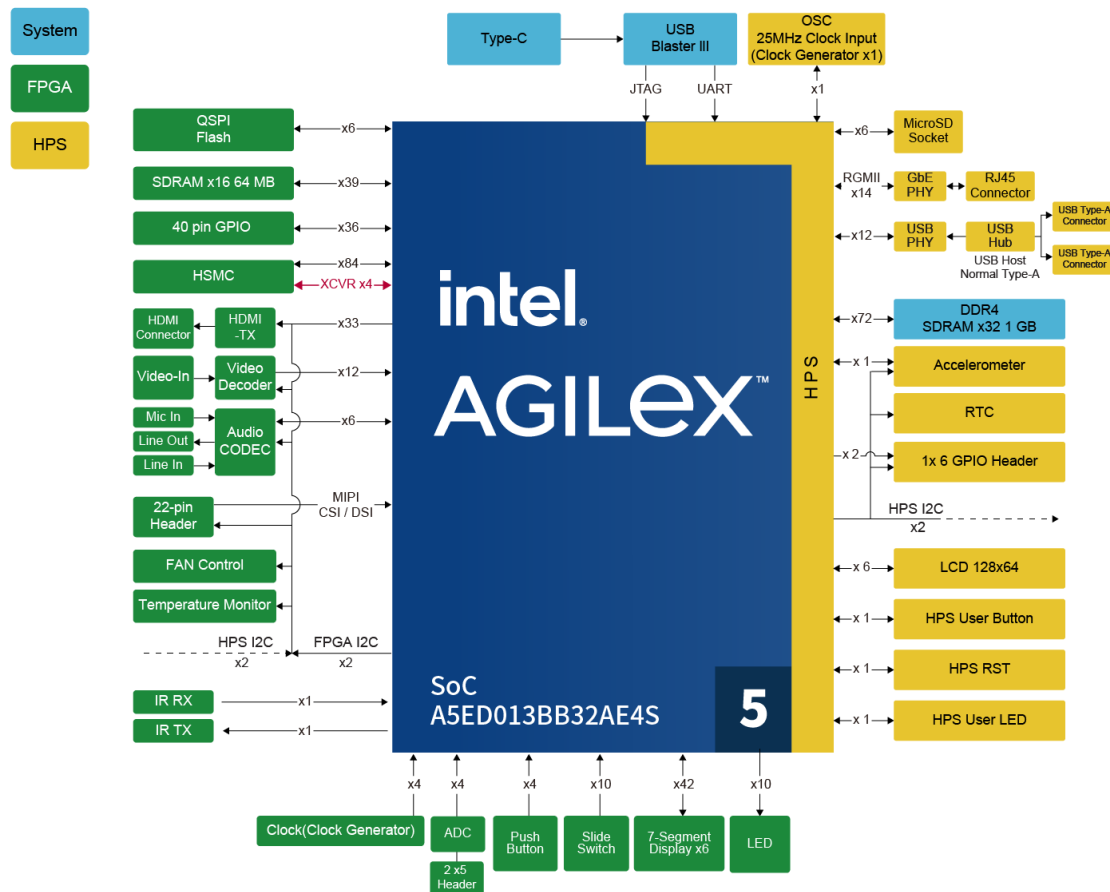


Figure 2-3 Block diagram of DE25-Standard

Detailed information about **Figure 2-3** are listed below.

FPGA Device

- Agilex™ 5 SoC FPGA : A5ED013BB32AE4SR1
- ARM Cortex Processor with 2×A55 and 2×A76
- 138K programmable logic elements
- 8.42 Mbit embedded memory
- 376 18-bit × 19-bit multipliers
- MIPI D-PHY v2.5
-

Configuration and Debug

- Support ASx4 Configure Mode with 128Mbits QSPI Flash
- Onboard USB-Blaster III (USB Type-C connector)

Memory Device

- 64MB (32M×16) SDRAM on FPGA
- 1GB (2×256M×16) DDR4 SDRAM shared with HPS
- Micro SD card socket on HPS

Communication

- Two port USB 2.0 Host (ULPI interface with USB type A connector)
- UART to USB (USB Mini-C connector)
- 10/100/1000 Ethernet
- IR emitter/receiver

Connectors

- One HSMC (Configurable I/O standards 1.8/2.5/3.3V)
- One 40-pin expansion headers
- One 10-pin ADC input header
- One 1×6 GPIO header (one I2C interface and two GPIO)

Display

- HDMI 2.0 Output Port (Support 1080P)
- 128×64 pixel LCD module with backlight

Audio

- 24-bit CODEC, Line-in, Line-out, and microphone-in jacks

Video Input

- Composite color video decoder (NTSC/PAL/SECAM) and composite-video-in connector

ADC

- Interface: SPI
- Fast throughput rate: 1MSPS
- Channel number: 8
- Resolution: 12-bit
- Analog input range : 0 ~ 3.4 V

Switches, Buttons, and Indicators

- 5 user buttons (FPGA ×4, HPS ×1)
- 10 user switches (FPGA ×10)
- 11 user LEDs (FPGA ×10, HPS × 1)
- 1 HPS reset buttons (HPS_Cold_RESET_n)
- Six 7-segment displays

Sensors

- Accelerometer (G-Sensor) on HPS

Power

- 12V DC input

Chapter 3

Using the DE25-Standard Board

This chapter provides instructions for using the board and describes its peripherals.

3.1 Settings of FPGA Configuration Mode

When the DE25-Standard board is powered on, the FPGA is configured from QSPI FLASH or the HPS. The MSEL[2:0] switches are used to select the configuration scheme, implemented as a 4-pin DIP switch **SW10** on the DE25-Standard board, as shown in **Figure 3-1**.

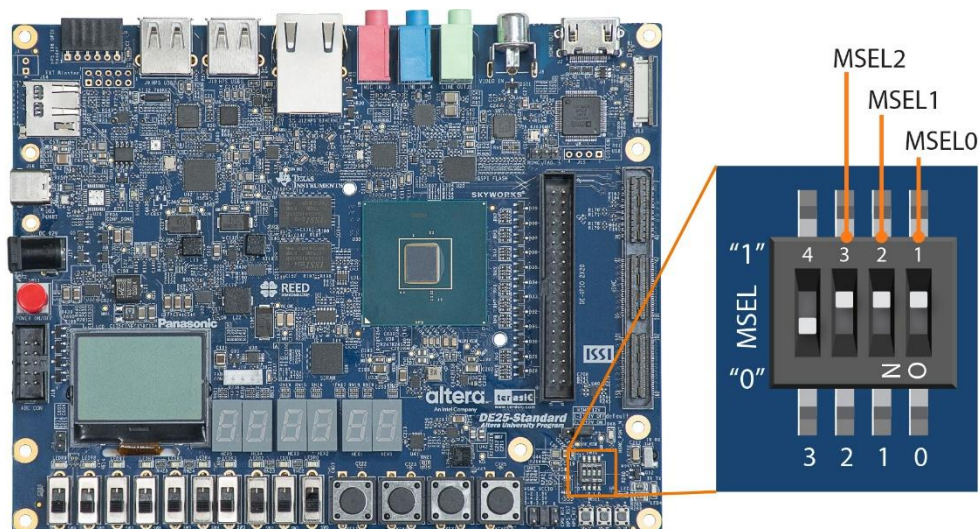


Figure 3-1 DIP switch (SW10) setting of Active Serial (AS) mode on DE25-Standard board

Table 3-1 shows the relation between MSEL[2:0] and DIP switch (SW10).

Table 3-1 FPGA Configuration Mode Switch (SW10)

Board Reference	Signal Name	Description	Default AS Mode
SW10.1	MSEL0	Use these pins to set the FPGA Configuration scheme	OFF ("1")
SW10.2	MSEL1		ON ("0")
SW10.3	MSEL2		ON ("0")
SW10.4	N/A	N/A	N/A

Figure 3-1 shows MSEL[2:0] setting of Active Serial (AS) Fast mode, which is the default setting on the DE25-Standard. When the board is powered on, the FPGA is configured from QSPI Flash, which is pre-programmed with a default configuration.

Table 3-2 MSEL Pin Settings for FPGA Configure of DE25-Standard

<i>MSEL[2:0]</i>	<i>Configuration Scheme</i>	<i>Description</i>
001	AS Fast	FPGA configured from QSPI Flash (default)
111	JTAG	You can configure the FPGA using the dedicated JTAG interface and circuit.

3.2 Configuration of Agilex 5 SoC FPGA on DE25-Standard

There are two programming methods supported by DE25-Standard:

1. JTAG programming: This is named after the IEEE standards Joint Test Action Group. The configuration bitstream is downloaded directly to the Agilex 5 SoC FPGA. The FPGA will retain its current status as long as the power is applied to the board; the configuration information will be lost when the power is turned off.
2. AS programming: The other programming method is Active Serial configuration. The configuration bitstream is written to the quad serial configuration device (QSPI Flash), which provides non-volatile storage for the bit stream. The information is retained within QSPI Flash even if the DE25-Standard board is turned off. When the board is powered on, the configuration data in the QSPI Flash device is automatically loaded into the Agilex 5 SoC FPGA.

■ JTAG Chain on DE25-Standard Board

As shown in **Figure 3-2**, the DE25-Standard uses the on-board USB Blaster III (via USB Type-C) as the JTAG master. This circuit connects JTAG signals to both the Agilex 5 FPGA and the HSMC connector. Users can use a 3-pin header to decide whether to include the HSMC JTAG bus in the board's JTAG chain. By default, it is disconnected. For how to set the 3-pin header related to the HSMC connector, please refer to Section 3.3 HSMC JTAG Header part.

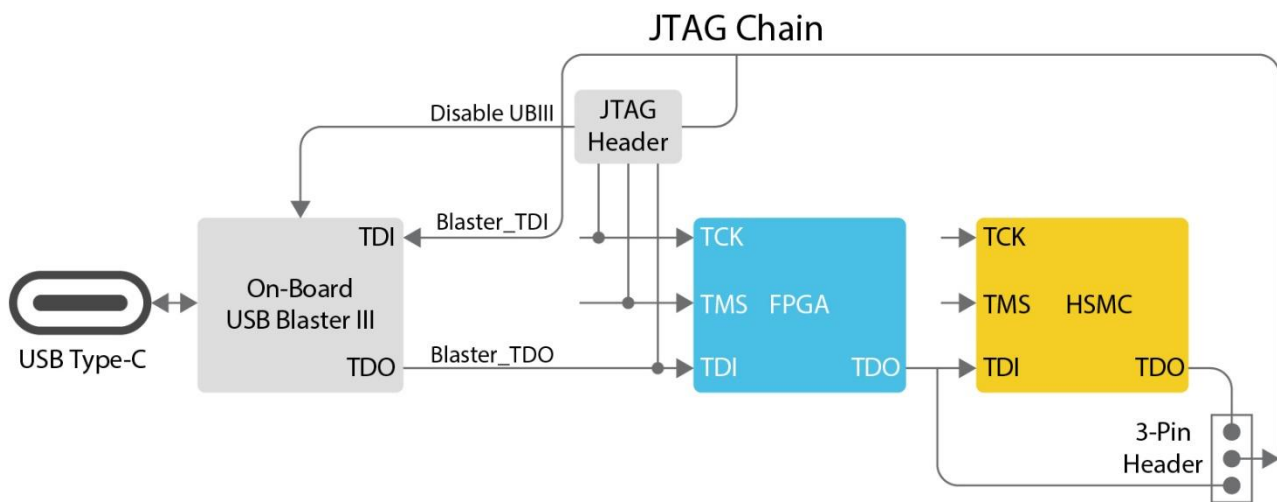


Figure 3-2 Block diagram of the JTAG chain

■ Configuring the FPGA in JTAG Mode

The following explains step-by-step how to program the FPGA in JTAG mode.

1. Make sure the Quartus Pro and the driver of USB Blaster III are installed on your Host.
2. Set the FPGA Configuration Mode Switch (SW10) to JTAG mode.
3. Connect the board's Type-C port to the host using a USB cable, and power up the board.
4. Open the Quartus Programmer tool, make sure the USB blaster III ("DE25-Standard Development Kit[USB-x]") is found in "Hardware Setup.." tab.

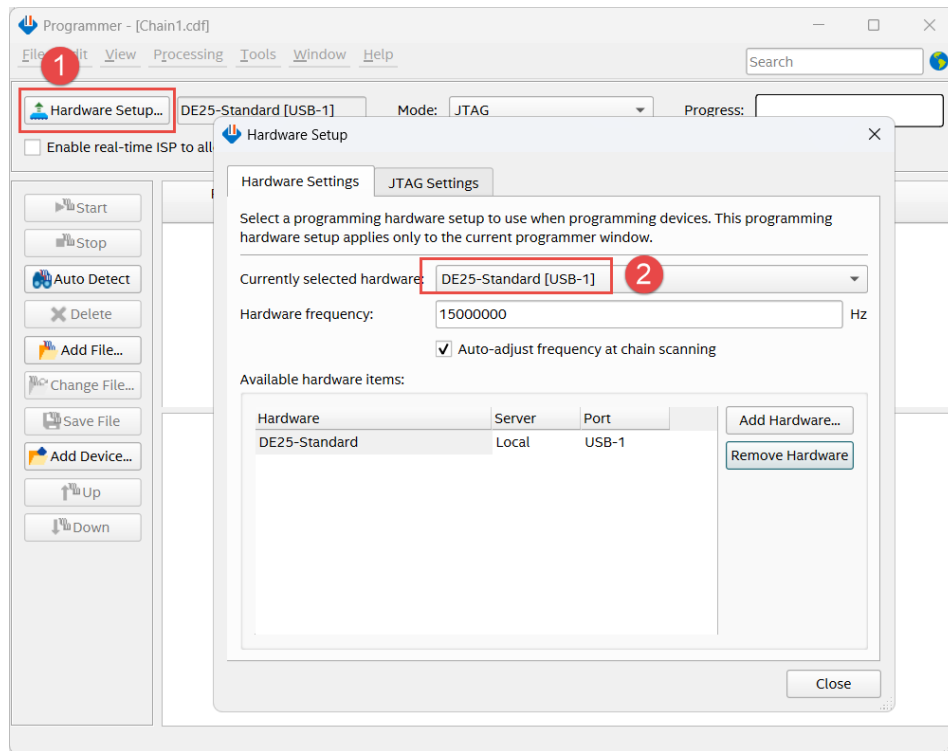


Figure 3-3 USB blaster III is found in Programmer

5. Open the Programmer and click “Auto Detect”, as shown in **Figure 3-4**

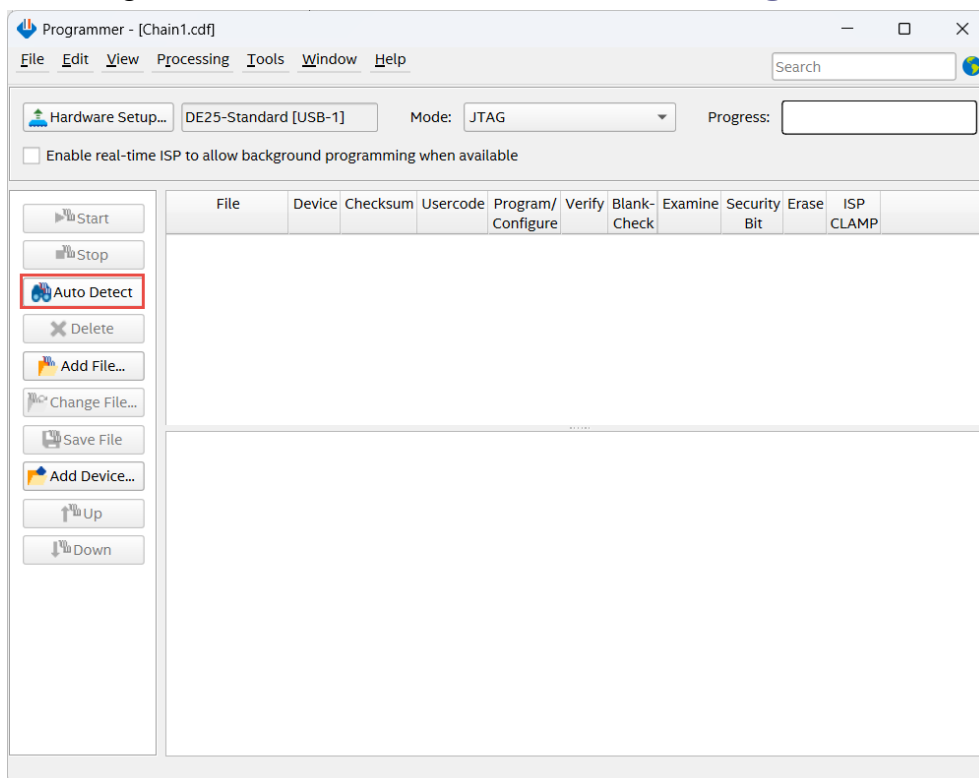


Figure 3-4 Detect FPGA device in JTAG mode

●

6. The Agilex 5 FPGA should be detected, as shown in **Figure 3-5**.

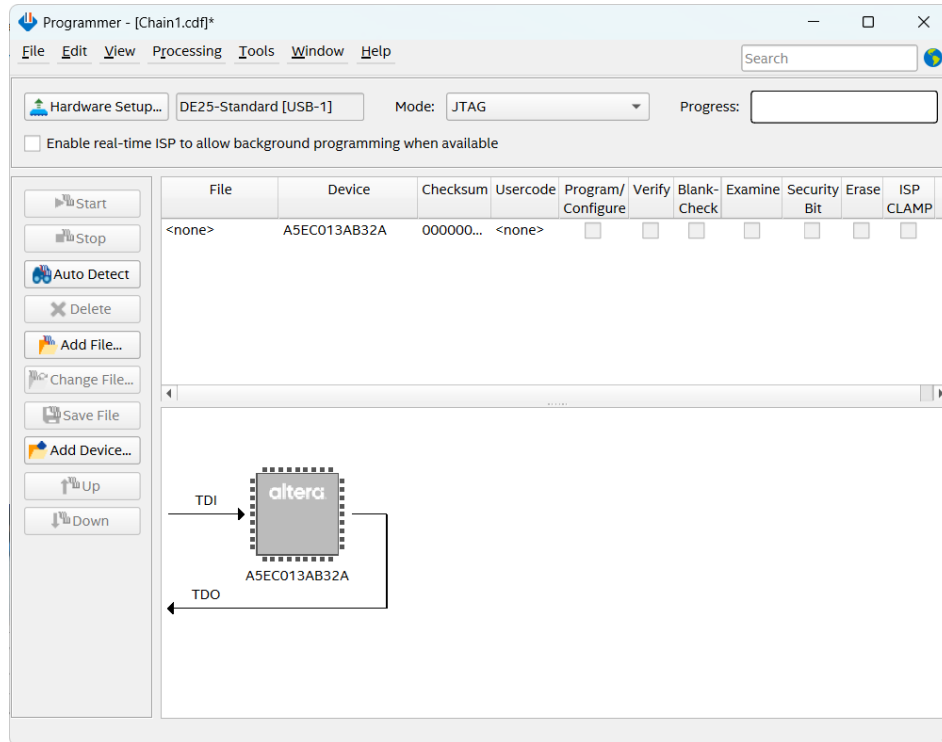


Figure 3-5 FPGA detected in Quartus programmer

7. Right click on the FPGA device and open the .sof file to be programmed, as shown in **Figure 3-6**.

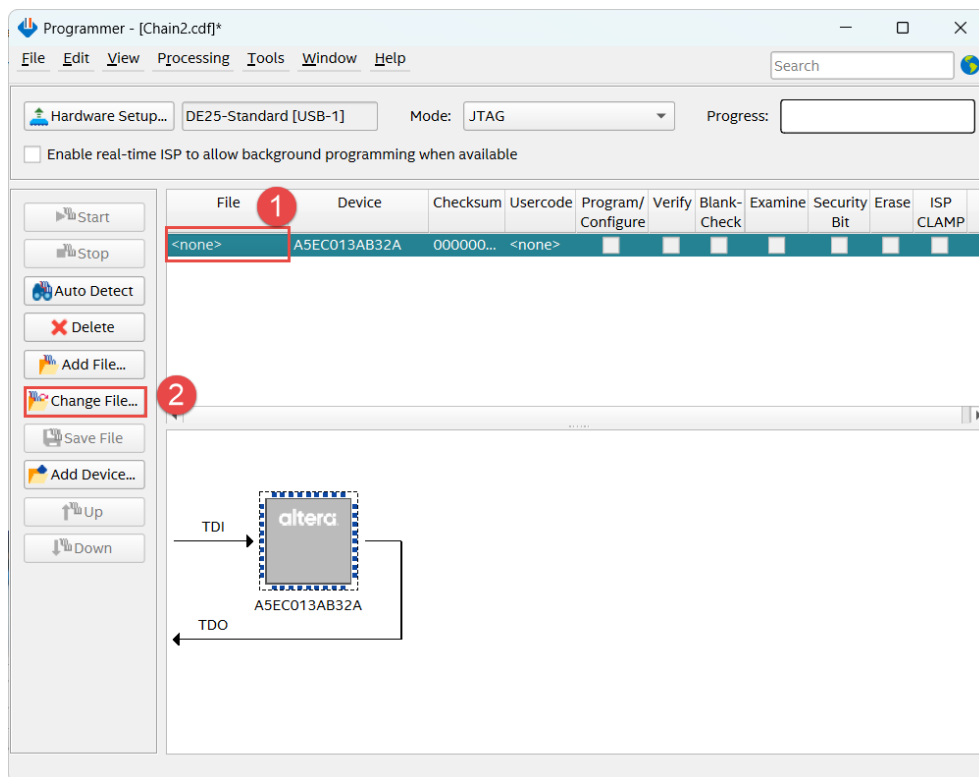


Figure 3-6 Open the .sof file to be programmed into the FPGA device

8. Select the .sof file to be programmed, as shown in **Figure 3-7**.

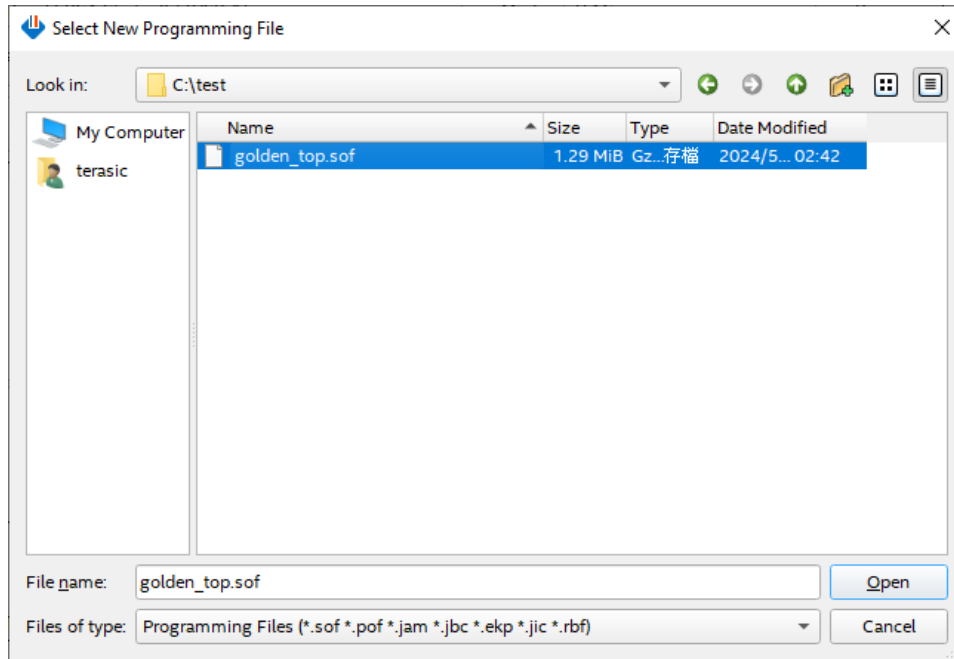


Figure 3-7 Select the .sof file to be programmed into the FPGA device

9. Click the “Program/Configure” checkbox and click “Start” button to download the .sof file into the FPGA device, as shown in **Figure 3-8**.

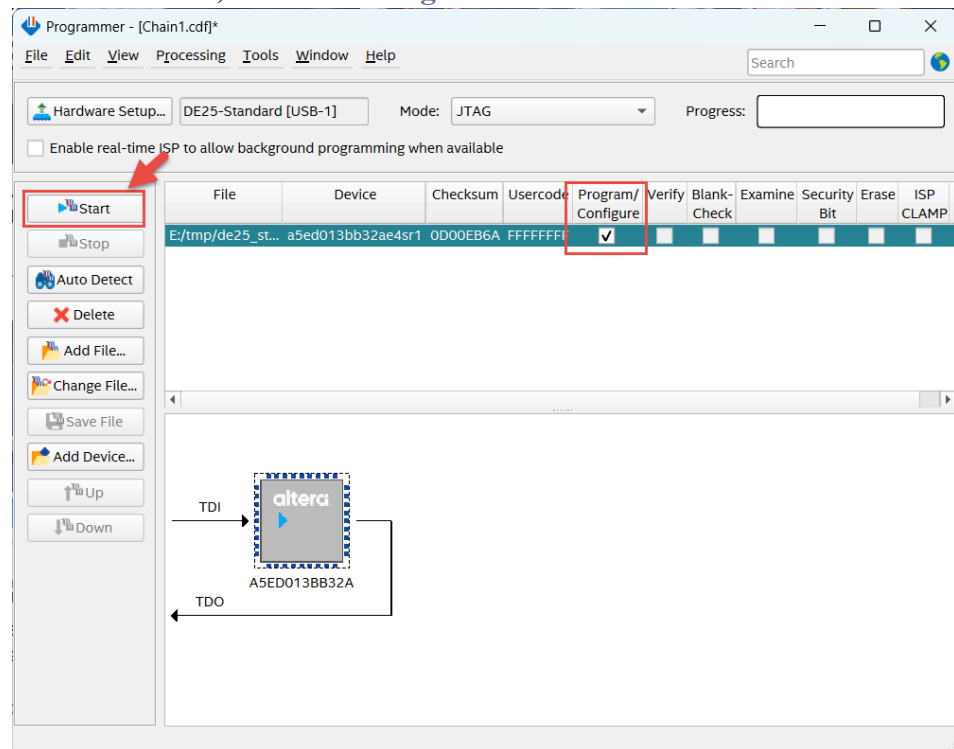


Figure 3-8 Program .sof file into the FPGA device

3.3 Board Setup Elements

This section introduces the configuration components on the DE25-Standard development board, explaining their functions and how to set them up, to help users understand how to operate these components.

■ FPGA Configuration Mode Switch

The FPGA Configuration Mode Switch is used to set the FPGA's MSEL (Mode Select) pins. These pins determine the startup (configuration) mode of the FPGA, specifying where the device will load its configuration bitstream from upon power-up or reset. The DE25-Standard supports both AS and JTAG modes. For detailed settings, please refer to Section 3.1.

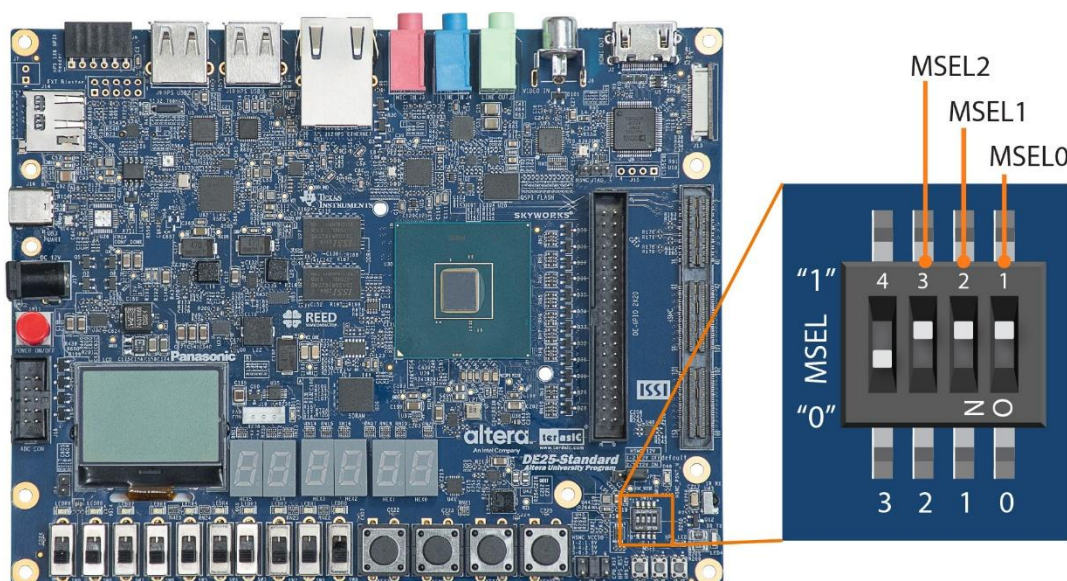


Figure 3-9 FPGA Configuration Mode Switch

■ HSMC JTAG Header

As described in Section 3.2 (JTAG chain part), the HSMC JTAG header determines whether the JTAG interface of the HSMC connector is included in the board's JTAG chain. Users can use a 2-pin jumper to short Pin1/Pin2 or Pin2/Pin3 to enable or bypass the HSMC JTAG interface. **Figure 3-10** shows the location of this header, and **Table 3-3** describes the configuration options.

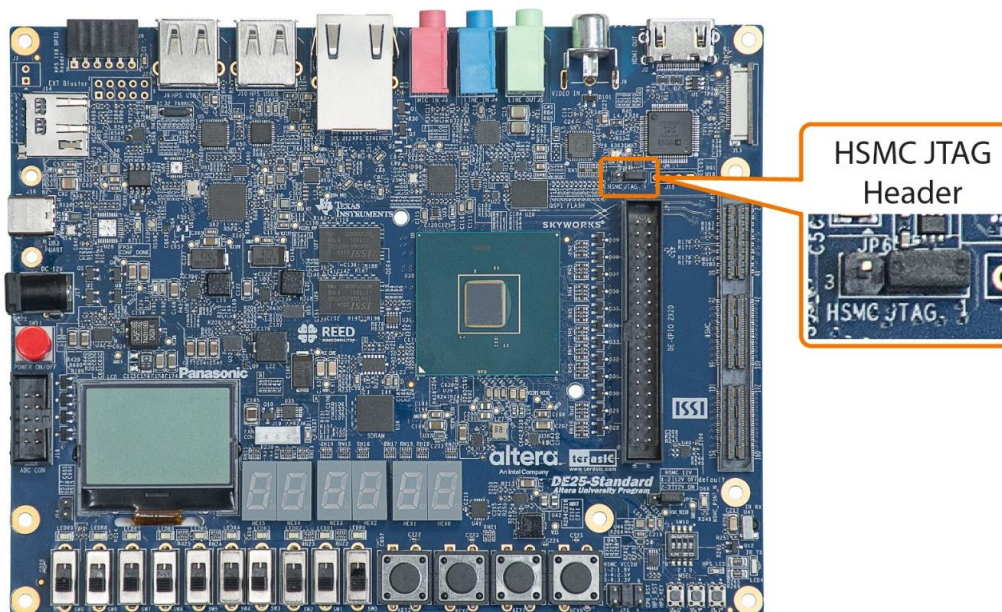




Figure 3-10 HSMC JTAG Header position

Table 3-3 Jumper Settings for HSMC JTAG Header

Jumper Settings	Setting Figure	Description
Short Pins 1 and 2		Bypass the JTAG interface of the HSMC connector(Default)
Short Pins 2 and 3		Enable the JTAG interface of the HSMC connector

■ HSMC 12V Power Header

This header is used to control whether the 12V power supplied to the HSMC connector is enabled. By default, the 12V power is disabled. This setting helps prevent accidental short circuits between the HSMC 12V power and FPGA I/O, which could otherwise cause damage when the HSMC connector is not in use. **Figure 3-11** shows the location of the header, and **Table 3-4** provides the configuration details.

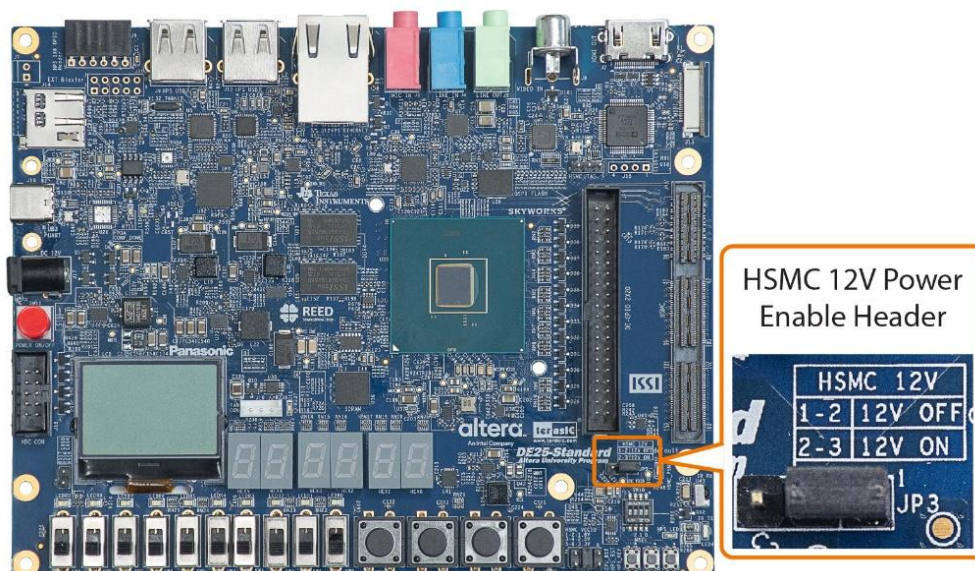




Figure 3-11 HSMC 12V Power Header position

Table 3-4 Jumper Settings for HSMC 12V Power Header

Jumper Settings	Setting Figure	Description
Short Pins 1 and 2		Disable 12V poer for HSMCconnector(Default)
Short Pins 2 and 3		Enable 12V poer for HSMC connector

■ HSMC VCCIO Header

This header determines the I/O voltage standard (3.3V, 2.5V, or 1.8V; default is 3.3V) for the I/Os connecting the HSMC connector to the FPGA, allowing the HSMC interface to support a wider variety of daughter cards. **Figure 3-12** shows the location of the header, and **Table 3-5** provides the configuration details.

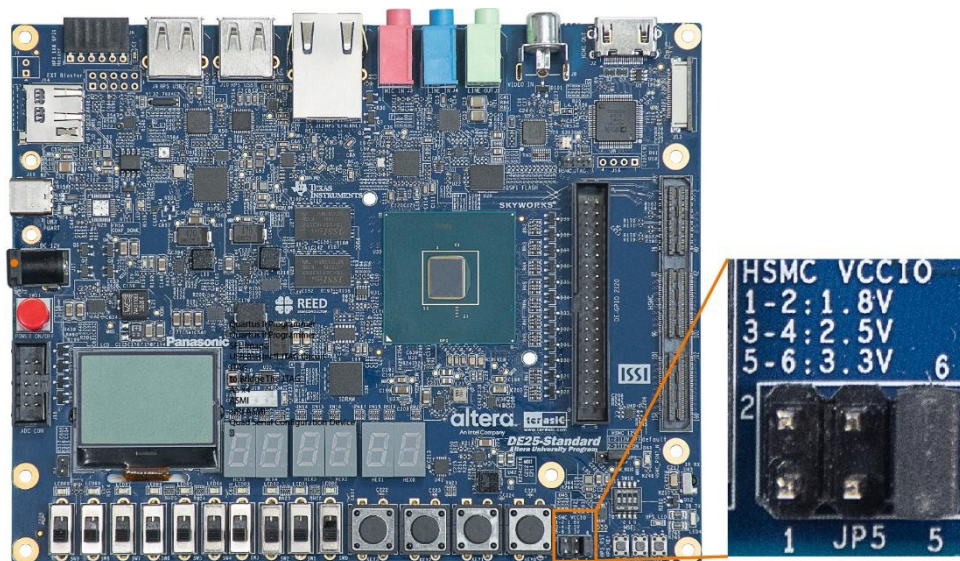
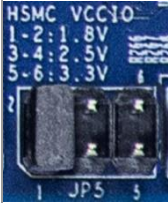




Figure 3-12 HSMC VCCIO Header position

Table 3-5 Jumper Settings for different I/O Standards

JP3 Jumper Settings	Setting Figure	IO Voltage of HSMC Connector (JP5)
Short Pins 1 and 2		1.8V
Short Pins 3 and 4		2.5V
Short Pins 5 and 6		3.3V (Default)

3.4 Board Status Elements

In addition to the LEDs that the FPGA can control, there are 6 indicators that indicate the board status (see [Figure 3-13](#)). [Table 3-7](#) shows the JTAG Blaster LED status (for USB blaster III) and its meaning. [Table 3-7](#) shows the status and description of other LEDs.

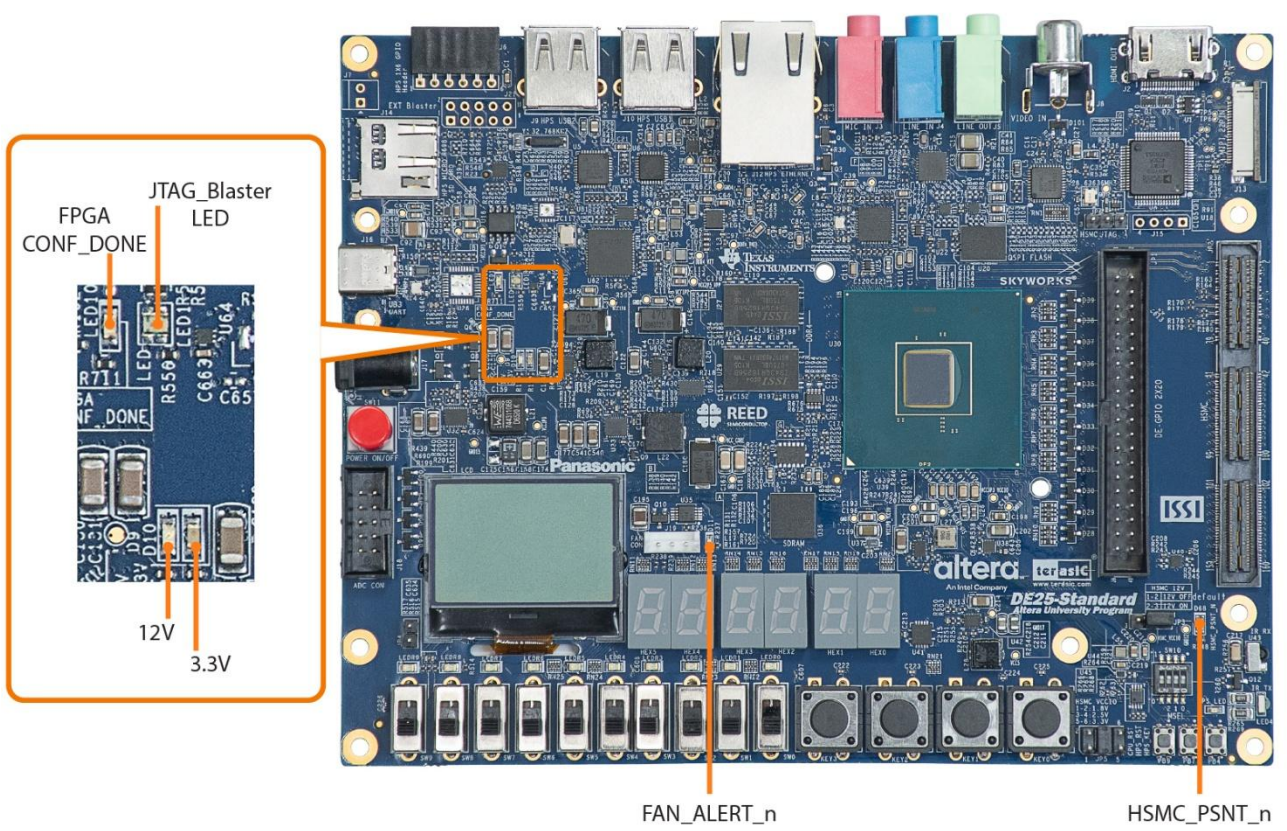


Figure 3-13 LED Indicators on the DE25-Standard

Table 3-6 JTAG blaster LED status

Color	Meaning
Off	No power / not connected / suspend mode
Blue	Connected, not in use
Green	Connected, an application is using JTAG, no traffic
Green flickering	Connected, data is moving through the JTAG interface
Purple flashing	Identify function has been triggered on this cable

Table 3-7 LED Indicators

Board Reference	LED Name	Description
-----------------	----------	-------------

D9	12V	Illuminates when 12V power is active.
D10	3.3V	Illuminates when 3.3V power is active.
LED10	FPGA_CONF_DONE	Illuminates when FPGA configuration is complete and successful
D11	FAN_ALERT	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
D68	HSMC_PSNT_n	Illuminates when a HSMC daughter card is connected to the board.

3.5 Board Reset Elements

The board provides 3 reset buttons for different system reset situations (see [Figure 3-14](#)). These buttons can reset the CPU and FPGA. [Table 3-8](#) lists the details.

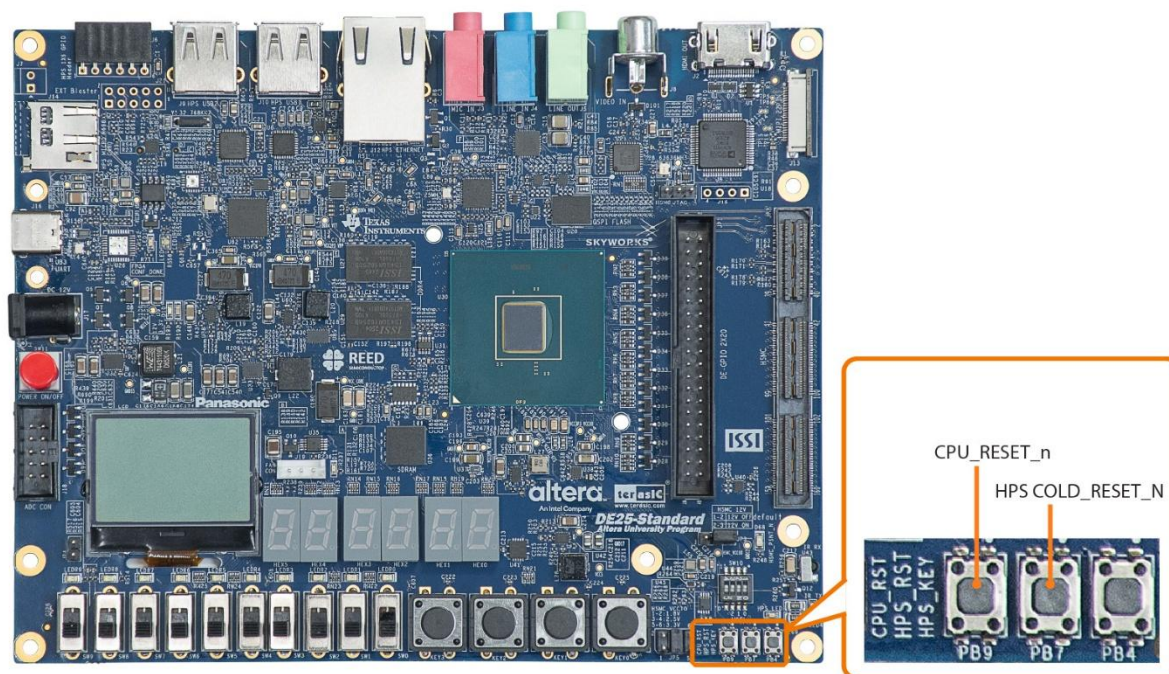


Figure 3-14 Reset buttons on DE25-Standard

Table 3-8 Description of the three Reset Buttons on the DE25-Standard

Board Reference	Signal Name	Description
PB7	HPS_COLD_RESET_N	Cold reset to the HPS, Ethernet PHY and USB host device. Active low input which resets all HPS logics that can be reset.
PB9	CPU_RESET_n	This button can be used to reset the FPGA (Need user setting or logic)

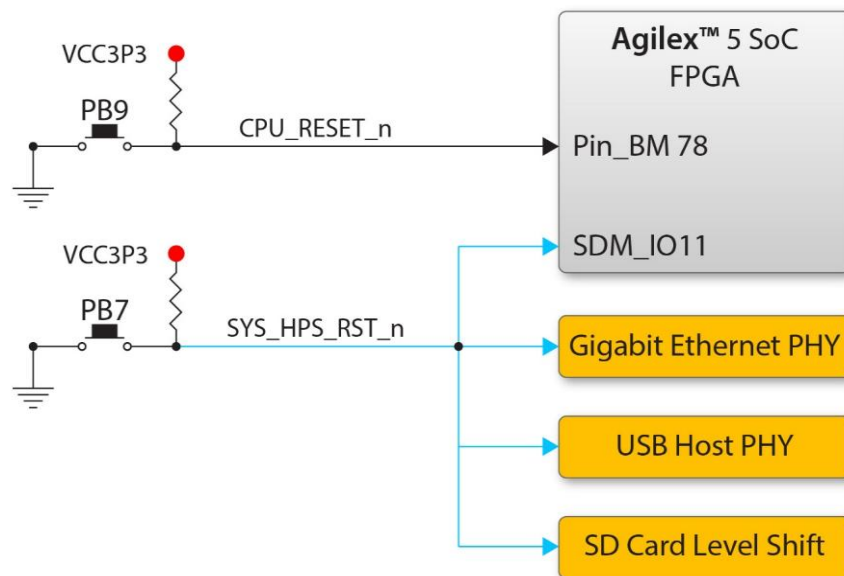


Figure 3-15 Block diagram of reset buttons the DE25-Standard

3.6 Clock Circuitry

Figure 3-16 shows the default frequency of all external clocks fed to the Agilex 5 SoC FPGA. A clock generator is used to distribute clock signals with low jitter. The three 50 MHz clock signals connected to the FPGA are used as clock sources for user logic. One 25 MHz clock signal is connected to HPS clock inputs, and the 150 MHz clock is the reference clock for DDR4 interface. A 125 MHz clock is used for FPGA configuration bank (OSC_CLK1).

For peripheral devices, one 25 MHz clock is fed to the clock input of Gigabit Ethernet PHY. Two 24 MHz clock signals are connected to the clock inputs of the USB Host/OTG PHY and USB hub controller. The pin assignments of clock inputs to FPGA I/O pins is listed in **Table 3-9**.

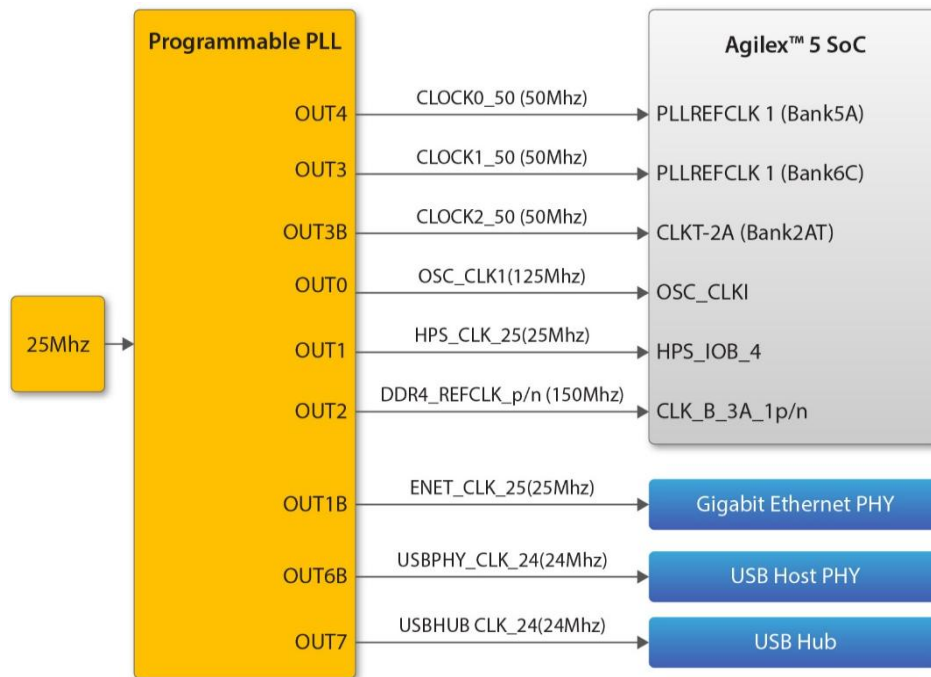


Figure 3-16 Block diagram of the clock distribution on the DE25-Standard

Table 3-9 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
CLOCK0_50	PIN_CH128	50 MHz clock input	3.3V
CLOCK1_50	PIN_D8	50 MHz clock input	1.8V
CLOCK2_50	PIN_BM71	50 MHz clock input	1.2V
HPS_CLK_25	PIN_AG123	25 MHz clock input	1.8V
DDR4_REFCLK_P	PIN_AB117	150 MHz clock input	1.2V TRUE DIFFERENTIAL SIGNALING

3.7 I2C Bus

There are many devices controlled by the I2C interface on the DE25-Standard board, such as the Audio codec, ADC sensor and accelerometer. Most of the devices on the board are connected to the I2C bus named FPGA_I2C_SCL/SDA, and this bus is also connected to the HPS I2C bus (HPS_I2C_SCL /SDA), so users can access these devices from either the FPGA or HPS. The pin assignment of the I2C bus is listed in [Table 3-10](#).

DE25-Standard I2C Diagram

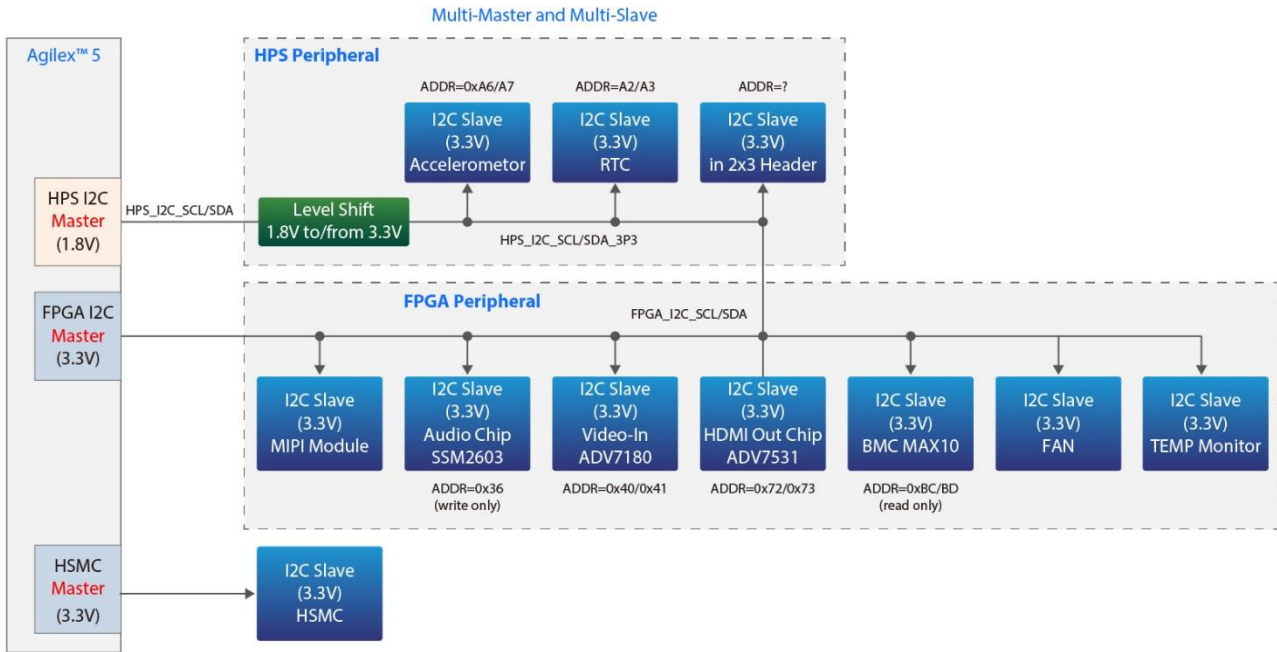


Figure 3-17 Control mechanism for the I2C multiplexer

Table 3-10 I2C Bus Pin Assignments

Signal Name	FPGA Pin No.	Description	I/O Standard
FPGA_I2C_SCL	PIN_BF120	FPGA I2C Clock	3.3V
FPGA_I2C_SDA	PIN_BH118	FPGA I2C Data	3.3V
HPS_I2C_SCL	PIN_K127	I2C Clock of the first HPS I2C controller	1.8V
HPS_I2C_SDA	PIN_M127	I2C Data of the first HPS I2C controller	1.8V
HSMC_I2C_SCL	PIN_BR11	HSMC I2C Clock	3.3V
HSMC_I2C_SDA	PIN_BM109	HSMC I2C Data	3.3V

3.8 Peripherals Connected to the FPGA

This section describes the interfaces connected to the FPGA. Users can control or monitor these interfaces with user logic in the FPGA.

3.8.1 User Push-buttons, Switches and LEDs

The board has four push-buttons connected to the FPGA, as shown in [Figure 3-18](#). A Schmitt trigger circuit acts as a switch debouncer in [Figure 3-19](#) for the connected buttons. The four buttons named KEY0, KEY1, KEY2, and KEY3 coming out of the Schmitt trigger device are connected directly to

the Agilex 5 SoC FPGA. Each push-button generates a low logic level when it is pressed (Active low). Since the push-buttons are debounced, they can be used as reset inputs in a circuit.

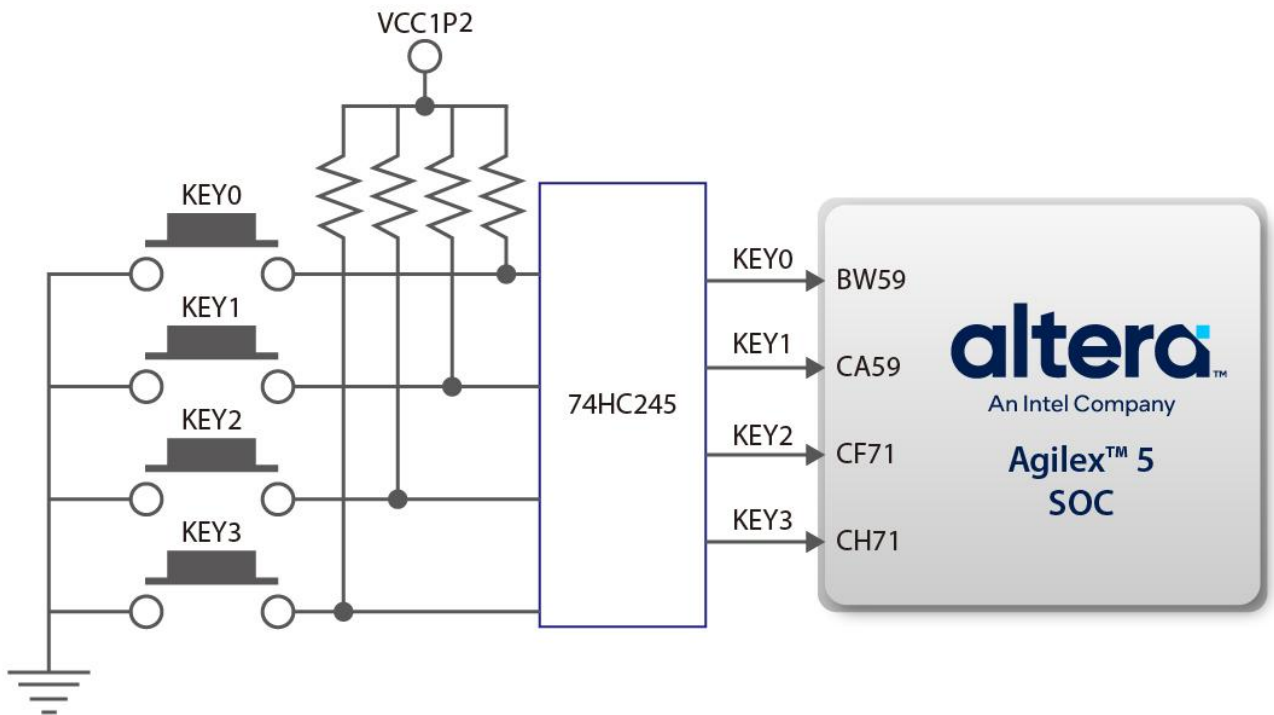


Figure 3-18 Connections between the push-buttons and the Agilex 5 SoC FPGA

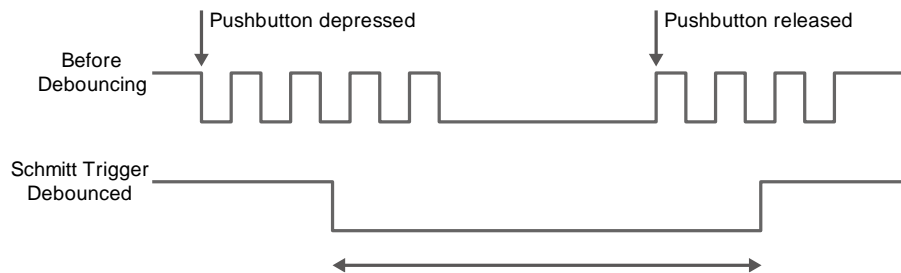


Figure 3-19 Switch debouncing

There are ten slide switches connected to the FPGA, as shown in [Figure 3-20](#). These switches are not debounced and may be used as level-sensitive data inputs to a circuit. Each switch is connected directly and individually to the FPGA. When the switch is set to the DOWN position (towards the edge of the board), it sends a low logic level to the FPGA. When the switch is set to the UP position, a high logic level is sent to the FPGA



Figure 3-20 Connections between the slide switches and the Agilex 5 SoC FPGA

There are also ten user-controllable LEDs connected to the FPGA. Each LED is driven directly and individually by the Agilex 5 SoC FPGA; driving its associated pin to a “low” logic level turn the LED “on”. **Figure 3-21** shows the connections between LEDs and Agilex 5 SoC FPGA.

Table 3-11, **Table 3-12** and **Table 3-13** list the pin assignment of user push-buttons, switches, and LEDs.



Figure 3-21 Connections between the LEDs and the Agilex 5 SoC FPGA

Table 3-11 Pin Assignments of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW[0]	PIN_BM62	Slide Switch[0]	1.2V
SW[1]	PIN_BP62	Slide Switch[1]	1.2V
SW[2]	PIN_BH62	Slide Switch[2]	1.2V
SW[3]	PIN_BH59	Slide Switch[3]	1.2V
SW[4]	PIN_BM59	Slide Switch[4]	1.2V
SW[5]	PIN_BK59	Slide Switch[5]	1.2V
SW[6]	PIN_BU62	Slide Switch[6]	1.2V
SW[7]	PIN_CF59	Slide Switch[7]	1.2V
SW[8]	PIN_BU59	Slide Switch[8]	1.2V
SW[9]	PIN_BR59	Slide Switch[9]	1.2V

Table 3-12 Pin Assignments of Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY[0]	PIN_BW59	Push-button[0]	1.2V
KEY[1]	PIN_CA59	Push-button[1]	1.2V
KEY[2]	PIN_CF71	Push-button[2]	1.2V
KEY[3]	PIN_CH71	Push-button[3]	1.2V

Table 3-13 Pin Assignments of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR[0]	PIN_CC71	LED [0]	1.2V
LEDR[1]	PIN_BH78	LED [1]	1.2V
LEDR[2]	PIN_CH69	LED [2]	1.2V
LEDR[3]	PIN_CF69	LED [3]	1.2V
LEDR[4]	PIN_CA62	LED [4]	1.2V
LEDR[5]	PIN_CC62	LED [5]	1.2V
LEDR[6]	PIN_CF62	LED [6]	1.2V
LEDR[7]	PIN_BM69	LED [7]	1.2V
LEDR[8]	PIN_CA71	LED [8]	1.2V
LEDR[9]	PIN_BR62	LED [9]	1.2V

3.8.2 7-segment Displays

The DE25-Standard board has six 7-segment displays ideal for displaying numbers. **Figure 3-22** shows the connection of the seven segments (common anode) to pins on the Agilex 5 SoC FPGA. Each segment can be turned on by applying a low logic level from the FPGA.

Each segment in a display is indexed from 0 to 6, with corresponding positions given in **Figure 3-22**. **Table 3-14** shows the FPGA pin assignments for the 7-segment displays.

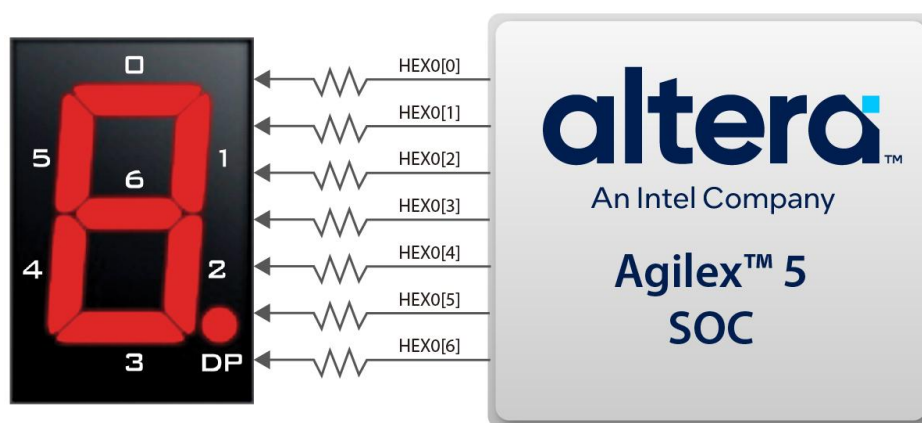


Figure 3-22 Connections between the 7-segment display HEX0 and the Agilex 5 SoC FPGA

Table 3-14 Pin Assignment of 7-segment Displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX0[0]	PIN_BP81	Seven Segment Digit 0[0]	1.2V
HEX0[1]	PIN_BM81	Seven Segment Digit 0[1]	1.2V
HEX0[2]	PIN_BM89	Seven Segment Digit 0[2]	1.2V
HEX0[3]	PIN_BK89	Seven Segment Digit 0[3]	1.2V
HEX0[4]	PIN_BH92	Seven Segment Digit 0[4]	1.2V
HEX0[5]	PIN_BM92	Seven Segment Digit 0[5]	1.2V
HEX0[6]	PIN_BP92	Seven Segment Digit 0[6]	1.2V
HEX1[0]	PIN_CA78	Seven Segment Digit 1[0]	1.2V
HEX1[1]	PIN_BW78	Seven Segment Digit 1[1]	1.2V
HEX1[2]	PIN_BU78	Seven Segment Digit 1[2]	1.2V
HEX1[3]	PIN_BR78	Seven Segment Digit 1[3]	1.2V
HEX1[4]	PIN_BU81	Seven Segment Digit 1[4]	1.2V
HEX1[5]	PIN_BR81	Seven Segment Digit 1[5]	1.2V
HEX1[6]	PIN_CA89	Seven Segment Digit 1[6]	1.2V
HEX2[0]	PIN_BW89	Seven Segment Digit 2[0]	1.2V
HEX2[1]	PIN_BU92	Seven Segment Digit 2[1]	1.2V
HEX2[2]	PIN_BR92	Seven Segment Digit 2[2]	1.2V
HEX2[3]	PIN_BU89	Seven Segment Digit 2[3]	1.2V
HEX2[4]	PIN_BR89	Seven Segment Digit 2[4]	1.2V
HEX2[5]	PIN_CF78	Seven Segment Digit 2[5]	1.2V
HEX2[6]	PIN_CH78	Seven Segment Digit 2[6]	1.2V
HEX3[0]	PIN_CC81	Seven Segment Digit 3[0]	1.2V
HEX3[1]	PIN_CA81	Seven Segment Digit 3[1]	1.2V
HEX3[2]	PIN_CH81	Seven Segment Digit 3[2]	1.2V
HEX3[3]	PIN_CF81	Seven Segment Digit 3[3]	1.2V
HEX3[4]	PIN_CF89	Seven Segment Digit 3[4]	1.2V
HEX3[5]	PIN_CH89	Seven Segment Digit 3[5]	1.2V
HEX3[6]	PIN_CH92	Seven Segment Digit 3[6]	1.2V
HEX4[0]	PIN_CF92	Seven Segment Digit 4[0]	1.2V
HEX4[1]	PIN_CA92	Seven Segment Digit 4[1]	1.2V

HEX4[2]	PIN_CC92	Seven Segment Digit 4[2]	1.2V
HEX4[3]	PIN_CL76	Seven Segment Digit 4[3]	1.2V
HEX4[4]	PIN_CK76	Seven Segment Digit 4[4]	1.2V
HEX4[5]	PIN_CL82	Seven Segment Digit 4[5]	1.2V
HEX4[6]	PIN_CK80	Seven Segment Digit 4[6]	1.2V
HEX5[0]	PIN_CL85	Seven Segment Digit 5[0]	1.2V
HEX5[1]	PIN_CK85	Seven Segment Digit 5[1]	1.2V
HEX5[2]	PIN_BK69	Seven Segment Digit 5[2]	1.2V
HEX5[3]	PIN_BP71	Seven Segment Digit 5[3]	1.2V
HEX5[4]	PIN_BH89	Seven Segment Digit 5[4]	1.2V
HEX5[5]	PIN_BH71	Seven Segment Digit 5[5]	1.2V
HEX5[6]	PIN_CH62	Seven Segment Digit 5[6]	1.2V

3.8.3 2x20 GPIO Expansion Header

The board has one 40-pin expansion header. The header has 36 user pins connected directly to the Agilex 5 SoC FPGA. It also includes DC +5V (VCC5), DC +3.3V (VCC3P3), and two GND pins. The maximum power consumption allowed for a daughter card connected to one GPIO ports is shown in [Table 3-15](#).

Table 3-15 Voltage and Max. Current Limit of Expansion Header(s)

<i>Supplied Voltage</i>	<i>Max. Current Limit</i>
5V	1A
3.3V	1.5A

Each pin on the expansion header is connected to two diodes and a resistor for protection against high or low voltages. [Figure 3-23](#) shows the protection circuitry on each of the 36 data pins. [Table 3-16](#) shows the pin assignment of the GPIO header.

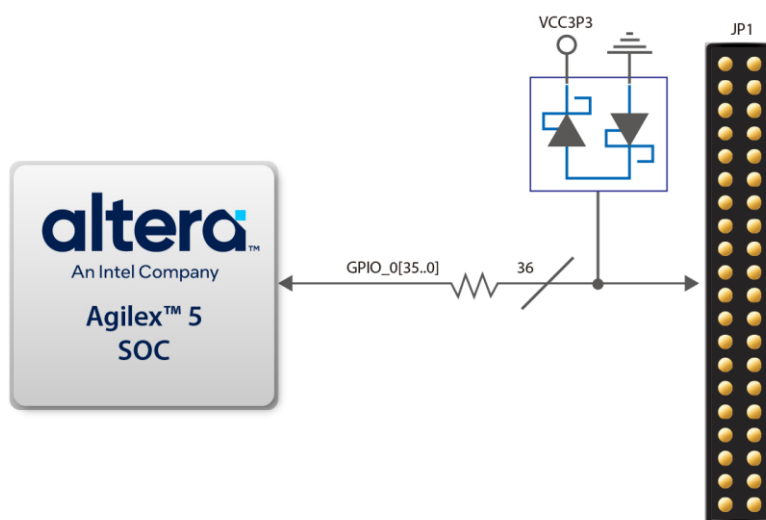


Figure 3-23 Connections between the GPIO header and Agilex 5 SoC FPGA

Table 3-16 Pin Assignment of Expansion Headers

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
GPIO[0]	PIN_BK31	GPIO Connection 0[0]	3.3V
GPIO[1]	PIN_BE43	GPIO Connection 0[1]	3.3V
GPIO[2]	PIN_BF29	GPIO Connection 0[2]	3.3V
GPIO[3]	PIN_BF40	GPIO Connection 0[3]	3.3V
GPIO[4]	PIN_BK28	GPIO Connection 0[4]	3.3V
GPIO[5]	PIN_BM31	GPIO Connection 0[5]	3.3V
GPIO[6]	PIN_BM28	GPIO Connection 0[6]	3.3V
GPIO[7]	PIN_BP31	GPIO Connection 0[7]	3.3V
GPIO[8]	PIN_BR31	GPIO Connection 0[8]	3.3V
GPIO[9]	PIN_BU28	GPIO Connection 0[9]	3.3V
GPIO[10]	PIN_BU31	GPIO Connection 0[10]	3.3V
GPIO[11]	PIN_BW28	GPIO Connection 0[11]	3.3V
GPIO[12]	PIN_BR22	GPIO Connection 0[12]	3.3V
GPIO[13]	PIN_BU19	GPIO Connection 0[13]	3.3V
GPIO[14]	PIN_BU22	GPIO Connection 0[14]	3.3V
GPIO[15]	PIN_BW19	GPIO Connection 0[15]	3.3V
GPIO[16]	PIN_BH28	GPIO Connection 0[16]	3.3V
GPIO[17]	PIN_BR28	GPIO Connection 0[17]	3.3V
GPIO[18]	PIN_BF36	GPIO Connection 0[18]	3.3V
GPIO[19]	PIN_BE29	GPIO Connection 0[19]	3.3V
GPIO[20]	PIN_BM22	GPIO Connection 0[20]	3.3V
GPIO[21]	PIN_BK22	GPIO Connection 0[21]	3.3V
GPIO[22]	PIN_BR19	GPIO Connection 0[22]	3.3V
GPIO[23]	PIN_BM19	GPIO Connection 0[23]	3.3V
GPIO[24]	PIN_BK19	GPIO Connection 0[24]	3.3V
GPIO[25]	PIN_BH19	GPIO Connection 0[25]	3.3V
GPIO[26]	PIN_BF25	GPIO Connection 0[26]	3.3V
GPIO[27]	PIN_CF9	GPIO Connection 0[27]	3.3V
GPIO[28]	PIN_CH12	GPIO Connection 0[28]	3.3V
GPIO[29]	PIN_CF12	GPIO Connection 0[29]	3.3V
GPIO[30]	PIN_CK2	GPIO Connection 0[30]	3.3V
GPIO[31]	PIN_CJ2	GPIO Connection 0[31]	3.3V
GPIO[32]	PIN_BE25	GPIO Connection 0[32]	3.3V
GPIO[33]	PIN_BF21	GPIO Connection 0[33]	3.3V
GPIO[34]	PIN_BF16	GPIO Connection 0[34]	3.3V
GPIO[35]	PIN_BE21	GPIO Connection 0[35]	3.3V

3.8.4 HSMC Connector

The board contains a High Speed Mezzanine Card (HSMC) interface to provide a mechanism for adding FPGA peripherals on daughter cards, which can address today's high speed signaling requirements as well as low-speed device interface support. The HSMC interface supports JTAG, clock outputs and inputs, high-speed serial I/O (transceivers), and single-ended signals. Signals on

the HSMC port are shown in **Figure 3-24**. **Table 3-17** shows the maximum power consumption of the daughter card that connects to the HSMC port.

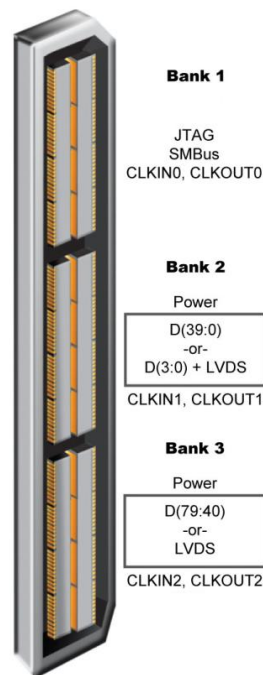


Figure 3-24 HSMC Signal Bank Diagram

Table 3-17 Power Supply of the HSMC

Supplied Voltage	Max. Current Limit
12V	1A
3.3V	1.5A

■ Adjustable I/O Standards

The voltage level of the I/O pins on the HSMC connector can be set to 3.3V, 2.5V or 1.8V using **HSMC VCCIO Header** (The default setting is 3.3V). Because the HSMC I/Os are connected to Banks 6E, 6F, 6G and 6H of the FPGA and the VCCIO voltage of these two banks are controlled by the header, users can use a jumper to select the input voltage of VCCIO6E~VCCIO6H to 3.3V, 2.5V and 1.8V to control the voltage level of the I/O pins. Please refer to **Section 3.3: HSMC VCCIO Header** part for detailed HSMC VCCIO header settings.

■ JTAG Bypass Setting

The JTAG chain on the board supports a JTAG interface extension to the HSMC connector so that the JTAG device on the user's HSMC daughter card can be joined with JTAG chain on the board. Users can enable this feature through **HSMC JTAG Header**. Please refer to **Section 3.3: HSMC JTAG Header** part for detailed HSMC JTAG header settings. In the board's default setting, the JTAG interface of the HSMC connector is bypassed to keep the board JTAG chain closed.

■ 12V Power Setting

The 12V power on the HSMC connector can be configured to be enabled or disabled by **HSMC 12V Power Header**. By default, the 12V power is disabled. This setting helps prevent accidental short circuits between the HSMC 12V power and FPGA I/O, which could otherwise cause damage when the HSMC connector is not in use. Please refer to **Section 3.3: HSMC 12V Power Header** part for detailed HSMC JTAG header settings.

■ Single-ended I/O

One big difference between the DE25-Standard and other previous DE series boards is that most FPGA I/O connected to the HSMC connector can only use **single-ended I/O** standards because they are connected to the **HVIO** bank of the Agilex 5 SoC. Other differential signal formats are not supported on the DE25-Standard.

■ High Speed GTS Transceivers

Finally, there are 4 pair of GTS transceivers connected to the Agilex SoC FPGA on the HSMC connector, which have a maximum transmission speed of 10 Gbps NRZ. User can use these GTS transceivers on high speed communication interface.

Table 3-18 Pin Assignments for HSMC connector

<i>Board Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>	<i>HSMC Pin Defined Name</i>
HSMC_D[0]	PIN_K34	CMOS I/O	Depend on JP5	HSMC_D[0]
HSMC_D[1]	PIN_F34	CMOS I/O	Depend on JP5	HSMC_D[1]
HSMC_D[2]	PIN_K37	CMOS I/O	Depend on JP5	HSMC_D[2]
HSMC_D[3]	PIN_H37	CMOS I/O	Depend on JP5	HSMC_D[3]
HSMC_D[4]	PIN_P34	CMOS I/O	Depend on JP5	HSMC_TX_D_P[0]
HSMC_D[5]	PIN_M37	CMOS I/O	Depend on JP5	HSMC_TX_D_N[0]
HSMC_D[6]	PIN_Y34	CMOS I/O	Depend on JP5	HSMC_RX_D_P[0]
HSMC_D[7]	PIN_Y15	CMOS I/O	Depend on JP5	HSMC_RX_D_N[0]
HSMC_D[8]	PIN_AK32	CMOS I/O	Depend on JP5	HSMC_TX_D_P[1]
HSMC_D[9]	PIN_M34	CMOS I/O	Depend on JP5	HSMC_TX_D_N[1]
HSMC_D[10]	PIN_AL32	CMOS I/O	Depend on JP5	HSMC_RX_D_P[1]
HSMC_D[11]	PIN_AK21	CMOS I/O	Depend on JP5	HSMC_RX_D_N[1]
HSMC_D[12]	PIN_AG29	CMOS I/O	Depend on JP5	HSMC_TX_D_P[2]
HSMC_D[13]	PIN_AL16	CMOS I/O	Depend on JP5	HSMC_TX_D_N[2]
HSMC_D[14]	PIN_AL29	CMOS I/O	Depend on JP5	HSMC_RX_D_P[2]
HSMC_D[15]	PIN_AJ1	CMOS I/O	Depend on JP5	HSMC_RX_D_N[2]
HSMC_D[16]	PIN_AL25	CMOS I/O	Depend on JP5	HSMC_TX_D_P[3]
HSMC_D[17]	PIN_AB8	CMOS I/O	Depend on JP5	HSMC_TX_D_N[3]

HSMC_D[18]	PIN_AK25	CMOS I/O	Depend on JP5	HSMC_RX_D_P[3]
HSMC_D[19]	PIN_Y8	CMOS I/O	Depend on JP5	HSMC_RX_D_N[3]
HSMC_D[20]	PIN_AK16	CMOS I/O	Depend on JP5	HSMC_TX_D_P[4]
HSMC_D[21]	PIN_AF2	CMOS I/O	Depend on JP5	HSMC_TX_D_N[4]
HSMC_D[22]	PIN_AG13	CMOS I/O	Depend on JP5	HSMC_RX_D_P[4]
HSMC_D[23]	PIN_AB4	CMOS I/O	Depend on JP5	HSMC_RX_D_N[4]
HSMC_D[24]	PIN_AH8	CMOS I/O	Depend on JP5	HSMC_TX_D_P[5]
HSMC_D[25]	PIN_AD1	CMOS I/O	Depend on JP5	HSMC_TX_D_N[5]
HSMC_D[26]	PIN_AH4	CMOS I/O	Depend on JP5	HSMC_RX_D_P[5]
HSMC_D[27]	PIN_AD2	CMOS I/O	Depend on JP5	HSMC_RX_D_N[5]
HSMC_D[28]	PIN_AE4	CMOS I/O	Depend on JP5	HSMC_TX_D_P[6]
HSMC_D[29]	PIN_V8	CMOS I/O	Depend on JP5	HSMC_TX_D_N[6]
HSMC_D[30]	PIN_T15	CMOS I/O	Depend on JP5	HSMC_RX_D_P[6]
HSMC_D[31]	PIN_Y4	CMOS I/O	Depend on JP5	HSMC_RX_D_N[6]
HSMC_D[32]	PIN_T34	CMOS I/O	Depend on JP5	HSMC_TX_D_P[7]
HSMC_D[33]	PIN_AA1	CMOS I/O	Depend on JP5	HSMC_TX_D_N[7]
HSMC_D[34]	PIN_T37	CMOS I/O	Depend on JP5	HSMC_RX_D_P[7]
HSMC_D[35]	PIN_AC43	CMOS I/O	Depend on JP5	HSMC_RX_D_N[7]
HSMC_D[36]	PIN_AC36	CMOS I/O	Depend on JP5	HSMC_TX_D_P[8]
HSMC_D[37]	PIN_Y27	CMOS I/O	Depend on JP5	HSMC_TX_D_N[8]
HSMC_D[38]	PIN_AG36	CMOS I/O	Depend on JP5	HSMC_RX_D_P[8]
HSMC_D[39]	PIN_Y24	CMOS I/O	Depend on JP5	HSMC_RX_D_N[8]
HSMC_D[40]	PIN_AB27	CMOS I/O	Depend on JP5	HSMC_TX_D_P[9]
HSMC_D[41]	PIN_AB18	CMOS I/O	Depend on JP5	HSMC_TX_D_N[9]
HSMC_D[42]	PIN_AB24	CMOS I/O	Depend on JP5	HSMC_RX_D_P[9]
HSMC_D[43]	PIN_T8	CMOS I/O	Depend on JP5	HSMC_RX_D_N[9]
HSMC_D[44]	PIN_V27	CMOS I/O	Depend on JP5	HSMC_TX_D_P[10]
HSMC_D[45]	PIN_U1	CMOS I/O	Depend on JP5	HSMC_TX_D_N[10]
HSMC_D[46]	PIN_AG21	CMOS I/O	Depend on JP5	HSMC_RX_D_P[10]
HSMC_D[47]	PIN_T18	CMOS I/O	Depend on JP5	HSMC_RX_D_N[10]
HSMC_D[48]	PIN_T27	CMOS I/O	Depend on JP5	HSMC_TX_D_P[11]
HSMC_D[49]	PIN_T4	CMOS I/O	Depend on JP5	HSMC_TX_D_N[11]
HSMC_D[50]	PIN_AJ2	CMOS I/O	Depend on JP5	HSMC_RX_D_P[11]
HSMC_D[51]	PIN_R2	CMOS I/O	Depend on JP5	HSMC_RX_D_N[11]
HSMC_D[52]	PIN_AB15	CMOS I/O	Depend on JP5	HSMC_TX_D_P[12]
HSMC_D[53]	PIN_P15	CMOS I/O	Depend on JP5	HSMC_TX_D_N[12]
HSMC_D[54]	PIN_Y18	CMOS I/O	Depend on JP5	HSMC_RX_D_P[12]
HSMC_D[55]	PIN_P4	CMOS I/O	Depend on JP5	HSMC_RX_D_N[12]
HSMC_D[56]	PIN_T24	CMOS I/O	Depend on JP5	HSMC_TX_D_P[13]
HSMC_D[57]	PIN_N2	CMOS I/O	Depend on JP5	HSMC_TX_D_N[13]
HSMC_D[58]	PIN_W1	CMOS I/O	Depend on JP5	HSMC_RX_D_P[13]
HSMC_D[59]	PIN_L1	CMOS I/O	Depend on JP5	HSMC_RX_D_N[13]
HSMC_D[60]	PIN_P24	CMOS I/O	Depend on JP5	HSMC_TX_D_P[14]
HSMC_D[61]	PIN_M4	CMOS I/O	Depend on JP5	HSMC_TX_D_N[14]
HSMC_D[62]	PIN_U2	CMOS I/O	Depend on JP5	HSMC_RX_D_P[14]
HSMC_D[63]	PIN_M8	CMOS I/O	Depend on JP5	HSMC_RX_D_N[14]

HSMC_D[64]	PIN_M27	CMOS I/O	Depend on JP5	HSMC_TX_D_P[15]
HSMC_D[65]	PIN_M15	CMOS I/O	Depend on JP5	HSMC_TX_D_N[15]
HSMC_D[66]	PIN_M24	CMOS I/O	Depend on JP5	HSMC_RX_D_P[15]
HSMC_D[67]	PIN_M18	CMOS I/O	Depend on JP5	HSMC_RX_D_N[15]
HSMC_D[68]	PIN_N1	CMOS I/O	Depend on JP5	HSMC_TX_D_P[16]
HSMC_D[69]	PIN_K15	CMOS I/O	Depend on JP5	HSMC_TX_D_N[16]
HSMC_D[70]	PIN_K27	CMOS I/O	Depend on JP5	HSMC_RX_D_P[16]
HSMC_D[71]	PIN_K18	CMOS I/O	Depend on JP5	HSMC_RX_D_N[16]
HSMC_D[72]	PIN_F37	CMOS I/O	Depend on JP5	HSMC_CLKOUT0
HSMC_D[73]	PIN_Y37	CMOS I/O	Depend on JP5	HSMC_CLKOUT_P1
HSMC_D[74]	PIN_AC46	CMOS I/O	Depend on JP5	HSMC_CLKOUT_N1
HSMC_D[75]	PIN_AG40	CMOS I/O	Depend on JP5	HSMC_CLKIN_N1
HSMC_D[76]	PIN_K24	CMOS I/O	Depend on JP5	HSMC_CLKOUT_P2
HSMC_B5B_D[0]	PIN_BF107	CMOS I/O	Depend on JP5	HSMC_CLKOUT_N2
HSMC_B5B_D[1]	PIN_BF104	CMOS I/O	Depend on JP5	HSMC_CLKIN_N2
HSMC_CLKIN0	PIN_V18	Dedicated clock input	Depend on JP5	HSMC_CLKIN0
HSMC_CLKIN1	PIN_W2	Dedicated clock input	Depend on JP5	HSMC_CLKIN_P1
HSMC_CLKIN2	PIN_V37	Dedicated clock input	Depend on JP5	HSMC_CLKIN_P2
FPGA_I2C_SCL	PIN_BR112	Management serial clock	3.3V	HSMC_SCL
FPGA_I2C_SDA	PIN_BM109	Management serial data	3.3V	HSMC_SDA
HSMC_GTS_TX_P[0]	PIN_AU129	GTS Transceiver TX bit 0	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_TX_P[0]
HSMC_GTS_TX_P[1]	PIN_AR129	GTS Transceiver TX bit 1	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_TX_P[1]
HSMC_GTS_TX_P[2]	PIN_AN129	GTS Transceiver TX bit 1	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_TX_P[2]
HSMC_GTS_TX_P[3]	PIN_AL129	GTS Transceiver TX bit 3	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_TX_P[3]
HSMC_GTS_RX_P[0]	PIN_AT135	GTS Transceiver RX bit 0	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_RX_P[0]
HSMC_GTS_RX_P[1]	PIN_AP135	GTS Transceiver RX bit 1	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_RX_P[1]
HSMC_GTS_RX_P[2]	PIN_AM135	GTS Transceiver RX bit 1	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_RX_P[2]
HSMC_GTS_RX_P[3]	PIN_AK135	GTS Transceiver RX bit 3	HIGH SPEED DIFFERENTIAL I/O	HSMC_XCVR_RX_P[3]
HSMC_GTS_RX_REF CLK_P	PIN_AT120	GTS RX Reference Clock	CML	HSMC_XCVR_RX_P[7]
HSMC_GTS_REFCLK _P	PIN_AP120	GTS Reference Clock	CML	HSMC_XCVR_RX_P[6]

3.8.5 24-bit Audio CODEC

The DE25-Standard board offers high-quality 24-bit audio via the Analog Devices SSM2603 (compatible with the Wolfson WM8731) audio CODEC (Encoder/Decoder). This chip supports

microphone-in, line-in, and line-out ports, with adjustable sample rates from 8 kHz to 96 kHz. The WM8731 is controlled via the serial I2C bus, which is connected to the HPS or Agilex 5 SoC FPGA through an I2C multiplexer. The connection of the audio circuitry to the FPGA is shown in **Figure 3-25**, and the associated FPGA pin assignments are listed in **Table 3-19**. More information about the WM8731 codec is available in its datasheet, which can be found on the manufacturer’s website, or in the directory “\datasheets\Audio CODEC” on the DE25-Standard Resource Package.

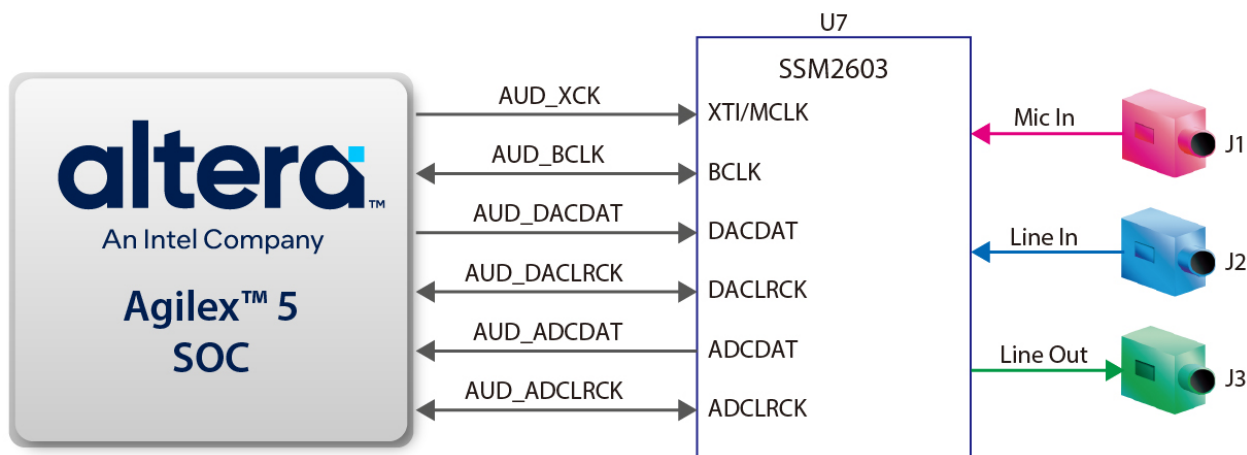


Figure 3-25 Connections between the FPGA and audio CODEC

Table 3-19 Pin Assignment of Audio CODEC

Signal Name	FPGA Pin No.	Description	I/O Standard
AUD_ADCLCK	PIN_CK88	Audio CODEC ADC LR Clock	1.2V
AUD_ADCCDAT	PIN_CL91	Audio CODEC ADC Data	1.2V
AUD_DACLCK	PIN_CK94	Audio CODEC DAC LR Clock	1.2V
AUD_DACDAT	PIN_CL88	Audio CODEC DAC Data	1.2V
AUD_XCK	PIN_CK97	Audio CODEC Chip Clock	1.2V
AUD_BCLK	PIN_CL97	Audio CODEC Bit-stream Clock	1.2V
FPGA_I2C_SCL	PIN_BR112	I2C Clock	3.3V
FPGA_I2C_SDA	PIN_BM109	I2C Data	3.3V

3.8.6 HDMI Output

The development board provides a high performance HDMI transmitter via the Analog Devices ADV7513, which incorporates HDMI v1.4 features, including 3D video support and 165 MHz support for all video formats up to 1080p and UXGA. The ADV7513 is controlled via a serial I2C bus interface, which is connected to pins on the Agilex 5 SoC FPGA. A schematic diagram of the audio circuitry is shown in **Figure 3-26**. Detailed information on using the ADV7513 HDMI TX is available on the manufacturer’s website, or under the Datasheets\HDMI folder on the DE25-Standard Resource Package.

Table 3-20 lists the HDMI Interface pin assignments and signal names relative to the FPGA.

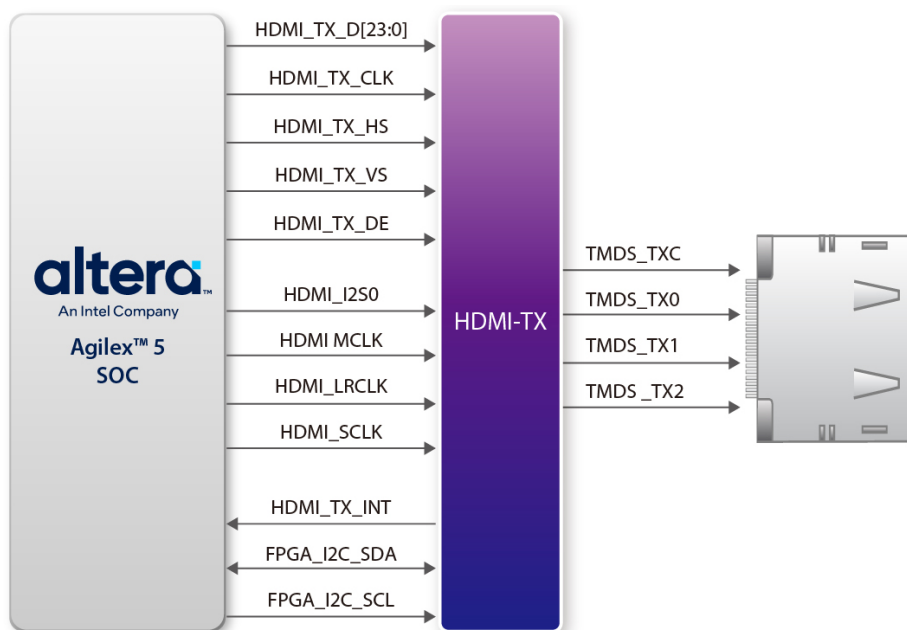


Figure 3-26 Connections between the FPGA and HDMI Transmitter Chip

Table 3-20 Pin Assignment of HMDI

Signal Name	FPGA Pin No.	Description	I/O Standard
HDMI_TX_D0	PIN_CD134	Video Data bus	3.3V
HDMI_TX_D1	PIN_CD135	Video Data bus	3.3V
HDMI_TX_D2	PIN_CG134	Video Data bus	3.3V
HDMI_TX_D3	PIN_CG135	Video Data bus	3.3V
HDMI_TX_D4	PIN_CH132	Video Data bus	3.3V
HDMI_TX_D5	PIN_CF132	Video Data bus	3.3V
HDMI_TX_D6	PIN_CF128	Video Data bus	3.3V
HDMI_TX_D7	PIN_CK134	Video Data bus	3.3V
HDMI_TX_D8	PIN_CL125	Video Data bus	3.3V
HDMI_TX_D9	PIN_CF121	Video Data bus	3.3V
HDMI_TX_D10	PIN_CF118	Video Data bus	3.3V
HDMI_TX_D11	PIN_BU118	Video Data bus	3.3V
HDMI_TX_D12	PIN_BR118	Video Data bus	3.3V
HDMI_TX_D13	PIN_CA118	Video Data bus	3.3V
HDMI_TX_D14	PIN_BW118	Video Data bus	3.3V
HDMI_TX_D15	PIN_CL128	Video Data bus	3.3V
HDMI_TX_D16	PIN_CL130	Video Data bus	3.3V
HDMI_TX_D17	PIN_CK125	Video Data bus	3.3V
HDMI_TX_D18	PIN_CK128	Video Data bus	3.3V
HDMI_TX_D19	PIN_BF111	Video Data bus	3.3V
HDMI_TX_D20	PIN_BH109	Video Data bus	3.3V
HDMI_TX_D21	PIN_BE115	Video Data bus	3.3V
HDMI_TX_D22	PIN_BF115	Video Data bus	3.3V
HDMI_TX_D23	PIN_BU109	Video Data bus	3.3V
HDMI_TX_CLK	PIN_CH59	Video Clock	3.3V

HDMI_TX_DE	PIN_BK109	Data Enable Signal for Digital Video.	3.3V
HDMI_TX_HS	PIN_BR109	Horizontal Synchronization	3.3V
HDMI_TX_VS	PIN_BE107	Vertical Synchronization	3.3V
HDMI_TX_INT	PIN_BE111	Interrupt Signal	3.3V
HDMI_I2S	PIN_BK118	I2S Channel 0 Audio Data Input	3.3V
HDMI_MCLK	PIN_BM118	Audio Reference Clock Input	3.3V
HDMI_LRCLK	PIN_BP112	Audio Left/Right Channel Signal Input	3.3V
HDMI_SCLK	PIN_BM112	I2S Audio Clock Input	3.3V
FPGA_I2C_SCL	PIN_BR112	FPGA I2C Clock	3.3V
FPGA_I2C_SDA	PIN_BM109	FPGA I2C Data	3.3V

3.8.7 Color Composite Video Decoder

The DE25-Standard board is equipped with an Analog Device ADV7180 TV decoder chip. The ADV7180 is an integrated video decoder which automatically detects and converts a standard analog color composite baseband television signal (NTSC, PAL, and SECAM) into 4:2:2 component video data, which is compatible with the 8-bit ITU-R BT.656 interface standard. The ADV7180 is compatible with wide range of video devices, including DVD players, tape-based sources, broadcast sources, and security/surveillance cameras.

The registers in the TV decoder can be accessed and set through the serial I2C bus by the Agilex 5 SoC FPGA or HPS. Note that the I2C address W/R of the TV decoder (U4) is 0x40/0x41. The pin assignments of the TV decoder is listed in [Table 3-21](#). More information about the ADV7180 is available on the manufacturer's website, or in the directory \DE1_SOC_datasheets\Video Decoder of the DE25-Standard Resource Package.

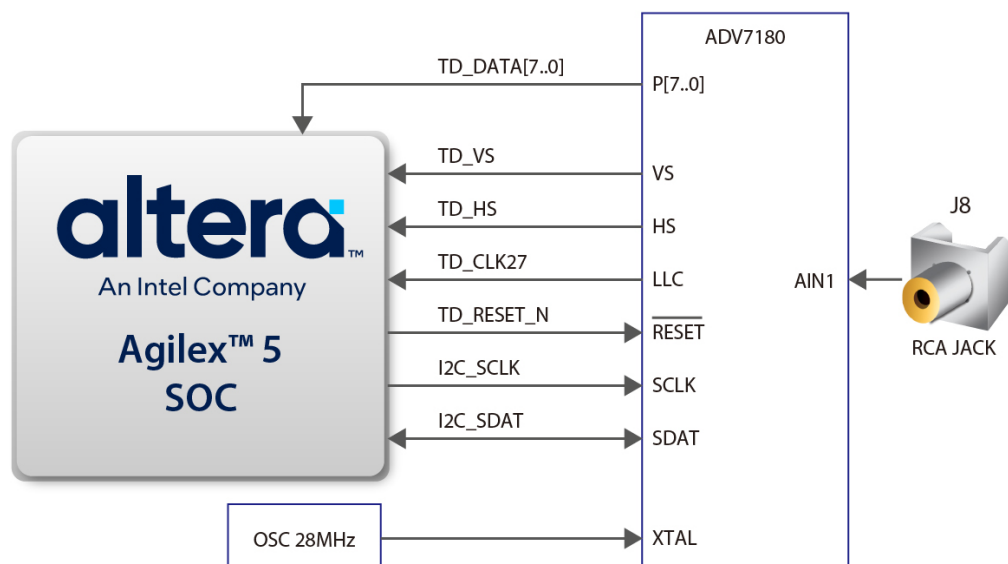


Figure 3-27 Connections between the FPGA and TV Decoder

Table 3-21 Pin Assignment of TV Decoder

Signal Name	FPGA Pin No.	Description	I/O Standard
TD_DATA [0]	PIN_BF72	TV Decoder Data[0]	1.2V
TD_DATA [1]	PIN_BE75	TV Decoder Data[1]	1.2V
TD_DATA [2]	PIN_BE79	TV Decoder Data[2]	1.2V
TD_DATA [3]	PIN_BF83	TV Decoder Data[3]	1.2V
TD_DATA [4]	PIN_BE83	TV Decoder Data[4]	1.2V
TD_DATA [5]	PIN_BE86	TV Decoder Data[5]	1.2V
TD_DATA [6]	PIN_BF86	TV Decoder Data[6]	1.2V
TD_DATA [7]	PIN_BF90	TV Decoder Data[7]	1.2V
TD_HS	PIN_BE93	TV Decoder H_SYNC	1.2V
TD_VS	PIN_BE96	TV Decoder V_SYNC	1.2V
TD_CLK27	PIN_BF75	TV Decoder Clock Input.	1.2V
TD_RESET_N	PIN_BF93	TV Decoder Reset	1.2V
FPGA_I2C_SCL	PIN_BR112	I2C Clock	3.3V
FPGA_I2C_SDA	PIN_BM109	I2C Data	3.3V

3.8.8 IR Receiver

The board comes with an infrared remote-control receiver module (model: IRM-V538/TR1), whose datasheet is provided in the directory \Datasheets\ IR Receiver and Emitter of the DE25-Standard Resource Package. The remote control, which is optional and can be ordered from the website, uses an encoding chip (uPD6121G) for generating infrared signals. **Figure 3-28** shows the connection of the IR receiver to the FPGA. **Table 3-22** shows the pin assignments of the IR receiver to the FPGA.

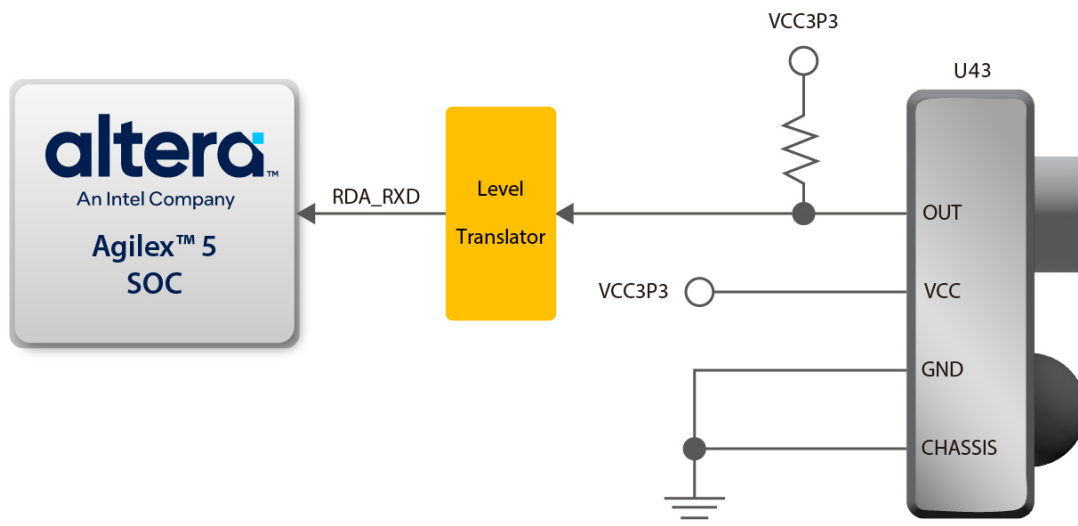


Figure 3-28 Connection between the FPGA and IR Receiver

Table 3-22 Pin Assignment of IR Receiver

Signal Name	FPGA Pin No.	Description	I/O Standard
IRDA_RXD	PIN_BH81	IR Receiver	1.2V

3.8.9 IR Emitter LED

The board has an IR emitter LED for IR communication, which is widely used for operating television device wirelessly from a short line-of-sight distance. It can also be used to communicate with other systems by matching this IR emitter LED with another IR receiver on the other side. **Figure 3-29** shows the connection of IR emitter LED to the FPGA. **Table 3-23** shows the pin assignment of IR emitter LED to the FPGA.

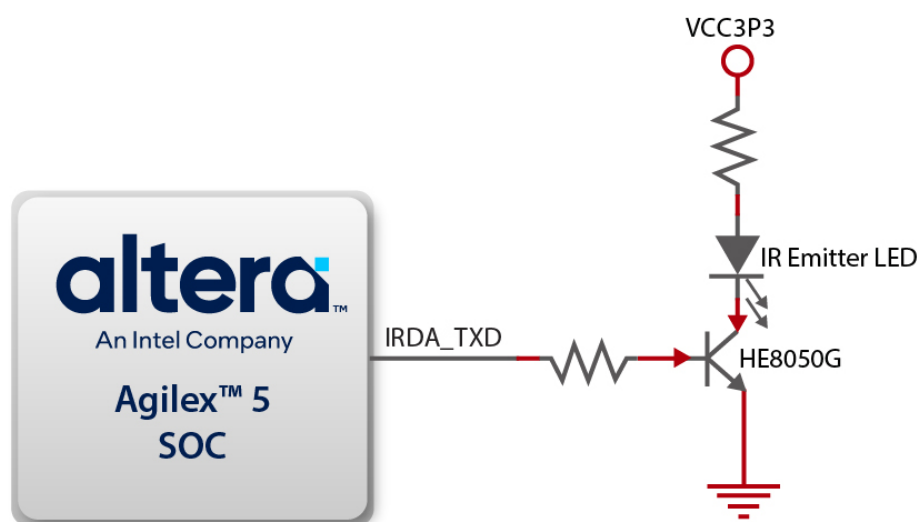


Figure 3-29 Connection between the FPGA and IR emitter LED

Table 3-23 Pin Assignment of IR Emitter LED

Signal Name	FPGA Pin No.	Description	I/O Standard
IRDA_TXD	PIN_BK78	IR Emitter	1.2V

3.8.10 DDR4 Memory

The board supports 1 GB of DDR4 SDRAM comprising two 16-bit DDR4 devices for the FPGA fabric or HPS. The I/O bank where DDR4 is located can implement the Intel Agilex 5 FPGA EMIF IP with the Hard Processor Subsystem (HPS). If no HPS EMIF IP is used in a system, the DDR4A bank can be used for the EMIF IP of the FPGA. The DDR4 SDRAM on the board can run at a clock frequency of 1200 MHz.

Figure 3-30 shows the connections between the DDR4 and the Agilex 5 SoC FPGA. **Table 3-24** lists the pin assignments of the DDR4 and their I/O standards.

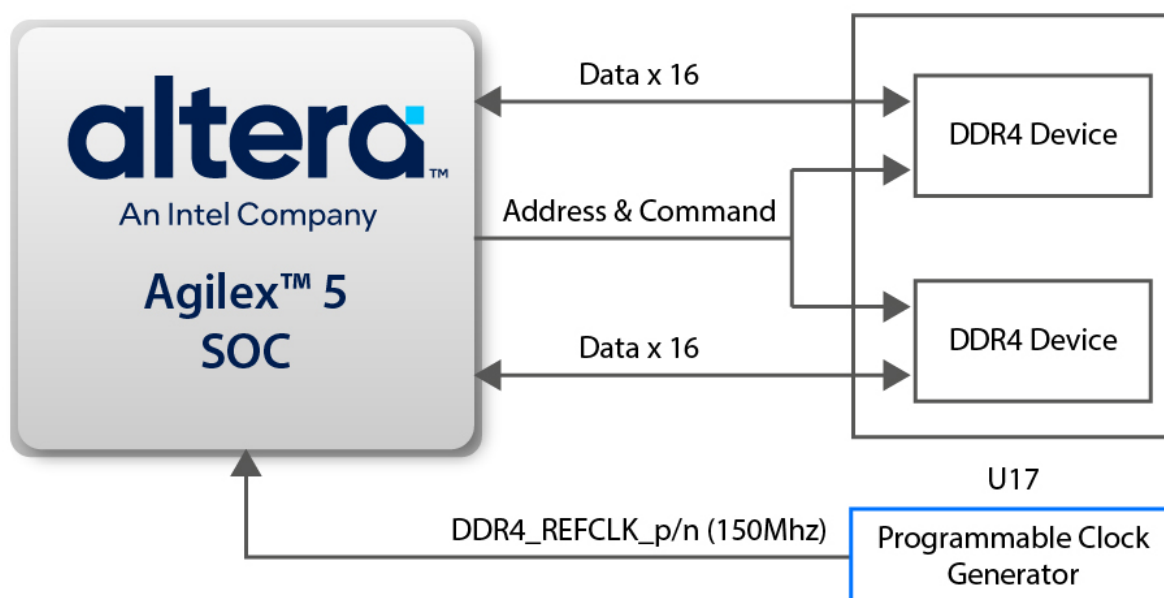


Figure 3-30 Connections between FPGA and DDR4

Table 3-24 Pin Assignment of DDR4 Memory

Signal Name	FPGA Pin No.	Description	I/O Standard
DDR4_A[0]	PIN_T114	DDR4 Address[0]	SSTL-12
DDR4_A[1]	PIN_P114	DDR4 Address[1]	SSTL-12
DDR4_A[2]	PIN_V117	DDR4 Address[2]	SSTL-12
DDR4_A[3]	PIN_T117	DDR4 Address[3]	SSTL-12
DDR4_A[4]	PIN_M114	DDR4 Address[4]	SSTL-12
DDR4_A[5]	PIN_K114	DDR4 Address[5]	SSTL-12
DDR4_A[6]	PIN_V108	DDR4 Address[6]	SSTL-12
DDR4_A[7]	PIN_T108	DDR4 Address[7]	SSTL-12
DDR4_A[8]	PIN_T105	DDR4 Address[8]	SSTL-12
DDR4_A[9]	PIN_P105	DDR4 Address[9]	SSTL-12
DDR4_A[10]	PIN_M105	DDR4 Address[10]	SSTL-12
DDR4_A[11]	PIN_K105	DDR4 Address[11]	SSTL-12
DDR4_A[12]	PIN_AG111	DDR4 Address[12]	SSTL-12
DDR4_A[13]	PIN_Y114	DDR4 Address[13]	SSTL-12
DDR4_A[14]	PIN_AB114	DDR4 Address[14]	SSTL-12
DDR4_A[15]	PIN_AK107	DDR4 Address[15]	SSTL-12
DDR4_A[16]	PIN_AK104	DDR4 Address[16]	SSTL-12
DDR4_BA[0]	PIN_AB108	DDR4 Bank Address[0]	SSTL-12
DDR4_BA[1]	PIN_Y105	DDR4 Bank Address[1]	SSTL-12
DDR4_BG[0]	PIN_AB105	Bank Group Select[0]	SSTL-12
DDR4_CKE	PIN_F105	DDR4 Clock Enable	SSTL-12
DDR4_CK	PIN_H108	DDR4 Clock p	DIFFERENTIAL 1.2-V SSTL
DDR4_CK_N	PIN_F108	DDR4 Clock	DIFFERENTIAL 1.2-V SSTL
DDR4_CS_N	PIN_K117	DDR4 Chip Select	SSTL-12

DDR4_DBI_N[0]	PIN_B119	Data Bus Inversion[0]	1.2-V POD
DDR4_DBI_N[1]	PIN_AC90	Data Bus Inversion[1]	1.2-V POD
DDR4_DBI_N[2]	PIN_V87	Data Bus Inversion[2]	1.2-V POD
DDR4_DBI_N[3]	PIN_H87	Data Bus Inversion[3]	1.2-V POD
DDR4_DQ[0]	PIN_B128	DDR4 Data[0]	1.2-V POD
DDR4_DQ[1]	PIN_A116	DDR4 Data[1]	1.2-V POD
DDR4_DQ[2]	PIN_A128	DDR4 Data[2]	1.2-V POD
DDR4_DQ[3]	PIN_B116	DDR4 Data[3]	1.2-V POD
DDR4_DQ[4]	PIN_B130	DDR4 Data[4]	1.2-V POD
DDR4_DQ[5]	PIN_B113	DDR4 Data[5]	1.2-V POD
DDR4_DQ[6]	PIN_A130	DDR4 Data[6]	1.2-V POD
DDR4_DQ[7]	PIN_A113	DDR4 Data[7]	1.2-V POD
DDR4_DQ[8]	PIN_AG100	DDR4 Data[8]	1.2-V POD
DDR4_DQ[9]	PIN_Y98	DDR4 Data[9]	1.2-V POD
DDR4_DQ[10]	PIN_AG104	DDR4 Data[10]	1.2-V POD
DDR4_DQ[11]	PIN_Y95	DDR4 Data[11]	1.2-V POD
DDR4_DQ[12]	PIN_AC96	DDR4 Data[12]	1.2-V POD
DDR4_DQ[13]	PIN_Y87	DDR4 Data[13]	1.2-V POD
DDR4_DQ[14]	PIN_AC100	DDR4 Data[14]	1.2-V POD
DDR4_DQ[15]	PIN_Y84	DDR4 Data[15]	1.2-V POD
DDR4_DQ[16]	PIN_T95	DDR4 Data[16]	1.2-V POD
DDR4_DQ[17]	PIN_K84	DDR4 Data[17]	1.2-V POD
DDR4_DQ[18]	PIN_P95	DDR4 Data[18]	1.2-V POD
DDR4_DQ[19]	PIN_M84	DDR4 Data[19]	1.2-V POD
DDR4_DQ[20]	PIN_T98	DDR4 Data[20]	1.2-V POD
DDR4_DQ[21]	PIN_V98	DDR4 Data[21]	1.2-V POD
DDR4_DQ[22]	PIN_T84	DDR4 Data[22]	1.2-V POD
DDR4_DQ[23]	PIN_P84	DDR4 Data[23]	1.2-V POD
DDR4_DQ[24]	PIN_M98	DDR4 Data[24]	1.2-V POD
DDR4_DQ[25]	PIN_D84	DDR4 Data[25]	1.2-V POD
DDR4_DQ[26]	PIN_K98	DDR4 Data[26]	1.2-V POD
DDR4_DQ[27]	PIN_K87	DDR4 Data[27]	1.2-V POD
DDR4_DQ[28]	PIN_F98	DDR4 Data[28]	1.2-V POD
DDR4_DQ[29]	PIN_F84	DDR4 Data[29]	1.2-V POD
DDR4_DQ[30]	PIN_H98	DDR4 Data[30]	1.2-V POD
DDR4_DQ[31]	PIN_M87	DDR4 Data[31]	1.2-V POD
DDR4_DQS_N[0]	PIN_A125	DDR4 Data Strobe n[0]	DIFFERENTIAL 1.2-V POD
DDR4_DQS_N[1]	PIN_AG93	DDR4 Data Strobe n[1]	DIFFERENTIAL 1.2-V POD
DDR4_DQS_N[2]	PIN_M95	DDR4 Data Strobe n[2]	DIFFERENTIAL 1.2-V POD
DDR4_DQS_N[3]	PIN_D95	DDR4 Data Strobe n[3]	DIFFERENTIAL 1.2-V POD
DDR4_DQS[0]	PIN_B122	DDR4 Data Strobe p[0]	DIFFERENTIAL 1.2-V POD

DDR4_DQS[1]	PIN_AG90	DDR4 Data Strobe p[1]	DIFFERENTIAL 1.2-V POD
DDR4_DQS[2]	PIN_K95	DDR4 Data Strobe p[2]	DIFFERENTIAL 1.2-V POD
DDR4_DQS[3]	PIN_F95	DDR4 Data Strobe p[3]	DIFFERENTIAL 1.2-V POD
DDR4_ODT	PIN_F114	DDR4 On-die Termination	SSTL-12
DDR4_PAR	PIN_K108	DDR4 Command and Address Parity Input	SSTL-12
DDR4_RESET_N	PIN_H117	DDR4 Reset	SSTL-12
DDR4_ACT_N	PIN_M117	DDR4 Activation Command Input	SSTL-12
DDR4_ALERT_N	PIN_Y108	DDR4 Register ALERT_n output	1.2 V
DDR4_RZQ	PIN_AK111	External reference ball for output drive calibration	1.2 V
DDR4_REFCLK_p	PIN_AB117	DDR4 Reference Clock p	1.2V TRUE DIFFERENTIAL SIGNALING

3.8.11 SDRAM Memory

The board features 64 MB of SDRAM with a single 64MB (32M×16) SDRAM chip. The chip connects to the FPGA with 16 data lines, 13 address lines and control lines. This chip uses the 1.8V LVC MOS signaling standard. Connections between the FPGA and SDRAM are shown in [Figure 3-31](#), and the pin assignment is listed in [Table 3-25](#).



Figure 3-31 Connections between the FPGA and SDRAM

Table 3-25 Pin Assignment of SDRAM

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
DRAM_ADDR[0]	PIN_F27	SDRAM Address[0]	1.8V
DRAM_ADDR[1]	PIN_F24	SDRAM Address[1]	1.8V
DRAM_ADDR[2]	PIN_H27	SDRAM Address[2]	1.8V
DRAM_ADDR[3]	PIN_D24	SDRAM Address[3]	1.8V
DRAM_ADDR[4]	PIN_H18	SDRAM Address[4]	1.8V
DRAM_ADDR[5]	PIN_D15	SDRAM Address[5]	1.8V
DRAM_ADDR[6]	PIN_F18	SDRAM Address[6]	1.8V
DRAM_ADDR[7]	PIN_F15	SDRAM Address[7]	1.8V
DRAM_ADDR[8]	PIN_K8	SDRAM Address[8]	1.8V
DRAM_ADDR[9]	PIN_F8	SDRAM Address[9]	1.8V
DRAM_ADDR[10]	PIN_C2	SDRAM Address[10]	1.8V
DRAM_ADDR[11]	PIN_A17	SDRAM Address[11]	1.8V
DRAM_ADDR[12]	PIN_D4	SDRAM Address[12]	1.8V
DRAM_DQ[0]	PIN_A14	SDRAM Data[0]	1.8V
DRAM_DQ[1]	PIN_A11	SDRAM Data[1]	1.8V
DRAM_DQ[2]	PIN_B14	SDRAM Data[2]	1.8V
DRAM_DQ[3]	PIN_B11	SDRAM Data[3]	1.8V
DRAM_DQ[4]	PIN_A20	SDRAM Data[4]	1.8V
DRAM_DQ[5]	PIN_A8	SDRAM Data[5]	1.8V
DRAM_DQ[6]	PIN_A23	SDRAM Data[6]	1.8V
DRAM_DQ[7]	PIN_B4	SDRAM Data[7]	1.8V
DRAM_DQ[8]	PIN_B20	SDRAM Data[8]	1.8V
DRAM_DQ[9]	PIN_B23	SDRAM Data[9]	1.8V
DRAM_DQ[10]	PIN_B26	SDRAM Data[10]	1.8V
DRAM_DQ[11]	PIN_B30	SDRAM Data[11]	1.8V
DRAM_DQ[12]	PIN_A39	SDRAM Data[12]	1.8V
DRAM_DQ[13]	PIN_A30	SDRAM Data[13]	1.8V
DRAM_DQ[14]	PIN_A35	SDRAM Data[14]	1.8V
DRAM_DQ[15]	PIN_A33	SDRAM Data[15]	1.8V
DRAM_BA[0]	PIN_D34	SDRAM Bank Address[0]	1.8V
DRAM_BA[1]	PIN_F4	SDRAM Bank Address[1]	1.8V
DRAM_LDQM	PIN_K4	SDRAM byte Data Mask[0]	1.8V
DRAM_UDQM	PIN_G2	SDRAM byte Data Mask[1]	1.8V
DRAM_RAS_N	PIN_G1	SDRAM Row Address Strobe	1.8V
DRAM_CAS_N	PIN_J1	SDRAM Column Address Strobe	1.8V
DRAM_CKE	PIN_B35	SDRAM Clock Enable	1.8V
DRAM_CLK	PIN_B39	SDRAM Clock	1.8V
DRAM_WE_N	PIN_J2	SDRAM Write Enable	1.8V
DRAM_CS_N	PIN_H8	SDRAM Chip Select	1.8V

3.8.12 A/D Converter and 2x5 Header

The DE25-Standard features the TI TLA2518, an 8-channel, multiplexed, 12-bit successive approximation register (SAR) analog-to-digital converter capable of sampling rates up to 1 MSPS. The analog input range for all input channels extends from 0 V to 3.4V (default setting is 3.4V, it can be modified to 5.1 V). The flexible SPI interface allows the external serial output data clock (SCLK) to operate at frequencies up to 60 MHz. The ADC can be configured to accept eight single-ended analog input signals at ADC_IN0 through ADC_IN7. Alternatively, these pins can be reconfigured as digital inputs or outputs in GPIO mode. These eight signals are routed to a 2×5 header, as shown in **Figure 3-32**.

More information about the A/D converter chip is available in its datasheet, which can be found on the manufacturer's website or in the directory \datasheet\ADC of the DE25-Standard Resource Package.

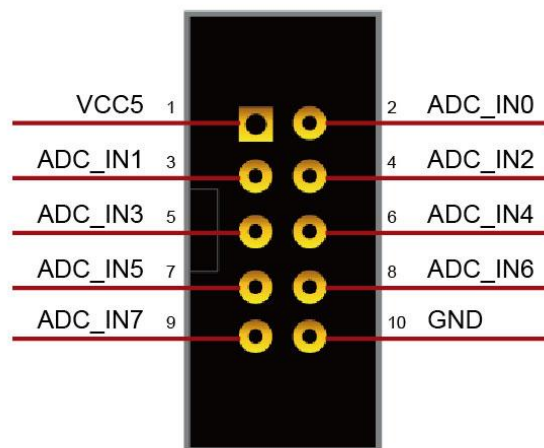


Figure 3-32 Signals of the 2x5 Header

Figure 3-33 shows the connections between the FPGA, 2×5 header, and the A/D converter. **Table 3-26** shows the pin assignment of the A/D converter.

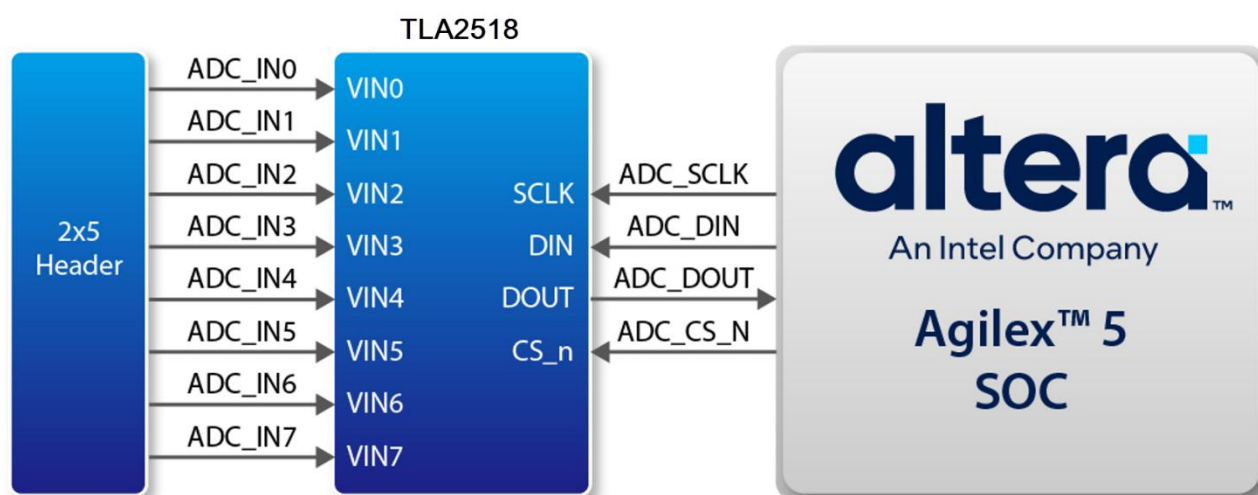


Figure 3-33 Connections between the FPGA, 2x5 header, and the A/D converter

Table 3-26 Pin Assignment of ADC

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
ADC_CONVST	PIN_BP22	Conversion Start	3.3V
ADC_DOUT	PIN_CK4	Digital data input	3.3V
ADC_DIN	PIN_BF32	Digital data output	3.3V
ADC_SCLK	PIN_CH4	Digital clock input	3.3V

3.8.13 MIPI Connector

The Agilex 5 devices offer a native mobile industry processor interface (MIPI) D-PHY. This support complies with MIPI D-PHY version 2.5 and allows transmission or reception of data with MIPI D-PHY interfaces. It provides the PHY-protocol interface (PPI) to connect with camera serial interface (CSI) and display serial interface (DSI) applications.

The board provides a 22-pin FPC connector (1 clock lane and 2 data lanes), allowing users to connect MIPI interface cameras and display devices through a FPC cable (see [Figure 3-34](#)). Users can use this connector and camera cable to connect to devices such as Raspberry Pi camera modules. In addition, it can also be connected with a display device such as a Raspberry Pi MIPI display module.

[Figure 3-35](#) shows the connections between the FPGA and the 22-pin MIPI connector. [Table 3-27](#) shows the pin assignments of the 22-pin MIPI connector.

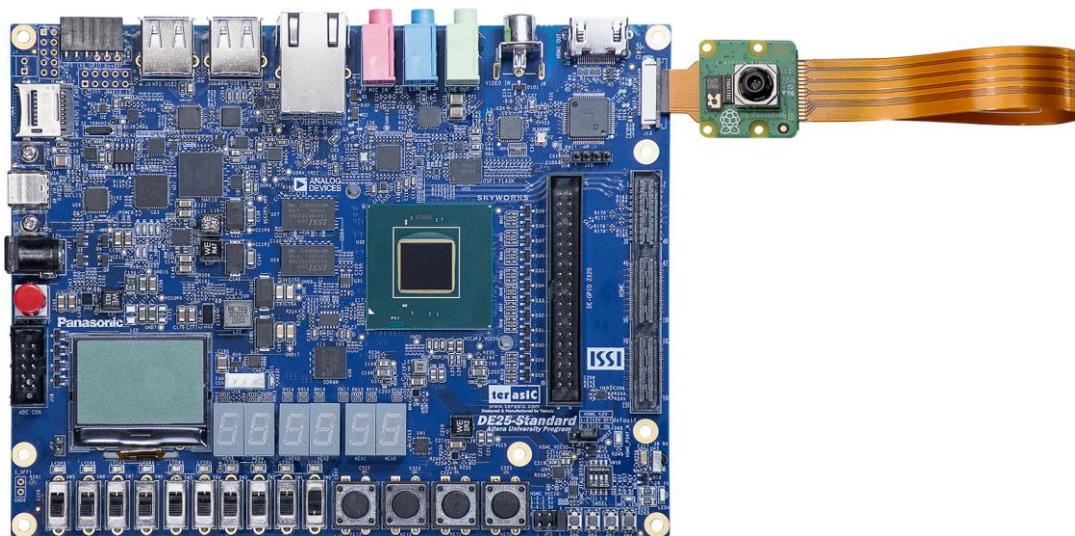


Figure 3-34 MIPI camera module connects to the board via cable

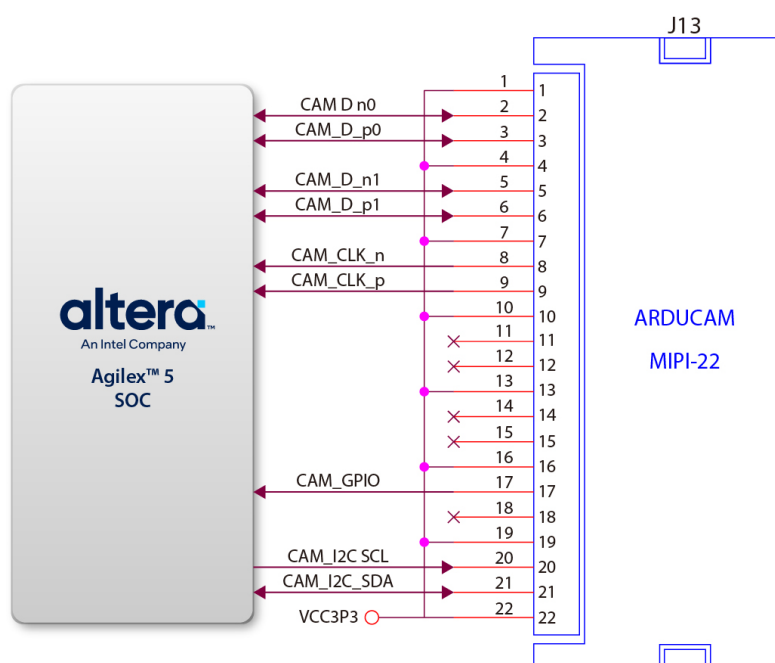


Figure 3-35 Connections between the FPGA and the 22-pin MIPI connector

Table 3-27 Pin Assignment of 22-pin MIPI connector

Signal Name	FPGA Pin No.	Description	I/O Standard
CAM_CLK_P	PIN_BW69	MIPI Clock positive	DPHY
CAM_CLK_N	PIN_CA69	MIPI Clock negative	DPHY
CAM_D_P[0]	PIN_BR69	MIPI Data 0 positive	DPHY
CAM_D_P[1]	PIN_BR71	MIPI Data 1 positive	DPHY
CAM_D_N[0]	PIN_BU69	MIPI Data 0 negative	DPHY
CAM_D_N[1]	PIN_BU71	MIPI Data 1 negative	DPHY
CAM_I2C_SCL (FPGA_I2C_SCL)	PIN_BF120	I2C clock	3.3V

CAM_I2C_SDA (FPGA_I2C_SDA)	PIN_BH118	I2C data	3.3V
CAM_GPIO	PIN_BK112	GPIO signal	3.3V
CAM_RZQ1	PIN_BH69	External reference ball for output drive calibration	1.2V

3.9 Peripherals Connected to the Hard Processor System (HPS)

This section introduces the interfaces connected to the HPS section of the Agilex 5 SoC FPGA. Users can access these interfaces via the HPS processors.

3.9.1 User Push-buttons and LEDs

Similar to the FPGA, the HPS is directly connected to its own pushbutton and LED through its GPIO interface, which can be read or written from code running on the HPS processors.

Table 3-28 gives the pin assignment of all the LEDs, switches, and push-buttons.

Table 3-28 Pin Assignment of LEDs, Switches and Push-buttons

<i>Signal Name</i>	<i>HPS GPIO</i>	<i>FPGA Pin No.</i>	<i>Function</i>
HPS_KEY	GPIO1_IO15	PIN_K124	I/O
HPS_LED	GPIO1_IO16	PIN_Y127	I/O

3.9.2 Gigabit Ethernet

The board supports Gigabit Ethernet communication through an external Micrel KSZ9031RN PHY chip and HPS Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports an RGMII MAC interface. **Figure 3-36** shows the connections between the HPS, Gigabit Ethernet PHY, and RJ-45 connector.

The pin assignment associated with the Gigabit Ethernet interface is listed in **Table 3-29**. More information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, is available on the manufacturer's website.

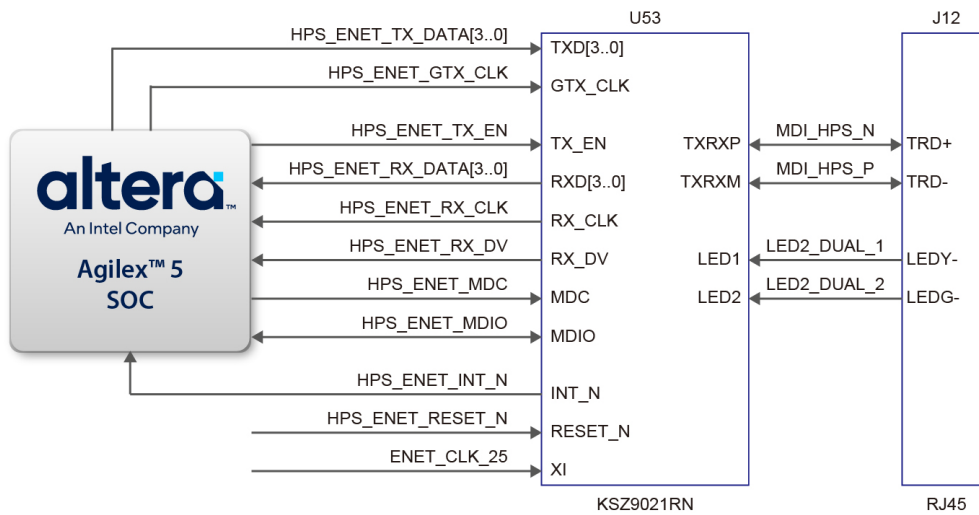


Figure 3-36 Connections between the HPS and Gigabit Ethernet

Table 3-29 Pin Assignment of Gigabit Ethernet PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_ENET_TX_CTL	PIN_L135	GMII and MII transmit enable	1.8V
HPS_ENET_TX_DATA[0]	PIN_M132	GMII and MII transmit data[0]	1.8V
HPS_ENET_TX_DATA[1]	PIN_AD134	GMII and MII transmit data[1]	1.8V
HPS_ENET_TX_DATA[2]	PIN_J134	GMII and MII transmit data[2]	1.8V
HPS_ENET_TX_DATA[3]	PIN_AG120	GMII and MII transmit data[3]	1.8V
HPS_ENET_TX_CLK	PIN_P132	GMII and MII transmit clock	1.8V
HPS_ENET_RX_CTL	PIN_AD135	GMII and MII receive data valid	1.8V
HPS_ENET_RX_DATA[0]	PIN_K132	GMII and MII receive data[0]	1.8V
HPS_ENET_RX_DATA[1]	PIN_AG129	GMII and MII receive data[1]	1.8V
HPS_ENET_RX_DATA[2]	PIN_G134	GMII and MII receive data[2]	1.8V
HPS_ENET_RX_DATA[3]	PIN_G135	GMII and MII receive data[3]	1.8V
HPS_ENET_RX_CLK	PIN_J135	GMII and MII receive clock	1.8V
HPS_ENET_MDIO	PIN_F124	Management Data	1.8V
HPS_ENET_MDC	PIN_D124	Management Data Clock Reference	1.8V

There are two LEDs, green LED (LEDG) and yellow LED (LEDY), which report the status of Ethernet PHY (KSZ9031RNI). The LED control signals are connected to the LEDs on the RJ45 connector. The state and definition of LEDG and LEDY are listed in Table 3-30. For instance, the LEDG light indicates the connection from the board to the Gigabit Ethernet interface has been established.

Table 3-30 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)

H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	10 Link / Activity (RX, TX)

3.9.3 UART to USB

The board provides a UART interface for users to communicate and transfer data with the HPS through the host. The interface is implemented via the FT2232H chip in the USB Blaster III circuit. Connecting a USB cable between the DE25-Standard's Type-C port and the host enables both USB Blaster III and HPS UART functions.

Figure 3-37 shows the connections between the FPGA (HPS), FT2232H chip, and the USB Type-C connector. **Table 3-31** lists the pin assignments of the UART interface connected to the HPS.

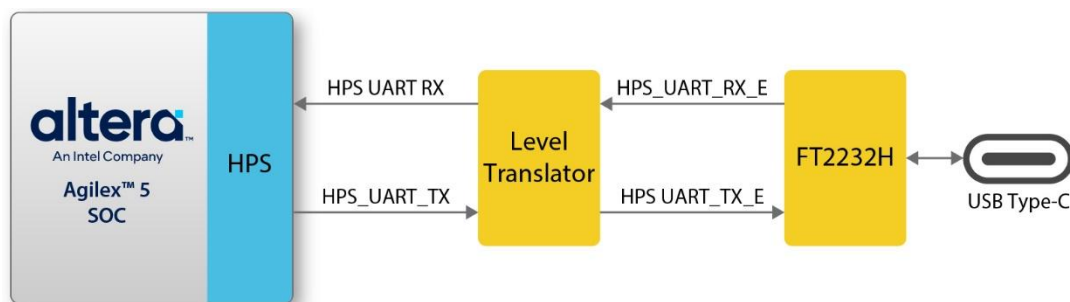


Figure 3-37 Connections between the HPS and CP2105 Chip

Table 3-31 Pin Assignment of UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_AB127	HPS UART Receiver	1.8V
HPS_UART_TX	PIN_M124	HPS UART Transmitter	1.8V

3.9.4 Micro SD Card Socket

The board supports a Micro SD card interface with 4 data lines. It serves not only as an external storage for the HPS but also as an alternative boot option for the DE25-Standard board. **Figure 3-38** shows the signals connected between the HPS and the Micro SD card socket.

Table 3-32 lists the pin assignment of Micro SD card socket to the HPS.

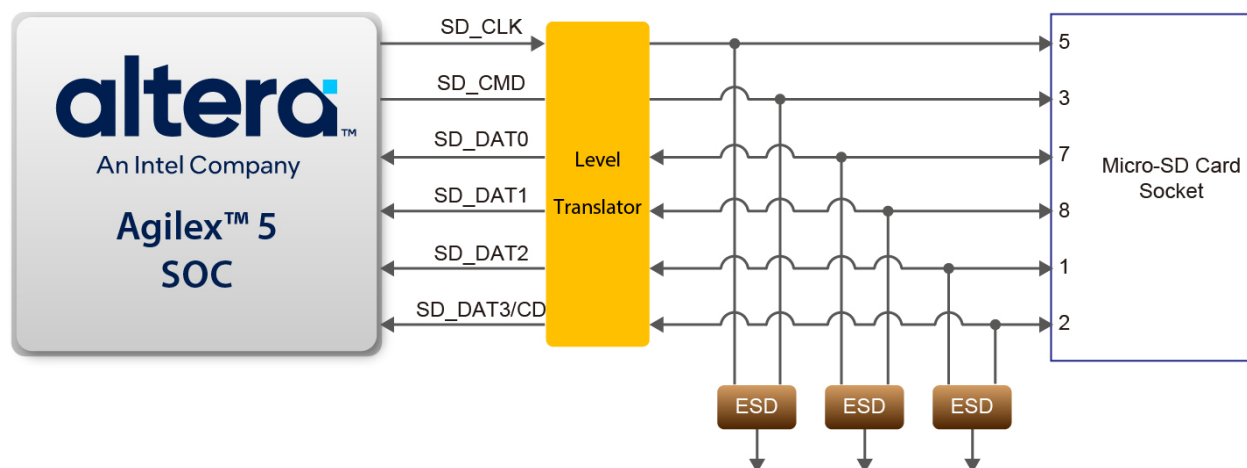


Figure 3-38 Connections between the FPGA and SD card socket

Table 3-32 Pin Assignment of Micro SD Card Socket

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_SD_CLK	PIN_D132	HPS SD Clock	1.8V
HPS_SD_CMD	PIN_AB132	HPS SD Command Line	1.8V
HPS_SD_DATA[0]	PIN_E135	HPS SD Data[0]	1.8V
HPS_SD_DATA[1]	PIN_F132	HPS SD Data[1]	1.8V
HPS_SD_DATA[2]	PIN_AA135	HPS SD Data[2]	1.8V
HPS_SD_DATA[3]	PIN_V127	HPS SD Data[3]	1.8V

3.9.5 2-port USB Host

The board has two USB 2.0 Type-A ports with a SMSC USB3300 controller and a 2-port hub controller. The SMSC USB3300 device in a 32-pin QFN package interfaces with the SMSC USB2512B hub controller. This device supports UTMI+ Low Pin Interface (ULPI), which communicates with the USB 2.0 controller in the HPS. The PHY operates in Host mode by connecting the ID pin of USB3300 to ground. When operating in Host mode, the device is powered by the two USB type-A ports. **Figure 3-39** shows the connections of USB PTG PHY to the HPS. **Table 3-33** lists the pin assignment of the USBOTG PHY to the HPS.

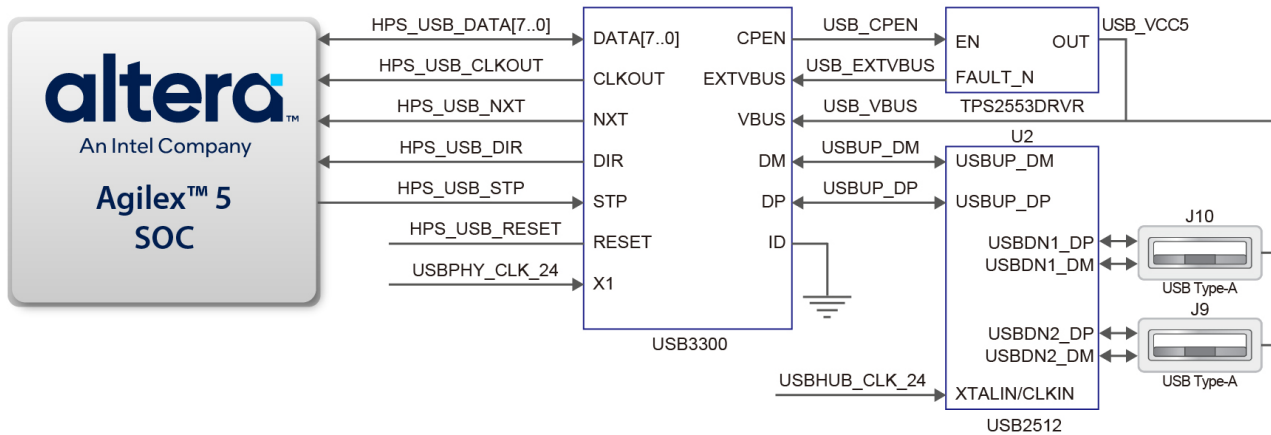


Figure 3-39 Connections between the HPS and USB OTG PHY

Table 3-33 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_USB_CLKOUT	PIN_W135	60MHz Reference Clock Output	1.8V
HPS_USB_DATA[0]	PIN_AK115	HPS USB_DATA[0]	1.8V
HPS_USB_DATA[1]	PIN_U134	HPS USB_DATA[1]	1.8V
HPS_USB_DATA[2]	PIN_R134	HPS USB_DATA[2]	1.8V
HPS_USB_DATA[3]	PIN_AG115	HPS USB_DATA[3]	1.8V
HPS_USB_DATA[4]	PIN_N135	HPS USB_DATA[4]	1.8V
HPS_USB_DATA[5]	PIN_AK120	HPS USB_DATA[5]	1.8V
HPS_USB_DATA[6]	PIN_N134	HPS USB_DATA[6]	1.8V
HPS_USB_DATA[7]	PIN_T132	HPS USB_DATA[7]	1.8V
HPS_USB_DIR	PIN_W134	Direction of the Data Bus	1.8V
HPS_USB_NXT	PIN_AL120	Throttle the Data	1.8V
HPS_USB_STP	PIN_U135	Stop Data Stream on the Bus	1.8V

3.9.6 Accelerometer (G-sensor)

The board comes with a digital accelerometer sensor module (ADXL345), commonly known as a G-sensor. This G-sensor is a small, thin, ultra-low-power-consumption 3-axis accelerometer with high-resolution measurement. Digitized output is formatted in 16-bit two's complement and can be accessed through an I2C interface. The I2C address of the G-sensor is 0xA6/0xA7. More information about this chip can be found in its datasheet, which is available on the manufacturer's website or in the \Datasheet folder of the DE25-Standard Resource Package. **Figure 3-40** shows the connections between the HPS and the G-sensor. **Table 3-34** lists the pin assignments of the G-sensor to the HPS.

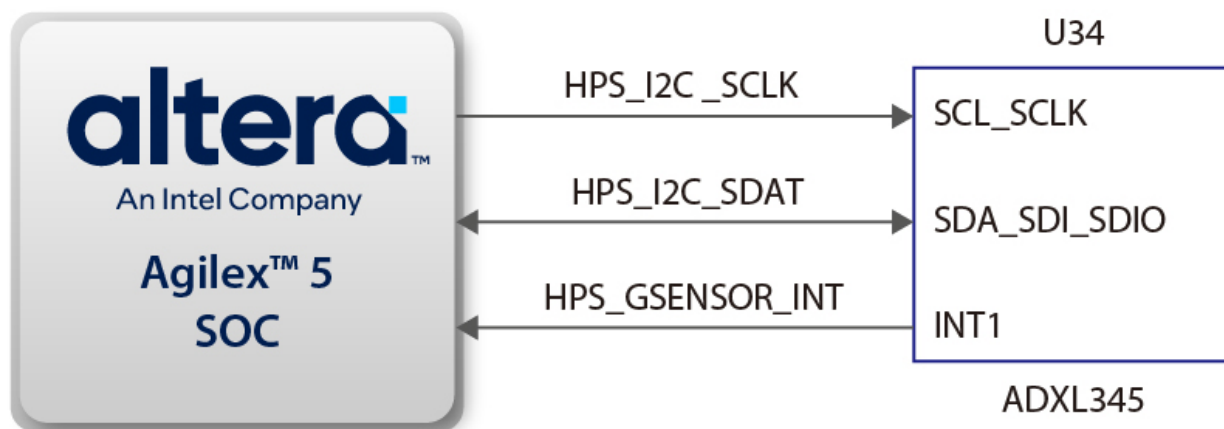


Figure 3-40 Connections between Agilex 5 SoC FPGA and G-Sensor

Table 3-34 Pin Assignment of G-senor

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_GSENSOR_INT	PIN_B134	HPS GSENSOR Interrupt Output	1.8V
HPS_I2C_SCL	PIN_K127	HPS I2C Clock	1.8V
HPS_I2C_SDA	PIN_M127	HPS I2C Data	1.8V

3.9.7 1×6 Header

The board has a 1×6 pin header connected to two GPIO pins and an I2C bus on the HPS. Users can connect these pins to a device and control it through the HPS. The header also provides one 3.3V power and one ground pin. Note that all I/Os on the header are connected to the FPGA via a level translator. Each I/O pin on the header can be connected with a 3.3V I/O standard. Connections between the HPS and the 1×6 pin header are shown in Figure 3-41, and the pin assignments of the 1×6 pin header is listed in

Table 3-35.

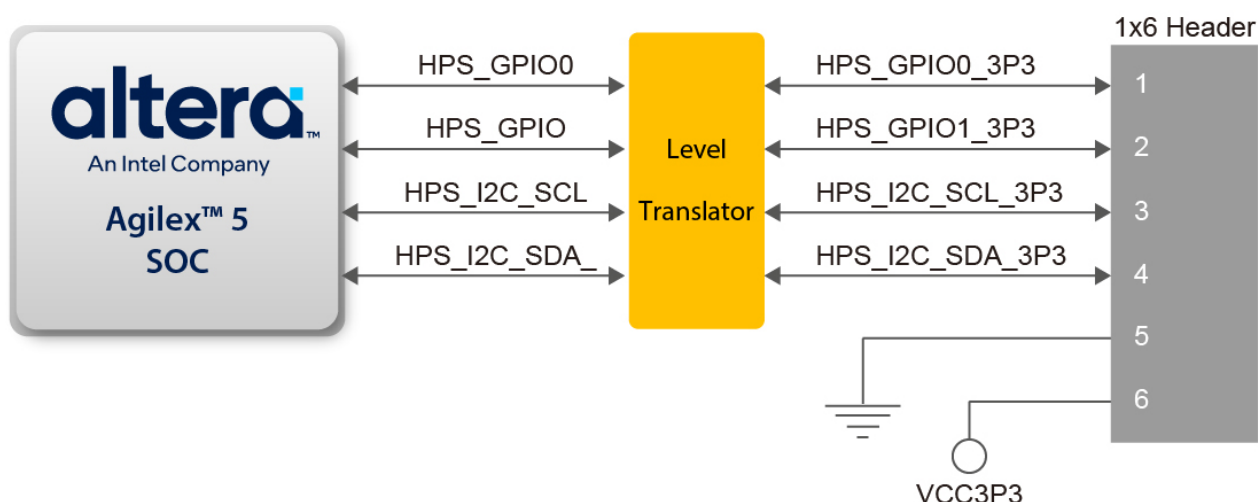


Figure 3-41 Connections between the HPS and 1x6 Header

Table 3-35 Pin Assignment of 1x6 GPIO Connector

Header Pin No.	Signal Name	FPGA Pin No.	Description	Header I/O Standard
1	HPS_GPIO0	PIN_T127	HPS GPIO 0	3.3V (1.8V to HPS via level translator)
2	HPS_GPIO1	PIN_Y132	HPS GPIO 1	3.3V (1.8V to HPS via level translator)
3	HPS_I2C_SCL	PIN_K127	HPS I2C Clock	3.3V (1.8V to HPS via level translator)
4	HPS_I2C_SDA	PIN_M127	HPS I2C Data	3.3V (1.8V to HPS via level translator)
5	GND	-	Ground	-
6	3.3V Power	-	3.3V Power	-

3.9.8 128×64 Pixel LCD

The board is equipped with a 128×64 pixel LCD Module. The LCD module communicates with the HPS through an SPI (serial peripheral interface) port. To use the LCD module, please refer to the datasheet folder in the Resource Package. **Figure 3-42** shows the connections between the HPS and LCD module. The default setting for the LCD backlight power is OFF (the pins of header JP4 are open). **Table 3-36** lists the pin assignments between the LCD module and the Agilinx 5 SoC FPGA.

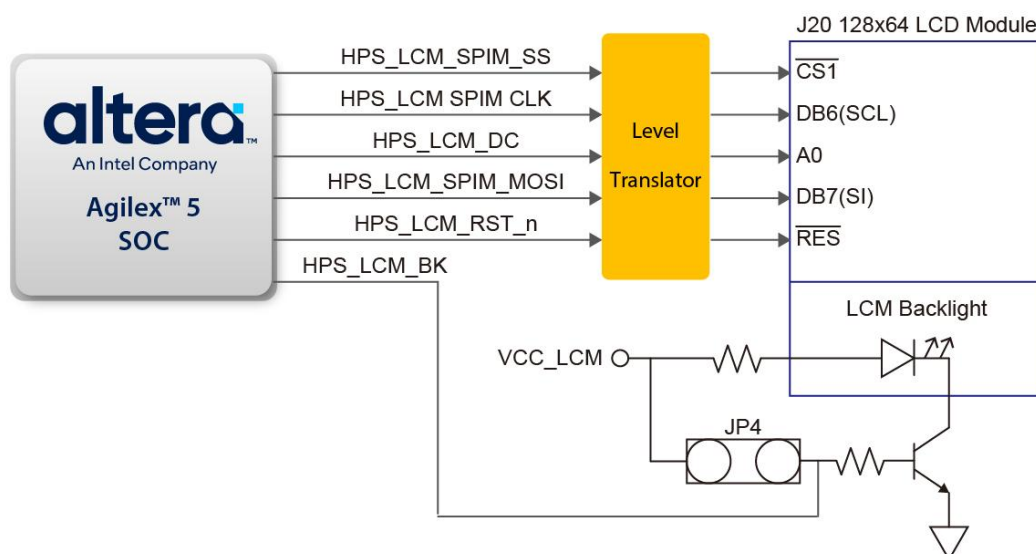


Figure 3-42 Connections between Agilinx 5 SoC FPGA and LCD Module

Table 3-36 LCD Module Pin Assignments

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_LCM_D_C	PIN_P124	HPS LCM Data bit is Data/Command	1.8V
HPS_LCM_RST_N	PIN_T124	HPS LCM Reset	1.8V
HPS_LCM_SPIM_CLK	PIN_F127	SPI Clock	1.8V
HPS_LCM_SPIM_MOSI	PIN_Y124	SPI Master Output /Slave Input	1.8V
HPS_LCM_SPIM_SS	PIN_AB124	SPI Slave Select	1.8V

3.9.9 Real-Time Clock (RTC)

The DE25-Standard development board features an onboard NXP PCF85263A Real-Time Clock (RTC) chip (see **Figure 3-43**). This device interfaces with the HPS (Hard Processor System) via the I²C bus, providing accurate and battery-backed time and date information to the system.

To ensure continuous timekeeping when the main power supply (VCC3P3) is turned off, the board is equipped with a CR1220 coin-cell battery holder (as shown in **Figure 3-44**). When the main power is interrupted, the RTC automatically switches to battery power, allowing the system to retain accurate time upon restart.

In addition, the board includes a 2-pin expansion header (J7, see **Figure 3-45**) designed to supply an independent 3.3 V power source to the PCF85263A. This header is not populated by default. **The 7-bit I²C device address of the PCF85263A is 0x51.**

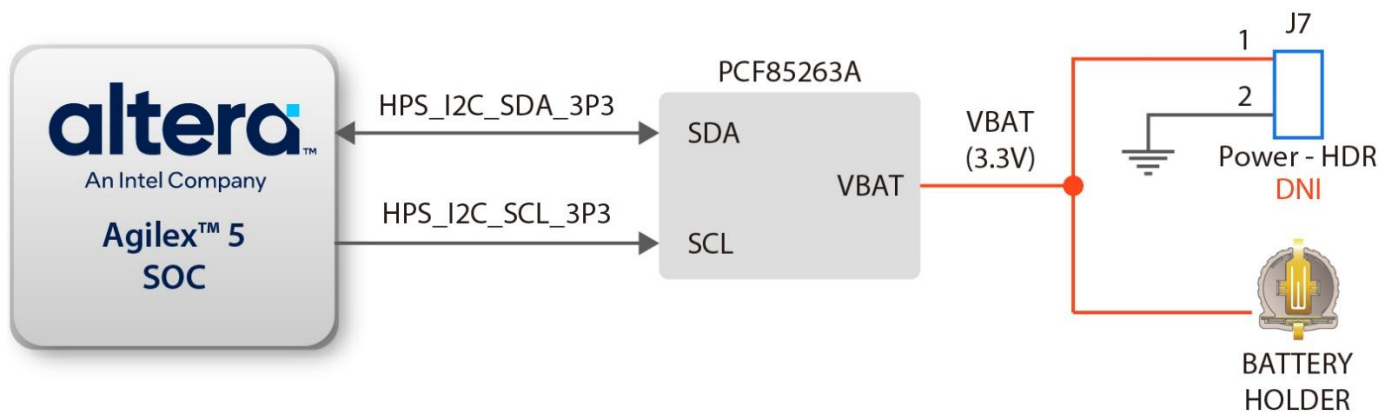


Figure 3-43 Connections between Agilex 5 SoC FPGA and RTC

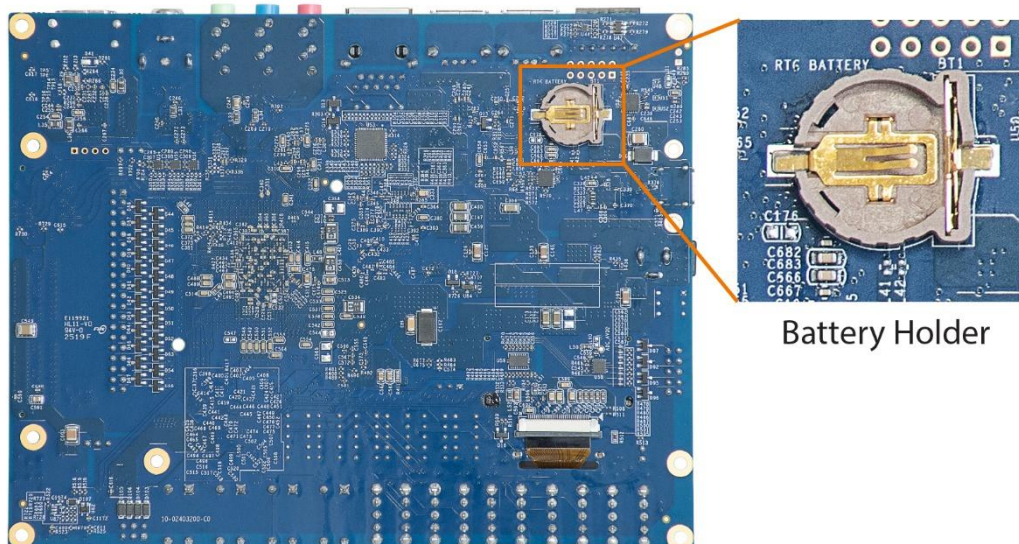


Figure 3-44 Battery Holder position

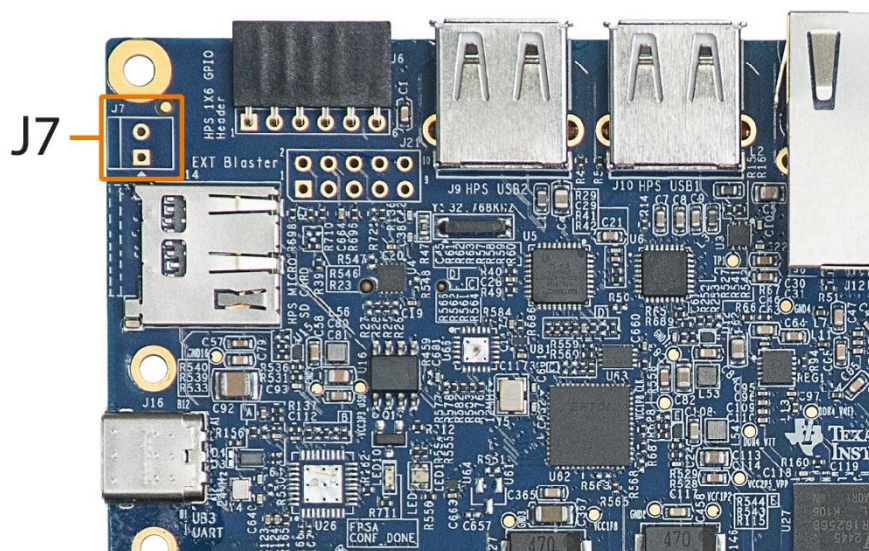


Figure 3-45 J7 Header position

Table 3-37 Pin Assignment of HPS I2C

Signal Name	FPGA Pin No.	Description	Header I/O Standard
HPS_I2C_SCL	PIN_K127	HPS I2C Clock	3.3V (1.8V to HPS via level translator)
HPS_I2C_SDA	PIN_M127	HPS I2C Data	3.3V (1.8V to HPS via level translator)

Chapter 4

DE25-Standard System Builder

The developers can start their Quartus project based on the golden_top quartus project included in the DE25-Standard Resource Package. Nevertheless, if developers plan to use Terasic daughters or require only a few interfaces in DE25-Standard, the System Builder can assist developers to establish Quartus project within minutes.

This chapter describes how users can create a custom design project with the tool named DE25-Standard System Builder.

4.1 Introduction

The DE25-Standard System Builder is a Windows-based utility. It is designed to help users create a Quartus II project for DE25-Standard within minutes. The generated Quartus II project files include:

- Quartus II project file (.qpf)
- Quartus II setting file (.qsf)
- Top-level design file (.v or .vhd)
- Synopsis design constraints file (.sdc)
- Pin assignment document (.htm)

The above files generated by the DE25-Standard System Builder can also prevent occurrence of situations that are prone to compilation error when users manually edit the top-level design file or place pin assignment. The common mistakes users may encounter are:

- Board is damaged due to incorrect bank voltage setting or pin assignment.
- Board is malfunctioned because of wrong device chosen, declaration of pin location or direction is incorrect or forgotten.
- Performance degradation due to improper pin assignment.

4.2 Design Flow

This section provides an introduction to the design flow of building a Quartus II project for DE25-

Standard under the DE25-Standard System Builder. The design flow is illustrated in **Figure 4-1**.

The DE25-Standard System Builder will generate two major files, a top-level design file (.v or .vhd) and a Quartus II setting file (.qsf) after users launch the DE25-Standard System Builder and create a new project according to their design requirements.

The top-level design file contains a top-level Verilog or VHDL HDL wrapper for users to add their own design/logic. The Quartus II setting file contains information such as FPGA device type, top-level pin assignment, and the I/O standard for each user-defined I/O pin.

Finally, the Quartus II programmer is used to download .sof file to the development board via JTAG interface.

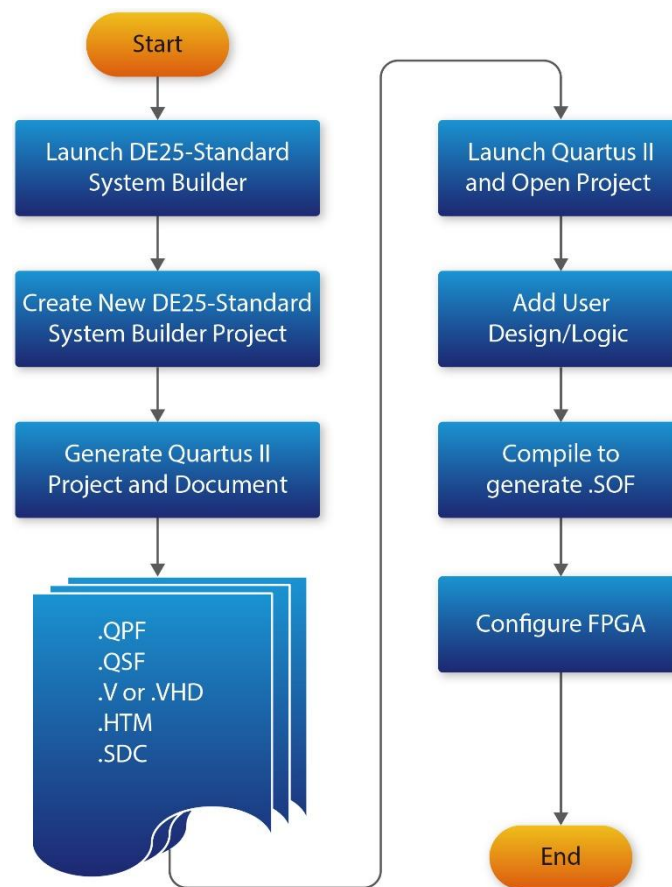


Figure 4-1 Design flow of building a project from the beginning to the end

4.3 Using DE25-Standard System Builder

This section provides the complete procedure on how to use the DE25-Standard System Builder.

■ Install and Launch the DE25-Standard System Builder

The DE25-Standard System Builder is located in the directory: “Tools\SystemBuilder” of the DE25-Standard Resource Package. Users can copy the entire folder to a host computer without installing the utility. A window will pop up, as shown in **Figure 4-2**, after executing the DE25-Standard SystemBuilder.exe on the host computer.

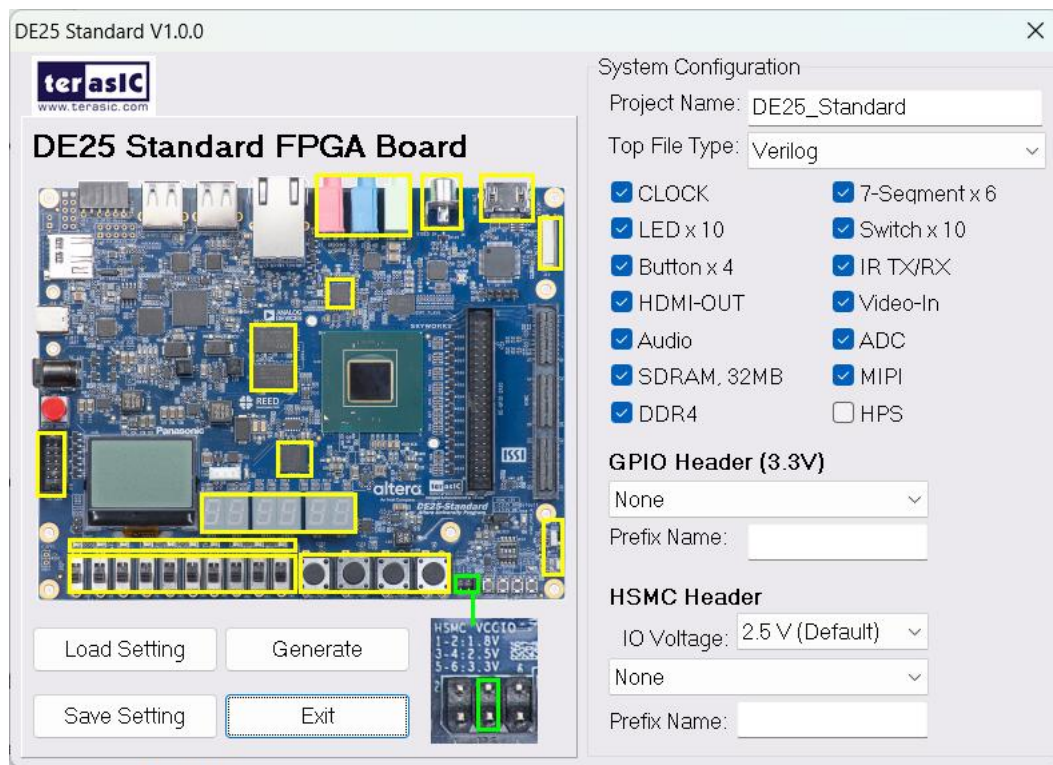


Figure 4-2 The GUI of DE25-Standard System Builder

■ Enter Project Name

Enter the project name in the circled area, as shown in **Figure 4-3**.

The project name typed in will be assigned automatically as the name of your top-level design entity.

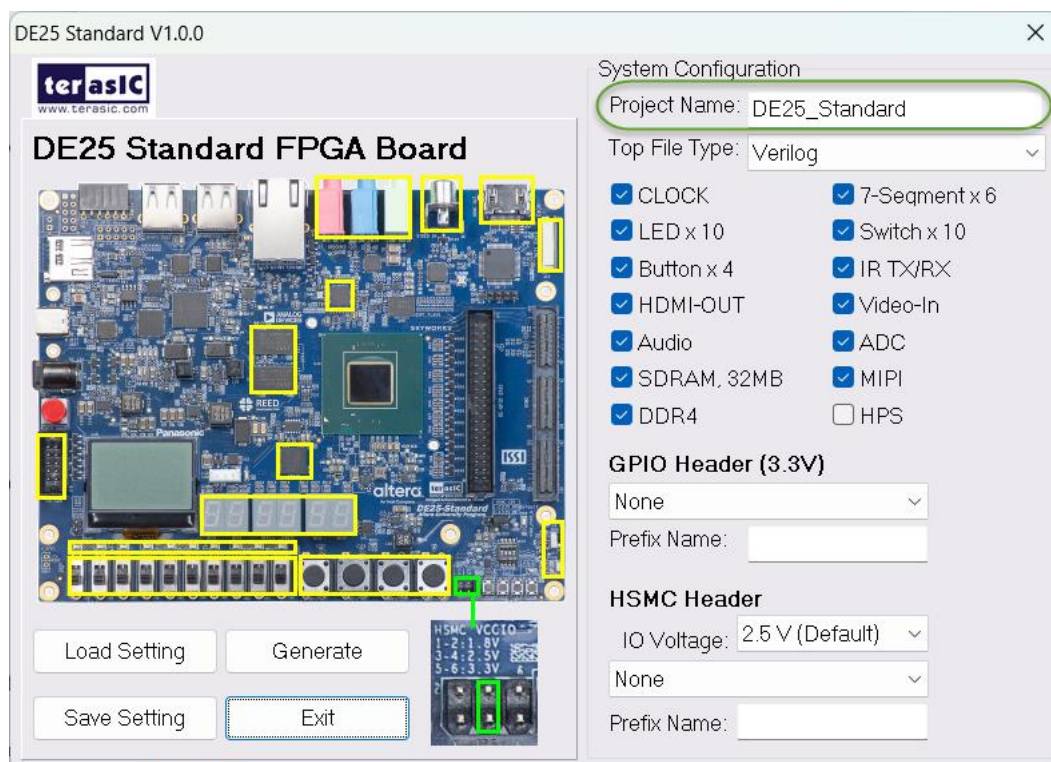


Figure 4-3 Enter the project name

■ Top File Type

Select the desired HDL type, as shown in **Figure 4-4**. If **Verilog** is selected, a .v Verilog HDL top file will be generated. If **VHDL** HDL is selected, a .vhd VHDL top file will be generated.

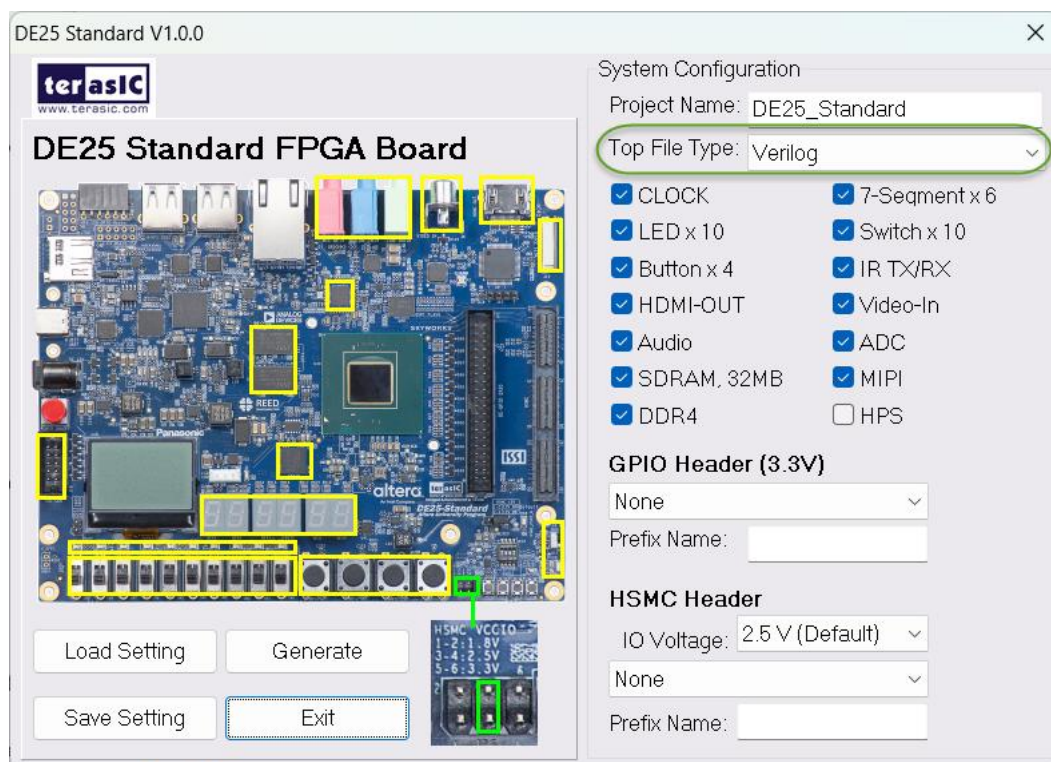


Figure 4-4 Select Top File Type

■ System Configuration

Users are given the flexibility in the System Configuration to include their choice of components in the project, as shown in [Figure 4-5](#). Each component onboard is listed and users can enable or disable one or more components at will. If a component is enabled, the DE25-Standard System Builder will automatically generate its associated pin assignment, including the pin name, pin location, pin direction, and I/O standard.

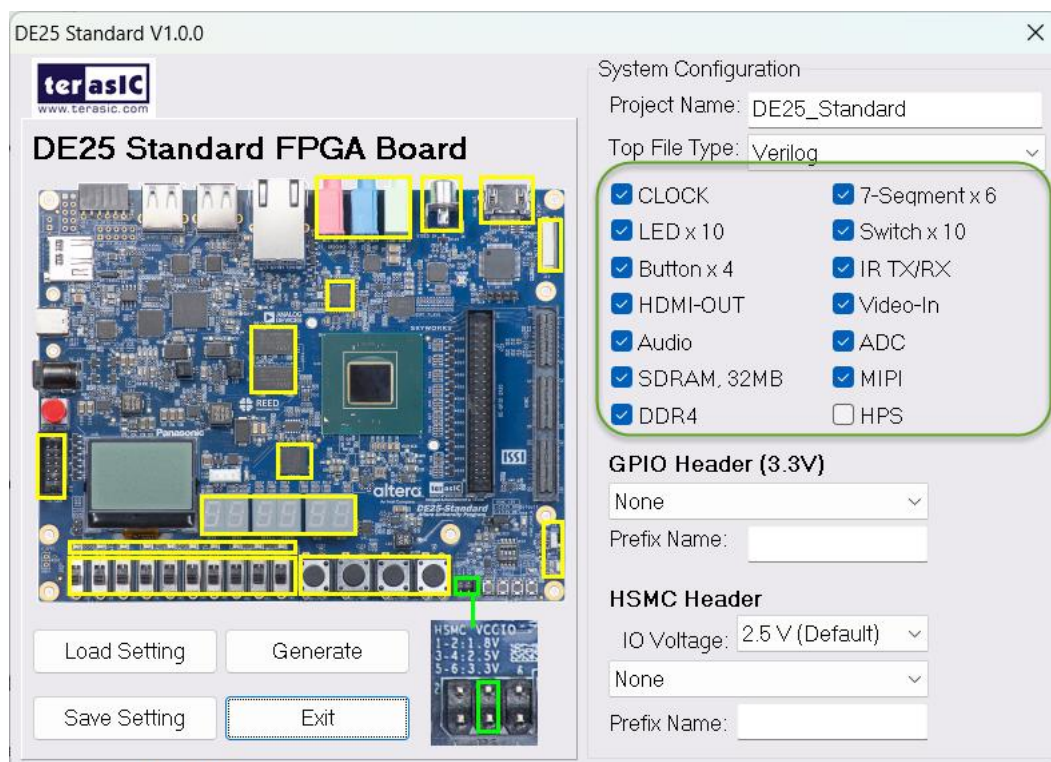


Figure 4-5 System configuration group

■ GPIO and HSMC Expansion

If users connect any Terasic GPIO-based or HSMC-based daughter cards to the GPIO connector or HSMC connector on DE25-Standard, the DE25-Standard System Builder can generate a project that include the corresponding module, as shown in [Figure 4-6](#). It will also generate the associated pin assignment automatically, including pin name, pin location, pin direction, and I/O standard.

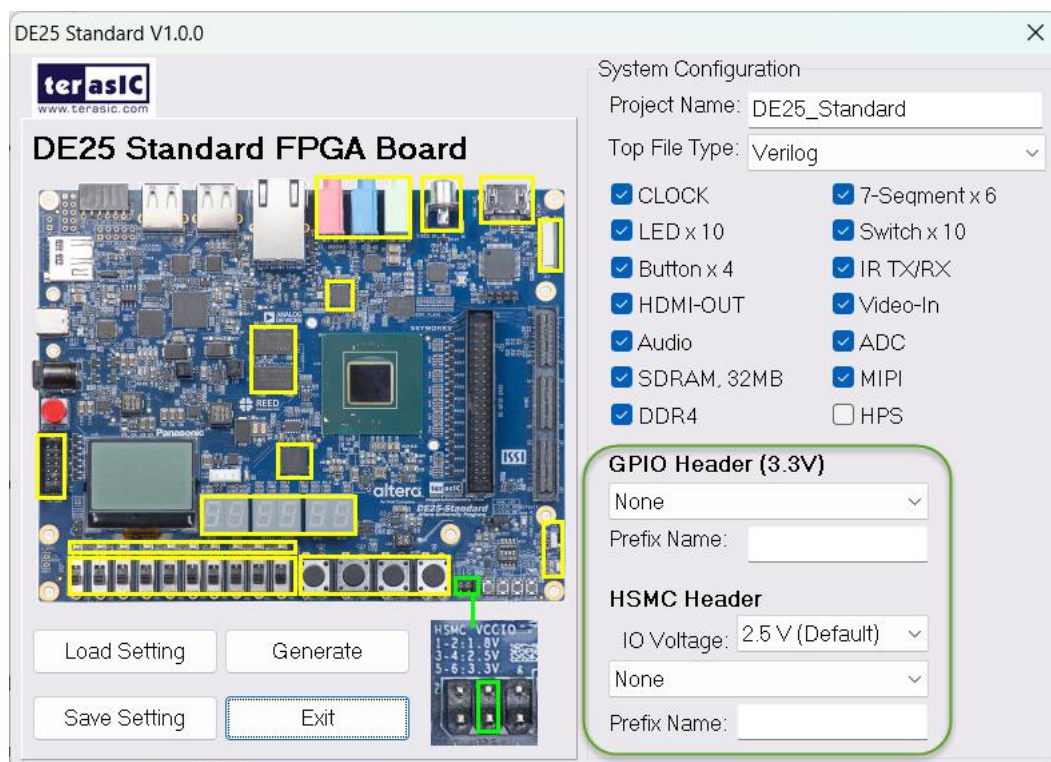


Figure 4-6 GPIO and HSMC expansion group

The “Prefix Name” is an optional feature that denotes the pin name of the daughter card assigned in your design. Users may leave this field blank.

■ Project Setting Management

The DE25-Standard System Builder also provides the option to load a setting or save users’ current board configuration in .cfg file, as shown in [Figure 4-7](#).

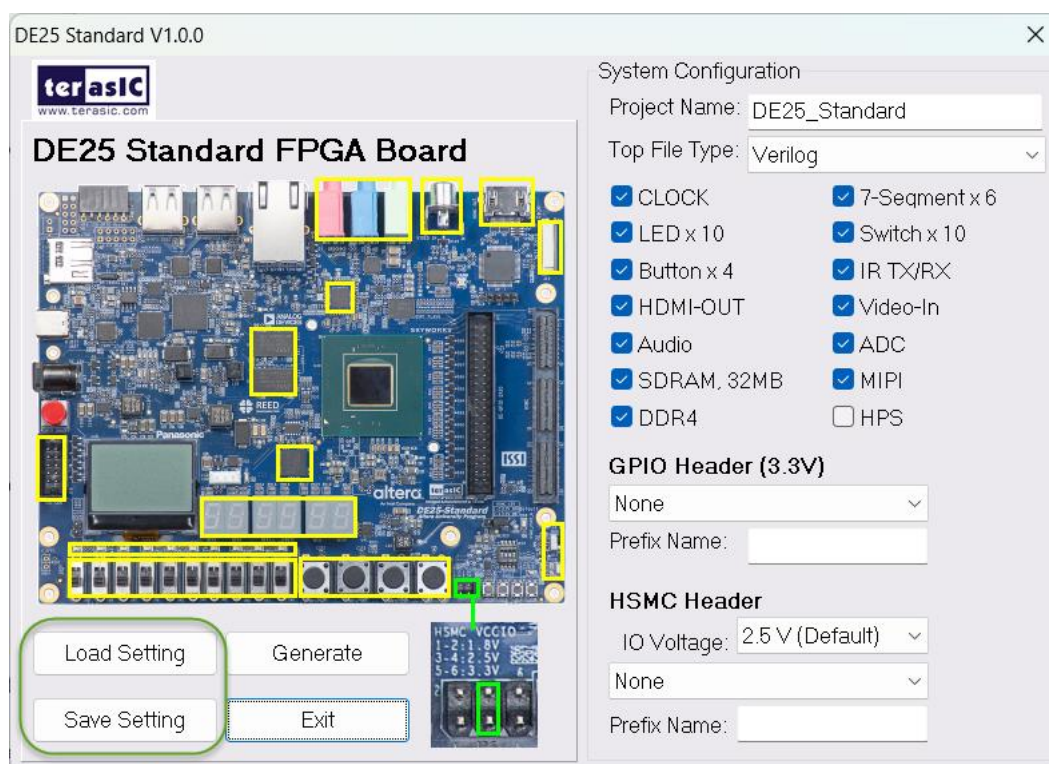


Figure 4-7 Project Settings

■ Project Generation

When users press the *Generate* button, the DE25-Standard System Builder will generate the corresponding Quartus II files and documents, as listed in [Table 4-1](#):

Table 4-1 Files generated by the DE25-Standard System Builder

No.	Filename	Description
1	<Project name>.v or .vhd	Top level Verilog or VHDL HDL file for Quartus II
2	<Project name>.qpf	Quartus II Project File
3	<Project name>.qsf	Quartus II Setting File
4	<Project name>.sdc	Synopsis Design Constraints file for Quartus II
5	<Project name>.htm	Pin Assignment Document

Users can add custom logic into the project in Quartus II and compile the project to generate the SRAM Object File (.sof).

5.1 Revision History

Version	Change Log
V1.0	Initial version
V1.1	Modify Table 3-11, Table 3-13, Table 3-14, Figure 3-19 and Table 3-10 for revB to revC pin assignment change
V1.2	Modify section 1.1 power adapter
V1.3	<ul style="list-style-type: none">• Modify Figure 3-17 for rev.D version. I²C address of the audio chip changed from 0x35 to 0x36.• Change FPGA to A5ED013BB32AE4SCS• Add chapter 4 system builder
V1.4	Add section 3.9.9 RTC
V1.5	Remove MAX10 reset function and modify clock circuit for revB to RevC

5.2 Copyright Statement

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