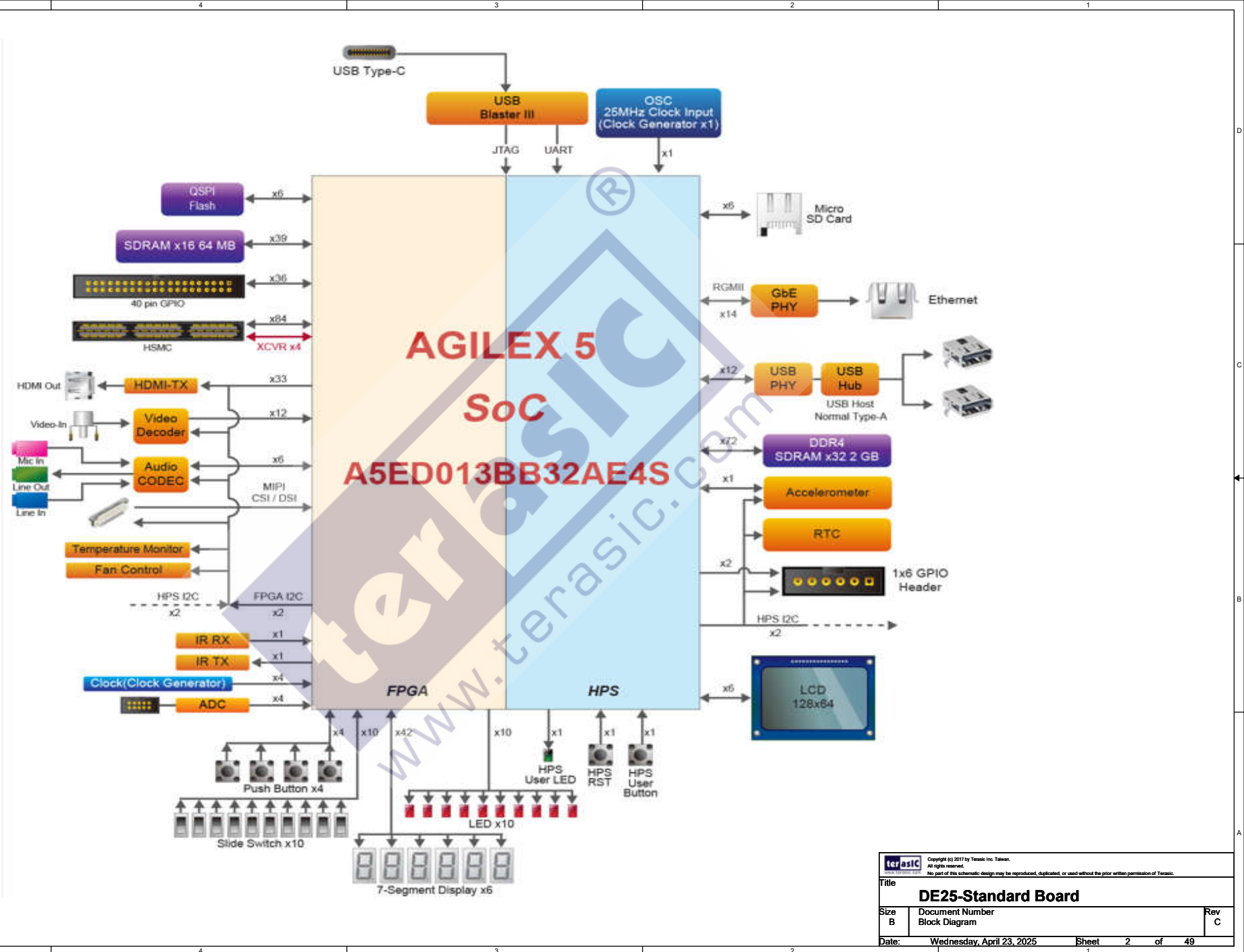
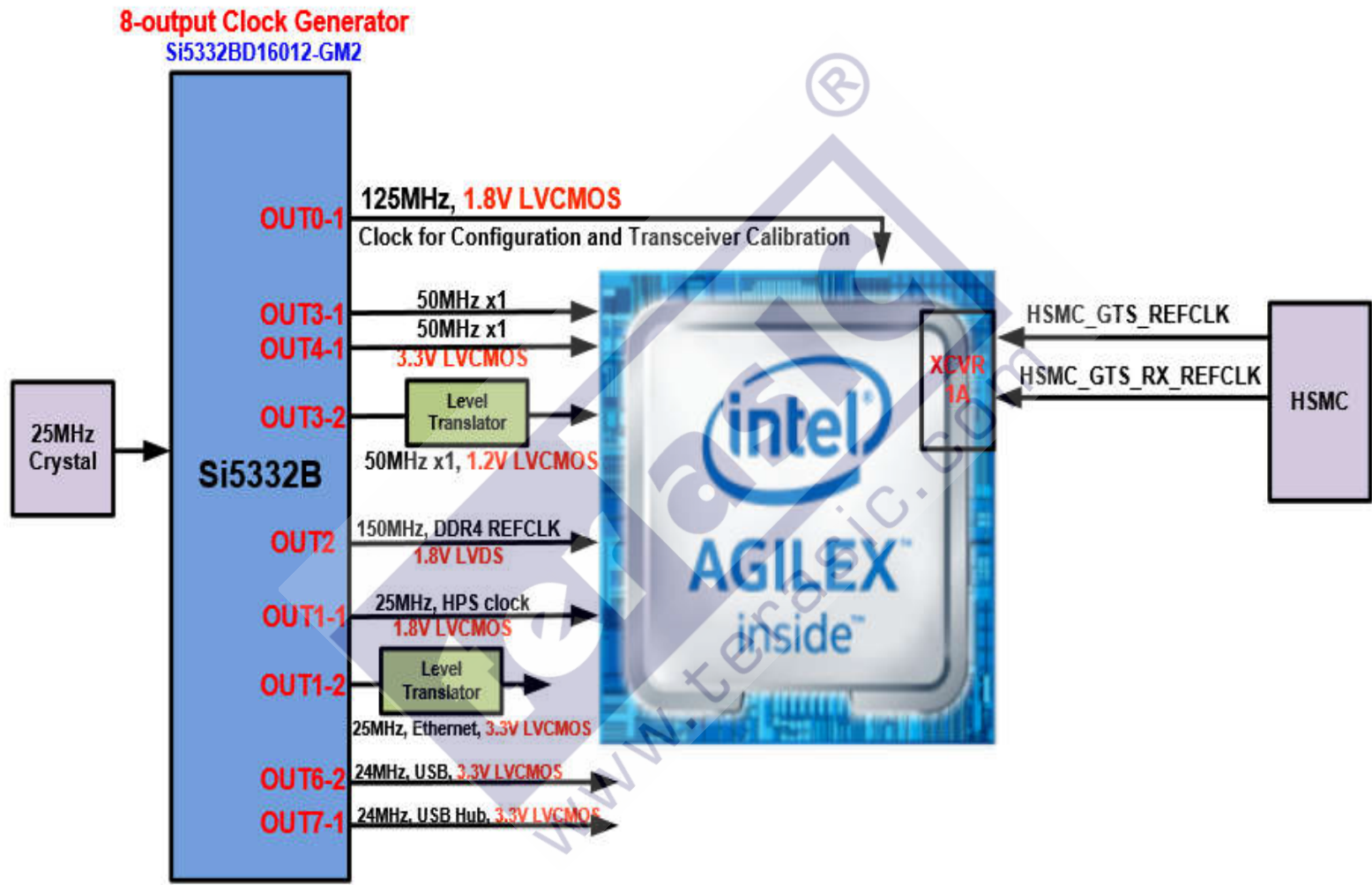


Block Diagram



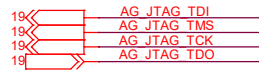
Clock Tree



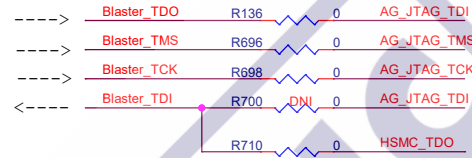
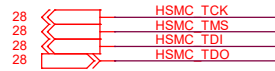
USB Blaster III



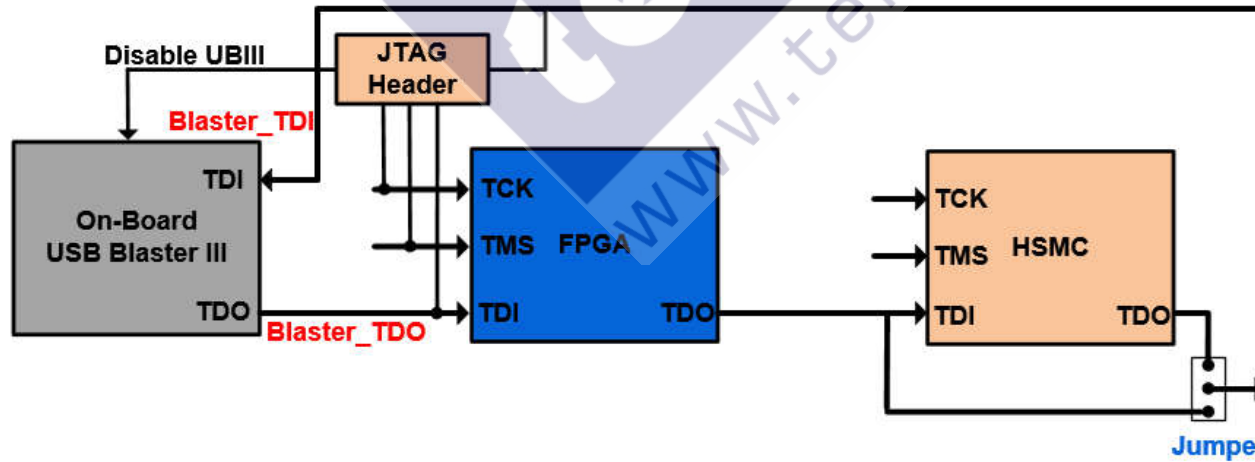
FPGA JTAG INTERFACE



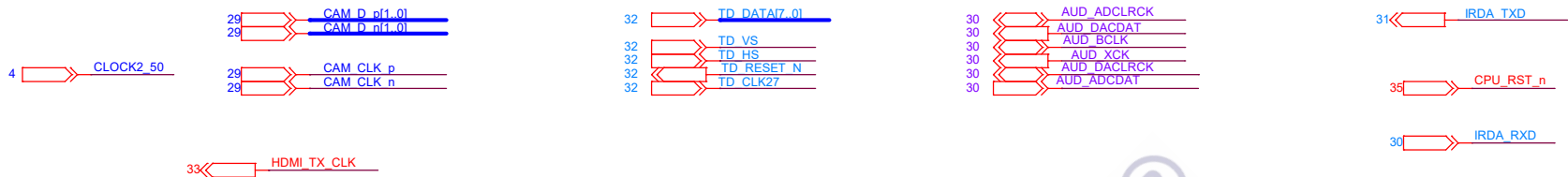
HSMC JTAG INTERFACE



JTAG Chain



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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	JTAG Chain	C
Date:	Tuesday, April 22, 2025	Sheet 6 of 49



U30C

VCCIO = 1.2V

HDMI_TX_CLK

SW7

HEX56

LED6

LED5

LED4

LED3

LED2

LED1

LED0

KEY3

KEY2

KEY1

KEY0

SW9

SW8

LED9

SW6

CAM_CLK_n

CAM_CLK_p

CAM_D_n1

CAM_D_p1

CAM_D_n0

CAM_D_p0

SW5

SW4

SW3

SW2

SW1

SW0

HEX52

LED7

HEX55

CAM_RZQ1

HEX53

CLOCK2_50

TD_DATA0

TD_CLK27

TD_DATA1

TD_DATA2

TD_DATA3

TD_DATA4

TD_DATA5

TD_DATA6

TD_DATA7

TD_RESET_N

TD_HS

TD_VS

CH59

CF59

CH62

CF62

CH62

CF62

CH62

CF69

CH69

CA71

CC71

CH71

CF71

CA59

BW59

BR59

BU59

BR62

BU62

CA69

BW69

BU71

BR71

BU69

BR69

BK59

BM59

BH59

BH62

BP62

BM62

BK69

BM69

BH71

BH69

BP71

BM71

BF72

BF75

BE75

BE79

BF83

BE83

BE86

BF86

BF90

BF93

BE93

BE96

IOB, DIFF, IO_2A_T1N, DQ0

IOB, DIFF, IO_2A_T1P, DQ0

IOB, DIFF, IO_2A_T2N, DQ0

IOB, DIFF, IO_2A_T2P, DQ0

IOB, DIFF, IO_2A_T3N, DQ0

IOB, DIFF, IO_2A_T3P, DQ0

IOB, DIFF, IO_2A_T4N, DQ0

IOB, DIFF, IO_2A_T4P, DQ0

IOB, CDR, DIFF, IO_2A_T5N, DQ0

IOB, CDR, DIFF, IO_2A_T5P, DQ0

IOB, DIFF, IO_2A_T6N, DQ0

IOB, DIFF, IO_2A_T6P, DQ0

IOB, DIFF, IO_2A_T7N, DQ0

IOB, DIFF, IO_2A_T7P, DQ0

IOB, DIFF, IO_2A_T8N, DQ0

IOB, DIFF, IO_2A_T8P, DQ0

IOB, DIFF, IO_2A_T9N, DQ0

IOB, DIFF, IO_2A_T9P, DQ0

IOB, DIFF, IO_2A_T10N, DQ0

IOB, DIFF, IO_2A_T10P, DQ0

IOB, CDR, DIFF, IO_2A_T11N, DQ0

IOB, CDR, DIFF, IO_2A_T11P, DQ0

IOB, DIFF, IO_2A_T12N, DQ0

IOB, DIFF, IO_2A_T12P, DQ0

IOB, DIFF, IO_2A_T13N, DQ0

IOB, DIFF, IO_2A_T13P, DQ0

IOB, DIFF, IO_2A_T14N, DQ0

IOB, DIFF, IO_2A_T14P, DQ0

IOB, DIFF, IO_2A_T15N, DQ0

IOB, DIFF, IO_2A_T15P, DQ0

IOB, PLL_2A_T_CLKOUT1N, DIFF, IO_2A_T16N, DQ0

IOB, PLL_2A_T_CLKOUT1P, DIFF, IO_2A_T16P, DQ0

IOB, CDR, DIFF, IO_2A_T17N, DQ0

IOB, RZQ, T_2A, CDR, DIFF, IO_2A_T17P, DQ0

IOB, CLK, T_2A_1N, DIFF, IO_2A_T18N, DQ0

IOB, CLK, T_2A_1P, DIFF, IO_2A_T18P, DQ0

IOB, CLK, T_2A_0N, DIFF, IO_2A_T19N, DQ0

IOB, CLK, T_2A_0P, DIFF, IO_2A_T19P, DQ0

IOB, DIFF, IO_2A_T20N, DQ0

IOB, DIFF, IO_2A_T20P, DQ0

IOB, PLL_2A_T_CLKOUT0N, DIFF, IO_2A_T21N, DQ0

IOB, PLL_2A_T_CLKOUT0P, DIFF, IO_2A_T21P, DQ0

IOB, DIFF, IO_2A_T22N, DQ0

IOB, DIFF, IO_2A_T22P, DQ0

IOB, CDR, DIFF, IO_2A_T23N, DQ0

IOB, CDR, DIFF, IO_2A_T23P, DQ0

IOB, DIFF, IO_2A_T24N, DQ0

IOB, DIFF, IO_2A_T24P, DQ0

BANK 2AT

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

BANK 2AB

I/O Lane 3

I/O Lane 2

I/O Lane 1

I/O Lane 0

IOB, CDR, DIFF, IO_2A_B1N, DQ4

IOB, CDR, DIFF, IO_2A_B1P, DQ4

IOB, DIFF, IO_2A_B2N, DQ4

IOB, DIFF, IO_2A_B2P, DQ4

IOB, DIFF, IO_2A_B3N, DQ4

IOB, DIFF, IO_2A_B3P, DQ4

IOB, PLL_2A_B_CLKOUT1N, DIFF, IO_2A_B4N, DQ4

IOB, PLL_2A_B_CLKOUT1P, DIFF, IO_2A_B4P, DQ4

IOB, CDR, DIFF, IO_2A_B5N, DQ4

IOB, RZQ, B_2A, CDR, DIFF, IO_2A_B5P, DQ4

IOB, CLK, B_2A_1N, DIFF, IO_2A_B6N, DQ4

IOB, CLK, B_2A_1P, DIFF, IO_2A_B6P, DQ4

IOB, CLK, B_2A_0N, CDR, DIFF, IO_2A_B7P, DQ5

IOB, CLK, B_2A_0P, CDR, DIFF, IO_2A_B7P, DQ5

IOB, DIFF, IO_2A_B8N, DQ5

IOB, DIFF, IO_2A_B8P, DQ5

IOB, PLL_2A_B_CLKOUT0N, DIFF, IO_2A_B9N, DQ5

IOB, PLL_2A_B_CLKOUT0P, DIFF, IO_2A_B9P, DQ5

IOB, DIFF, IO_2A_B10N, DQ5

IOB, DIFF, IO_2A_B10P, DQ5

IOB, CDR, DIFF, IO_2A_B11N, DQ5

IOB, CDR, DIFF, IO_2A_B11P, DQ5

IOB, DIFF, IO_2A_B12N, DQ5

IOB, DIFF, IO_2A_B12P, DQ5

IOB, CDR, DIFF, IO_2A_B13N, DQ6

IOB, CDR, DIFF, IO_2A_B13P, DQ6

IOB, DIFF, IO_2A_B14N, DQ6

IOB, DIFF, IO_2A_B14P, DQ6

IOB, DIFF, IO_2A_B15N, DQ6

IOB, DIFF, IO_2A_B15P, DQ6

IOB, DIFF, IO_2A_B16N, DQ6

IOB, DIFF, IO_2A_B16P, DQ6

IOB, CDR, DIFF, IO_2A_B17N, DQ6

IOB, CDR, DIFF, IO_2A_B17P, DQ6

IOB, DIFF, IO_2A_B18N, DQ6

IOB, DIFF, IO_2A_B18P, DQ6

IOB, CDR, DIFF, IO_2A_B19N, DQ7

IOB, CDR, DIFF, IO_2A_B19P, DQ7

IOB, DIFF, IO_2A_B20N, DQ7

IOB, DIFF, IO_2A_B20P, DQ7

IOB, DIFF, IO_2A_B21N, DQ7

IOB, DIFF, IO_2A_B21P, DQ7

IOB, DIFF, IO_2A_B22N, DQ7

IOB, DIFF, IO_2A_B22P, DQ7

IOB, CDR, DIFF, IO_2A_B23N, DQ7

IOB, CDR, DIFF, IO_2A_B23P, DQ7

IOB, DIFF, IO_2A_B24N, DQ7

IOB, DIFF, IO_2A_B24P, DQ7

BK78

BM78

BH78

BH81

BP81

BM81

BM89

BK89

BH89

BM92

BP92

CA78

BW78

BU78

BR78

BU81

BR81

CA89

BW89

BU89

BR89

CF78

CH78

CC81

CA81

CH81

CF81

CF89

CH89

CH92

CF92

CA92

CC92

CL76

CK76

CL82

CK80

CL85

CK85

CK88

CL88

CL97

CK97

CK94

CL91

IRDA_TXD

CPU_RST_n

LED1

IRDA_RXD

HEX00

HEX01

HEX02

HEX03

HEX04

HEX05

HEX06

HEX10

HEX11

HEX12

HEX13

HEX14

HEX15

HEX16

HEX20

HEX21

HEX22

HEX23

HEX24

HEX25

HEX26

HEX30

HEX31

HEX32

HEX33

HEX34

HEX35

HEX36

HEX40

HEX41

HEX42

HEX43

HEX44

HEX45

HEX46

HEX50

HEX51


AUD_ADCLCK

AUD_DACDAT

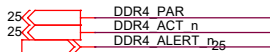
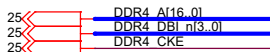
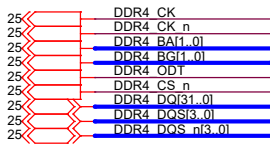
AUD_BCLK



A5ED013BB32AE4S

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Title			
DE25-Standard Board			
Size	Document Number		Rev
B	FPGA NC (2B)		C
Date:	Tuesday, April 22, 2025		Sheet 8 of 49

DDR4



RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14

DDR4_DQ25	D84
DDR4_DQ29	F84
DDR4_DQ31	M87
DDR4_DQ27	K87
DDR4_DBI_n3	F87
DDR4_DQS_n3	H87
DDR4_DQS3	D95
DDR4_DQ26	F95
DDR4_DQ24	M98
DDR4_DQ28	F98
DDR4_DQ30	H98
DDR4_DQ23	P84
DDR4_DQ22	T84
DDR4_DQ19	M84
DDR4_DQ17	K84
DDR4_DBI_n2	T87
DDR4_DQS_n2	V87
DDR4_DQS2	K95
DDR4_DQ16	T95
DDR4_DQ18	P95
DDR4_DQ20	T98
DDR4_DQ21	V98
DDR4_DQ15	Y84
DDR4_DQ13	Y87
DDR4_DQ11	Y95
DDR4_DQ9	Y98
DDR4_DBI_n1	AC86
DDR4_DQS_n1	AC90
DDR4_DQS1	AC93
DDR4_DQ12	AC96
DDR4_DQ14	AC100
DDR4_DQ10	AG104
DDR4_DQ8	AG100

U30E

BANK 3AT

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

IOB, DIFF_IO_3A_T1N, DQ16	
IOB, DIFF_IO_3A_T1P, DQ16	
IOB, DIFF_IO_3A_T2N, DQ16	
IOB, DIFF_IO_3A_T2P, DQ16	
IOB, DIFF_IO_3A_T3N, DQ16	
IOB, DIFF_IO_3A_T3P, DQ16, AVST_READY	
IOB, DIFF_IO_3A_T4N, DQSN16	
IOB, DIFF_IO_3A_T4P, DQS16	
IOB, CDR, DIFF_IO_3A_T5N, DQ16	
IOB, CDR, DIFF_IO_3A_T5P, DQ16	
IOB, DIFF_IO_3A_T6N, DQ16	
IOB, DIFF_IO_3A_T6P, DQ16	
IOB, DIFF_IO_3A_T7N, DQ17, AVST_DATA10	
IOB, DIFF_IO_3A_T7P, DQ17, AVST_DATA9	
IOB, DIFF_IO_3A_T8N, DQ17, AVST_DATA8	
IOB, DIFF_IO_3A_T8P, DQ17, AVST_VALID	
IOB, DIFF_IO_3A_T9N, DQ17, AVST_DATA7	
IOB, DIFF_IO_3A_T9P, DQ17, AVST_DATA6	
IOB, DIFF_IO_3A_T10N, DQSN17, AVST_DATA5	
IOB, DIFF_IO_3A_T10P, DQS17, AVST_DATA4	
IOB, CDR, DIFF_IO_3A_T11N, DQ17, AVST_DATA3	
IOB, CDR, DIFF_IO_3A_T11P, DQ17, AVST_DATA2	
IOB, DIFF_IO_3A_T12N, DQ17, AVST_DATA1	
IOB, DIFF_IO_3A_T12P, DQ17, AVST_DATA0	
IOB, DIFF_IO_3A_T13N, DQ18	
IOB, DIFF_IO_3A_T13P, DQ18	
IOB, DIFF_IO_3A_T14N, DQ18	
IOB, DIFF_IO_3A_T14P, DQ18	
IOB, DIFF_IO_3A_T15N, DQ18	
IOB, DIFF_IO_3A_T15P, DQ18	
IOB, PLL_3A_T_CLKOUT1N, DIFF_IO_3A_T16N, DQSN18	
IOB, PLL_3A_T_CLKOUT1P, PLL_3A_T_CLKOUT1, PLL_3A_T_FB1, DIFF_IO_3A_T16P, DQS18	
IOB, CDR, DIFF_IO_3A_T17N, DQ18	
IOB, RZQ_T_3A, CDR, DIFF_IO_3A_T17P, DQ18	
IOB, CLK_T_3A_1N, DIFF_IO_3A_T18N, DQ18	
IOB, CLK_T_3A_1P, DIFF_IO_3A_T18P, DQ18	
IOB, CLK_T_3A_0N, DIFF_IO_3A_T19N, DQ19	
IOB, CLK_T_3A_0P, DIFF_IO_3A_T19P, DQ19	
IOB, DIFF_IO_3A_T20N, DQ19	
IOB, DIFF_IO_3A_T20P, DQ19	
IOB, PLL_3A_T_CLKOUT0N, DIFF_IO_3A_T21N, DQ19	
IOB, PLL_3A_T_CLKOUT0P, PLL_3A_T_CLKOUT0, PLL_3A_T_FB0, DIFF_IO_3A_T21P, DQ19	
IOB, DIFF_IO_3A_T22N, DQSN19, AVST_CLK	
IOB, DIFF_IO_3A_T22P, DQS19, AVST_DATA15	
IOB, CDR, DIFF_IO_3A_T23N, DQ19, AVST_DATA14	
IOB, CDR, DIFF_IO_3A_T23P, DQ19, AVST_DATA13	
IOB, DIFF_IO_3A_T24N, DQ19, AVST_DATA12	
IOB, DIFF_IO_3A_T24P, DQ19, AVST_DATA11	

VCCIO = 1.2V

BANK 3AB

I/O Lane 3

I/O Lane 2


I/O Lane 1

I/O Lane 0

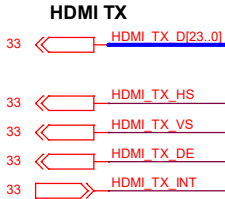
IOB, CDR, DIFF_IO_3A_B1N, DQ20	
IOB, CDR, DIFF_IO_3A_B1P, DQ20	
IOB, DIFF_IO_3A_B2N, DQ20	
IOB, DIFF_IO_3A_B2P, DQ20	
IOB, DIFF_IO_3A_B3N, DQ20	
IOB, DIFF_IO_3A_B3P, DQ20	
IOB, PLL_3A_B_CLKOUT1N, DIFF_IO_3A_B4N, DQSN20	
IOB, PLL_3A_B_CLKOUT1P, PLL_3A_B_CLKOUT1, PLL_3A_B_FB1, DIFF_IO_3A_B4P, DQS20	
IOB, CDR, DIFF_IO_3A_B5N, DQ20	
IOB, RZQ_B_3A, CDR, DIFF_IO_3A_B5P, DQ20	
IOB, CLK_B_3A_1N, DIFF_IO_3A_B6N, DQ20	
IOB, CLK_B_3A_1P, DIFF_IO_3A_B6P, DQ20	
IOB, DIFF_IO_3A_B7N, DQ21	
IOB, CLK_B_3A_0N, CDR, DIFF_IO_3A_B7P, DQ21	
IOB, CLK_B_3A_0P, CDR, DIFF_IO_3A_B7P, DQ21	
IOB, DIFF_IO_3A_B8N, DQ21	
IOB, DIFF_IO_3A_B8P, DQ21	
IOB, PLL_3A_B_CLKOUT0N, DIFF_IO_3A_B9N, DQ21	
IOB, PLL_3A_B_CLKOUT0P, PLL_3A_B_CLKOUT0, PLL_3A_B_FB0, DIFF_IO_3A_B9P, DQ21	
IOB, DIFF_IO_3A_B10N, DQSN21	
IOB, DIFF_IO_3A_B10P, DQS21	
IOB, CDR, DIFF_IO_3A_B11N, DQ21	
IOB, CDR, DIFF_IO_3A_B11P, DQ21	
IOB, DIFF_IO_3A_B12N, DQ21	
IOB, DIFF_IO_3A_B12P, DQ21	
IOB, CDR, DIFF_IO_3A_B13N, DQ22	
IOB, CDR, DIFF_IO_3A_B13P, DQ22	
IOB, DIFF_IO_3A_B14N, DQ22	
IOB, DIFF_IO_3A_B14P, DQ22	
IOB, DIFF_IO_3A_B15N, DQ22	
IOB, DIFF_IO_3A_B15P, DQ22	
IOB, DIFF_IO_3A_B16N, DQSN22	
IOB, DIFF_IO_3A_B16P, DQS22	
IOB, CDR, DIFF_IO_3A_B17N, DQ22	
IOB, CDR, DIFF_IO_3A_B17P, DQ22	
IOB, DIFF_IO_3A_B18N, DQ22	
IOB, DIFF_IO_3A_B18P, DQ22	
IOB, CDR, DIFF_IO_3A_B19N, DQ23	
IOB, CDR, DIFF_IO_3A_B19P, DQ23	
IOB, DIFF_IO_3A_B20N, DQ23	
IOB, DIFF_IO_3A_B20P, DQ23	
IOB, DIFF_IO_3A_B21N, DQ23	
IOB, DIFF_IO_3A_B21P, DQ23	
IOB, DIFF_IO_3A_B22N, DQSN23	
IOB, DIFF_IO_3A_B22P, DQS23	
IOB, CDR, DIFF_IO_3A_B23N, DQ23	
IOB, CDR, DIFF_IO_3A_B23P, DQ23	
IOB, DIFF_IO_3A_B24N, DQ23	
IOB, DIFF_IO_3A_B24P, DQ23	

AB105	DDR4_BG0
Y105	DDR4_BA1
AB108	DDR4_BA0
Y108	DDR4_ALERT_n
AK104	DDR4_A16
AK107	DDR4_A15
AB114	DDR4_A14
Y114	DDR4_A13
AG111	DDR4_A12
AK111	RZQ_B_3A_R418
Y117	DDR4_REFCLK_n
AB117	DDR4_REFCLK_p
K105	DDR4_A11
M105	DDR4_A10
P105	DDR4_A9
T105	DDR4_A8
T108	DDR4_A7
V108	DDR4_A6
K114	DDR4_A5
M114	DDR4_A4
T117	DDR4_A3
P117	DDR4_A2
P114	DDR4_A1
T114	DDR4_A0
K108	DDR4_PAR
M108	
F108	DDR4_CK_n
H108	DDR4_CK
D105	
F105	DDR4_CKE
D114	
F114	DDR4_ODT
M117	DDR4_ACT_n
K117	DDR4_CS_n
H117	DDR4_RESET_n
F117	DDR4_BG1
A113	DDR4_DQ7
B113	DDR4_DQ5
A116	DDR4_DQ1
B116	DDR4_DQ3
A122	
B119	DDR4_DBI_n0
A125	DDR4_DQS_n0
B122	DDR4_DQS0
A130	DDR4_DQ6
B130	DDR4_DQ4
A128	DDR4_DQ2
B128	DDR4_DQ0

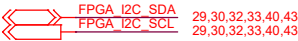


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Title DE25-Standard Board		
Size B	Document Number FPGA Bank 3A	Rev C
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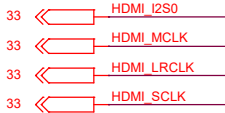




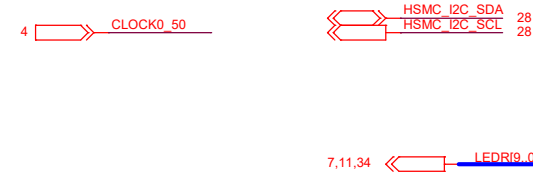
FPGA I2C Interface



HDMI Audio Interface



HSMC I2C Interface



U30G

VCCIO = 3.3V

HDMI TX D0	CD134
HDMI TX D1	CD135
HDMI TX D2	CG134
HDMI TX D3	CG135
HDMI TX D4	CH132
HDMI TX D5	CF132
HDMI TX D6	CF128
HDMI TX D7	CK134
CLOCK0_50	CH128
HDMI TX D8	CL125
HDMI TX D9	CF121
HDMI TX D10	CF118
HDMI TX D11	BU118
HDMI TX D12	BR118
HDMI TX D13	CA118
HDMI TX D14	BW118
HDMI TX D15	CL128
HDMI TX D16	CL130
HDMI TX D17	CK125
HDMI TX D18	CK128

HVIO_5A_1, SYSPLLREFCLK_L1A_0, TXCLK1, DATA_CTRL1
HVIO_5A_2, SYSPLLREFCLK_L1A_1, TXCLK2, DATA_CTRL2
HVIO_5A_3, SYSPLLREFCLK_L1B_0, TXCLK3, DATA_CTRL3
HVIO_5A_4, SYSPLLREFCLK_L1B_1, TXCLK4, DATA_CTRL4
HVIO_5A_5, PIN_PERST_N_CVP_L1A_0, TXCLK5, DATA_CTRL5
HVIO_5A_6, PIN_PERST_N_CVP_L1B_0, TXCLK6, DATA_CTRL6
HVIO_5A_7, PIN_PERST_N_CVP_L1C_0, TXCLK7, DATA_CTRL7
HVIO_5A_8, TXCLK8, DATA_CTRL8
HVIO_5A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_5A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_5A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_5A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_5A_13, TXCLK13, DATA_CTRL13
HVIO_5A_14, TXCLK14, DATA_CTRL14
HVIO_5A_15, TXCLK15, DATA_CTRL15
HVIO_5A_16, TXCLK16, DATA_CTRL16
HVIO_5A_17, TXCLK17, DATA_CTRL17
HVIO_5A_18, TXCLK18, DATA_CTRL18
HVIO_5A_19, SYSPLLREFCLK_L1C_0, TXCLK19, DATA_CTRL19
HVIO_5A_20, TXCLK20, DATA_CTRL20

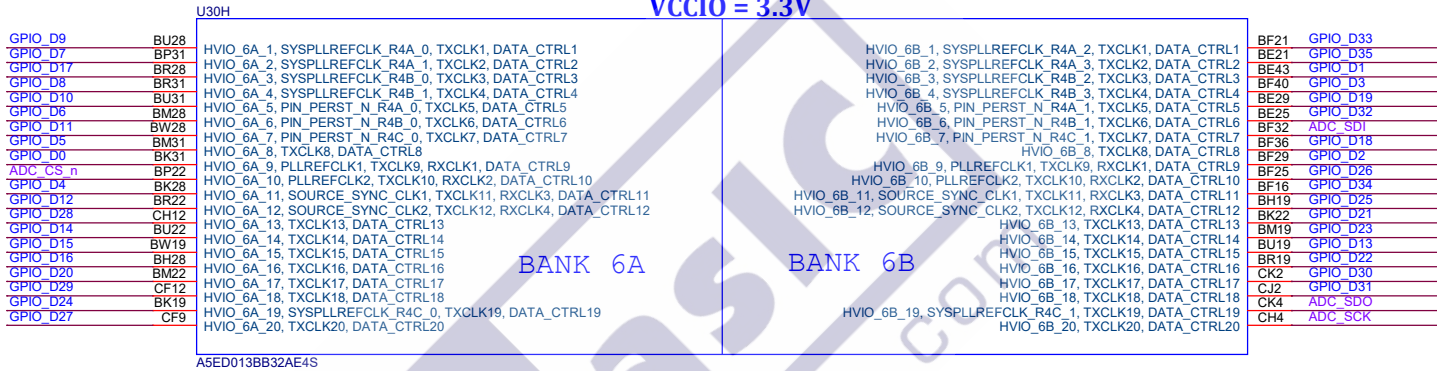
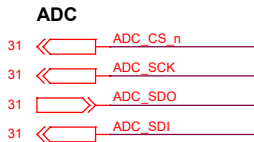
BANK 5A

HVIO_5B_1, SYSPLLREFCLK_L1A_2, TXCLK1, DATA_CTRL1
HVIO_5B_2, SYSPLLREFCLK_L1A_3, TXCLK2, DATA_CTRL2
HVIO_5B_3, SYSPLLREFCLK_L1B_2, TXCLK3, DATA_CTRL3
HVIO_5B_4, SYSPLLREFCLK_L1B_3, TXCLK4, DATA_CTRL4
HVIO_5B_5, PIN_PERST_N_CVP_L1A_1, TXCLK5, DATA_CTRL5
HVIO_5B_6, PIN_PERST_N_CVP_L1B_1, TXCLK6, DATA_CTRL6
HVIO_5B_7, PIN_PERST_N_CVP_L1C_1, TXCLK7, DATA_CTRL7
HVIO_5B_8, TXCLK8, DATA_CTRL8
HVIO_5B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_5B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_5B_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_5B_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_5B_13, TXCLK13, DATA_CTRL13
HVIO_5B_14, TXCLK14, DATA_CTRL14
HVIO_5B_15, TXCLK15, DATA_CTRL15
HVIO_5B_16, TXCLK16, DATA_CTRL16
HVIO_5B_17, TXCLK17, DATA_CTRL17
HVIO_5B_18, TXCLK18, DATA_CTRL18
HVIO_5B_19, SYSPLLREFCLK_L1C_1, TXCLK19, DATA_CTRL19
HVIO_5B_20, TXCLK20, DATA_CTRL20

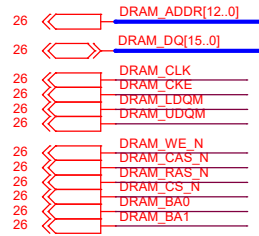
BANK 5B

BF111	HDMI TX D19
BH109	HDMI TX D20
BE115	HDMI TX D21
BF115	HDMI TX D22
BF107	HSMC B5B D0_E (Reset input in PCIE)
BU109	HDMI TX D23
BF104	HSMC B5B D1_E
BR109	HDMI TX_HS
BE107	HDMI TX_VS
BK109	HDMI TX_DE
BE111	HDMI TX_INT
BM109	HSMC I2C_SDA
BR112	HSMC I2C_SCL
BK118	HDMI_I2S0
BM118	HDMI_MCLK
BP112	HDMI_LRCLK
BM112	HDMI_SCLK
BK112	CAM_GPIO
BH118	FPGA I2C_SDA
BF120	FPGA I2C_SCL

A5ED013BB32AE4S



SDRAM



U30I

VCCIO = 1.8V

DRAM_ADDR0	F27
DRAM_ADDR1	F24
DRAM_ADDR2	H27
DRAM_ADDR3	D24
DRAM_ADDR4	H18
DRAM_ADDR5	D15
DRAM_ADDR6	F18
DRAM_ADDR7	F15
CLOCK1_50	D8
DRAM_ADDR8	K8
DRAM_ADDR9	F8
DRAM_CS_N	H8
DRAM_ADDR10	C2
DRAM_ADDR12	D4
DRAM_BA1	F4
DRAM_LDQM	K4
DRAM_UDQM	G2
DRAM_WE_N	J2
DRAM_CAS_N	J1
DRAM_RAS_N	G1

HVIO_6C_1, TXCLK1, DATA_CTRL1
HVIO_6C_2, TXCLK2, DATA_CTRL2
HVIO_6C_3, TXCLK3, DATA_CTRL3
HVIO_6C_4, TXCLK4, DATA_CTRL4
HVIO_6C_5, TXCLK5, DATA_CTRL5
HVIO_6C_6, TXCLK6, DATA_CTRL6
HVIO_6C_7, TXCLK7, DATA_CTRL7
HVIO_6C_8, TXCLK8, DATA_CTRL8
HVIO_6C_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6C_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6C_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6C_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6C_13, TXCLK13, DATA_CTRL13
HVIO_6C_14, TXCLK14, DATA_CTRL14
HVIO_6C_15, TXCLK15, DATA_CTRL15
HVIO_6C_16, TXCLK16, DATA_CTRL16
HVIO_6C_17, TXCLK17, DATA_CTRL17
HVIO_6C_18, TXCLK18, DATA_CTRL18
HVIO_6C_19, TXCLK19, DATA_CTRL19
HVIO_6C_20, TXCLK20, DATA_CTRL20


BANK 6C

BANK 6D

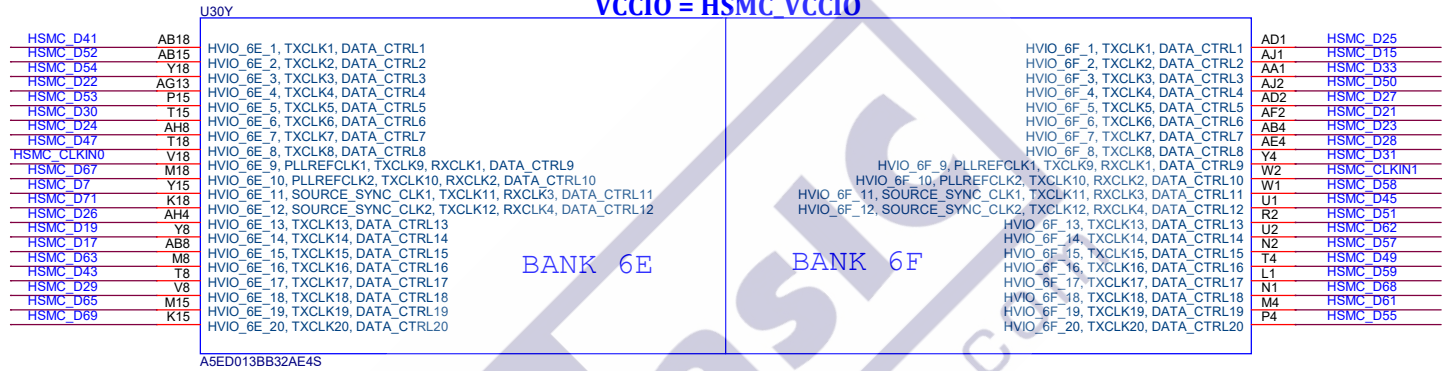
HVIO_6D_1, TXCLK1, DATA_CTRL1
HVIO_6D_2, TXCLK2, DATA_CTRL2
HVIO_6D_3, TXCLK3, DATA_CTRL3
HVIO_6D_4, TXCLK4, DATA_CTRL4
HVIO_6D_5, TXCLK5, DATA_CTRL5
HVIO_6D_6, TXCLK6, DATA_CTRL6
HVIO_6D_7, TXCLK7, DATA_CTRL7
HVIO_6D_8, TXCLK8, DATA_CTRL8
HVIO_6D_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6D_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6D_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6D_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6D_13, TXCLK13, DATA_CTRL13
HVIO_6D_14, TXCLK14, DATA_CTRL14
HVIO_6D_15, TXCLK15, DATA_CTRL15
HVIO_6D_16, TXCLK16, DATA_CTRL16
HVIO_6D_17, TXCLK17, DATA_CTRL17
HVIO_6D_18, TXCLK18, DATA_CTRL18
HVIO_6D_19, TXCLK19, DATA_CTRL19
HVIO_6D_20, TXCLK20, DATA_CTRL20

A8	DRAM_DQ5
B4	DRAM_DQ7
A11	DRAM_DQ1
B11	DRAM_DQ3
B14	DRAM_DQ2
A14	DRAM_DQ0
A20	DRAM_DQ4
A17	DRAM_ADDR11
A23	DRAM_DQ6
B20	DRAM_DQ8
B23	DRAM_DQ9
B26	DRAM_DQ10
B30	DRAM_DQ11
A30	DRAM_DQ13
A35	DRAM_DQ14
A33	DRAM_DQ15
A39	DRAM_DQ12
B35	DRAM_CKE
D34	DRAM_BA0
B39	DRAM_CLK

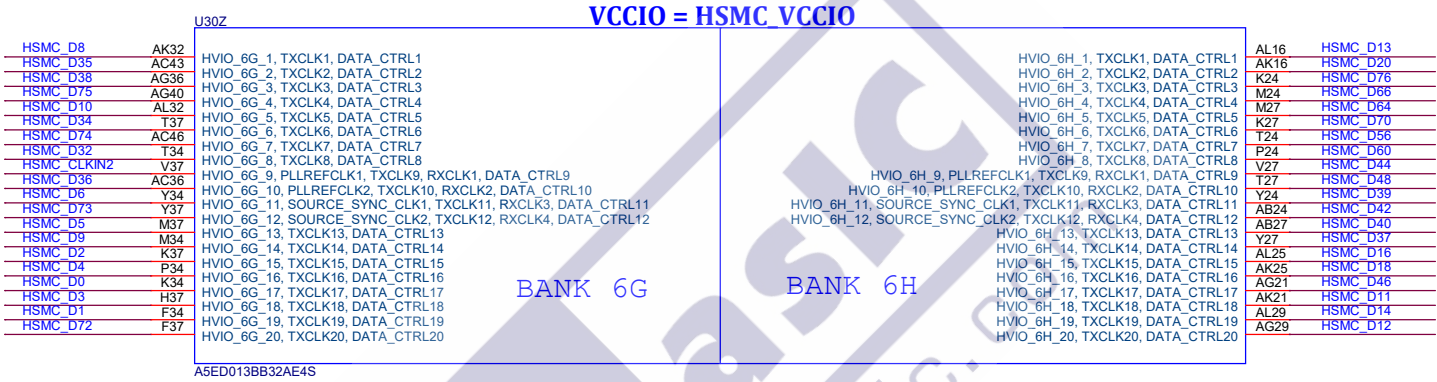
A5ED013BB32AE4S

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Title DE25-Standard Board		
Size B	Document Number FPGA Bank 6C - 6D	Rev C
Date:	Tuesday, April 22, 2025	Sheet 13 of 49

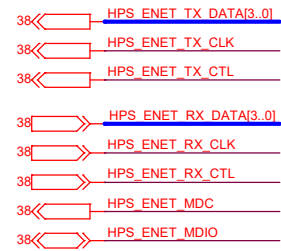
15,28 << HSMC_D[76..0]
15,28 << HSMC_CLKIN[2..0]



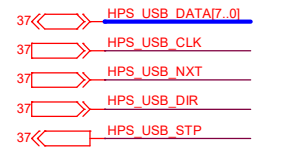
14,28 << HSMC_D[76..0]
14,28 << HSMC_CLKIN[2..0]



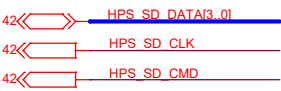
Ethernet PHY Interface (RGMII)



UBS PHY Interface (ULPI)



SD Card



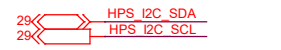
HPS 25MHz Clock



HPS GPIO



HPS I2C Interface



HPS User Button



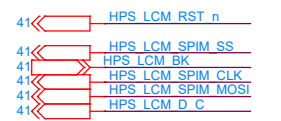
HPS User LED



UART Interface



HPS LCD



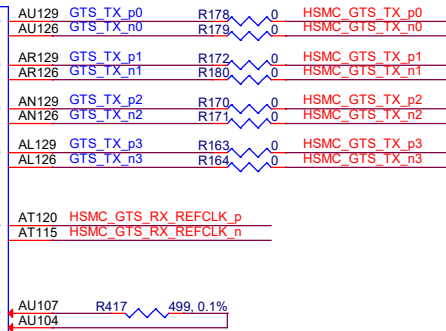
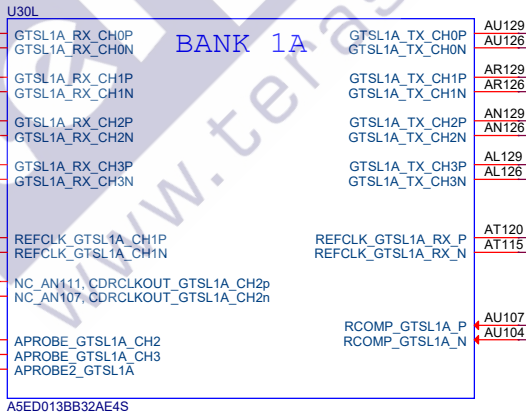
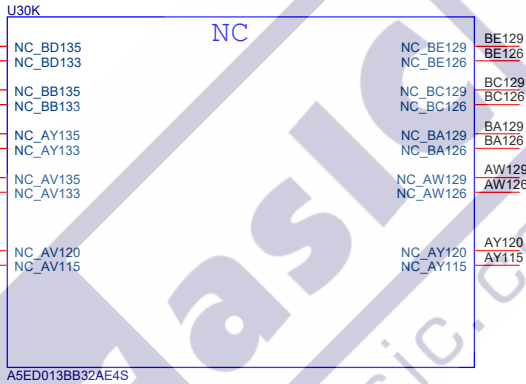
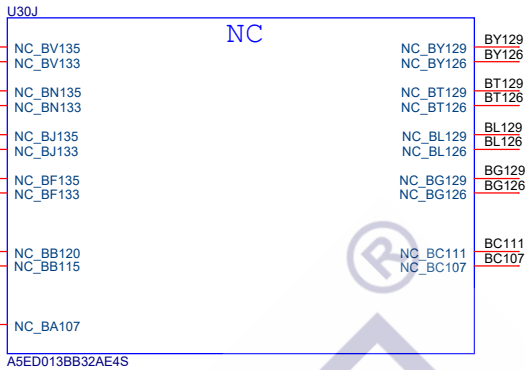
HPS_USB_CLK	W135
HPS_USB_STP	U135
HPS_USB_DIR	W134
HPS_USB_DATA0	AK115
HPS_USB_DATA1	U134
HPS_USB_NXT	AL120
HPS_USB_DATA2	R134
HPS_USB_DATA3	AG115
HPS_USB_DATA4	N135
HPS_USB_DATA5	AK120
HPS_USB_DATA6	N134
HPS_USB_DATA7	T132
HPS_ENET_TX_CTL	P132
HPS_ENET_TX_CLK	L135
HPS_ENET_RX_CLK	J135
HPS_ENET_RX_CTL	AD135
HPS_ENET_TX_DATA0	M132
HPS_ENET_TX_DATA1	AD134
HPS_ENET_RX_DATA0	K132
HPS_ENET_RX_DATA1	AG129
HPS_ENET_TX_DATA2	J134
HPS_ENET_TX_DATA3	AG120
HPS_ENET_RX_DATA2	G134
HPS_ENET_RX_DATA3	G135

HPS_SD_DATA0	E135
HPS_SD_DATA1	F132
HPS_SD_CLK	D132
HPS_CLK_25	AG123
HPS_GSENSOR_INT	B134
HPS_SD_DATA2	AA135
HPS_SD_DATA3	V127
HPS_SD_CMD	AB132
HPS_GPIO0	T127
HPS_GPIO1	T132
HPS_LCM_RST_n	T124
HPS_LCM_D_C	P124
HPS_I2C_SDA	M127
HPS_I2C_SCL	K127
HPS_UART_TX	M124
HPS_UART_RX	AB127
HPS_KEY	K124
HPS_LED	Y127
HPS_LCM_BK	H127
HPS_LCM_SPIM_SS	AB124
HPS_LCM_SPIM_CLK	F127
HPS_LCM_SPIM_MOSI	Y124
HPS_ENET_MDIO	F124
HPS_ENET_MDC	D124

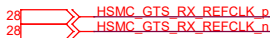
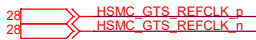
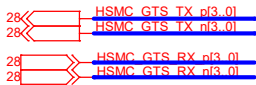
U30B	
HPS_IOA_1, GPIO0_I00, SPIM0_SS1_N, SPIS0_CLK, UART0_CTS_N, NAND_ADQ0, SDMMC_DATA0, USB0_CLK, EMAC0_PPS0, TRACE_D10	
HPS_IOA_2, GPIO0_I01, SPIM1_SS1_N, SPIS0_MOSI, UART0_RTS_N, NAND_ADQ1, SDMMC_DATA1, USB0_STP, EMAC0_PPSTRIG0, TRACE_D9	
HPS_IOA_3, GPIO0_I02, SPIS0_SS0_N, UART0_TX, I2C1_SDA, NAND_WE_N, SDMMC_CLK, USB0_DIR, EMAC1_PPS1, TRACE_D8	
HPS_IOA_4, GPIO0_I03, SPIS0_MISO, UART0_RX, I2C1_SCL, NAND_RE_N, USB0_DATA0, EMAC1_PPSTRIG1, TRACE_D7	
HPS_IOA_5, GPIO0_I04, SPIM0_CLK, UART1_CTS_N, I2C0_SDA, NAND_WP_N, SDMMC_WRITE_PROTECT, USB0_DATA1, EMAC2_PPS2, TRACE_D6	
HPS_IOA_6, GPIO0_I05, SPIM0_MOSI, UART1_RTS_N, I2C0_SCL, NAND_ADQ2, SDMMC_DATA2, USB0_NXT, EMAC2_PPSTRIG2, TRACE_D5	
HPS_IOA_7, GPIO0_I06, SPIM0_MISO, MDIO2_MDIO, UART1_TX, I2C_EMAC2_SDA, NAND_ADQ3, SDMMC_DATA3, USB0_DATA2, TRACE_D4	
HPS_IOA_8, GPIO0_I07, SPIM0_SS0_N, MDIO2_MDC, UART1_RX, I2C_EMAC2_SCL, NAND_CLE, SDMMC_CMD, USB0_DATA3, TRACE_D15	
HPS_IOA_9, GPIO0_I08, SPIM1_CLK, SPIS1_CLK, MDIO1_MDIO, I2C_EMAC1_SDA, NAND_ADQ4, SDMMC_DATA4, USB0_DATA4, I3C1_SCL, TRACE_D14	
HPS_IOA_10, GPIO0_I09, SPIM1_MOSI, SPIS1_MOSI, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ5, SDMMC_DATA5, USB0_DATA5, I3C1_SCL, TRACE_D13	
HPS_IOA_11, GPIO0_I010, SPIM1_MISO, SPIS1_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, USB0_DATA6, I3C0_SDA, TRACE_D12	
HPS_IOA_12, GPIO0_I011, SPIM1_SS0_N, SPIS1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, USB0_DATA7, I3C0_SCL, TRACE_D11	
HPS_IOA_13, GPIO0_I012, NAND_ALE, SDMMC_PU_PD_DATA2, USB1_CLK, EMAC0_TX_CLK, TRACE_D10	
HPS_IOA_14, GPIO0_I013, NAND_RB_N, SDMMC_BUS_PWR, USB1_STP, EMAC0_TX_CTL, TRACE_D9	
HPS_IOA_15, GPIO0_I014, NAND_CE_N, USB1_DIR, EMAC0_RX_CLK, TRACE_D8	
HPS_IOA_16, GPIO0_I015, NAND_DQS, SDMMC_DATA_STROBE, USB1_DATA0, EMAC0_RX_CTL, TRACE_D7	
HPS_IOA_17, GPIO0_I016, I3C1_SDA, NAND_ADQ8, USB1_DATA1, EMAC0_TXD0, TRACE_D6	
HPS_IOA_18, GPIO0_I017, I3C1_SCL, NAND_ADQ9, USB1_NXT, EMAC0_TXD1, TRACE_D5	
HPS_IOA_19, GPIO0_I018, I3C0_SDA, NAND_ADQ10, USB1_DATA2, EMAC0_RXD0, TRACE_D4	
HPS_IOA_20, GPIO0_I019, SPIM1_SS1_N, I3C0_SCL, NAND_ADQ11, USB1_DATA3, EMAC0_RXD1, TRACE_CLK	
HPS_IOA_21, GPIO0_I020, SPIM1_CLK, SPIS0_CLK, UART0_CTS_N, I2C1_SDA, NAND_ADQ12, USB1_DATA4, EMAC0_TXD2, TRACE_D0	
HPS_IOA_22, GPIO0_I021, SPIM1_MOSI, SPIS0_MOSI, UART0_RTS_N, I2C1_SCL, NAND_ADQ13, USB1_DATA5, EMAC0_TXD3, TRACE_D1	
HPS_IOA_23, GPIO0_I022, SPIM1_MISO, SPIS0_SS0_N, UART0_TX, I2C0_SDA, NAND_ADQ14, USB1_DATA6, EMAC0_RXD2, TRACE_D2	
HPS_IOA_24, GPIO0_I023, SPIM1_SS0_N, SPIS0_MISO, UART0_RX, I2C0_SCL, NAND_ADQ15, USB1_DATA7, EMAC0_RXD3, TRACE_D3	
HPS	
A5ED013BB32AE4S	


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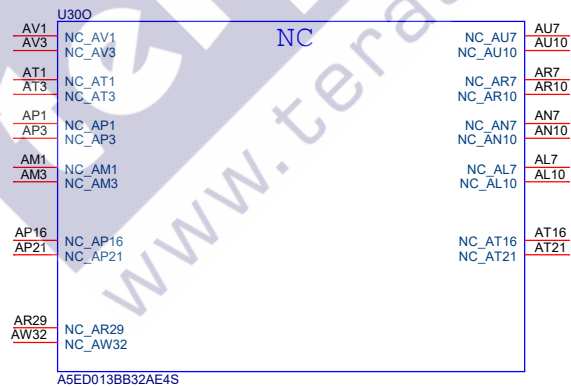
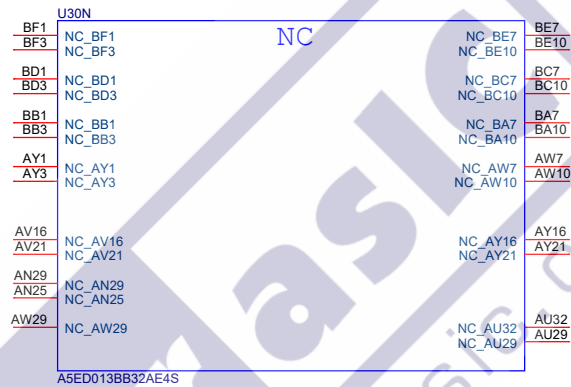
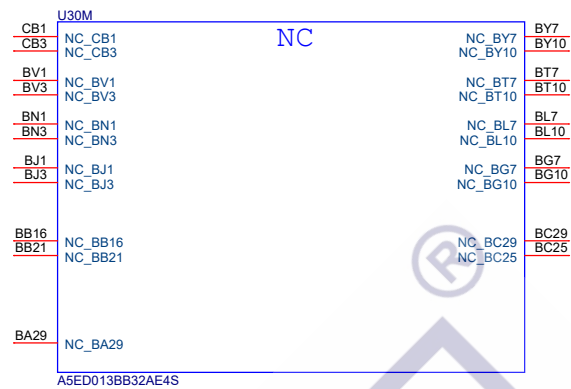
Title		
DE25-Standard Board		
Size	Document Number	Rev
B	FPGA Bank HPS	C
Date:	Tuesday, April 22, 2025	Sheet 16 of 49




HSMC Transceivers

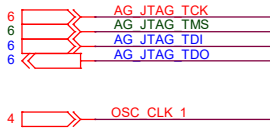


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Title			
DE25-Standard Board			
Size B	Document Number FPGA XCVR Bank 1A, NC (1B1C)		Rev C
Date:	Tuesday, April 22, 2025	Sheet	17 of 49



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Title					
DE25-Standard Board					
Size	Document Number		Rev		
B	FPGA NC (4A4B4C)		C		
Date:	Tuesday, April 22, 2025	Sheet 18 of 49			

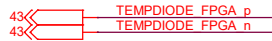
Agilex JTAG Interface



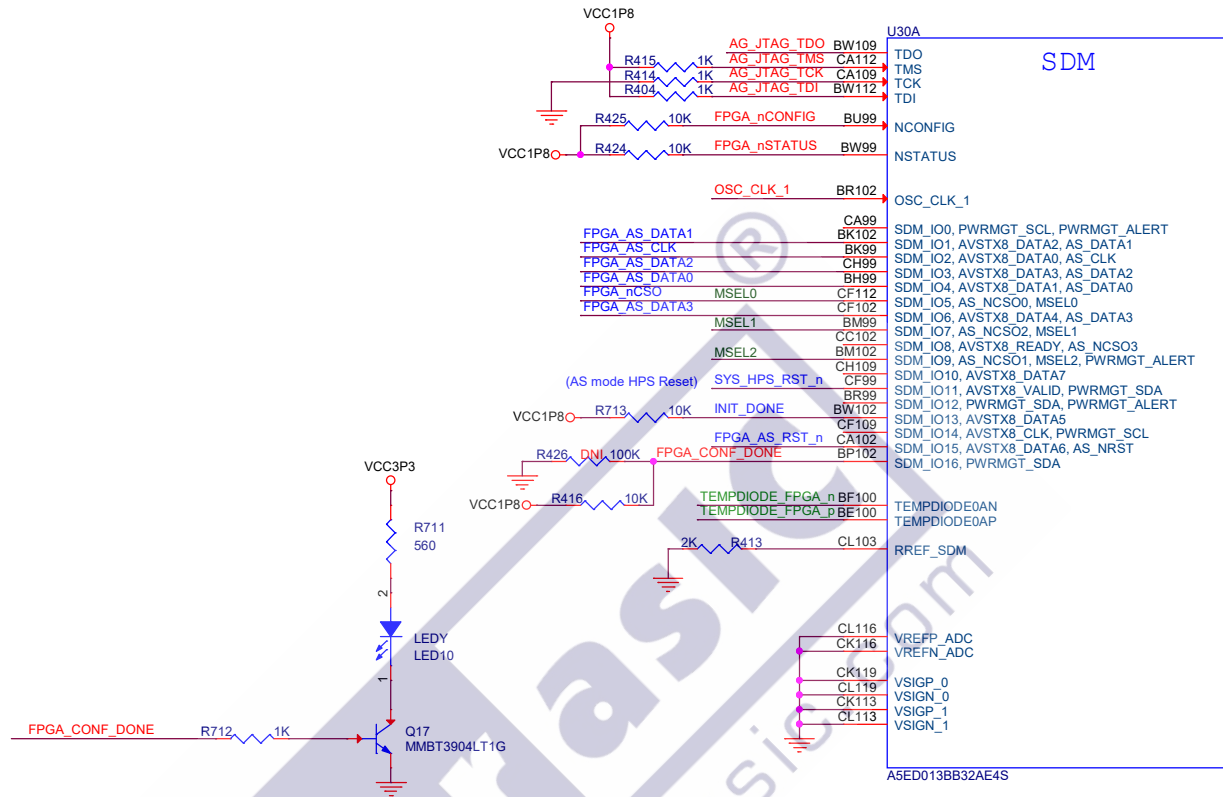
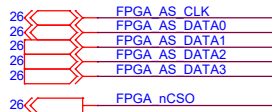
SYS_HPS_RST_n 36,37,38,42

FPGA_AS_RST_n 26

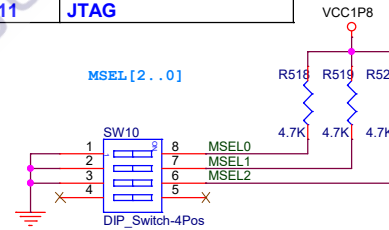
FPGA Temperature diode

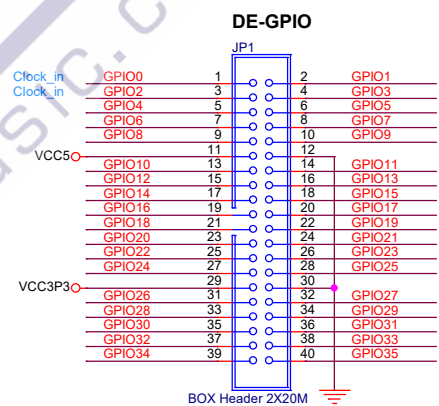
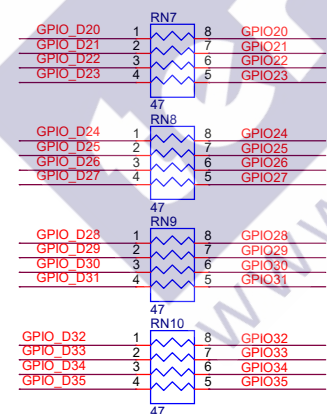
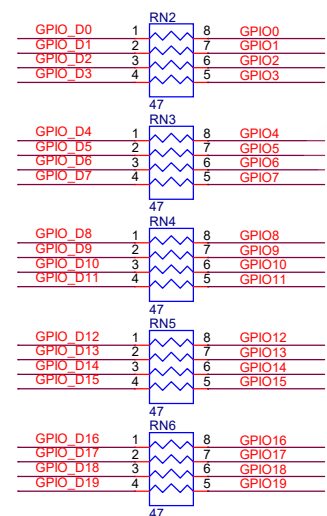
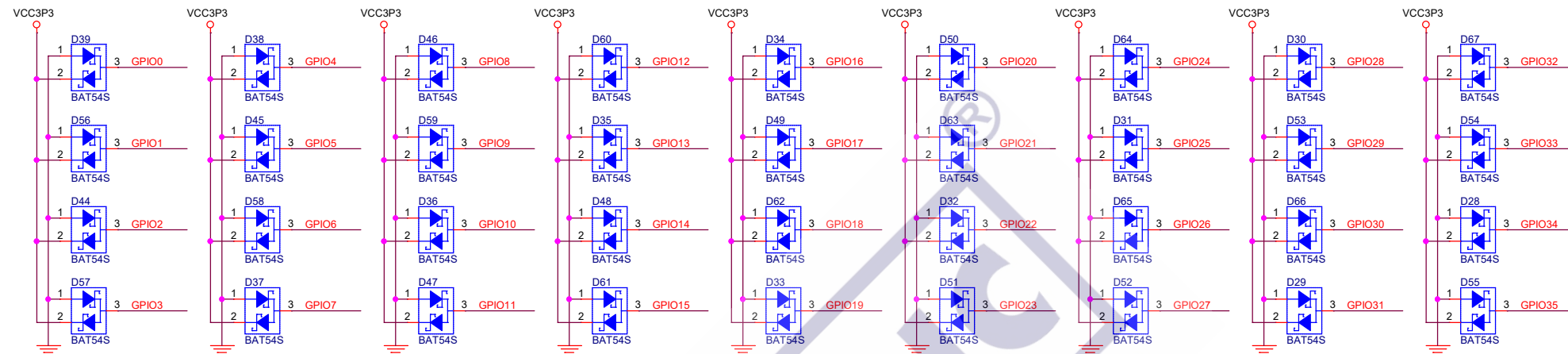


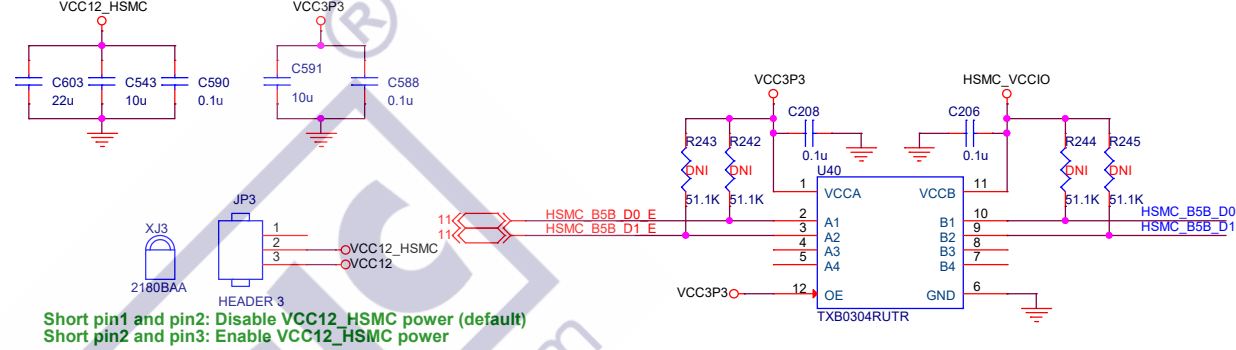
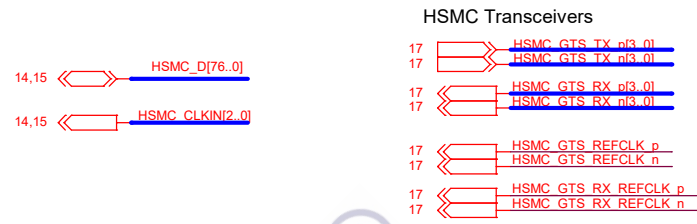
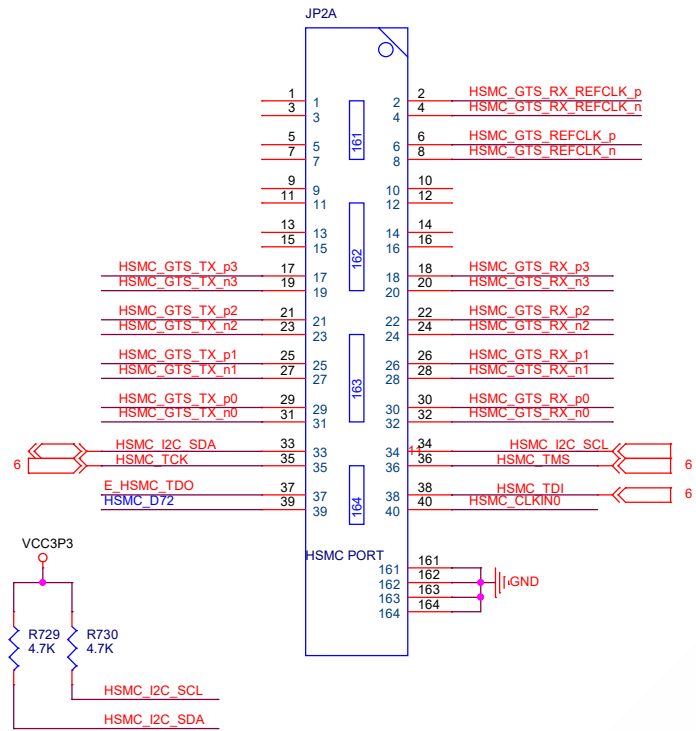
FPGA AS Configuration



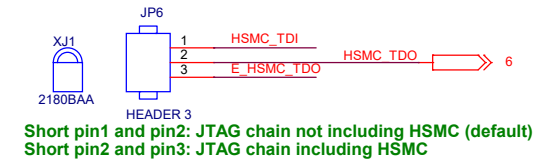
MSEL[2:0]	Configuration Mode
001	AS - Fast (Default Setting)
111	JTAG



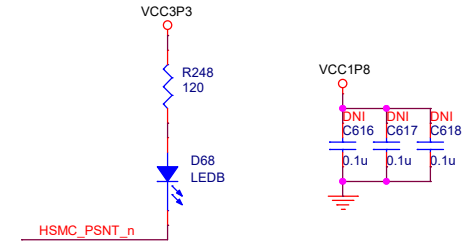


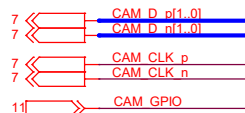


Short pin1 and pin2: Disable VCC12_HSMC power (default)
Short pin2 and pin3: Enable VCC12_HSMC power



Short pin1 and pin2: JTAG chain not including HSMC (default)
Short pin2 and pin3: JTAG chain including HSMC





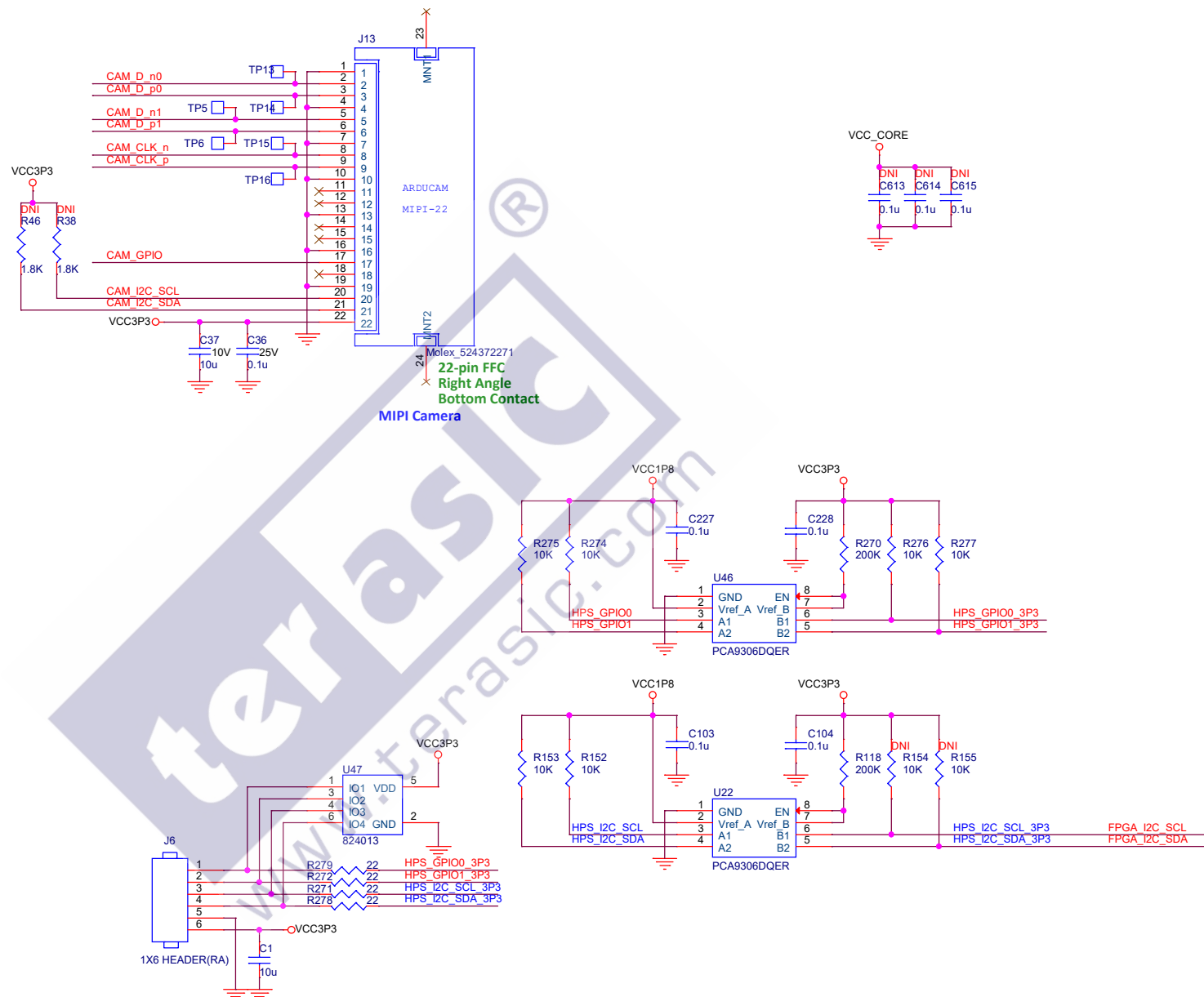
FPGA I2C Interface



HPS I2C Interface

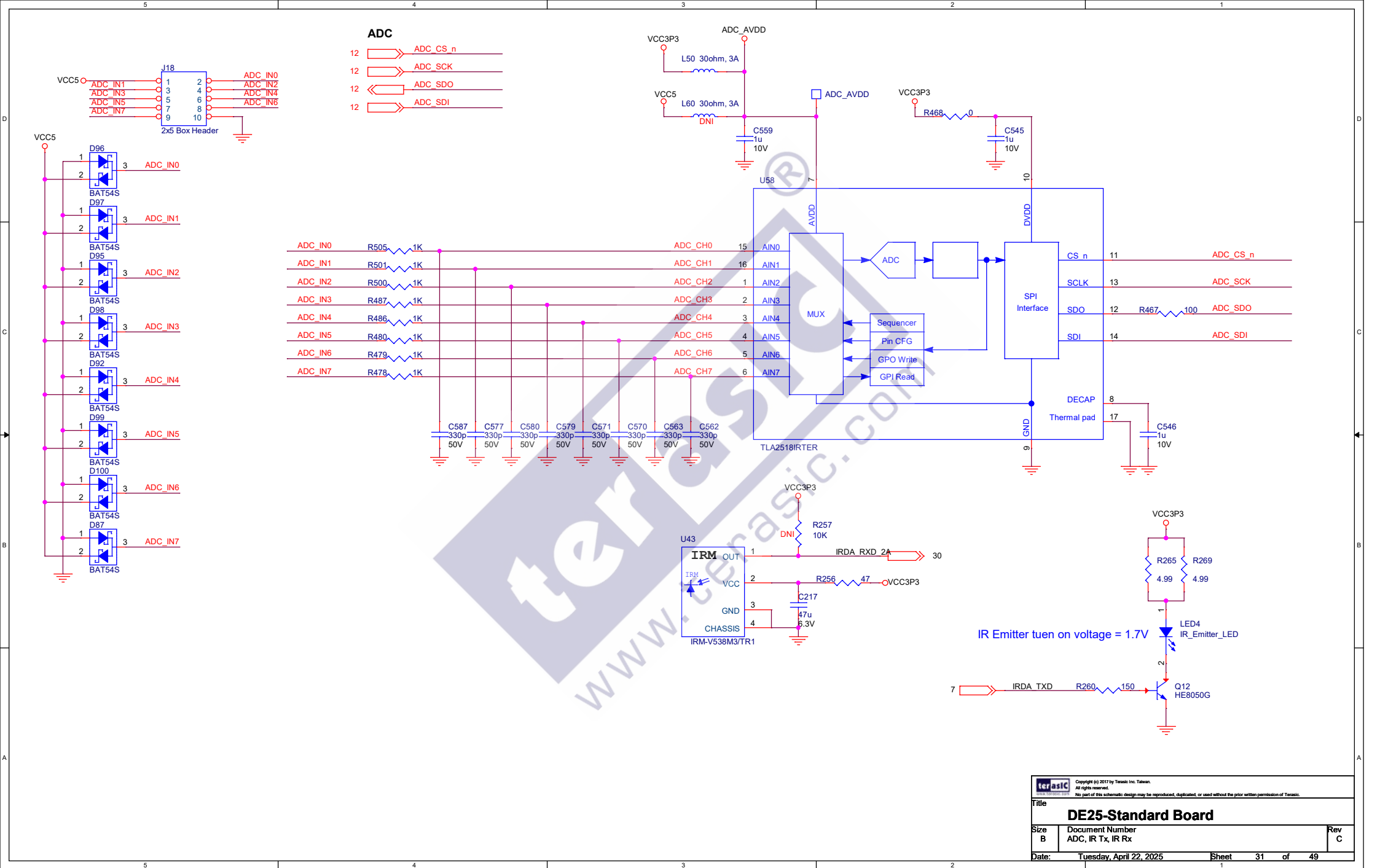


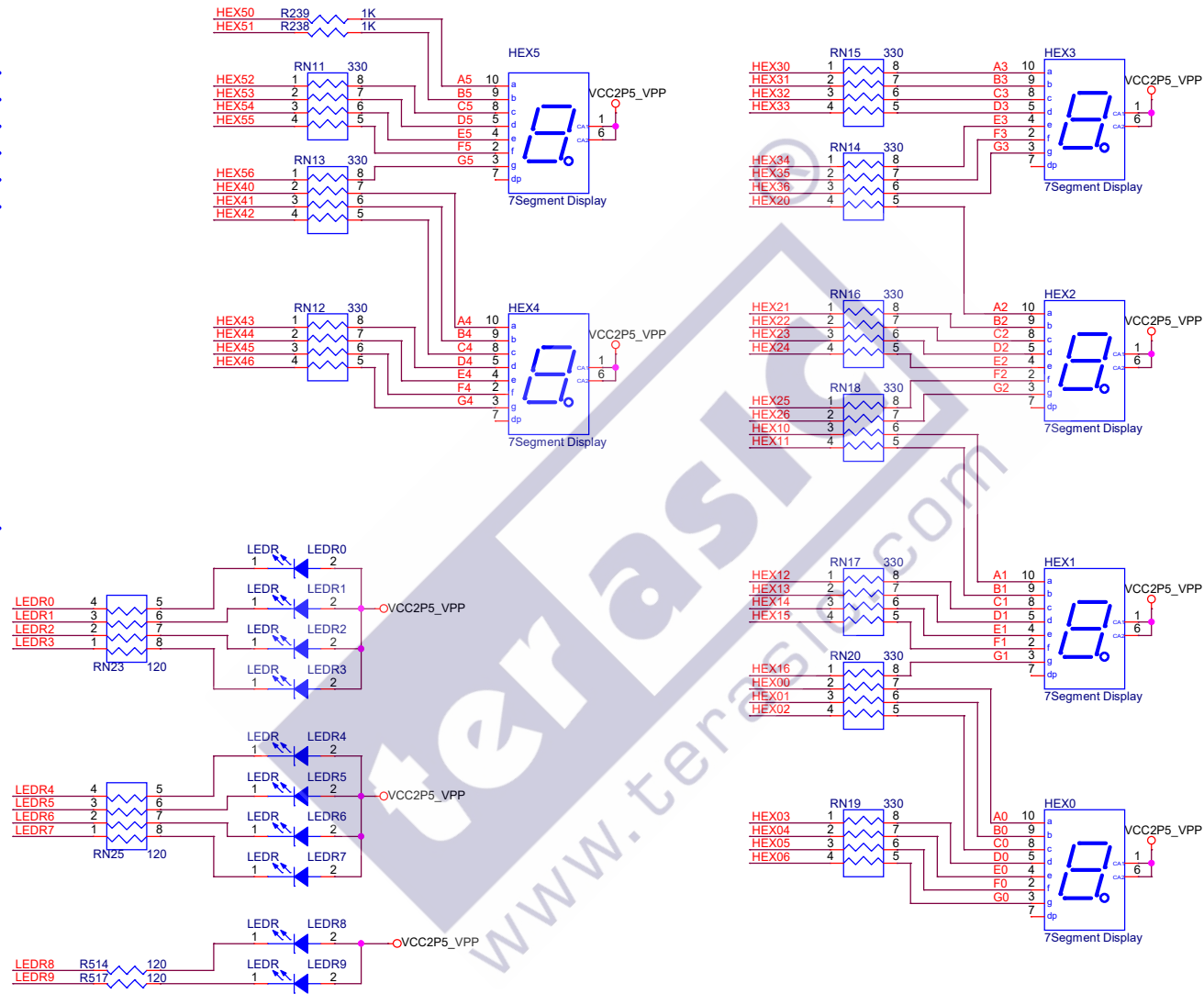
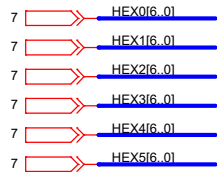
HPS GPIO

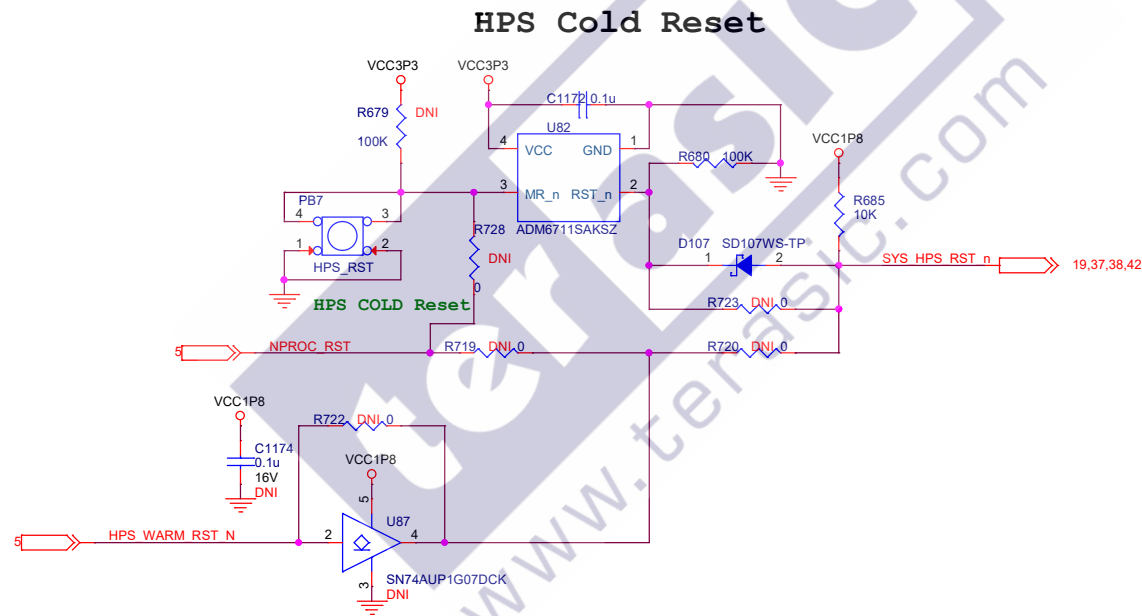
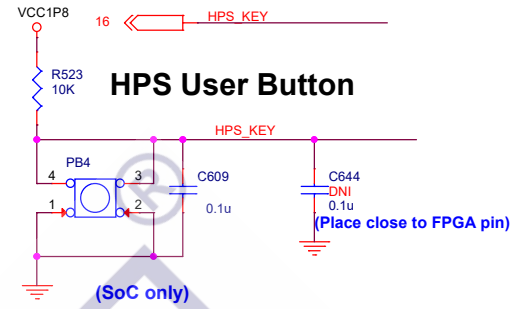
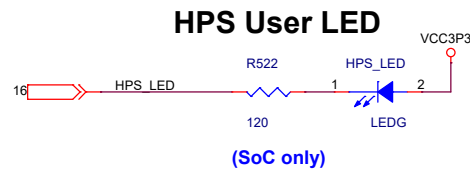



HPS 1x6 GPIO Header

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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	MIPI Connectors, HPS 1x6 GPIO	C
Date:	Wednesday, April 23, 2025	Sheet 29 of 49







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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	HPS BUTTON, HPS LED	C
Date:	Tuesday, April 22, 2025	Sheet 36 of 49