Intel Agilex® 5 FPGAs and SoCs Device Data Sheet

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Preliminary Documentation - Subject to Change

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Intel Agilex® 5 FPGAs and SoCs Device Data Sheet

This data sheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing.

Until the data sheet status for a device reaches Final, the specifications are subject to change at any time and at Intel's discretion.

Table 1. Data Sheet Status for Intel Agilex® 5 FPGAs and SoCs

Devices	Status
All devices	Preliminary

The following descriptors designate the status level currently applicable to the relevant variant:

- Advance: These are target specifications based on simulation.
- Preliminary: These specifications are based on simulation, early validation, and/or early characterization data.
- Final: These are production specifications based on silicon validation and/or characterization.

Table 2. Device Grades, Core Speed Grades, and Power Options Supported

For specification status, see the *Data Sheet Status* table

Series	Device Group	Temperature Grade	Speed Grade and Power Option Supported
D	A	Extended / Industrial	–1V (fastest)
			–2V
			–3V
E	A	Extended / Industrial	–1V (fastest)
			–2V

continued...

Series	Device Group	Temperature Grade	Speed Grade and Power Option Supported
			–2E
			–3V
	B	Extended / Industrial	–4S (fastest)
			–5S
			–6S
			–6X

The suffix after the speed grade denotes the power options offered.

- V—standard power (VID)
- E—low power (VID)
- S—standard power (fixed voltage)
- X—low power (fixed voltage)

Electrical Characteristics

Operating Conditions

The devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. D-Series FPGAs Absolute Maximum Ratings

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage supply	—	–0.5	1.21	V
V_{CCP}	Periphery supply voltage for the I/O banks	—	–0.5	1.21	V
V_{CCH_SDM}	SDM block AIB I/O supply voltage sense	—	–0.5	1.07	V
V_{CCPT}	Power supply for I/O, DTS, SDM, and system PLL	—	–0.5	2.08	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	–0.5	1.64	V
V_{CCBAT}	Battery back-up power supply (for design security volatile key register)	—	–0.5	2.08	V
$V_{CCIO\_PIO\_SDM}$	SDM block I/O supply voltage sense of bank 3A	1.00 V	–0.5	1.365	V
		1.05 V	–0.5	1.43	V
		1.1 V	–0.5	1.5	V
		1.2 V	–0.5	1.64	V
		1.3 V	–0.5	1.74	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	—	–0.5	1.21	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	–0.5	2.08	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	—	–0.5	1.21	V
V_{CCL_SDM}	SDM digital power supply	—	–0.5	1.07	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	—	–0.5	1.07	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	–0.5	1.07	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	–0.5	2.08	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	–0.5	2.08	V
V_{CCADC}	ADC voltage sensor power supply	—	–0.5	2.08	V
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	—	–0.5	1.21	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS A55 cores power rail	—	–0.5	1.21	V
$V_{CCL\_HPS\_CORE2}$	HPS A76 core power rail	—	–0.5	1.21	V
$V_{CCL\_HPS\_CORE3}$	HPS A76 core power rail	—	–0.5	1.21	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply	—	–0.5	1.21	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply	—	–0.5	1.21	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	—	–0.5	2.08	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	—	–0.5	2.08	V
V_{CCIO_HPS}	HPS I/O buffers power supply	—	–0.5	2.08	V
$V_{CCEHT\_GTS[L1, R4][A, B, C, D]}$	Transceiver PMA, TX PLL, transceiver reference clock, and global reference clock high-voltage analog power supply	—	–0.5	2.08	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CCERT\_GTS[L1, R4][A, B, C, D]}$	Transceiver PMA, transceiver reference clock, and global reference clock low-voltage analog power supply	—	–0.5	1.34	V
V_{CCIO_PIO}	HSIO bank power supply	V_{CCIO_PIO} = 1.0 V	–0.5	1.365	V
		V_{CCIO_PIO} = 1.05 V	–0.5	1.43	V
		V_{CCIO_PIO} = 1.1 V	–0.5	1.5	V
		V_{CCIO_PIO} = 1.2 V	–0.5	1.64	V
		V_{CCIO_PIO} = 1.3 V	–0.5	1.74	V
V_{CCIO_HVIO}	HVIO bank power supply	V_{CCIO_HVIO} = 3.3 V	–0.5	3.74	V
		V_{CCIO_HVIO} = 2.5 V	–0.5	2.83	V
		V_{CCIO_HVIO} = 1.8 V	–0.5	2.04	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	–0.5	2.04	V
V_I	DC input voltage	V_{CCIO_PIO} = 1.0 V(1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.05 V(1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.1 V(1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.2 V(1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.3 V(1) (2)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3	$V_{CCIO\_SDM(MAX)}$ + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3	$V_{CCIO\_HPS(MAX)}$ + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3	$V_{CCIO\_HVIO(MAX)}$ + 0.3	V

continued...

(1) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

(2) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to $V_{CCIO\_PIO(MAX)}$ + 0.3 V.

Symbol	Description	Condition	Minimum	Maximum	Unit
I_{OUT} (3) (4)	DC output current per pin	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V (5) (6)	–7.5	7.5	mA
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V (7)	–20	20	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V(8)	–10	10	mA
T_J (9)	Absolute junction temperature	—	–40	125	°C
T_{STG}	Storage temperature	—	–55	150	°C

(3) Total current per I/O bank must not exceed 100 mA.

(4) Applies to all I/O standards and settings supported by I/O banks, including single-ended and differential I/Os.

(5) The maximum current allowed through any HSIO bank pin during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed 1.2 V or the V_{CCIO_PIO} supply rail of the bank where the I/O pin resides in, whichever is the lower voltage. While this device is not turned on, the I/O pin should be tri-stated or not driven with any external voltages.

(6) The DC output current per pin may exceed 7.5 mA with a duration limit. For more details, refer to the related information.

(7) The maximum current allowed through any HPS/SDM pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HPS} or V_{CCIO_SDM} supply rail of the bank where the I/O pin resides in.

(8) The maximum current allowed through any HVIO pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HVIO} supply rail of the bank where the I/O pin resides in.

(9) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

Table 4. E-Series FPGAs Absolute Maximum Ratings

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
V_{CCP}	Periphery supply voltage for the I/O banks	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S, –5S, –6S, –6X	–0.5	1.07	V
V_{CCH_SDM}	SDM block AIB I/O supply voltage sense	Fixed Voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
V_{CCPT}	Power supply for I/O, DTS, SDM, and system PLL	—	–0.5	2.08	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	–0.5	1.64	V
V_{CCBAT}	Battery back-up power supply (for design security volatile key register)	—	–0.5	2.08	V
$V_{CCIO\_PIO\_SDM}$	SDM block I/O supply voltage sense of bank 3A	1.00 V	–0.5	1.365	V
		1.05 V	–0.5	1.43	V
		1.1 V	–0.5	1.5	V
		1.2 V	–0.5	1.64	V
		1.3 V	–0.5	1.74	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S, –5S, –6S, –6X	–0.5	1.07	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCIO_SDM}	SDM block configuration pins power supply	—	–0.5	2.08	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
V_{CCL_SDM}	SDM digital power supply	Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	–0.5	2.08	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	–0.5	2.08	V
V_{CCADC}	ADC voltage sensor power supply	—	–0.5	2.08	V
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS A55 cores power rail	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CCL\_HPS\_CORE2}$	HPS A76 core power rail	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CCL\_HPS\_CORE3}$	HPS A76 core power rail	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	—	–0.5	2.08	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	—	–0.5	2.08	V
V_{CCIO_HPS}	HPS I/O buffers power supply	—	–0.5	2.08	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CCEHT\_GTS[L1, R4][A, B, C]}$	Transceiver PMA, TX PLL, transceiver reference clock, and global reference clock high-voltage analog power supply	—	–0.5	2.08	V
$V_{CCERT\_GTS[L1, R4][A, B, C]}$	Transceiver PMA, transceiver reference clock, and global reference clock low-voltage analog power supply	—	–0.5	1.34	V
V_{CCIO_PIO}	HSIO bank power supply	V_{CCIO_PIO} = 1.0 V	–0.5	1.365	V
		V_{CCIO_PIO} = 1.05 V	–0.5	1.43	V
		V_{CCIO_PIO} = 1.1 V	–0.5	1.5	V
		V_{CCIO_PIO} = 1.2 V	–0.5	1.64	V
		V_{CCIO_PIO} = 1.3 V	–0.5	1.74	V
V_{CCIO_HVIO}	HVIO bank power supply	V_{CCIO_HVIO} = 3.3 V	–0.5	3.74	V
		V_{CCIO_HVIO} = 2.5 V	–0.5	2.83	V
		V_{CCIO_HVIO} = 1.8 V	–0.5	2.04	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	–0.5	2.04	V
V_I	DC input voltage	V_{CCIO_PIO} = 1.0 V (10) (11)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.05 V (10) (11)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.1 V (10) (11)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.2 V (10) (11)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.3 V (10) (11)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V

continued...

(10) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

(11) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to $V_{CCIO\_PIO(MAX)}$ + 0.3 V.

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_SDM} = 1.8 V	–0.3	$V_{CCIO\_SDM(MAX)}$ + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3	$V_{CCIO\_HPS(MAX)}$ + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3	$V_{CCIO\_HVIO(MAX)}$ + 0.3	V
I_{OUT} (12) (13)	DC output current per pin	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V (14) (15)	–7.5	7.5	mA
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V (16)	–20	20	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V (17)	–10	10	mA
T_J (18)	Absolute junction temperature	—	–40	125	°C
T_{STG}	Storage temperature	—	–55	150	°C

(12) Total current per I/O bank must not exceed 100 mA.

(13) Applies to all I/O standards and settings supported by I/O banks, including single-ended and differential I/Os.

(14) The maximum current allowed through any HSIO bank pin during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed 1.2 V or the V_{CCIO_PIO} supply rail of the bank where the I/O pin resides in, whichever is the lower voltage. While this device is not turned on, the I/O pin should be tri-stated or not driven with any external voltages.

(15) The DC output current per pin may exceed 7.5 mA with a duration limit. For more details, refer to the related information.

(16) The maximum current allowed through any HPS/SDM pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HPS} or V_{CCIO_SDM} supply rail of the bank where the I/O pin resides in.

(17) The maximum current allowed through any HVIO pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HVIO} supply rail of the bank where the I/O pin resides in.

(18) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

Related Information

- Recommended Operating Conditions on page 19
- I/O Standard Specifications on page 41

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, the toggling input data or clock signals may overshoot to the voltage listed in the following tables and undershoot to the following limits for input currents less than 100 mA and periods shorter than 20 ns.

- Undershoot limit of –1.1 V when using V_{CCIO_HPS} or V_{CCIO_SDM} of 1.8 V.
- Undershoot limit of –0.3 V when using V_{CCIO_PIO} of 1.3 V, 1.2 V, 1.1 V, 1.05 V, and 1.0 V.

No overshooting beyond 1.602 V and undershooting below 0.273 V is allowed when using True Differential Signaling I/O standard at V_{CCIO_PIO} = 1.3 V.

No overshooting beyond 1.177 V and undershooting below 0.573 V is allowed when using True Differential Signaling I/O standard at V_{CCIO_PIO} = 1.2 V, 1.1 V, and 1.05 V.

The maximum allowed overshoot duration is specified as a percentage of high time (calculated as ([delta T]/T) × 100) over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

Table 5. Maximum Allowed Overshoot During Transitions for 1.0 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[19]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

(19) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Table 6. Maximum Allowed Overshoot During Transitions for 1.05 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[20]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 7. Maximum Allowed Overshoot During Transitions for 1.1 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[21]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

(20) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

(21) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Table 8. Maximum Allowed Overshoot During Transitions for 1.2 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30(22)	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 9. Maximum Allowed Overshoot During Transitions for 1.3 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30(23)	65	%
		V_{CCIO_PIO} + 0.35	7	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

(22) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

(23) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Table 10. Maximum Allowed Overshoot During Transitions for 1.8 V I/O in HPS and SDM I/O Banks

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_SDM} + 0.30, V_{CCIO_HPS} + 0.30	100	%
		V_{CCIO_SDM} + 0.35, V_{CCIO_HPS} + 0.35	60	%
		V_{CCIO_SDM} + 0.40, V_{CCIO_HPS} + 0.40	30	%
		V_{CCIO_SDM} + 0.45, V_{CCIO_HPS} + 0.45	20	%
		V_{CCIO_SDM} + 0.50, V_{CCIO_HPS} + 0.50	10	%
		V_{CCIO_SDM} + 0.55, V_{CCIO_HPS} + 0.55	6	%
		> V_{CCIO_SDM} + 0.55, > V_{CCIO_HPS} + 0.55	No overshoot allowed	%

Table 11. Maximum Allowed Overshoot During Transitions for 1.8 V, 2.5 V, and 3.3 V in HVIO Bank

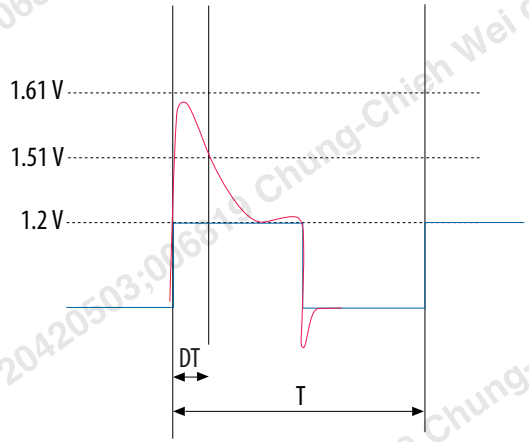
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_HVIO} + 0.30	100	%
		V_{CCIO_HVIO} + 0.35	42	%
		V_{CCIO_HVIO} + 0.40	18	%
		V_{CCIO_HVIO} + 0.45	9	%
		V_{CCIO_HVIO} + 0.50	4	%
		> V_{CCIO_HVIO} + 0.55	No overshoot allow	%

For example, when using 1.2 V I/O standard with 1.26 V V_{CCIO_PIO}, a signal that overshoots to 1.61 V can only be at 1.61 V for ~4% over the lifetime of the device. For an overshoot of 1.51 V, the percentage of high time for the overshoot can be as high as 100% over the lifetime of the device.

Figure 1. Overshoot Duration Example (for 1.2 V HSIO Bank at V_{CCIO_PIO} = 1.26 V)



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters.

Recommended Operating Conditions

Table 12. D-Series FPGAs Recommended Operating Conditions

This table lists the steady-state voltage values expected. Power supply ramps must all be strictly monotonic, without plateaus.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum[24]	Typical	Maximum[24]	Unit
V_{CC}	Core voltage supply	SmartVID[25] : –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90[26]	(Typical) + 3%	V
V_{CCP}	Periphery supply voltage for the I/O banks	SmartVID[25]: –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90[26]	(Typical) + 3%	V
V_{CCH_SDM}	SDM block AIB I/O supply voltage sense	—	0.975	1	1.025	V
V_{CCPT} [27]	Power supply for I/O, DTS, SDM, and system PLL	—	1.746	1.8	1.854	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	1.14	1.2	1.26	V
V_{CCBAT}	Battery back-up power supply (for design security volatile key register)	—	1	1 – 1.80	1.8	V

continued...

(24) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(25) The use of Power Management Bus (PMBus*) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

(26) The typical value is based on the SmartVID programmed value.

(27) Must use a tolerance of ±3% when sharing with V_{CCIO_HVIO}. A tolerance of ±5% is only allowed when V_{CCPT} is not shared with other rails.

Symbol	Description	Condition	Minimum[24]	Typical	Maximum[24]	Unit
I_{BAT}	Battery back-up power supply (for design security volatile key register)	V_{CCBAT} = 1.2 V	—	—	200	nA
$V_{CCIO\_PIO\_SDM}$ [28]	SDM block I/O supply voltage sense of bank 3A	1.00 V	0.95	1	1.05	V
		1.05 V[29]	1.0185	1.05	1.0815	V
		1.1 V[29]	1.067	1.1	1.133	V
		1.2 V[29]	1.164	1.2	1.236	V
		1.3 V	1.261	1.3	1.339	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	SmartVID[25]: –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90[26]	(Typical) + 3%	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	SmartVID[25]: –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90[26]	(Typical) + 3%	V

continued...

(24) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(28) Must be powered up with the same voltage level as $V_{CCIO\_PIO\_3A}$. Must be supplied at 1.2 V when using Avalon® Streaming ×16 configuration schemes.

(29) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes:

- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

Symbol	Description	Condition	Minimum[24]	Typical	Maximum[24]	Unit
V_{CCL_SDM}	SDM digital power supply	—	0.776	0.8	0.824	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	0.776	0.8	0.824	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	1.71	1.8	1.89	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCIO_PIO}	HSIO bank power supply	1.0 V	0.95	1	1.05	V
		1.05 V[29]	1.0185	1.05	1.0815	V
		1.1 V[29]	1.067	1.1	1.133	V
		1.2 V[29]	1.164	1.2	1.236	V
		1.3 V	1.261	1.3	1.339	V
V_{CCIO_HVIO}	HVIO bank power supply	3.3 V	3.201	3.3	3.399	V
		2.5 V	2.425	2.5	2.575	V
		1.8 V	1.746	1.8	1.854	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	1.746	1.8	1.854	V
V_I [30]	DC input voltage	V_{CCIO_PIO} = 1.0 V[31]	–0.3000	—	V_{CCIO_PIO} + 0.25	V

continued...

(24) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(30) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(31) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

Symbol	Description	Condition	Minimum[24]	Typical	Maximum[24]	Unit
		V_{CCIO_PIO} = 1.05 V[32] [31]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.1 V[32] [31]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.2 V[32] [31]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.3 V[32] [31]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3000	—	V_{CCIO_SDM} + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3000	—	V_{CCIO_HPS} + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3000	—	V_{CCIO_HVIO} + 0.3	V
V_O	Output voltage	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V	0	—	V_{CCIO_PIO}	V
		V_{CCIO_SDM} = 1.8 V	0	—	V_{CCIO_SDM}	V
		V_{CCIO_HPS} = 1.8 V	0	—	V_{CCIO_HPS}	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	0	—	V_{CCIO_HVIO}	V

continued...

(24) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(32) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

Symbol	Description	Condition	Minimum[24]	Typical	Maximum[24]	Unit
T_J	Operating junction temperature	Extended	0	—	100[33]	°C
		Industrial	–40	—	100[33]	°C
t_{RAMP} [34] [35]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

Table 13. E-Series FPGAs Recommended Operating Conditions

This table lists the steady-state voltage values expected. Power supply ramps must all be strictly monotonic, without plateaus.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum[36]	Typical	Maximum[36]	Unit
V_{CC}	Core voltage supply	SmartVID[37] : –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[38]	(Typical) + 3%	V
		Fixed voltage: –4S	0.776	0.8	0.824	V

continued...

(24) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(33) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

(34) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies. The ramp time applies to both the ramp-up and ramp-down of the power rails.

(35) To support AS fast mode, all power supplies to the device must be fully ramped-up within 10 ms to the recommended operating conditions.

(36) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(37) The use of Power Management Bus (PMBus) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

(38) The typical value is based on the SmartVID programmed value.

Symbol	Description	Condition	Minimum[36]	Typical	Maximum[36]	Unit
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCP}	Periphery supply voltage for the I/O banks	SmartVID[37]: –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[38]	(Typical) + 3%	V
		Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCH_SDM}	SDM block AIB I/O supply voltage sense	Without transceiver: –4S	0.776	0.8	0.824	V
		Without transceiver: –5S	0.756	0.78	0.803	V
		Without transceiver: –6S, –6X	0.7275	0.75	0.7725	V
		With transceiver	0.975	1	1.025	V
V_{CCPT} [39]	Power supply for I/O, DTS, SDM, and system PLL	—	1.746	1.8	1.854	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	1.14	1.2	1.26	V
V_{CCBAT}	Battery back-up power supply (for design security volatile key register)	—	1	1 – 1.80	1.8	V

continued...

(36) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(39) Must use a tolerance of ±3% when sharing with V_{CCIO_HVIO}. A tolerance of ±5% is only allowed when V_{CCPT} is not shared with other rails.

Symbol	Description	Condition	Minimum[36]	Typical	Maximum[36]	Unit
I_{BAT}	Battery back-up power supply (For design security volatile key register)	V_{CCBAT} = 1.2 V	—	—	200	nA
$V_{CCIO\_PIO\_SDM}$ [40]	SDM block I/O supply voltage sense of bank 3A	1.0 V	0.95	1	1.05	V
		1.05 V[41]	1.0185	1.05	1.0815	V
		1.1 V[41]	1.067	1.1	1.133	V
		1.2 V[41]	1.164	1.2	1.236	V
		1.3 V	1.261	1.3	1.339	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	SmartVID[37]: –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[38]	(Typical) + 3%	V
		Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS	SmartVID[37]: –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[38]	(Typical) + 3%	V

continued...

(36) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(40) Must be powered up with the same voltage level as $V_{CCIO\_PIO\_3A}$. Must be supplied at 1.2 V when using Avalon Streaming ×16 configuration schemes.

Symbol	Description	Condition	Minimum[36]	Typical	Maximum[36]	Unit
	digital supply on HPS devices, core supply on non-HPS devices	Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCL_SDM}	SDM digital power supply	Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	1.71	1.8	1.89	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCIO_PIO}	HSIO bank power supply	1.0 V	0.95	1	1.05	V
		1.05 V[41]	1.0185	1.05	1.0815	V

continued...

(36) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

Symbol	Description	Condition	Minimum[36]	Typical	Maximum[36]	Unit
		1.1 V[41]	1.067	1.1	1.133	V
		1.2 V[41]	1.164	1.2	1.236	V
		1.3 V	1.261	1.3	1.339	V
V_{CCIO_HVIO}	HVIO bank power supply	3.3 V	3.201	3.3	3.399	V
		2.5 V	2.425	2.5	2.575	V
		1.8 V	1.746	1.8	1.854	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	1.746	1.8	1.854	V
V_I [42]	DC input voltage	V_{CCIO_PIO} = 1.0 V[43]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.05 V[44] [43]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.1 V[44] [43]	–0.3000	—	V_{CCIO_PIO} + 0.25	V

continued...

(36) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(41) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes:
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

(42) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(43) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

(44) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

Symbol	Description	Condition	Minimum[36]	Typical	Maximum[36]	Unit
		V_{CCIO_PIO} = 1.2 V[44] [43]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.3 V[44] [43]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3000	—	V_{CCIO_SDM} + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3000	—	V_{CCIO_HPS} + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3000	—	V_{CCIO_HVIO} + 0.3	V
V_O	Output voltage	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V	0	—	V_{CCIO_PIO}	V
		V_{CCIO_SDM} = 1.8 V	0	—	V_{CCIO_SDM}	V
		V_{CCIO_HPS} = 1.8 V	0	—	V_{CCIO_HPS}	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	0	—	V_{CCIO_HVIO}	V
T_J	Operating junction temperature	Extended	0	—	100[45]	°C
		Industrial	–40	—	100[45]	°C
t_{RAMP} [46] [47]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

(36) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(45) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

(46) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies. The ramp time applies to both the ramp-up and ramp-down of the power rails.

(47) To support AS fast mode, all power supplies to the device must be fully ramped-up within 10 ms to the recommended operating conditions.

Related Information

I/O Standard Specifications on page 41

GTS Transceiver Power Supply Operating Conditions

Table 14. D-Series FPGAs GTS Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended VR Accuracy (% of Typical DC Level)	Recommended VR Ripple (% of Typical DC Level)	Recommended AC Transient (% of Typical DC Level)	Maximum (VR Accuracy + Ripple + AC Transient) (% of Typical DC Level)(48)	Unit
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	0.8	±0.5	±2.5		±3	V
$V_{CCEHT\_GTS[L1, R4][A, B, C, D]}$ (49)	Transceiver PMA, transceiver PLL, and transceiver reference clock high voltage analog power supply	1.8	±0.5	±2.0		±2.5	V
$V_{CCERT\_GTS[L1, R4][A, B, C, D]}$	Transceiver PMA and transceiver reference clock low voltage analog power supply	1	±0.5	±2.0		±2.5	V

(48) For scope measurement, 20 MHz bandwidth is sufficient. During measurement, put the ground pin as close to the power rail pin as possible.

(49) HF noise requires AC 30 mVpp above 1 MHz.

Table 15. E-Series FPGAs GTS Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Speed Grade	Typical DC Level (V)	Recommended VR Accuracy (% of Typical DC Level)	Recommended VR Ripple (% of Typical DC level)	Recommended AC Transient (% of Typical DC level)	Maximum (VR Accuracy + Ripple + AC Transient) (% of Typical DC Level)(50)	Unit
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	–6S, –6X	0.75	±0.5	±2.5		±3	V
		–5S	0.78	±0.5	±2.5		±3	V
		–1V, –2V, –2E, –3V, –4S	0.8	±0.5	±2.5		±3	V
$V_{CCEHT\_GTS[L1,R4][A, B, C]}$ (51)	Transceiver PMA, transceiver PLL, and transceiver reference clock high voltage analog power supply	—	1.8	±0.5	±2.0		±2.5	V
$V_{CCERT\_GTS[L1, R4][A, B, C]}$	Transceiver PMA and transceiver reference clock low voltage analog power supply	—	1	±0.5	±2.0		±2.5	V

(50) For scope measurement, 20 MHz bandwidth is sufficient. During measurement, put the ground pin as close to the power rail pin as possible.

(51) HF noise requires AC 30 mVpp above 1 MHz.

HPS Power Supply Operating Conditions

Table 16. D-Series FPGAs HPS Power Supply Operating Conditions

This table lists the steady-state voltage and current values expected for system-on-a-chip (SoC) devices with Arm*-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions* table for the steady-state voltage values expected from the FPGA portion of the SoC devices.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	SmartVID: –1V, –2V, –3V[52]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS Cortex-A55 core 0 and core 1 power rail	SmartVID: –1V, –2V, –3V[52]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE2}$	HPS Cortex-A76 core 2 power rail	SmartVID: –1V, –2V, –3V[52]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE3}$	HPS Cortex-A76 core 3 power rail	SmartVID: –1V, –2V, –3V[52]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –3V[52]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –3V[52]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

(52) The use of Power Management Bus (PMBus) voltage regulator dedicated to the SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

Table 17. E-Series FPGAs HPS Power Supply Operating Conditions

This table lists the steady-state voltage and current values expected for system-on-a-chip (SoC) devices with Arm-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions* table for the steady-state voltage values expected from the FPGA portion of the SoC devices.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	SmartVID: –1V, –2V, –2E, –3V(53)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS Cortex-A55 core 0 and core 1 power rail	SmartVID: –1V, –2V, –2E, –3V(53)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE2}$	HPS Cortex-A76 core 2 power rail	SmartVID: –1V, –2V, –2E, –3V(53)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE3}$	HPS Cortex-A76 core 3 power rail	SmartVID: –1V, –2V, –2E, –3V(53)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V

continued...

(53) The use of Power Management Bus (PMBus) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –2E, –3V(53)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –2E, –3V(53)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- Recommended Operating Conditions on page 19
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance on page 97

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Intel FPGA Power and Thermal Calculator (PTC) and the Intel Quartus® Prime Power Analyzer feature.

Use the PTC before you start your design to estimate the supply current for your design. The PTC provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

HSIO DC Characteristics

HSIO I/O Pin Leakage Current

Table 18. HSIO I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA

HSIO OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 19. HSIO OCT Calibration Accuracy Specifications

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

These specifications require RZQ reference accuracy of 240 Ω ±1%.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S (54)	Internal series termination with calibration (34-Ω and 40-Ω setting)	SSTL-12, HSTL-12, HSUL-12, and POD12 I/O standards	20	%
34-Ω and 40-Ω R_S (54)	Internal series termination with calibration (34-Ω and 40-Ω setting)	POD11 and LVSTL11 I/O standards	20	%
34-Ω and 40-Ω R_S (54)	Internal series termination with calibration (34-Ω and 40-Ω setting)	LVSTL105 I/O standard	20	%
40-Ω R_S (54)	Internal series termination with calibration (40-Ω setting)	LVSTL700 I/O standard	20	%
45-Ω R_S	Internal series termination with calibration (45-Ω setting)	DPHY and SLVS400 I/O standards	20	%
50-Ω and 60-Ω R_T (54)	Internal parallel termination with calibration (50-Ω and 60-Ω setting)	SSTL-12 and HSTL-12 I/O standards	20	%
40-Ω, 50-Ω, and 60-Ω R_T (54)	Internal parallel termination with calibration (40-Ω, 50-Ω, and 60-Ω setting)	POD11 and POD12 I/O standards	20	%
		LVSTL11, LVSTL105, and LVSTL700 I/O standards	20	%
100-Ω R_D	Internal differential termination with calibration (100-Ω setting)	DPHY and SLVS400 I/O standards	–15 to +25	%

(54) This specification applies to both single-ended and pseudo-differential I/O buffers.

HSIO OCT Without Calibration Resistance Tolerance Specifications

Table 20. HSIO OCT Without Calibration Resistance Tolerance Specifications

This table lists the GPIO OCT without calibration resistance tolerance to PVT changes.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.3 V LVCMOS I/O standard	30	%
34-Ω and 40-Ω R_S (55)	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.2 V LVCMOS, SSTL-12, HSTL-12, HSUL-12, and POD12 I/O standards	25	%
34-Ω and 40-Ω R_S (55)	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.1 V LVCMOS, POD11, and LVSTL11 I/O standards	25	%
34-Ω and 40-Ω R_S (55)	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.05 V LVCMOS and LVSTL105 I/O standards	25	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.0 V LVCMOS I/O standard	30	%
50-Ω R_T (55)	Internal parallel termination without calibration (50-Ω setting)	SSTL-12 and HSTL-12 I/O standards	25	%
		POD11 and POD12 I/O standards	25	%
		LVSTL11 and LVSTL105 I/O standards	25	%
100-Ω R_D	Internal differential termination (100-Ω setting)	True differential signaling I/O standard at V_{CCIO_PIO} = 1.05	40	%

continued...

(55) This specification applies to both single-ended and pseudo-differential I/O buffers.

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.1	40	%
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.2	40	%
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.3	40	%

HSIO Pin Capacitance

Table 21. HSIO Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	2.6(56)	pF

HSIO Internal Weak Pull-Up Resistor

All I/O pins in GPIO bank have an option to enable weak pull-up when using 1.0 V, 1.05 V, 1.1 V, 1.2 V, and 1.3 V LVCMOS I/O standards.

Table 22. HSIO Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO_PIO} = 1.3 ±3%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.2 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.1 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.05 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.0 ±5%	3	10	30	kΩ

(56) This value refers to die-level pin capacitance without the device package.

HVIO DC Characteristics

HVIO I/O Pin Leakage Current

Table 23. HVIO I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to V_{CCIO_HVIO} = 1.8 V	0.01	4.6	µA
		V_I = 0 V to V_{CCIO_HVIO} = 2.5 V	0.02	7.4	µA
		V_I = 0 V to V_{CCIO_HVIO} = 3.3 V	0.04	9.2	µA
I_{OZ}	Tri-stated I/O pin	V_I = 0 V to V_{CCIO_HVIO} = 1.8 V	0.01	4.6	µA
		V_I = 0 V to V_{CCIO_HVIO} = 2.5 V	0.02	7.4	µA
		V_I = 0 V to V_{CCIO_HVIO} = 3.3 V	0.04	9.2	µA

HVIO Pin Capacitance

Table 24. HVIO Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	4(57)	pF

HVIO Internal Weak Pull-Up and Pull-Down Resistor

Only input and bidirectional pins in HVIO bank have an option to enable weak pull-up and pull-down when using LVCMOS I/O standard.

(57) This value refers to die-level pin capacitance without the device package.

Table 25. HVIO Internal Weak Pull-Up and Pull-Down Resistor Values

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_HVIO} = 1.8, 2.5, 3.3 ±3%	15	20	25	kΩ

HVIO Hysteresis Specifications for Schmitt Trigger Input

Table 26. HVIO Hysteresis Specifications for Schmitt Trigger Input

This device supports Schmitt trigger input on HVIO I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_HVIO} = 1.8 V	—	200	—	mV
		V_{CCIO_HVIO} = 2.5 V	—	250	—	mV
		V_{CCIO_HVIO} = 3.3 V	—	250	—	mV

HPS and SDM I/O DC Characteristics

HPS and SDM I/O Pin Leakage Current

Table 27. HPS and SDM I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input or tri-stated I/O pin	V_I, V_O = 0 V	0.015	6	µA
		V_I, V_O = $V_{CCIO\_HPS\ (MAX)}$, $V_{CCIO\_SDM\ (MAX)}$	0.01	1	µA

HPS and SDM I/O Pin Capacitance

Table 28. HPS and SDM I/O Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	5[58]	pF

HPS and SDM I/O Internal Weak Pull-Up Resistor

The I/O pins in SDM and HPS bank are supported with weak pull-up and weak pull-down options. For SDM I/O pins, the weak pull-up and weak pull-down features are pre-configured according to the configuration mode.

Table 29. HPS and SDM I/O Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_SDM} = 1.8 ±5%, V_{CCIO_HPS} = 1.8 ±5%	15	20	25	kΩ
50 kΩ R_{PU}, 50 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_SDM} = 1.8 ±5%, V_{CCIO_HPS} = 1.8 ±5%	37.5	50	62.5	kΩ
80 kΩ R_{PU}, 80 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the	V_{CCIO_SDM} = 1.8 ±5%, V_{CCIO_HPS} = 1.8 ±5%	60	80	100	kΩ

continued...

(58) This value refers to die-level pin capacitance without the device package.

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
	programmable pull-up or pull-down resistor option.					

HPS and SDM I/O Hysteresis Specifications for Schmitt Trigger Input

Table 30. HPS and SDM I/O Hysteresis Specifications for Schmitt Trigger Input

This device supports Schmitt trigger input on HPS I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_HPS} = 1.8 V	180	250	350	mV

I/O Standard Specifications

HSIO I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_PIO} values. For maximum voltage values, use the maximum V_{CCIO_PIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general-purpose I/O standards.

Related Information

Recommended Operating Conditions on page 19

HSIO Single-Ended I/O Standards Specifications

Table 31. HSIO Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)(59)	V_{OH} (V)(59)
	Min	Typ	Max	Min	Max	Min	Max(60)	Max	Min
1.3 V LVCMOS	1.261	1.3	1.339	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.2 V LVCMOS	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.1 V LVCMOS	1.045	1.1	1.155	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.05 V LVCMOS	0.9975	1.05	1.1025	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.0 V LVCMOS	0.95	1	1.05	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}

HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications

Table 32. HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			Internal V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
HSTL-12	1.14	1.2	1.26	0.47 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.53 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}

continued...

(59) Applicable to test condition of I_{OH} and I_{OL} at 2 mA.

(60) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{IH(max)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

I/O Standard	V_{CCIO_PIO} (V)			Internal V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSUL-12[61]	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
POD12[62]	1.164	1.2	1.236	0.69 × V_{CCIO_PIO}	0.7 × V_{CCIO_PIO}	0.71 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—
POD11[62]	1.067	1.1	1.133	0.69 × V_{CCIO_PIO}	0.7 × V_{CCIO_PIO}	0.71 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—

HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

Table 33. HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	$V_{IL(DC)}$ (V)	$V_{IH(DC)}$ (V)	$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)
	Max	Min	Max	Min
SSTL-12	V_{REF} – 0.075	V_{REF} + 0.075	V_{REF} – 0.100	V_{REF} + 0.100
HSTL-12	V_{REF} – 0.080	V_{REF} + 0.080	V_{REF} – 0.150	V_{REF} + 0.150
HSUL-12	V_{REF} – 0.100	V_{REF} + 0.100	V_{REF} – 0.135	V_{REF} + 0.135
POD12	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070
POD11	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070

Note: For output voltage swing calculation example, refer to the *General-Purpose I/O User Guide* for this device. Differential voltage referenced I/O standard uses two single-ended outputs with second output programmed as inverted.

(61) Usage of receiver termination is optional.

(62) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.

- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

HSIO Single-Ended LVSTL I/O Standards Specifications

Table 34. HSIO Single-Ended LVSTL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Max	Min	Max	Min	Max
LVSTL11(63)	1.067	1.1	1.133	–0.2	0.07	0.35	V_{CCIO_PIO} + 0.2	–0.2	0.02	0.4	V_{CCIO_PIO} + 0.2
LVSTL105(63)	1.0185	1.05	1.0815	–0.2	0.07	0.35	V_{CCIO_PIO} + 0.2	–0.2	0.02	0.4	V_{CCIO_PIO} + 0.2
LVSTL700(63)	1.067	1.1	1.133	–0.2	0.07	0.35	V_{CCIO_PIO} + 0.2	–0.2	0.02	0.4	V_{CCIO_PIO} + 0.2
	1.0185	1.05	1.0815								

(63) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications

Table 35. HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (V)			$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Max	Min	Max	Min	Min	Typ	Max	Min	Typ	Max
SSTL-12(64)	1.14	1.2	1.26	–0.15	0.15	–0.2	0.2	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSTL-12(64)	1.14	1.2	1.26	–0.16	0.16	–0.3	0.3	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSUL-12(64)	1.14	1.2	1.26	–0.2	0.2	–0.27	0.27	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12

HSIO Differential POD I/O Standards Specifications

Table 36. HSIO Differential POD I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)(65)
	Min	Typ	Max	Max	Min	Max	Min	Max
POD12(66)	1.164	1.2	1.236	–0.11	0.11	–0.14	0.14	25
POD11(66)	1.067	1.1	1.133	–0.11	0.11	–0.14	0.14	25

(64) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

(65) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

HSIO Differential LVSTL I/O Standards Specifications

Table 37. HSIO Differential LVSTL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)(67)
	Min	Typ	Max	Max	Min	Max	Min	Max
LVSTL11(68)	1.067	1.1	1.133	–0.11	0.11	–0.14	0.14	25
LVSTL105(68)	1.0185	1.05	1.0815	–0.11	0.11	–0.14	0.14	25
LVSTL700(68)	1.067	1.1	1.133	–0.11	0.11	–0.14	0.14	25
	1.0185	1.05	1.0815					

(66) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

(67) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

(68) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

HSIO Differential I/O Standards Specifications

Table 38. HSIO Differential I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV)(69) (70)			V_{OCM} (V)(69)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
True Differential Signaling -1.3 V (Transmitter and Receiver) (71)	1.261	1.3	1.339	100	454	0.5	—	1.375(72)	247	—	360	0.9	1	1.1
True Differential Signaling -1.2 V (Receiver only)(71)	1.14	1.2	1.26	100	454	0.8	—	0.95	—	—	—	—	—	—
True Differential Signaling	1.045	1.1	1.155	100	454	0.8	—	0.95	—	—	—	—	—	—

continued...

(69) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(70) The specification is only applicable to default V_{OD} and pre-emphasis setting.

(71) The True Differential Signaling input buffer is supported on 1.05 V, 1.1 V, 1.2 V, and 1.3 V V_{CCIO_PIO} banks. The maximum input voltage driven into the True Differential Signaling input buffer must not exceed $V_{ICM(max)} + V_{ID(max)}/2$.

(72) The $V_{ICM(DC)}$ voltage must not exceed 1.2 V when on-chip differential termination (R_D OCT) is disabled with the use of external on-board termination.

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV)[69] [70]			V_{OCM} (V)[69]		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
-1.1 V (Receiver only)[71]														
True Differential Signaling -1.05 V (Receiver only)[71]	0.9975	1.05	1.1025	100	454	0.8	—	0.95	—	—	—	—	—	—
SLVS400	1.164	1.2	1.236	70	—	0.07	0.2	0.33	140	200	270	0.15	0.2	0.25
	1.067	1.1	1.133											

[69] R_L range: 90 ≤ R_L ≤ 110 Ω.

[70] The specification is only applicable to default V_{OD} and pre-emphasis setting.

MIPI D-PHY I/O Standards Specifications

Table 39. D-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
		Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
DPHY	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	—	0.55	0.74	—	1.1	1.2	1.3	–0.05	—	0.05
	Data rate > 1.5 Gbps to 3.5 Gbps								0.95	—	1.3			
	Data rate ≤ 1.5 Gbps	1.067	1.1	1.133					1	1.1	1.2			
	Data rate > 1.5 Gbps to 3.5 Gbps								0.85	—	1.2			

Table 40. D-Series FPGAs MIPI D-PHY High-Speed I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition	V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			V_{OD} (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
		Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
DPHY	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	0.07	—	0.07	—	0.33	0.14	0.2	0.27	0.15	0.2	0.25	–0.04	0.46
	Data rate > 1.5				0.04												

continued...

I/O Standard	Condition	V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			V_{OD} (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
		Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
	Gbps to 3.5 Gbps																
	Data rate ≤ 1.5 Gbps	1.067	1.1	1.133	0.07												
	Data rate > 1.5 Gbps to 3.5 Gbps				0.04												

Table 41. E-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition		V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
	Device Group	Data rate	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
DPHY	A	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	—	0.55	0.74	—	1.1	1.2	1.3	−0.05	—	0.05
		Data rate > 1.5 Gbps to 3.5 Gbps								0.95	—	1.3			
		Data rate ≤ 1.5 Gbps	1.067	1.1	1.133					1	1.1	1.2			

continued...

I/O Standard	Condition		V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
	Device Group	Data rate	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
		Data rate > 1.5 Gbps to 3.5 Gbps								0.85	—	1.2			
	B	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	—	0.55	0.74	—	1.1	1.2	1.3	-0.05	—	0.05
		Data rate > 1.5 Gbps to 2.5 Gbps								0.95	—	1.3			
		Data rate ≤ 1.5 Gbps	1.067	1.1	1.133					1	1.1	1.2			
		Data rate > 1.5 Gbps to 2.5 Gbps								0.85	—	1.2			

Table 42. E-Series FPGAs MIPI D-PHY High-Speed I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition		V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			V_{OD} (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
	Device Group	Data Rate	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
DPHY	A	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	0.07	—	0.07	—	0.33	0.14	0.2	0.27	0.15	0.2	0.25	−0.04	0.46
		Data rate > 1.5 Gbps to 3.5 Gbps				0.04												
		Data rate ≤ 1.5 Gbps	1.067	1.1	1.133	0.07												
		Data rate > 1.5 Gbps to 3.5 Gbps				0.04												
	B	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	0.07	—	0.07	—	0.33	0.14	0.2	0.27	0.15	0.2	0.25	−0.04	0.46
		Data rate > 1.5				0.04												

continued...

I/O Standard	Condition		V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			V_{OD} (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
	Device Group	Data Rate	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
		Gbps to 2.5 Gbps																
		Data rate ≤ 1.5 Gbps	1.067	1.1	1.133	0.07												
		Data rate > 1.5 Gbps to 2.5 Gbps				0.04												

HVIO I/O Standard Specifications

Related Information

Recommended Operating Conditions on page 19

HVIO Single-Ended I/O Standards Specifications

Table 43. HVIO Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_HVIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)(73)	V_{OH} (V)(73)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min
1.8 V LVCMOS 1.8 V LVTTL	1.746	1.8	1.854	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45
2.5 V LVCMOS	2.425	2.5	2.575	—	0.7	1.7	—	0.4	2

continued...

(73) Applicable to test condition of I_{OH} and I_{OL} at 3 mA.

I/O Standard	V_{CCIO_HVIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)[73]	V_{OH} (V)[73]
	Min	Typ	Max	Min	Max	Min	Max	Max	Min
2.5 V LVTTL									
3.3 V LVCMOS 3.3 V LVTTL	3.201	3.3	3.399	—	0.8	2	—	0.4	2.4

HPS and SDM I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_HPS} or V_{CCIO_SDM} values. For maximum voltage values, use the maximum V_{CCIO_HPS} or V_{CCIO_SDM} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general-purpose I/O standards.

Related Information

Recommended Operating Conditions on page 19

[73] Applicable to test condition of I_{OH} and I_{OL} at 3 mA.

HPS and SDM Single-Ended I/O Standards Specifications

Table 44. HPS and SDM Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_HPS}, V_{CCIO_SDM} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)(74)	I_{OH} (mA)(74)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min	Max	Min
1.8 V LVCMOS	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO_HPS}, 0.35 × V_{CCIO_SDM}	0.65 × V_{CCIO_HPS}, 0.65 × V_{CCIO_SDM}	V_{CCIO_HPS} + 0.3, V_{CCIO_SDM} + 0.3	0.4	V_{CCIO_HPS} – 0.4, V_{CCIO_SDM} – 0.4	8	–8

Switching Characteristics

This section provides the performance characteristics of core and periphery blocks.

Core Performance Specifications

Clock Tree Specifications

Table 45. D-Series FPGAs Clock Tree Performance Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Performance		Unit
	–1V, –2V	–3V	
Programmable clock routing	1,000	780	MHz

(74) To meet the I_{OH} and I_{OL} specifications, you must set the current strength settings accordingly. For example, to meet the 1.8 V LVCMOS specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OH} and I_{OL} specifications in the data sheet.

Table 46. E-Series FPGAs Clock Tree Performance Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Performance					Unit
	–1V, –2V, –2E	–3V	–4S	–5S	–6S, –6X	
Programmable clock routing	1,000	780	850	710	554	MHz

I/O PLL Specifications

Table 47. D-Series FPGAs I/O PLL Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency source from core clock input and reference clock input	–1V	10	—	1,100(75)	MHz
		–2V	10	—	1,000(75)	MHz
		–3V	10	—	780(75)	MHz
	Input clock frequency source from I/O clock input	–1V	10	—	800(75)	MHz
		–2V	10	—	717(75)	MHz
		–3V	10	—	625(75)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	I/O PLL VCO operating range	–1V	600	—	3,200	MHz
		–2V	600	—	3,200	MHz
		–3V	600	—	2,400	MHz
f_{CLBW}	I/O PLL closed-loop bandwidth	—	0.5	—	20	MHz

continued...

(75) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OUT}	Output frequency for internal clock (C counter)	–1V	—	—	1,100	MHz
		–2V	—	—	1,000	MHz
		–3V	—	—	780	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1V	—	—	800	MHz
		–2V	—	—	717	MHz
		–3V	—	—	625	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	f_{OUT_EXT} < 300 MHz	45	50	55	%
		f_{OUT_EXT} ≥ 300 MHz	40/45 (76)	50	55 (76)/60	%
t_{FCOMP} (77)	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for mgmt_clk	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	—	1	ms
t_{PLL_PSERR} (78)	Accuracy of PLL phase shift	—	—	—	±50	ps

continued...

(76) To achieve 5% duty cycle for f_{OUT_EXT} ≥ 300 MHz, you only can use `tx_outclk` port from the LVDS SERDES Intel FPGA IP. Refer to the *Clocking and PLL User Guide* for the detail design guidelines.

(77) Not applicable for fabric-feeding I/O PLL.

(78) PLL phase shift accuracy is 50 ps with the assumption of f_{VCO} = 1.6 GHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ}	Input clock cycle-to-cyle jitter	f_{REF} < 100 MHz (79)	—	—	750	ps (p-p)
		f_{REF} ≥ 100 MHz (79)	—	—	0.15	UI (p-p)
t_{REFPJ}	Reference phase jitter (rms)(80)	Carrier frequency: 100 MHz with integrated bandwidth of 10 kHz to 50 MHz	—	—	1.42	ps
t_{REFPN}	Reference phase noise(81) (80)	10 Hz	—	—	–90	dBc/Hz
		100 Hz	—	—	–100	dBc/Hz
		1 kHz	—	—	–110	dBc/Hz
		10 kHz	—	—	–120	dBc/Hz
		100 kHz	—	—	–130	dBc/Hz
		1 MHz	—	—	–138	dBc/Hz
		10 MHz	—	—	–142	dBc/Hz
		100 MHz	—	—	–144	dBc/Hz
t_{OUTPJ_DC} (77) (82)	Period jitter for dedicated clock output	f_{OUT} < 100 MHz (79)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (79)	—	—	175	ps (p-p)

continued...

(79) f_{REF} is f_{IN}/N, specification applies when N = 1.

(80) Requirement for DDR/LPDDR protocol and LVDS SERDES applications only.

(81) The phase noise numbers in this table are the maximum acceptable phase noise values measured at a carrier frequency of 100 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 100 MHz + (20 × log10 (f/100)).

(82) This jitter specification does not include the effect of spread-spectrum clock. The magnitude of jitter deterioration is largely depend on the spread-spectrum clock profile used. Refer to the *Clocking and PLL User Guide* for the recommended spread-spectrum clock profile.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTCCJ_DC} (77) (82)	Cycle-to-cycle jitter for dedicated clock output	f_{OUT} < 100 MHz (79)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (79)	—	—	175	ps (p-p)
t_{OUTPJ_IO} (83) (82)	Period jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (79)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (79)	—	—	600	ps (p-p)
t_{OUTCCJ_IO} (83) (82)	Cycle-to-cycle jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (79)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (79)	—	—	600	ps (p-p)
$t_{CASC\_OUTPJ\_DC}$ (77)	Period jitter for dedicated clock output in cascaded PLLs	f_{OUT} < 100 MHz (79)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (79)	—	—	175	ps (p-p)

Table 48. E-Series FPGAs I/O PLL Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency source from core clock input and reference clock input	–1V, –4S	10	—	1,100(84)	MHz
		–2V, –2E, –5S	10	—	1,000(84)	MHz
		–3V, –6S, –6X	10	—	780(84)	MHz
	Input clock frequency source from I/O clock input	–1V, –4S	10	—	800(84)	MHz
		–2V, –2E, –5S	10	—	717(84)	MHz
		–3V, –6S, –6X	10	—	625(84)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz

continued...

(83) External memory interface clock output jitter specifications use a different measurement method, which are available in the *Memory Output clock Jitter Specifications* table.

(84) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO}	I/O PLL VCO operating range	–1V, –4S	600	—	3,200	MHz
		–2V, –2E, –5S	600	—	3,200	MHz
		–3V, –6S, –6X	600	—	2,400	MHz
f_{CLBW}	I/O PLL closed-loop bandwidth	—	0.5	—	20	MHz
f_{OUT}	Output frequency for internal clock (C counter)	–1V,–4S	—	—	1,100	MHz
		–2V, –2E, –5S	—	—	1,000	MHz
		–3V, –6S, –6X	—	—	780	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1V, –4S	—	—	800	MHz
		–2V, –2E, –5S	—	—	717	MHz
		–3V, –6S, –6X	—	—	625	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	f_{OUT_EXT} < 300 MHz	45	50	55	%
		f_{OUT_EXT} ≥ 300 MHz	40/45 (85)	50	55 (85)/60	%
t_{FCOMP} (86)	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for mgmt_clk	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms

continued...

(85) To achieve 5% duty cycle for f_{OUT_EXT} ≥ 300 MHz, you only can use `tx_outclk` port from the LVDS SERDES Intel FPGA IP. Refer to the *Clocking and PLL User Guide* for the detail design guidelines.

(86) Not applicable for fabric-feeding I/O PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	—	1	ms
t_{PLL_PSERR} (87)	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ}	Input clock cycle-to-cyle jitter	f_{REF} < 100 MHz (88)	—	—	750	ps (p-p)
		f_{REF} ≥ 100 MHz (88)	—	—	0.15	UI (p-p)
t_{REFPJ}	Reference phase jitter (rms)(89)	Carrier frequency: 100 MHz with integrated bandwidth of 10 kHz to 50 MHz	—	—	1.42	ps
t_{REFPN}	Reference phase noise(90) (89)	10 Hz	—	—	–90	dBc/Hz
		100 Hz	—	—	–100	dBc/Hz
		1 kHz	—	—	–110	dBc/Hz
		10 kHz	—	—	–120	dBc/Hz
		100 kHz	—	—	–130	dBc/Hz
		1 MHz	—	—	–138	dBc/Hz

continued...

(87) PLL phase shift accuracy is 50 ps with the assumption of f_{VCO} = 1.6 GHz.

(88) f_{REF} is f_{IN}/N, specification applies when N = 1.

(89) Requirement for DDR/LPDDR protocol and LVDS SERDES applications only.

(90) The phase noise numbers in this table are the maximum acceptable phase noise values measured at a carrier frequency of 100 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 100 MHz + (20 × log10 (f/100)).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		10 MHz	—	—	–142	dBc/Hz
		100 MHz	—	—	–144	dBc/Hz
t_{OUTPJ_DC} (86) (91)	Period jitter for dedicated clock output	f_{OUT} < 100 MHz (88)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (88)	—	—	175	ps (p-p)
t_{OUTCCJ_DC} (86) (91)	Cycle-to-cycle jitter for dedicated clock output	f_{OUT} < 100 MHz (88)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (88)	—	—	175	ps (p-p)
t_{OUTPJ_IO} (92) (91)	Period jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (88)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (88)	—	—	600	ps (p-p)
t_{OUTCCJ_IO} (92) (91)	Cycle-to-cycle jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (88)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (88)	—	—	600	ps (p-p)
$t_{CASC\_OUTPJ\_DC}$ (86)	Period jitter for dedicated clock output in cascaded PLLs	f_{OUT} < 100 MHz (88)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (88)	—	—	175	ps (p-p)

Related Information

Memory Output Clock Jitter Specifications on page 84
Provides more information about the external memory interface clock output jitter specifications.

(91) This jitter specification does not include the effect of spread-spectrum clock. The magnitude of jitter deterioration is largely depend on the spread-spectrum clock profile used. Refer to the *Clocking and PLL User Guide* for the recommended spread-spectrum clock profile.

(92) External memory interface clock output jitter specifications use a different measurement method, which are available in the *Memory Output clock Jitter Specifications* table.

DSP Block Specifications

Table 49. D-Series FPGAs DSP Block Performance Specifications for Single DSP Block

For specification status, see the *Data Sheet Status* table

Mode	Performance			Unit
	–1V	–2V	–3V	
Fixed-point 18 × 19 multiplication mode	768	655	574	MHz
Fixed-point 27 × 27 multiplication mode	768	655	574	MHz
Fixed-point 18 × 19 multiplier adder mode	768	655	574	MHz
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode	768	655	574	MHz
Fixed-point six 9 × 9 multiplier adder mode	768	655	574	MHz
FP32 floating-point multiplication mode	637	492	431	MHz
FP32 floating-point adder or subtract mode	637	492	431	MHz
FP32 floating-point multiplier adder or subtract mode	637	492	431	MHz
FP32 floating-point multiplier accumulate mode	637	492	431	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	637	492	431	MHz
Sum/sub of two FP16 multiplications with FP32 (addition/subtraction)	637	492	431	MHz
Sum/sub of two FP16 multiplications with accumulation (addition/ subtraction)	637	492	431	MHz

continued...

Mode	Performance			Unit
	–1V	–2V	–3V	
Tensor floating-point mode	637	492	431	MHz
Tensor accumulation mode: fp32	637	492	431	MHz
Tensor fixed-point mode	768	655	574	MHz
INT16 complex multiplication mode	768	655	574	MHz

Table 50. D-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks

For specification status, see the *Data Sheet Status* table

Mode	Performance			Unit
	–1V	–2V	–3V	
Fixed-point 18 x 19 complex multiplication mode	768	655	574	MHz
Fixed-point 18 × 19 FIR systolic mode	768	655	574	MHz
FP32 floating-point complex multiplication	637	492	431	MHz
FP32 floating-point vector dot product	637	492	431	MHz
FP16 floating-point complex multiplication	637	492	431	MHz
FP16 floating-point vector dot product	637	492	431	MHz
Tensor floating-point cascade chain	637	492	431	MHz
Tensor fixed-point cascade chain	768	655	574	MHz

Table 51. E-Series FPGAs DSP Block Performance Specifications for Single DSP Block

For specification status, see the *Data Sheet Status* table

Mode	Performance						Unit
	–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
Fixed-point 18 × 19 multiplication mode	768	655	574	558	489	408	MHz
Fixed-point 27 × 27 multiplication mode	768	655	574	558	489	408	MHz
Fixed-point 18 × 19 multiplier adder mode	768	655	574	558	489	408	MHz
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode	768	655	574	558	489	408	MHz
Fixed-point six 9 × 9 multiplier adder mode	768	655	574	558	489	408	MHz
FP32 floating-point multiplication mode	637	492	431	418	367	306	MHz
FP32 floating-point adder or subtract mode	637	492	431	418	367	306	MHz
FP32 floating-point multiplier adder or subtract mode	637	492	431	418	367	306	MHz
FP32 floating-point multiplier accumulate mode	637	492	431	418	367	306	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	637	492	431	418	367	306	MHz

continued...

Mode	Performance						Unit
	–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
Sum/sub of two FP16 multiplications with FP32 (addition/ subtraction)	637	492	431	418	367	306	MHz
Sum/sub of two FP16 multiplications with accumulation (addition/ subtraction)	637	492	431	418	367	306	MHz
Tensor floating-point mode	637	492	431	418	367	306	MHz
Tensor accumulation mode: fp32	637	492	431	418	367	306	MHz
Tensor fixed-point mode	768	655	574	558	489	408	MHz
INT16 complex multiplication mode	768	655	574	558	489	408	MHz

Table 52. E-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks

For specification status, see the *Data Sheet Status* table

Mode	Performance						Unit
	–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
Fixed-point 18 x 19 complex multiplication mode	768	655	574	558	489	408	MHz
Fixed-point 18 × 19 FIR systolic mode	768	655	574	558	489	408	MHz
FP32 floating-point complex multiplication	637	492	431	418	367	306	MHz

continued...

Mode	Performance						Unit
	–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
FP32 floating-point vector dot product	637	492	431	418	367	306	MHz
FP16 floating-point complex multiplication	637	492	431	418	367	306	MHz
FP16 floating-point vector dot product	637	492	431	418	367	306	MHz
Tensor floating-point cascade chain	637	492	431	418	367	306	MHz
Tensor fixed-point cascade chain	768	655	574	558	489	408	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 53. D-Series FPGAs Memory Block Performance Specifications

For specification status, see the *Data Sheet Status* table

Memory	Mode	Performance			Unit
		–1V	–2V	–3V	
MLAB	Single-port RAM/ROM Simple dual-port RAM	1,000	782	667	MHz
	Simple dual-port RAM with read-during-write option	630	510	460	MHz
M20K block[93]	Single-port RAM/ROM	1000 (HS)	782 (HS)	667 (HS)	MHz

continued...

(93) For M20K block, timing/power optimization feature is available. The available options are high speed (HS) and low power (LP).

Memory	Mode	Performance			Unit
		–1V	–2V	–3V	
	Simple dual-port RAM	850 (LP)	664 (LP)	567 (LP)	
	Simple dual-port RAM, coherent read enabled	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	MHz
	Single-port RAM with the read-during-write option set to Old Data Simple dual-port RAM with the read-during-write option set to Old Data	800 (HS) 680 (LP)	640 (HS) 540 (LP)	560 (HS) 476 (LP)	MHz
	Simple dual-port RAM with ECC enabled, 512 × 32	600 (HS) 500 (LP)	480 (HS) 400 (LP)	420 (HS) 357 (LP)	MHz
	Simple dual-port RAM with ECC, optional pipeline registers enabled, 512 × 32	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	MHz
	Dual-port ROM True dual-port RAM	600 (HS)	500 (HS)	420 (HS)	MHz
	Simple quad-port RAM	600 (HS)	500 (HS)	420 (HS)	MHz

Table 54. E-Series FPGAs Memory Block Performance Specifications

For specification status, see the *Data Sheet Status* table

Memory	Mode	Performance						Unit
		–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
MLAB	Single-port RAM/ROM Simple dual-port RAM	850	750	510	600	469	400	MHz
	Simple dual-port RAM with read-during-write option	530	450	380	400	310	280	MHz

continued...

Memory	Mode	Performance						Unit
		–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
M20K block(94)	Single-port RAM/ROM Simple dual-port RAM	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	700 (HS) 595 (LP)	550 (HS) 470 (LP)	465 (HS) 400 (LP)	MHz
	Simple dual-port RAM, coherent read enabled	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	700 (HS) 595 (LP)	550 (HS) 470 (LP)	465 (HS) 400 (LP)	MHz
	Single-port RAM with the read-during-write option set to Old Data Simple dual-port RAM with the read-during-write option set to Old Data	800 (HS) 680 (LP)	640 (HS) 540 (LP)	560 (HS) 476 (LP)	560 (HS) 475 (LP)	440 (HS) 375 (LP)	370 (HS) 320 (LP)	MHz
	Simple dual-port RAM with ECC enabled, 512 × 32	600 (HS) 500 (LP)	480 (HS) 400 (LP)	420 (HS) 357 (LP)	420 (HS) 355 (LP)	330 (HS) 280 (LP)	280 (HS) 240 (LP)	MHz
	Simple dual-port RAM with ECC, optional pipeline registers enabled, 512 × 32	1000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	700 (HS) 595 (LP)	550 (HS) 470 (LP)	465 (HS) 400 (LP)	MHz
	Dual-port ROM True dual-port RAM	600 (HS)	500 (HS)	420 (HS)	445 (HS)	335 (HS)	280 (HS)	MHz
	Simple quad-port RAM	600 (HS)	500 (HS)	420 (HS)	445 (HS)	335 (HS)	280 (HS)	MHz

(94) For M20K block, timing/power optimization feature is available. The available options are high speed (HS) and low power (LP).

Local Temperature Sensor Specifications

Table 55. Local Temperature Sensor Specifications

For specification status, see the *Data Sheet Status* table

Description	Temperature Range	Accuracy	Sampling Rate[95]	Conversion Time
Local temperature sensor	–40 to 125°C[96]	±5°C	1 KSPS	< 1 ms

Related Information

Recommended Operating Conditions on page 19

Remote Temperature Diode Specifications

Note the following for the remote temperature diode specifications:

- The temperature diode characteristics in this table target for three-currents temperature sensing chip implementation. The characteristics can also apply to two-currents temperature sensing chip implementation.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

Table 56. Remote Temperature Diode Specifications (Core Fabric TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	170	µA
V_{bias}, voltage across diode	0.54	—	0.83	V
Series resistance	—	—	<5.5	Ω
Diode ideality factor	—	1.006[97]	—	—

(95) The read out is subject to the SDM mailbox activity status.

(96) Temperature range refers to junction temperature.

(97) When using lower injection current (two-currents) implementation, the ideality factor is 1.009.

Voltage Sensor Specifications

Table 57. Voltage Sensor Specifications

For specification status, see the *Data Sheet Status* table

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	7	—	Bit
Sampling rate(98)		—	—	1	KSPS
Input capacitance		—	—	40	pF
External reference voltage		1.125	1.25	1.375	V
Voltage sensor accuracy, V_{in} range: 0 V to 1.1 V(99)		—	—	±3.5	%
Unipolar input mode	Input signal range for Vsigp	—	—	1.35	V
	Common mode voltage on Vsign	—	—	0.25	V
	Input signal range for Vsigp – Vsign	—	—	1.1	V

Periphery Performance Specifications

This section describes the periphery performance, LVDS SERDES, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

(98) The read out is subject to the SDM mailbox activity status.

(99) For 1.2 V and 1.8 V voltage rails in channel 3, 4, 5, and 9, the accuracy is ±4.5%.

LVDS SERDES Specifications

Table 58. D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 4 and 8.

DDR registers support SERDES factor J = 1 and 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock frequency	f_{HSCLK_in} (input clock frequency) True Differential Signaling I/O Standards	Clock boost factor W = 1 to 40(100)	10	—	800	10	—	800	10	—	625	MHz
	f_{HSCLK_in} (input clock frequency) SLVS400 I/O Standards	Clock boost factor W = 1 to 40(100)	10	—	435.5	10	—	435.5	10	—	435.5	MHz
	f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards	Clock boost factor W = 1 to 40(100)	10	—	625	10	—	625	10	—	525	MHz

continued...

(100) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	f_{HSCLK_OUT} (output clock frequency) True Differential Signaling I/O Standards	—	—	—	800	—	—	800	—	—	625	MHz
Transmitter	True Differential Signaling I/O Standards - f_{HSDR} (data rate)(101)	SERDES factor J = 4 and 8(102) (103) (104)	600	—	1,600	600	—	1,600	600	—	1,250	Mbps
		SERDES factor J = 2, uses DDR registers	150	—	840(105)	150	—	(105)	150	—	(105)	Mbps
		SERDES factor J = 1, uses DDR registers	150	—	420(105)	150	—	(105)	150	—	(105)	Mbps

continued...

(101) Requires package skew compensation with PCB trace length.

(102) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(103) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(104) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(105) The maximum ideal data rate is the SERDES factor (J) × the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	t_x Jitter - True Differential Signaling I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	≤1,600 Mbps: 160 ≤1,434 Mbps: 200 ≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			≤1,600 Mbps: 160 ≤1,434 Mbps: 200 ≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			ps
	t_{DUTY} (106)	TX output clock duty cycle for True Differential Signaling I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} and t_{FALL} (103) (107)	True Differential Signaling I/O Standards	—	—	160	—	—	160	—	—	200	ps
	T_{CCS} (101) (106)	True Differential Signaling I/O Standards	—	—	330	—	—	330	—	—	330	ps
Receiver	True Differential Signaling I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(102) (103) (104)	600	—	1,600	600	—	1,600	600	—	1,250	Mbps

continued...

(106) Not applicable for DIVCLK = 1.

(107) This applies to default pre-emphasis and V_{OD} settings only.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SLVS400 I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(102) (103) (104)	600	—	871	600	—	871	600	—	871	Mbps
	f_{HSDR} (data rate) (without DPA)(101)	SERDES factor J = 4 and 8(102) (103) (104)	(104)	—	(108)	(104)	—	(108)	(104)	—	(108)	Mbps
		SERDES factor J = 2, uses DDR registers	(104)	—	(105)	(104)	—	(105)	(104)	—	(105)	Mbps
		SERDES factor J = 1, uses DDR registers	(104)	—	(105)	(104)	—	(105)	(104)	—	(105)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	≤10,000	—	—	≤10,000	—	—	≤10,000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling window	—	—	—	330	—	—	330	—	—	330	ps

(108) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Table 59. E-Series Device Group B FPGAs LVDS SERDES Specifications

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 4 and 8.

DDR registers support SERDES factor J = 1 and 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock frequency	f_{HSCLK_in} (input clock frequency) True Differential Signaling I/O Standards	Clock boost factor W = 1 to 40(109)	10	—	625	10	—	625	10	—	500	MHz
	f_{HSCLK_in} (input clock frequency) SLVS400 I/O Standards	Clock boost factor W = 1 to 40(109)	10	—	435.5	10	—	435.5	10	—	435.5	MHz
	f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards	Clock boost factor W = 1 to 40(109)	10	—	625	10	—	625	10	—	525	MHz
	f_{HSCLK_OUT} (output clock frequency)	—	—	—	625	—	—	625	—	—	500	MHz

continued...

(109) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	True Differential Signaling I/O Standards											
Transmitter	True Differential Signaling I/O Standards - f_{HSDR} (data rate)(110)	SERDES factor J = 4 and 8(111) (112) (113)	600	—	1,250	600	—	1,250	600	—	1,000	Mbps
		SERDES factor J = 2, uses DDR registers	150	—	840(114)	150	—	(114)	150	—	(114)	Mbps
		SERDES factor J = 1, uses DDR registers	150	—	420(114)	150	—	(114)	150	—	(114)	Mbps

continued...

(110) Requires package skew compensation with PCB trace length.

(111) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(112) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(113) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(114) The maximum ideal data rate is the SERDES factor (J) × the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	t_x Jitter - True Differential Signaling I/O Standards	Total jitter for data rate, 600 Mbps – 1.25 Gbps	≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			ps
	t_{DUTY} (115)	TX output clock duty cycle for True Differential Signaling I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} and t_{FALL} (112) (116)	True Differential Signaling I/O Standards	—	—	160	—	—	160	—	—	200	ps
	T_{CCS} (110) (115)	True Differential Signaling I/O Standards	—	—	330	—	—	330	—	—	330	ps
Receiver	True Differential Signaling I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(111) (112) (113)	600	—	1,250	600	—	1,250	600	—	1,000	Mbps

continued...

(115) Not applicable for DIVCLK = 1.

(116) This applies to default pre-emphasis and V_{OD} settings only.

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SLVS400 I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(111) (112) (113)	600	—	871	600	—	871	600	—	871	Mbps
	f_{HSDR} (data rate) (without DPA)(110)	SERDES factor J = 4 and 8(111) (112) (113)	(113)	—	(117)	(113)	—	(117)	(113)	—	(117)	Mbps
		SERDES factor J = 2, uses DDR registers	(113)	—	(114)	(113)	—	(114)	(113)	—	(114)	Mbps
		SERDES factor J = 1, uses DDR registers	(113)	—	(114)	(113)	—	(114)	(113)	—	(114)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	≤10,000	—	—	≤10,000	—	—	≤10,000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling window	—	—	—	330	—	—	330	—	—	330	ps

(117) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Table 60. DPA Lock Time Specifications

The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

For specification status, see the *Data Sheet Status* table

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(118)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	768
Parallel Rapid I/O	00001111	2	128	768
	10010000	4	64	768
Miscellaneous	10101010	8	32	768
	01010101	8	32	768

(118) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications

Figure 2. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

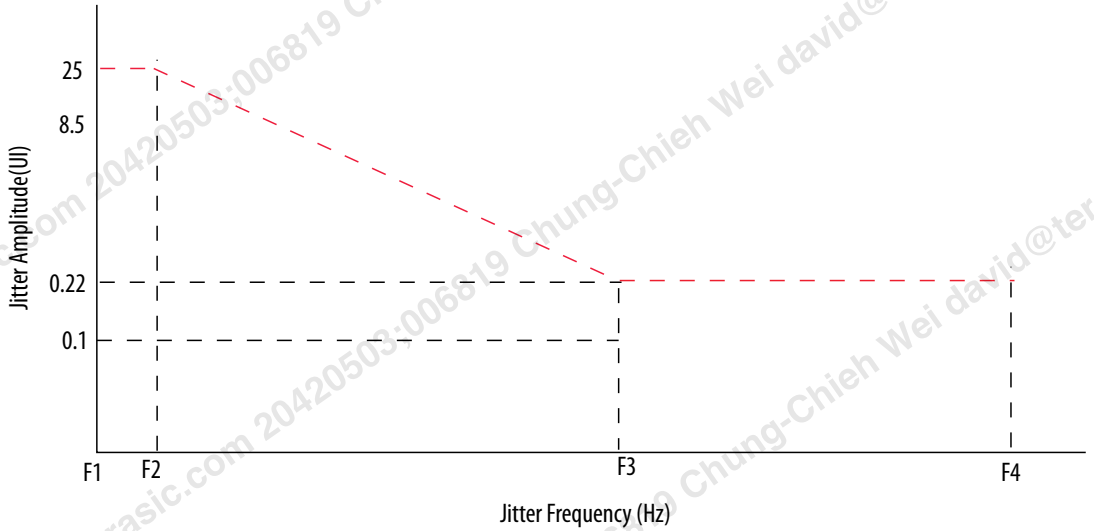
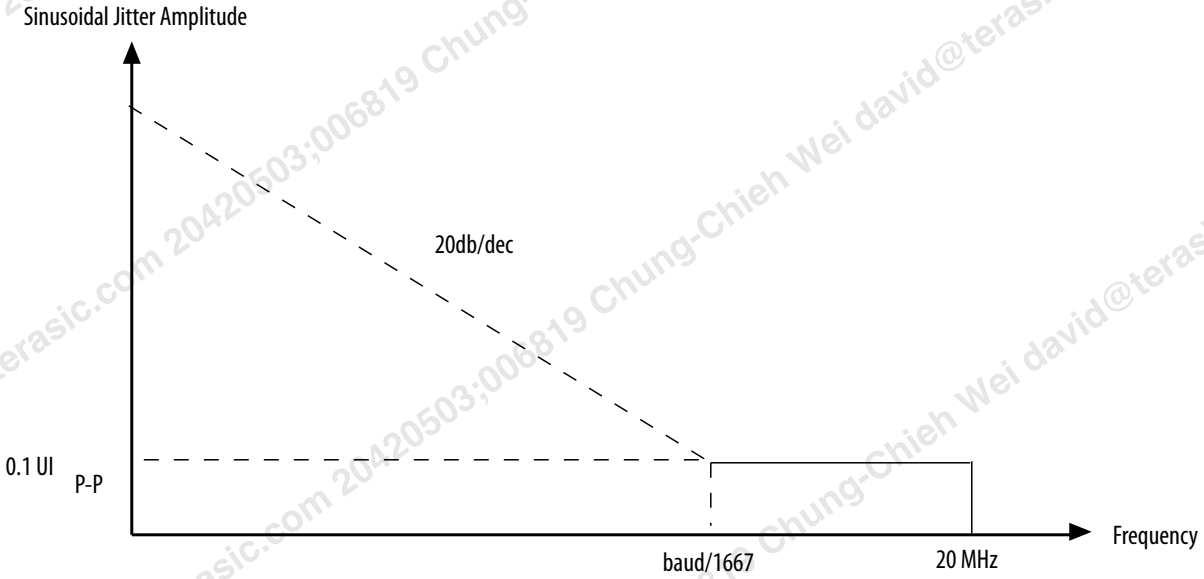


Table 61. LVDS SERDES Soft-CDR Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps

For specification status, see the *Data Sheet Status* table

Parameter	Jitter Frequency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25
F2	17,565	25
F3	1,493,000	0.22
F4	50,000,000	0.22

Figure 3. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



Memory Standards Supported

Table 62. D-Series FPGAs Memory Standards Supported

This table lists the overall capability of External Memory Interface supported by D-Series FPGAs. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	Hard memory controller	1,600
DDR5 SDRAM	Hard memory controller	2,000
LPDDR4 SDRAM	Hard memory controller	2,133
LPDDR5 SDRAM	Hard memory controller	2,133

continued...

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	HPS hard memory controller	1,600
DDR5 SDRAM	HPS hard memory controller	2,000
LPDDR4 SDRAM	HPS hard memory controller	2,133
LPDDR5 SDRAM	HPS hard memory controller	2,133
QDR-IV XP	Soft memory controller	1,066

Table 63. E-Series Device Group A FPGAs Memory Standards Supported

This table lists the overall capability of External Memory Interface supported by E-Series Device Group A. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	Hard memory controller	1,333
DDR5 SDRAM	Hard memory controller	1,800
LPDDR4 SDRAM	Hard memory controller	1,866
LPDDR5 SDRAM	Hard memory controller	1,866
DDR4 SDRAM	HPS hard memory controller	1,333
DDR5 SDRAM	HPS hard memory controller	1,800
LPDDR4 SDRAM	HPS hard memory controller	1,866
LPDDR5 SDRAM	HPS hard memory controller	1,866

Table 64. E-Series Device Group B FPGAs Memory Standards Supported

This table lists the overall capability of External Memory Interface supported by E-Series Device Group B. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	Hard memory controller	1,200
LPDDR4 SDRAM	Hard memory controller	1,333
LPDDR5 SDRAM	Hard memory controller	1,200
DDR4 SDRAM	HPS hard memory controller	1,200
LPDDR4 SDRAM	HPS hard memory controller	1,333
LPDDR5 SDRAM	HPS hard memory controller	1,200

Memory Output Clock Jitter Specifications

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory clock output jitter is within the JEDEC* specifications when the phase jitter (integration bandwidth 10 kHz to 50 MHz) of the input clock is not more than 20 ps peak-to-peak, or 1.42 ps RMS at $1e^{-12}$ BER and 1.22 ps at $1e^{-16}$ BER.

MIPI D-PHY Performance

Table 65. D-Series FPGAs MIPI D-PHY Performance

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MIPI D-PHY transmitter or receiver	High-speed interface, Hs	Long reference(119)	150	—	2,500	150	—	2,500	150	—	2,500	Mbps
		Short reference and standard reference(119)	150	—	3,500	150	—	3,500	150	—	3,500	Mbps
	Low-power interface, Lp	—	—	—	20	—	—	20	—	—	20	MHz

Table 66. E-Series FPGAs MIPI D-PHY Performance

For specification status, see the *Data Sheet Status* table

Parameter	Device Group	Symbol	Condition	–1, –4 Speed Grade			–2, –5 Speed Grade			–3, –6 Speed Grade			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MIPI D-PHY transmitter or receiver	A	High-speed interface, Hs	Long reference(120)	150	—	2,500	150	—	2,500	150	—	2,500	Mbps
			Short reference and	150	—	3,500	150	—	3,500	150	—	3,500	Mbps

continued...

(119) The long reference/standard reference/short reference is reference to the insertion loss condition from MIPI Alliance D-PHY specifications.

(120) The long reference/standard reference/short reference is reference to the insertion loss condition from MIPI Alliance D-PHY specifications.

Parameter	Device Group	Symbol	Condition	–1, –4 Speed Grade			–2, –5 Speed Grade			–3, –6 Speed Grade			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
			standard reference(120)										
		Low-power interface, Lp	—	—	—	20	—	—	20	—	—	20	MHz
MIPI D-PHY transmitter or receiver	B	High-speed interface, Hs	Short reference, standard reference, or long reference (120)	150	—	2,500	150	—	2,500	150	—	2,500	Mbps
		Low-power interface, Lp	—	—	—	20	—	—	20	—	—	20	MHz

GTS Transceiver Performance Specifications

GTS Transceiver Performance

Table 67. Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Transceiver Speed	Unit
Supported data rate for E-Series Device Group B (NRZ)	1 – 17.16	Gbps
Supported data rate for E-Series Device Group A (NRZ)	1 – 28.1	Gbps
Supported data rate for D-Series (NRZ)	1 – 28.1	Gbps

GTS Transceiver Reference Clock Specifications

Table 68. GTS Transceiver and System PLL Reference Clock Input Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
F_{REF}	Reference clock operating frequency	—	100[121]	—	380	MHz
$T_{REF-DUTY}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE/FALL}$	Rise and fall time (as percentage of period)	20% – 80%	—	—	0.15	T_{REF}
SSC	Spread-spectrum downspread	PCIe*	—	–5,000 to 0	—	ppm
$T_{REF-SINGLEEND-SKEW}$	Skew between REFCLKP and REFCLKN	—	—	—	50	ps
$Z_{REF-DIFF-DC}$	Reference clock differential input impedance – terminated mode	—	80	100	120	Ω
$V_{min-ABS}$	Absolute V_{min}	—	–0.15	—	—	V
$V_{max-ABS}$	Absolute V_{max}	—	—	—	0.85	V
$V_{REFIN-DIFF-AC}$	Input reference clock differential peak-to-peak voltage when AC-coupled on board	—	0.6	1.2	1.7	V
$V_{REFIN-IL-DC}$	Input reference clock input low voltage when DC-coupled on board	—	–0.15	0	0.15	V
$V_{REFIN-IH-DC}$	Input reference clock input high voltage when DC-coupled on board	—	0.66	0.7	0.85	V

continued...

(121) This value is 100 MHz for down spread spectrum clocking (SSC). This value can also be 25 MHz for HDMI rate of less than 1 Gbps.

Symbol	Description	Condition	Min	Typical	Max	Unit
$V_{REFIN-CM-AC}$	Input reference clock common-mode voltage when AC-coupled on board	—		Set on chip		V
$V_{REFIN-CM-DC}$	Input reference clock common-mode voltage when DC-coupled on board	—	0.255	0.35	0.5	V
PN_{REF}	Transmitter REFCLK phase noise (156.25 MHz)(122) (121)	10 kHz	—	—	–130	dBc/Hz
		100 kHz	—	—	–138	dBc/Hz
		500 kHz	—	—	–138	dBc/Hz
		3 MHz	—	—	–140	dBc/Hz
		10 MHz	—	—	–144	dBc/Hz
		20 MHz	—	—	–146	dBc/Hz
		1 GHz	—	—	–146	dBc/Hz
$V_{REFIN-RJ-RMS}$	RMS jitter integrated from 10 kHz – 20 MHz including spurs	—	—	—	522	fs
$V_{REFIN-PPM-ERROR}$	Reference clock frequency error	—	–350 + SSC	—	+350 + SSC	ppm
R_{COMP}	External resistor for calibration	—	—	499 ± 0.1%	—	Ω

Table 69. System PLL Reference Clock (Using HVIO) Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
F_{REF}	Clock input frequency	Powered by V_{CCIO_HVIO}	25	—	125	MHz
$T_{REF-DUTY}$	Clock input duty cycle		45	50	55	%

(122) To calculate the REFCLK phase noise requirement at frequencies other than 156.25 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 156.25 MHz + 20 × log(f/156.25 MHz).

Table 70. GTS Transceiver Reference Clock Output Driver Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
F_{REF_OUT}	Reference clock operating frequency	—	25	—	380	MHz
$T_{REF\text{-}DUTY\_OUT}$	Duty cycle	—	45	50	55	%
$T_{REF\text{-}RISE\_OUT/FALL\_OUT}$	Rise and fall time (as percentage of period)	20% – 80%	—	—	0.15	T_{REF}
$T_{REF\text{-}SINGLEEND\text{-}SKEW}$	Skew between REFCLKP and REFCLKN	—	—	—	50	ps
$Z_{REF\text{-}DIFF\text{-}DC\_OUT}$	Reference clock differential output impedance – terminated mode	—	80	100	120	Ω
$V_{REF\text{-}DIFF\text{-}AC\_OUT}$	Output reference clock differential peak to peak voltage when AC-coupled on board	—	0.9	1	1.1	V
$V_{REF\text{-}CM\text{-}OUT}$	Output reference clock common-mode	—	0.45	0.5	0.55	V

Transmitter Specifications

Table 71. Transmitter Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
On-chip termination	—	Transmitter differential on-chip termination resistors	—	80	90	120	Ω
Transmitter output eye specifications	$V_{TX\text{-}DIFF\text{-}PKPK}$	Back-porch transmit amplitude	—	300	—	1,050	mV
	$V_{TX\text{-}DEEMP\_STEP}$	Transmitter tap resolution	—	—	—	2	%

continued...

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	$D_{TX-PRE\_TAP\_2}$	Pre-cursor tap 2 de-emphasis	—	0	—	2.5	dB
	$D_{TX-PRE\_TAP\_1}$	Pre-cursor tap 1 de-emphasis	—	0	—	4.5	dB
	$D_{TX-POST\_TAP\_1}$	Post-cursor tap 1 de-emphasis	—	0	—	6.5	dB
	$T_{TX-SLEW}$	Rise/fall time at 20%–80%	—	10	—	20	ps
	T_{TX-DJ}	Transmitter deterministic jitter at 25 Gbps	—	—	—	0.15	UI_{pkpk}
	T_{TX-RJ}	Transmitter total peak-peak random jitter(123)	At BER of 10^{-12}	—	—	0.15	UI_{pkpk}
	T_{TX-TJ}	Transmitter total peak-peak jitter ($T_{TX-TJ} = T_{TX-DDJ} + T_{TX-PJ} + T_{TX-RJ}$)(123)(124)	At BER of 10^{-12}	—	—	0.28	UI_{pkpk}
Transmitter DC impedance	$Z_{TX-DIFF-DC}$	Transmitter output differential DC impedance with OCT 90 Ω mode while configured(125)	—	80	90	120	Ω
	$Z_{TX-CM-DC}$	Transmitter output common-mode DC impedance	—	20	22.5	30	Ω

continued...

(123) Assume a 1st order high-pass jitter measurement filter with a cutoff of $F_{BAUD}/F_{GPLL} = N_{GPLL}$, where N_{GPLL} is the ratio of the 3 dB cutoff frequency to the data rate, with typical value of 1,667.

(124) The maximum TJ value is slightly less than the sum of DDJ + PJ + RJ to take into consideration of the worst case probability, where both deterministic and random jitter component might present at the same time.

(125) TX pins are driven to 0 V before configuration.

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
Transmitter return loss	$Z_{RL-DIFF-DC}$	Transmitter differential DC return loss	—	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Transmitter differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	—	–6	dB
	Z_{RL-CMN}	Transmitter common-mode return loss below 10 GHz	—	—	—	–6	dB
Electrical idle	$V_{TX-IDLE}$	Electrical idle output voltage	PCIe/ SATA/SAS/USB	—	—	20	mV
	$V_{CM-DELTA-SQUELCH}$	Maximum common-mode step entering/ exiting squelch mode		—	—	100	mV
	$T_{TX-IDLE-LATENCY}$	Latency entering/ exiting electrical idle		—	—	8	µs
Receiver detect	$V_{TX-RCV-DETECT}$	Receiver detect voltage change allowed during receiver detection	PCIe/ SATA/SAS/USB	—	—	600	mV
Lane-to-lane output skew	—	Lane-to-lane output skew	4 < Lane count ≤ 8	—	—	2 UI + 250 ps	ps
			Lane count ≤ 4	—	—	2 UI + 166 ps	ps

Receiver Specifications

Table 72. Receiver Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
On-chip termination	—	Receiver differential on-chip termination resistors	—	65	85	102	Ω
				80	100	120	Ω
Receiver input eye specifications	$V_{RX-DIFF-PKPK}$	Receiver input differential peak-to-peak voltage(126)	—	—	—	1,200	mV
	V_{RX-MAX}	Receiver input maximum voltage(127)	—	—	—	1	V
	V_{RX-MIN}	Receiver input minimum voltage(127)	—	–0.3	—	—	V
	$V_{RX-CM-DC}$	Receiver input DC common-mode voltage(128)	When squelch detector is not enabled	0	—	700	mV
			When squelch detector is enabled	200	—	300	mV
	T_{RX-RJ}	Receiver input random jitter	At BER of 10^{-12}	—	—	0.15	UI_{pkpk}

continued...

(126) This is supported when the receiver is powered and configured, powered and unconfigured, or unpowered.

(127) V_{RX_MAX} and V_{RX_MIN} are before and after configuration.

(128) The specified common-mode range is supported when the receiver is powered and configured, powered and unconfigured, or unpowered. This specification is also supported before mode configuration. If squelch detect is used, receiver DC input common-mode voltage should be within 200 mV to 300 mV. Otherwise, use AC coupling capacitors on board.

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	T_{RX-PJ}	Receiver input periodic jitter (at high frequency(129))	—	—	—	0.05	UI_{pkpk}
Insertion loss specification	$I_{INS-LOSS-28Gb/s\_BER10-15}$	Insertion loss at Nyquist frequency ($F_{BAUD}/2$)(130)	At BER of 10^{-15}	—	—	–27	dB
	$I_{INS-LOSS-28Gb/s\_BER10-12}$		At BER of 10^{-12}	—	—	–30	dB
	$I_{INS-LOSS-17Gb/s\_BER10-12}$	Insertion loss at Nyquist frequency ($F_{BAUD}/2$)(130)	At BER of 10^{-12}	—	—	–30	dB
Receiver return loss	$Z_{RL-DIFF-DC}$	Receiver differential DC return loss	—	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Receiver differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	—	–6	dB
	Z_{RL-CM}	Receiver common-mode return loss below 10 GHz	—	—	—	–6	dB
Receiver DC impedance	$R_{DIFF-DC}$	Receiver differential DC impedance	85 Ω on-chip termination	65	85	102	Ω
			100 Ω on-chip termination	80	100	120	Ω
	R_{CM-DC}	Receiver common-mode DC impedance	—	20	25	30	Ω
Receiver signal detection(131)	$V_{IDLE-THRESH}$	Receiver signal detect input voltage threshold	—	75	120	175	mV

(129) High frequency is defined as frequencies beyond the CDR loop bandwidth (typically $F_{BAUD}/1,667$).

(130) COM compliant package and channel.

Electrical Compliance

Table 73. Electrical Compliance List

For specification status, see the *Data Sheet Status* table

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
XFP MSA	XFI	10.3125	10.3125
IEEE 802.3ba-2010	XLPPI	10.3125	10.3125
Serial-GMII Specification V1.7	1GE SGMII	1.25	1.25
IEEE 802.3ba	XLAUI	10.3125	10.3125
IEEE 802.3ba	CAUI-10	10.3125	10.3125
IEEE 802.3cd 109A/109B	25GAUI-C2C/C2M	—	1x25.78125
IEEE 802.3ap 2007	10GBASE-KR	10.3125	10.3125
IEEE 802.3by 111/110	25GBASE-KR/CR	—	25.78125
IEEE 803.3ap-2007 IEEE 802.3an-2006	1000BASE-KX/CX	1.25	1.25
CEI 4.0	CEI-11G SR/MR/LR	9.95 – 11.2	9.95 – 11.2
	CEI-6G SR/LR	4.976 – 6.375	4.976 – 6.375
G.709 G.sup56 G.sup43 G.sup58	OTU1	—	1.327451, 2.666
	OTU2	—	10.709, 11.049, 11.270
	OTU2e	—	11.095
	OTU2f	—	11.317, 11.846, 12.639
	OTU4 OTL4.4	—	4x27.952493
	OTU4 OTLC.4	—	4x28.076177

continued...

(131) Receiver signal detection values in this table are applicable to PCIe and similar standards, such as SATA, where a clock pattern like PCIe EIEOS 500 MHz clock pattern is used.

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
PCIe BASE 4.0 PIPE 4.4.1	PCIe 3.0 , PCIe 4.0	8, 16(132)	8, 16
SMPTE 259M	SDI SD	0.27	0.27
SMPTE 292M	SDI HD	1.485/1.483	1.485/1.483
SMPTE ST 424	SDI 3G	2.97/2.967	2.97/2.967
SMPTE ST 2081	SDI 6G	5.94/5.934	5.94/5.934
SMPTE ST 2082	SDI 12G	11.88/11.868	11.88/11.868
CPRI V7.0	CPRI	1.2288	1.2288
		2.4576	2.4576
		3.072	3.072
		4.9152	4.9152
		6.144	6.144
		8.1101	8.1101
		9.8304	9.8304
		10.1376	10.1376
		—	24.33024
JESD204B	JESD204B	up to 17.16	up to 19.66
JESD204C	JESD204C	up to 17.16	up to 28.1
DP 2.0	DisplayPort 1.4	1.62	1.62
		2.7	2.7
		5.4	5.4
		8.1	8.1

continued...

(132) PCIe 4.0 is supported for –4S (V_{CC} = 0.8 V) devices only.

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
	DisplayPort 2.0	10	10
		13.5	13.5
		—	20
FC-PI-2	Fiber Channel	1.0625	1.0625
		2.125	2.125
FC-PI-5		4.25	4.25
		8.5	8.5
10GFC		10.518	10.518
FC-PI-5		14.025	14.025
FC-PI-6		—	28.05
		—	4x28.05
Serial ATA revision 3.5a T10/BSR INCITS 519	Sata Gen 3	1.5 – 6	1.5 – 6
	SAS	1.5 – 12.0	1.5 – 22.5
G.984	GPON/EPON	—	1.244, 1.250, 2.488, 9.952, 10.313, 25
CEI-6G-SR	Interlaken	6.25	6.25
CEI-11G-SR		10.3125	10.3125
CEI-11G-SR+		12.5	12.5
OIF-28G MR (OIF-CEI3.0)		—	25.78125
HDMI 1.4	HDMI	3.4	3.4
HDMI 2.0		6	6
HDMI 2.1		up to 12	up to 12
SLVS-EC Specification Version 1.0	SLVS-EC RX	2.376	2.376
SLVS-EC Specification Version 2.0		5	5
SFF-8402	SFP+	9.95 – 11.2	9.95 – 11.2

continued...

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
SFF-8431 4.1			
SFF-8431 Rev 4.1			
SFF-8418			
USB 3.1, USB 3.2	USB 3.1 Gen 1	5	5
	USB 3.2 Gen 2 (133)	—	10 (133)
RapidIO™ Interconnect Specification	SRIO	2 – 16	2 – 16

HPS Performance Specifications

This section provides hard processor system (HPS) specifications and timing.

HPS Clock Performance

Table 74. D-Series SoC Maximum HPS Clock Frequencies

For specification status, see the *Data Sheet Status* table

Performance	V_{CCL_HPS} (V)(134)	Cortex-A55 Core Frequency (MHz)	Cortex-A76 Core Frequency (MHz)	DSU (DynamIQ Shared Unit) Frequency (MHz)	L3 Frequency (MHz) (l3_main_free_clk)	DDR4/LPDDR4/ DDR5/LPDDR5 Clock (MHz)
–1 speed grade	SmartVID	1,500	1,800	1,200	400	Refer to the *Memory Standards Supported* table.
–2 speed grade	SmartVID	1,333	1,600	1,066	400	
–3 speed grade	SmartVID	1,250	1,400	933	400	

(133) Gen 2 is supported using transceiver PMA only, with soft PIPE PCS and USB 3.1 controller in core fabric.

(134) V_{CCL_HPS} refers to $V_{CCL\_HPS\_CORE0\_CORE1}$ for HPS Cortex-A55 core 0 and core 1 power rail, $V_{CCL\_HPS\_CORE2}$ for HPS Cortex-A76 core 2 power rail, and $V_{CCL\_HPS\_CORE3}$ for HPS Cortex-A76 core 3 power rail.

Table 75. E-Series SoC Maximum HPS Clock Frequencies

For specification status, see the *Data Sheet Status* table

Performance	V_{CCL_HPS} (V)(135)	Cortex-A55 Core Frequency (MHz)	Cortex-A76 Core Frequency (MHz)	DSU (DynamIQ Shared Unit) Frequency (MHz)	L3 Frequency (MHz) (l3_main_free_clk)	DDR4/LPDDR4/ DDR5/LPDDR5 Clock (MHz)
–1 speed grade	SmartVID	1,500	1,800	1,200	400	Refer to the *Memory Standards Supported* table.
–2 speed grade	SmartVID	1,333	1,600	1,066	400	
–3 speed grade	SmartVID	1,250	1,400	933	400	
–4 speed grade	Fixed: 0.8	1,250	1,400	933	400	
–5 speed grade	Fixed: 0.78	800	800	533	400	
–6 speed grade	Fixed: 0.75	800	800	533	400	

Related Information

- HPS Power Supply Operating Conditions on page 31
- Memory Standards Supported on page 82

HPS Internal Oscillator Frequency

Table 76. HPS Internal Oscillator Frequency

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Internal oscillator frequency	150	300	400	MHz

(135) V_{CCL_HPS} refers to $V_{CCL\_HPS\_CORE0\_CORE1}$ for HPS Cortex-A55 core 0 and core 1 power rail, $V_{CCL\_HPS\_CORE2}$ for HPS Cortex-A76 core 2 power rail, and $V_{CCL\_HPS\_CORE3}$ for HPS Cortex-A76 core 3 power rail.

HPS PLL Specifications

Table 77. HPS PLL Input Requirements

The main HPS PLL receives its clock signals from the HPS_OSC_CLK pin. Refer to the *Pin Connection Guidelines* of this device for information about assigning this pin.

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	—	—	50	ppm
Clock input duty cycle	45	50	55	%

Table 78. HPS PLL Performance

For specification status, see the *Data Sheet Status* table

Description	Min	Max	Unit
Main PLL VCO output	—	4,000	MHz
Peripheral PLL VCO output	—	4,000	MHz
h2f_user0_clk(136)	—	500	MHz
h2f_user1_clk(136)	—	500	MHz

HPS Cold Reset

Table 79. HPS Cold Reset

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
t_{RST0}	Minimum time for HPS_COLD_nRESET asserted(137)	3	—	ms

(136) The HPS PLL provides this clock to the FPGA fabric.

(137) HPS_COLD_nRESET may be ignored if HPS is not running or if the device is being configured.

HPS SPI Timing Characteristics

Table 80. SPI Master Timing Requirements

You can adjust the input delay timing by programming the `rx_sample_dly` register.

For specification status, see the *Data Sheet Status* table

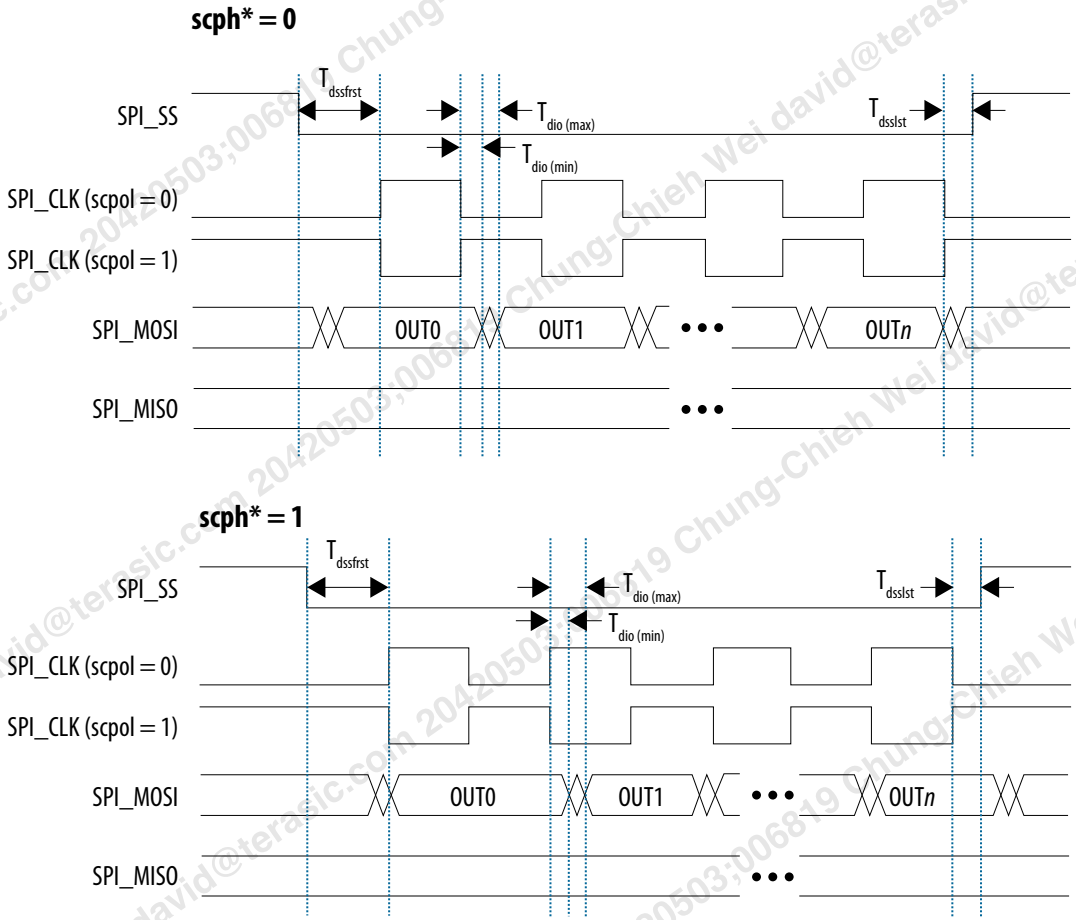
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	–3	—	2	ns
$T_{dssfrst}$ (138)	SPI_SS_N asserted to first SPIM_CLK edge	$(1.5 \times T_{clk}) - 2$	—	—	ns
T_{dsslst} (138)	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{clk} - 2$	—	—	ns
T_{su} (139)	SPIM_MISO setup time with respect to SPIM_CLK capture edge	5.0 – (`rx_sample_dly` x $T_{spi\_ref\_clk}$)(140)	—	—	ns
T_h (139)	Input hold in respect to SPIM_CLK capture edge	1.3 + (`rx_sample_dly` x $T_{spi\_ref\_clk}$)(140)	—	—	ns

(138) SPI_SS_N behavior differs depending on Motorola SPI protocols, Texas Instruments Synchronous Serial Protocols, or National Semiconductor Microwire operational mode.

(139) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for Texas Instruments Synchronous Serial Protocols, the capture edge is the falling edge; for National Semiconductor Microwire, the capture edge is the rising edge.

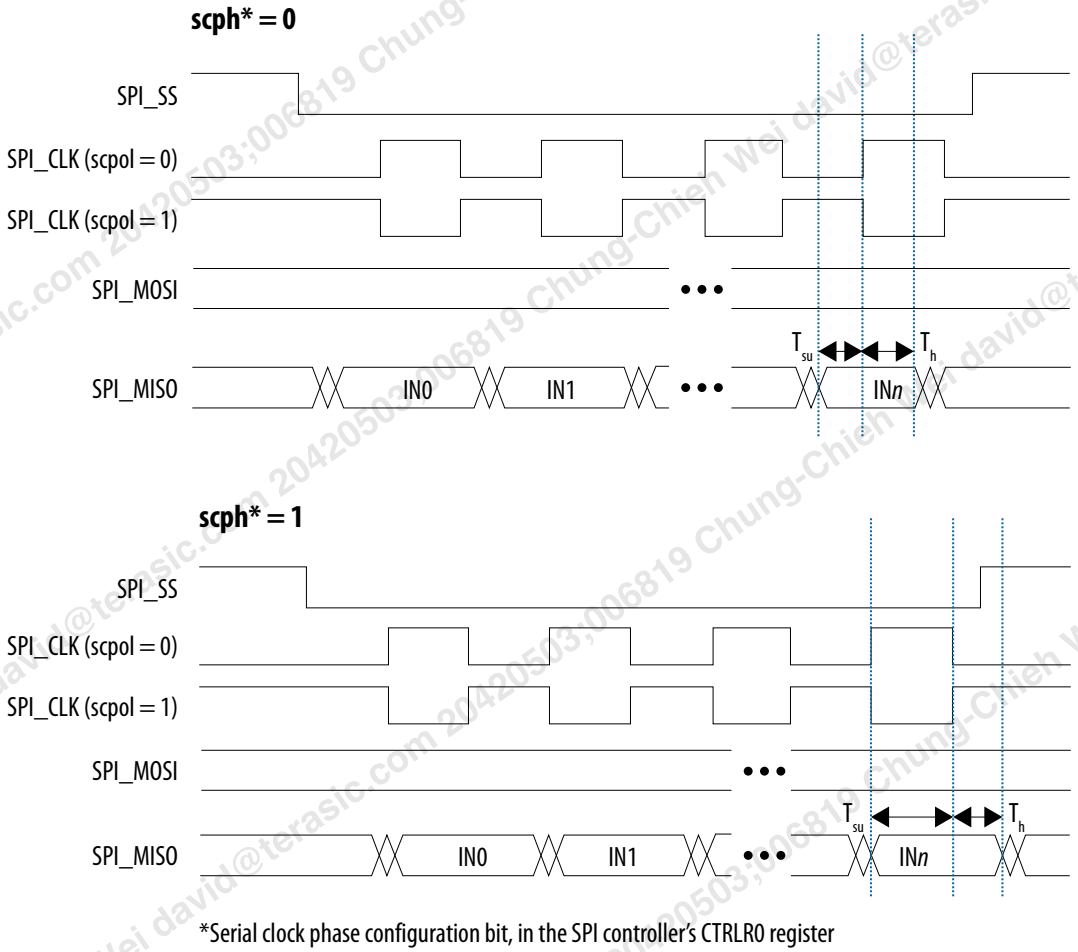
(140) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi\_ref\_clk}$ steps).

Figure 4. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 5. SPI Master Input Timing Diagram



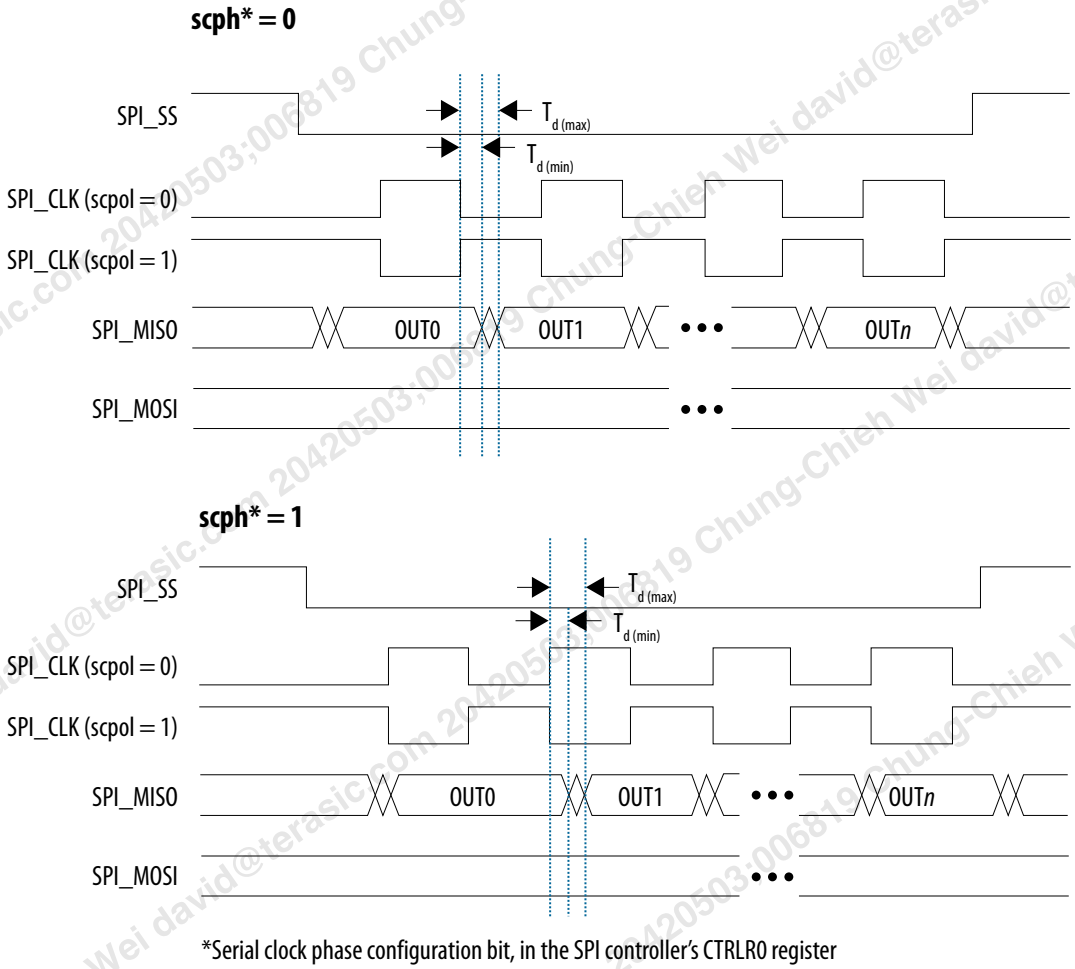
*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Table 81. SPI Slave Timing Requirements

For specification status, see the *Data Sheet Status* table

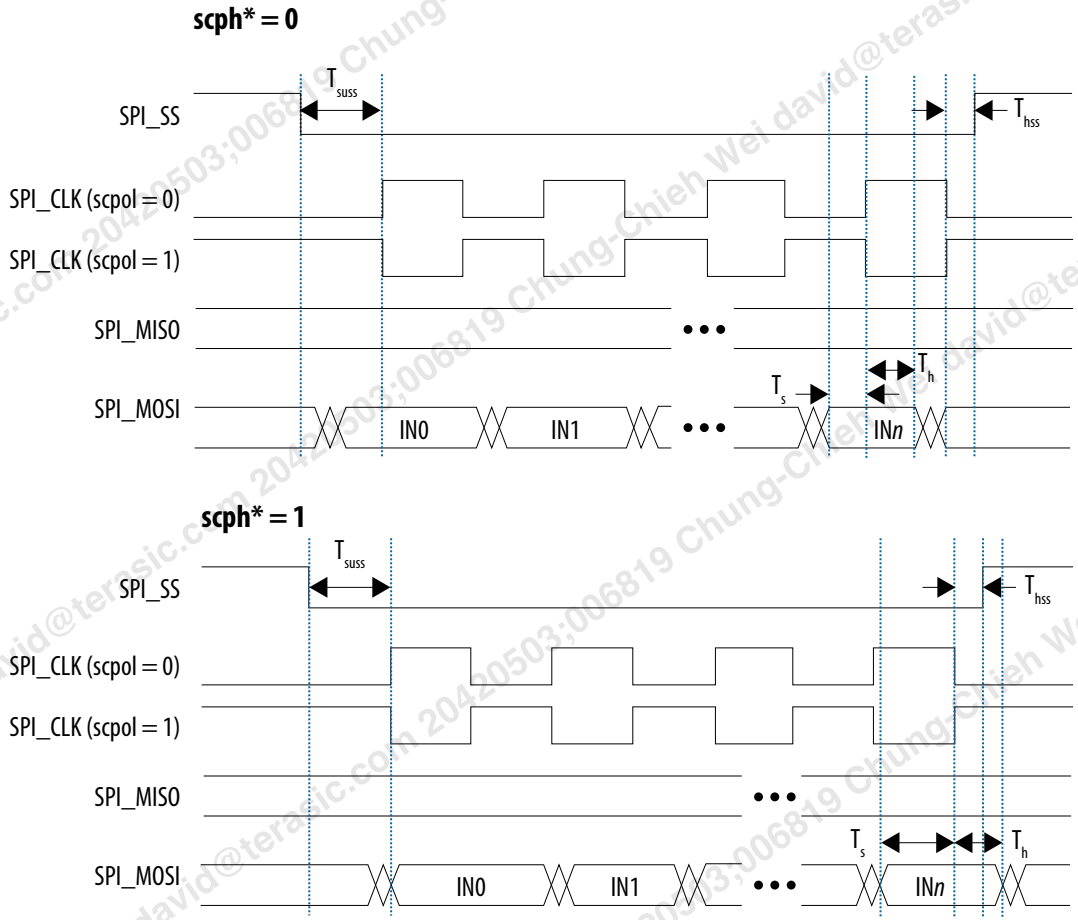
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	30	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T_{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T_h	Master-out slave-in (MOSI) hold time	9	—	—	ns
T_{suss}	SPI_SS_N asserted to first SPIM_CLK edge	$T_{spi\_ref\_clk} + 4.2$	—	—	ns
T_{hss}	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} + 4.2$	—	—	ns

Figure 6. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 7. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

HPS SD/eMMC Timing Characteristics

Table 82. HPS Secure Digital (SD)/Embedded MultiMediaCard (eMMC) Timing Requirements

Supports SD devices up to V6.1. Supports SDIO devices up to V4.1. Supports SD/eMMC devices up to V5.1.

These timings apply to SD, MMC, and eMMC cards operating at 1.8 V.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{sdmmc_cclk}	SD SDMMC_CCLK clock period (Identification mode, 400 kHz)	2,500	—	—	ns
	SD SDMMC_CCLK clock period (SDR12, 25 MHz)	40	—	—	ns
	SD SDMMC_CCLK clock period (SDR25, 50 MHz)	20	—	—	ns
	SD SDMMC_CCLK clock period (SDR50, 100 MHz)	10	—	—	ns
	SD SDMMC_CCLK clock period (SDR104, <200 MHz)	5	—	—	ns
	SD SDMMC_CCLK clock period (DDR50, 50 MHz)	20	—	—	ns
	eMMC SDMMC_CCLK clock period (Legacy, 25 MHz)	40	—	—	ns
	eMMC SDMMC_CCLK clock period (HS50 SDR, 50 MHz)	20	—	—	ns
	eMMC SDMMC_CCLK clock period (HS100 DDR, 100 MHz)	10	—	—	ns
	eMMC SDMMC_CCLK clock period (HS200 SDR, 200 MHz)	5	—	—	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
	eMMC SDMMC_CCLK clock period (HS400 DDR, 200 MHz)	5	—	—	ns
$T_{dutycycle}$	SDMMC_CCLK duty cycle	45	50	55	%
$T_{sdmmc\_cclk\_jitter}$	SDMMC_CCLK output jitter	—	—	2	%
T_{sdmmc_clk}	Internal reference clock before division by 4 (200 MHz)	5	—	—	ns

None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

Table 83. SD Input Timing (SDR104, SDR50, SD25, SDR12)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{is}	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR104)	1.4	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR50)	3	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR25)	6	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR12)	5	—	—	ns
T_{ih}	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR104)	0.8	—	—	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR50)	0.8	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR25)	2	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR12)	5	—	—	ns

Figure 8. SD Input (SDR104, SDR50, SD25, SDR12) Timing Diagram

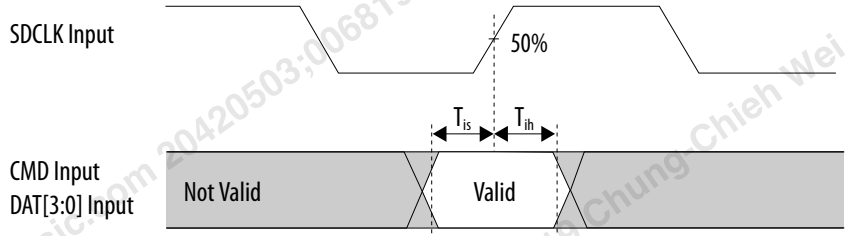


Table 84. SD Output Timing (SDR50, SDR25, SDR12)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{odly}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay (SDR50)	—	—	7.5	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] output delay (SDR25, SDR12)	—	—	14	ns
T_{ohld}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	1.5	—	—	ns

Figure 9. SD Output (SDR50, SDR25, SDR12) Timing Diagram

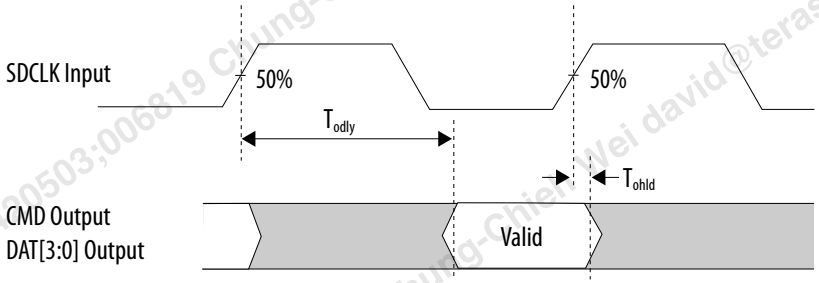


Table 85. SD Output Timing (SDR104)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{op}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{op}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	1,550	ps
T_{odw}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	3	—	—	ns

Figure 10. SD Output (SDR104) Timing Diagram

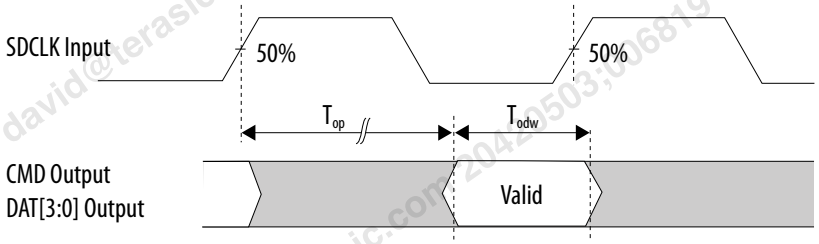


Table 86. SD Timing (DDR50)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	SDMMC_CMD input setup	6	—	—	ns
T_{ih}	SDMMC_CMD input hold	0.8	—	—	ns
T_{odly}	SDMMC_CMD output delay	—	—	13.7	ns
T_{oh}	SDMMC_CMD output hold	1.5	—	—	ns
T_{isu2x}	SDMMC_DATA[7:0] input setup	3	—	—	ns
T_{ih2x}	SDMMC_DATA[7:0] input hold	0.8	—	—	ns
T_{odly2x}	SDMMC_DATA[7:0] output delay	—	—	7	ns
T_{odly2x}	SDMMC_DATA[7:0] output hold	1.5	—	—	ns

Figure 11. SD (DDR50) Timing Diagram

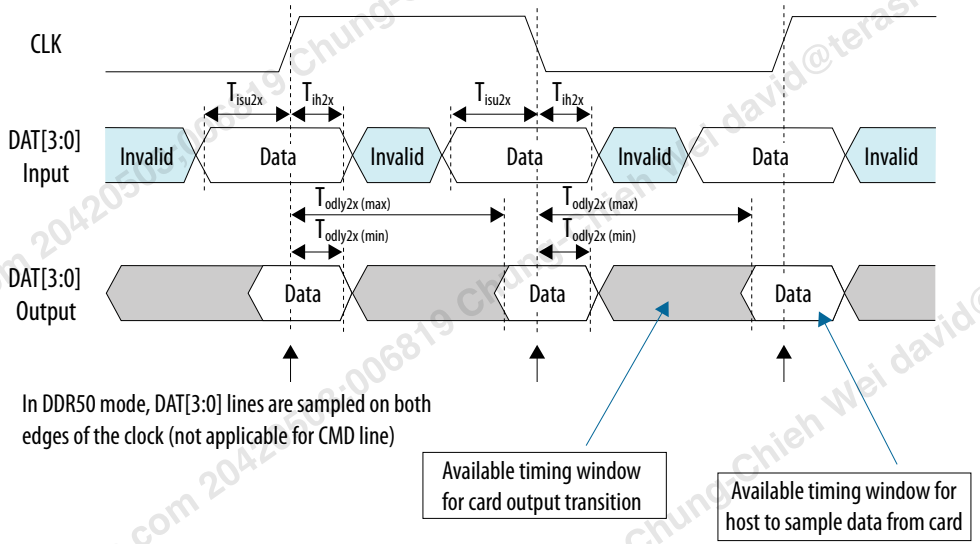


Table 87. eMMC Timing (Legacy, HS50 SDR)

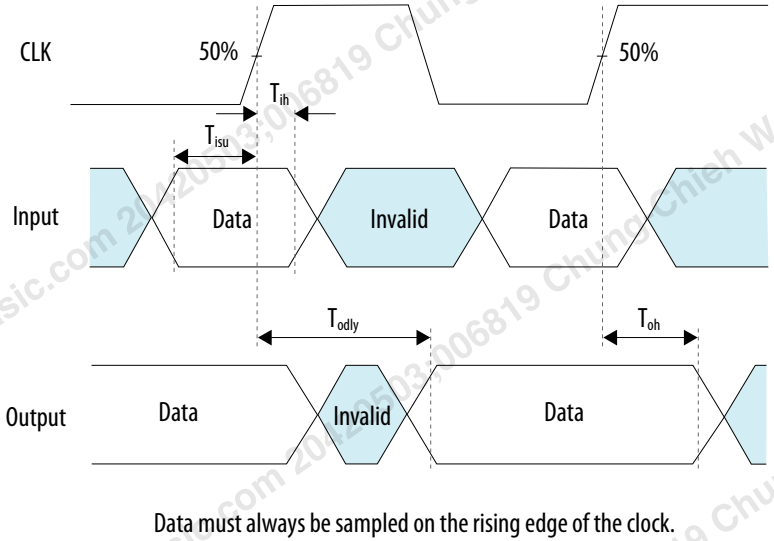
For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	EMMC_CMD_DATA input setup (Legacy)	3	—	—	ns
	EMMC_CMD_DATA input setup (HS50 SDR)	3	—	—	ns
T_{ih}	EMMC_CMD DATA_input hold (Legacy)	3	—	—	ns
	EMMC_CMD DATA_input hold (HS50 SDR)	3	—	—	ns
T_{odly}	EMMC_CMD_DATA output delay (Legacy)	—	—	13.7	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
	EMMC_CMD_DATA output delay (HS50 SDR)	—	—	13.7	ns
T_{oh}	EMMC_CMD_DATA output hold (Legacy)	8.3	—	—	ns
	EMMC_CMD DATA_output hold (HS50 SDR)	2.5	—	—	ns

Figure 12. eMMC (Legacy, HS50 SDR) Timing Diagram



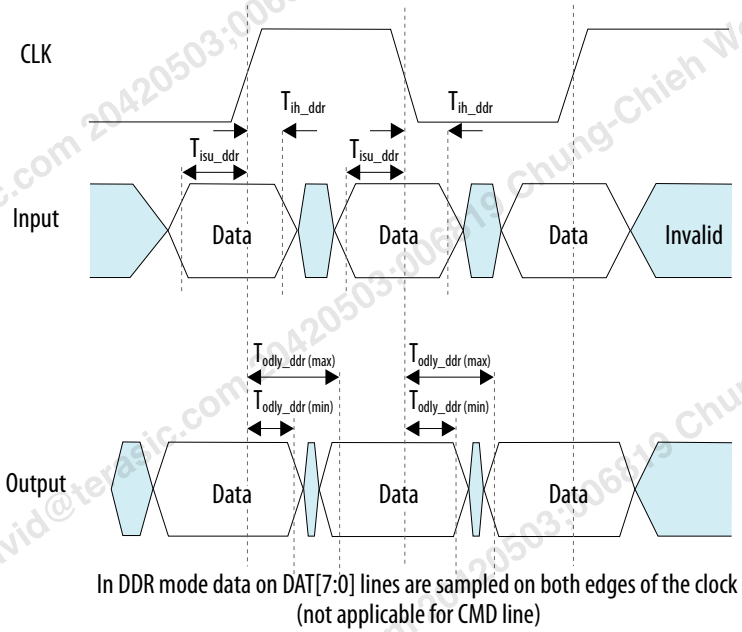
Data must always be sampled on the rising edge of the clock.

Table 88. eMMC Timing (HS100 DDR)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu_ddr}	EMMC_CMD_DATA input setup	2.5	—	—	ns
T_{ih_ddr}	EMMC_CMD DATA_input hold	2.5	—	—	ns
T_{odly_ddr}	EMMC_CMD_DATA output delay (max=delay, min=hold)	1.5	—	7	ns

Figure 13. eMMC (HS100 DDR) Timing Diagram



In DDR mode data on DAT[7:0] lines are sampled on both edges of the clock (not applicable for CMD line)

Table 89. eMMC Timing (HS200 SDR)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	EMMC_CMD_DATA input setup	1.4	—	—	ns
T_{ih}	EMMC_CMD DATA_input hold	0.8	—	—	ns
T_{ph}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{ph}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	1,550	ps
T_{vw}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	3	—	—	ns

Figure 14. eMMC Input (HS200 SDR) Timing Diagram

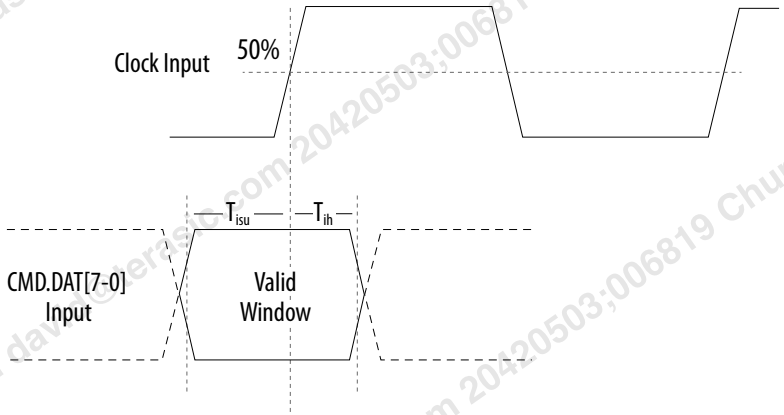


Figure 15. eMMC Output (HS200 SDR) Timing Diagram

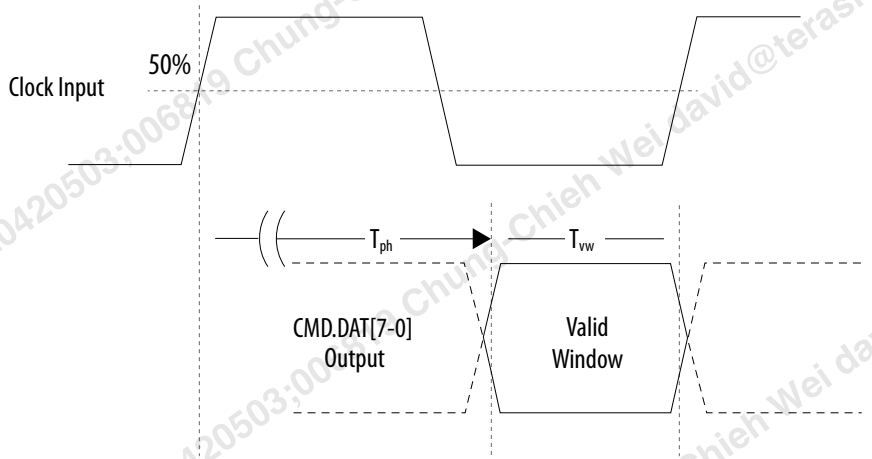


Table 90. eMMC Timing (HS400 DDR)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu_ddr}	EMMC_CMD_DATA input setup	0.4	—	—	ns
T_{ih_ddr}	EMMC_CMD DATA_input hold	0.4	—	—	ns
T_{rq}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{rq}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	200	ps
T_{rqh}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	2	—	—	ns

Figure 16. eMMC Input (HS400 DDR) Timing Diagram

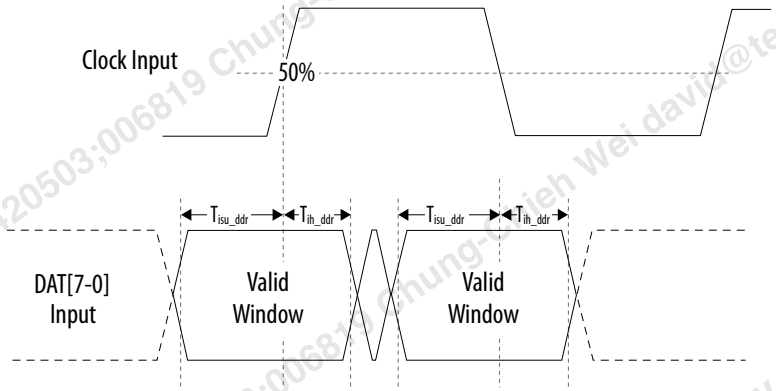
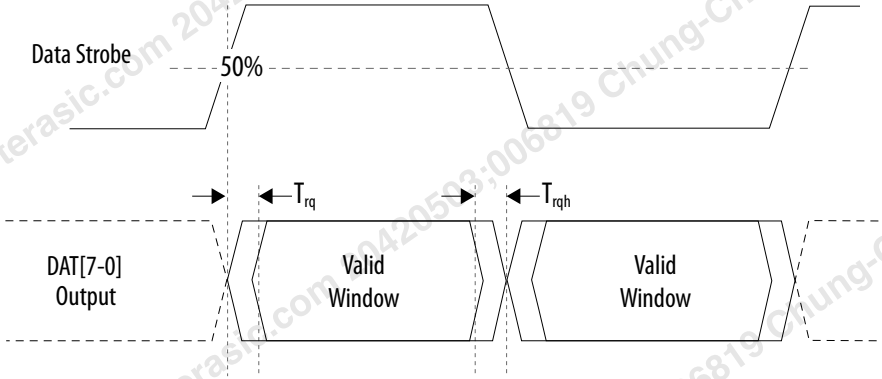


Figure 17. eMMC Output (HS400 DDR) Timing Diagram



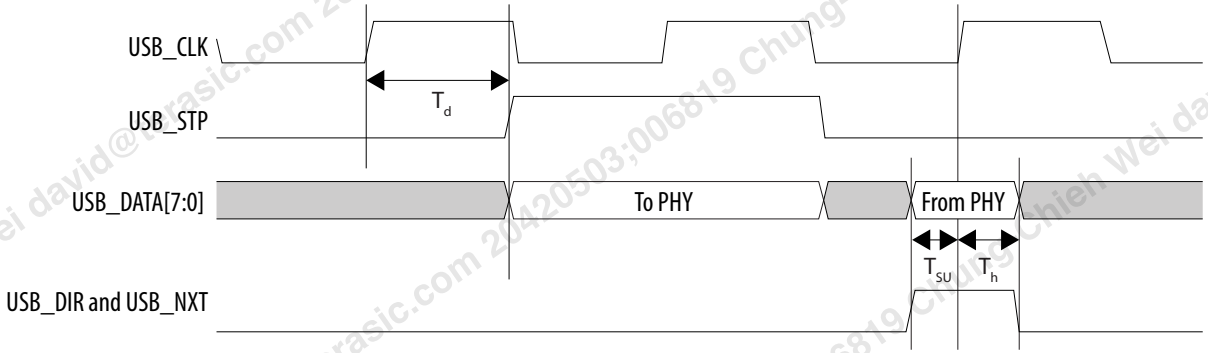
HPS USB 2.0 Timing Characteristics

Table 91. HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{usb_clk}	USB_CLK clock period (60 MHz)	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns

Figure 18. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

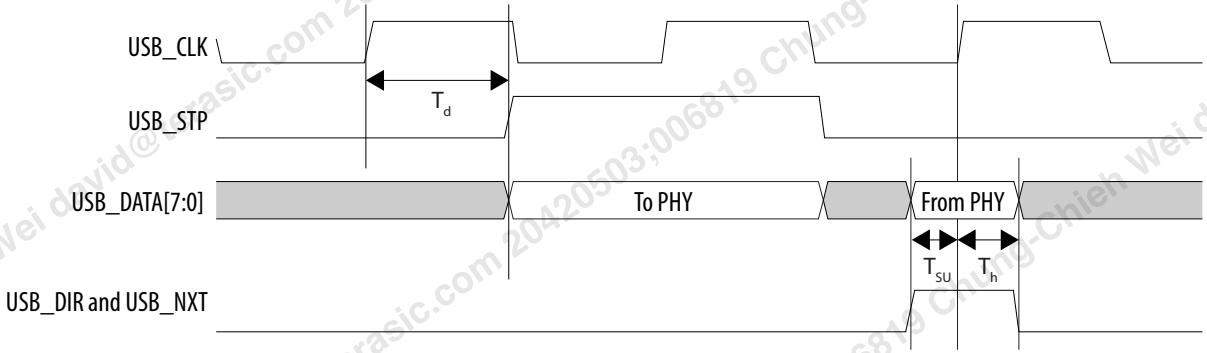
HPS USB 3.1 Timing Characteristics

Table 92. HPS USB 3.1 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{usb_clk}	USB_CLK clock period (60 MHz)	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns

Figure 19. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

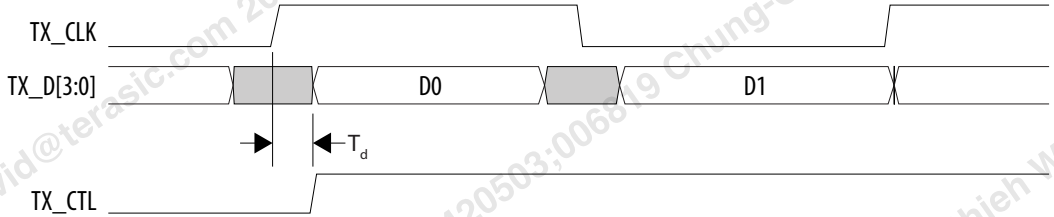
HPS Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 93. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d (141) (142)	TXD/TX_CTL to TX_CLK output skew	–0.5	—	0.5	ns

Figure 20. RGMII TX Timing Diagram



(141) Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.

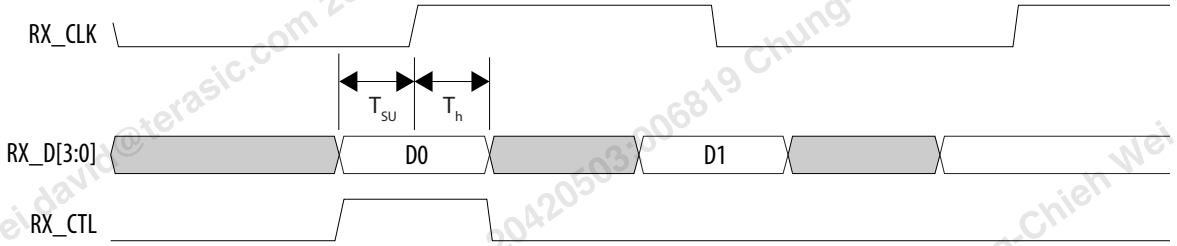
(142) If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5–2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1 ns data-to-clock skew requirement.

Table 94. RGMII RX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h (143)	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

Figure 21. RGMII RX Timing Diagram



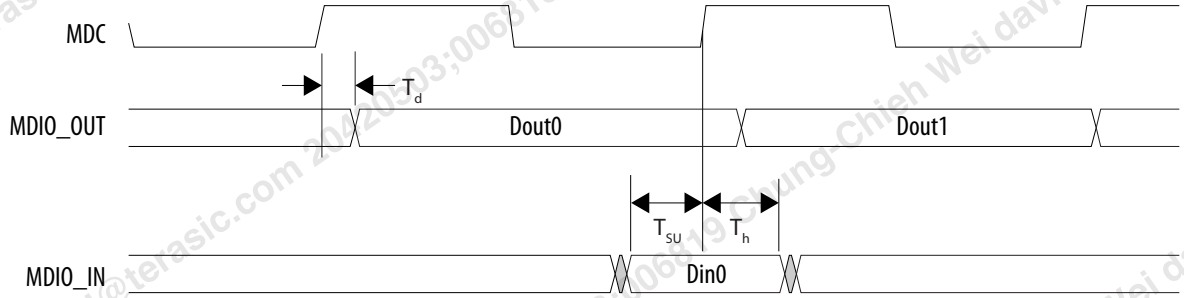
(143) If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5–2 ns, using the HPS I/O programmable delay.

Table 95. Management Data Input/Output (MDIO) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	400	—	—	ns
T_d	MDC to MDIO output data delay	10	—	300	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 22. MDIO Timing Diagram



SGMII Timing Requirements

SGMII operating mode is supported through FPGA fabric using SGMII PCS soft IP and LVDS SERDES IP. Refer to the *LVDS SERDES Specifications* section for timing specifications.

SGMII+ operating mode is supported through FPGA fabric using SGMII+ PCS soft IP and serial transceiver interface. Refer to the *Transceiver Performance Specifications* section for timing specifications.

Related Information

- LVDS SERDES Specifications on page 72
- GTS Transceiver Performance Specifications on page 86

HPS I²C Timing Characteristics

Table 96. HPS I²C Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
T_{clk_jitter}	I²C clock output jitter	—	2	—	2	%
T_{HIGH} (144)	SCL high period	4(145)	—	0.6(146)	—	µs
T_{LOW} (147)	SCL low period	4.7(148)	—	1.3(149)	—	µs
T_{SU_DAT}	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_{HD_DAT} (150)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs

continued...

(144) You can adjust T_{HIGH} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(145) The recommended minimum setting for `ic_ss_scl_hcnt` is 428. Refer to the SCL_High_time equation in the *Hard Processor System Technical Reference Manual*.

(146) The recommended minimum setting for `ic_fs_scl_hcnt` is 75. Refer to the SCL_High_time equation in the *Hard Processor System Technical Reference Manual*.

(147) You can adjust T_{LOW} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(148) The recommended minimum setting for `ic_ss_scl_lcnt` is 464. Refer to the SCL_Low_time equation in the *Hard Processor System Technical Reference Manual*.

(149) The recommended minimum setting for `ic_fs_scl_lcnt` is 163. Refer to the SCL_Low_time equation in the *Hard Processor System Technical Reference Manual*.

(150) T_{HD_DAT} is affected by the rise and fall time.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{VD_DAT} and T_{VD_ACK} (151)	SCL to SDA output data delay	—	3.45(152)	—	0.9(153)	µs
T_{SU_STA}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{HD_STA}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{SU_STO}	Setup time for a stop condition	4	—	0.6	—	µs
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
T_{scl_r} (154)	SCL rise time	—	1,000	20	300	ns
T_{scl_f} (154)	SCL fall time	—	300	6.54	300	ns
T_{sda_r} (154)	SDA rise time	—	1,000	20	300	ns
T_{sda_f} (154)	SDA fall time	—	300	6.54	300	ns

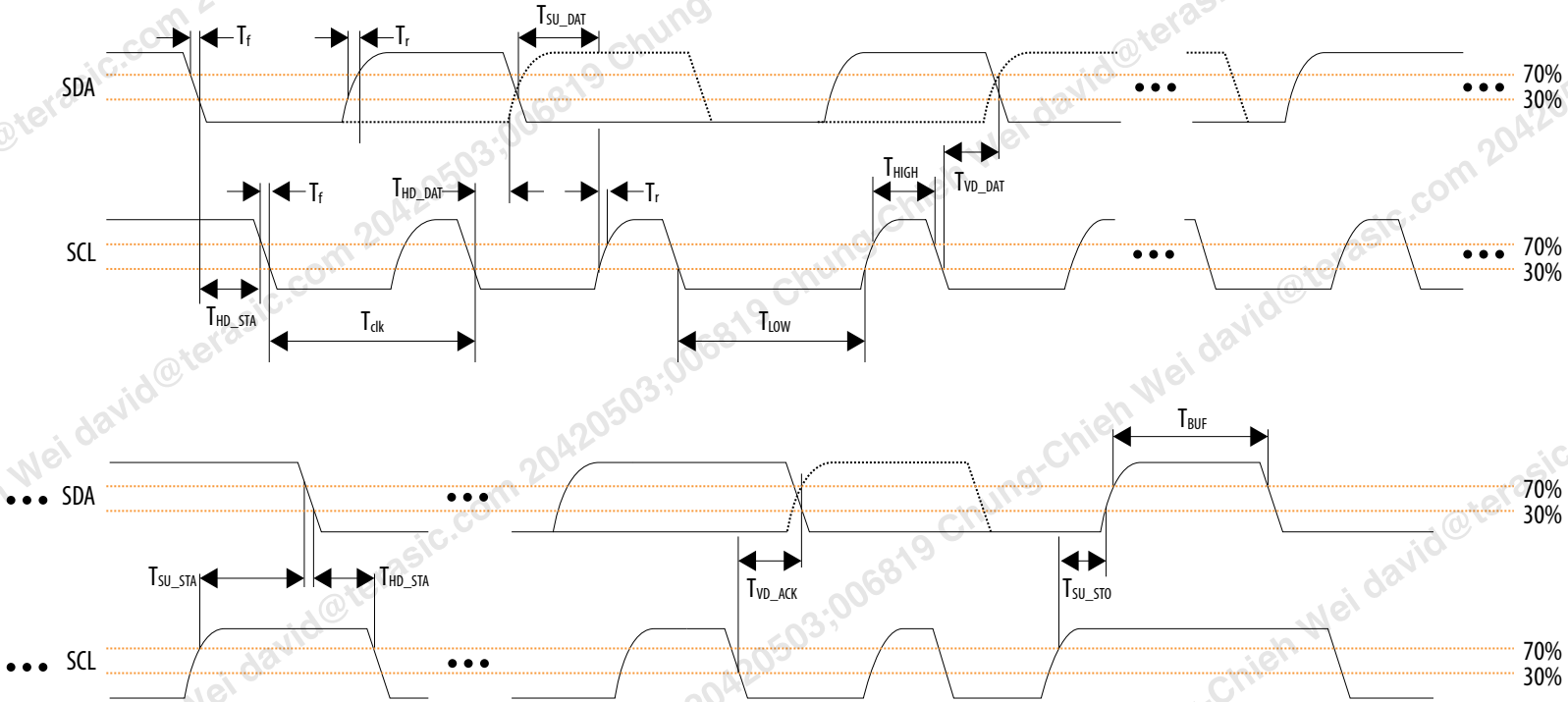
(151) T_{VD_DAT} and T_{VD_ACK} are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

(152) Use maximum SDA_HOLD = 240 to be within the specification.

(153) Use maximum SDA_HOLD = 60 to be within the specification.

(154) Rise and fall time parameters vary depending on external factors such as the characteristics of the I/O driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 23. I²C Timing Diagram



HPS I3C Timing Characteristics

Table 97. HPS I3C Timing Requirements When Communicating With I2C Legacy Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	0.4	0	1	MHz
T_{SCL}	Serial clock (SCL) clock period	—	2.5	—	1	µs
T_{clk_jitter}	I3C clock output jitter	—	2	—	2	%
T_{HIGH}	SCL high period	600	—	260	—	ns
T_{DIG_H}		$T_{HIGH} + T_{scl\_r}$	—	$T_{HIGH} + T_{scl\_r}$	—	ns
T_{LOW}	SCL low period	1,300	—	500	—	ns
T_{DIG_L}		$T_{LOW} + T_{scl\_r}$	—	$T_{LOW} + T_{scl\_r}$	—	ns
T_{SU_DAT}	Setup time for serial data line (SDA) data to SCL	100	—	50	—	ns
T_{HD_DAT}	Hold time for SCL to SDA data	—	—	—	—	—
T_{SU_STA}	Setup time for a repeated start condition	600	—	260	—	ns
T_{HD_STA}	Hold time for a repeated start condition	600	—	260	—	ns
T_{SU_STO}	Setup time for a stop condition	600	—	260	—	ns
T_{BUF}	SDA high pulse duration between STOP and START	1.3	—	0.5	—	µs
T_{scl_r}	SCL rise time	20	300	—	120	ns

continued...

Symbol	Description	Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	
T_{scl_f}	SCL fall time	20 × (V_{CCIO_HPS} / 5.5 V)(155)	300	20 × (V_{CCIO_HPS} / 5.5 V)(155)	120	ns
T_{sda_r}	SDA rise time	20	300	—	120	ns
T_{sda_f}	SDA fall time	20 × (V_{CCIO_HPS} / 5.5 V)(155)	300	20 × (V_{CCIO_HPS} / 5.5 V)(155)	120	ns
T_{SPIKE}	Pulse width of spikes that the spike filter must suppress	0	50	0	50	ns

Table 98. HPS I3C Open Drain Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{HIGH}	SCL high period	—	41	ns
T_{DIG_H}		—	T_{HIGH} + T_{CF}	ns
T_{LOW_OD}	SCL low period	200	—	ns
$T_{LOW\_OD\_L}$		T_{LOW_ODmin} + T_{fDA_ODmin}	—	ns
T_{fDA_OD}	SDA signal fall time	T_{CF}	12	ns
T_{SU_OD}	Setup time for serial data line (SDA) data to SCL	3	—	ns
T_{CAS} (156)	Clock after START Condition	38.4 ns	For ENTAS0: 1 µs	—
			For ENTAS1: 100 µs	—
			For ENTAS2: 2 ms	—
			For ENTAS3: 50 ms	—

continued...

(155) Refer to the *HPS Power Supply Operating Conditions* section for V_{CCIO_HPS} values.

(156) Enter Activity State (ENTAS) is a Common Command Code (CCC) supported by all I3C master and slave devices.

Symbol	Description	Min	Max	Unit
T_{CBP}	Clock before STOP Condition	$T_{CASmin}/2$	—	s
$T_{MMOverlap}$	Current master to secondary master overlap time during handoff	$T_{DIG\_OD\_Lmin}$	—	ns
T_{AVAL}	Bus available condition	1	—	µs
T_{IDLE}	Bus IDLE condition	200	—	µs
T_{MMLock}	Time internal where new master not driving SDA Low	$T_{AVALmin}$	—	µs

Table 99. HPS I3C Push-Pull Timing Requirements for SDR Mode

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz
T_{CLK}	Serial clock (SCL) clock period	100 µs	—	77.5 ns	—
T_{HIGH}	SCL clock high period	24	—	—	ns
T_{DIG_H}		32	—	—	ns
T_{LOW}	SCL clock low period	24	—	—	ns
T_{DIG_L}		32	—	—	ns
T_{HIGH_MIXED}	SCL clock high period for mixed bus(157)	24	—	—	ns
$T_{DIG\_H\_MIXED}$		32	—	45	ns
T_{SCO}	Clock in to data out for slave	—	—	12	ns
T_{CR}	SCL rise time	—	—	150e6 × $1/f_{SCL}$ (capped at 60 ns)	ns

continued...

(157) During I3C communication on a mixed bus, to avoid I2C controllers from interpreting I3C signaling as valid I2C signaling, the T_{DIG_H} period must be constrained.

Symbol	Description	Min	Typ	Max	Unit
T_{CF}	SCL fall time	—	—	150e6 × 1/f_{SCL} (capped at 60 ns)	ns
T_{HD_PP}	Hold time for SCL to SDA data (master)	T_{CR} + 3 and T_{CF} + 3	—	—	ns
	Hold time for SCL to SDA data (slave)	0	—	—	ns
T_{SU_PP}	SDA signal data setup time	3	—	—	ns
T_{CASr}	Clock after repeated START (Sr)	T_{CASmin}	—	—	ns
T_{CBSr}	Clock before repeated START (Sr)	T_{CASmin} / 2	—	—	ns
C_b	Capacitive load per bus Line (SDA/SCL)	—	—	50	pF

Figure 24. I³C Legacy Mode Timing Diagram

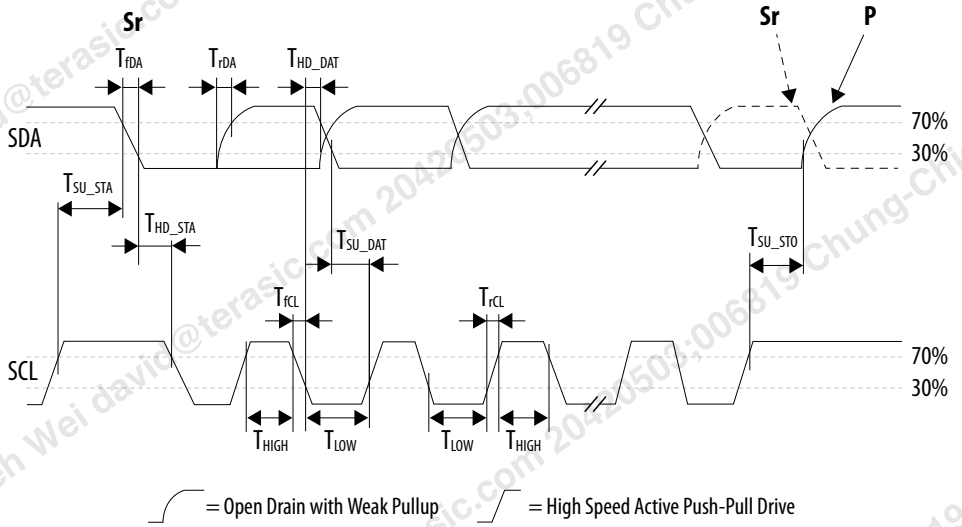


Figure 25. T_{DIG_H} and T_{DIG_L}

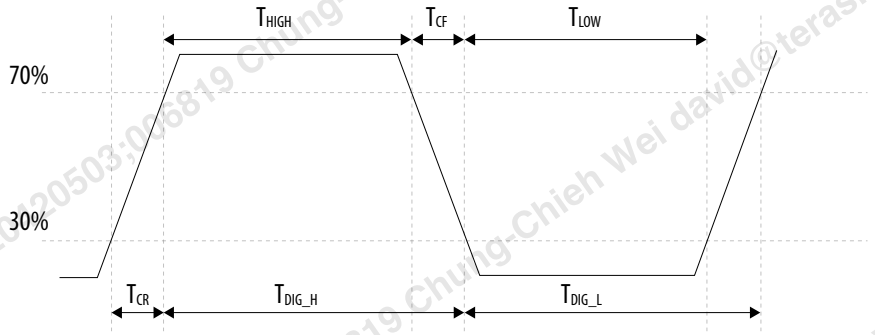


Figure 26. I3C Start Condition Timing Diagram

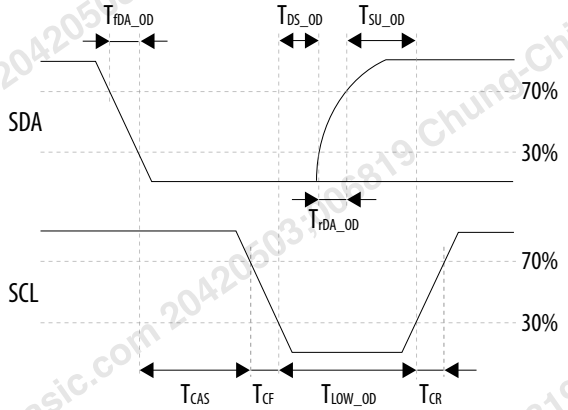


Figure 27. I3C Stop Condition Timing Diagram

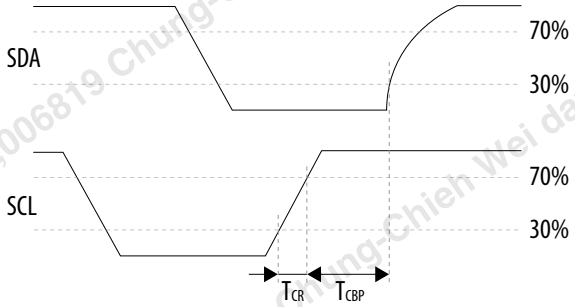


Figure 28. I3C Start Master Out Timing Diagram

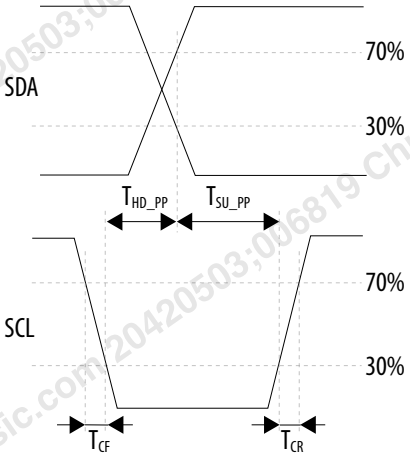


Figure 29. I3C Slave Out Timing Diagram

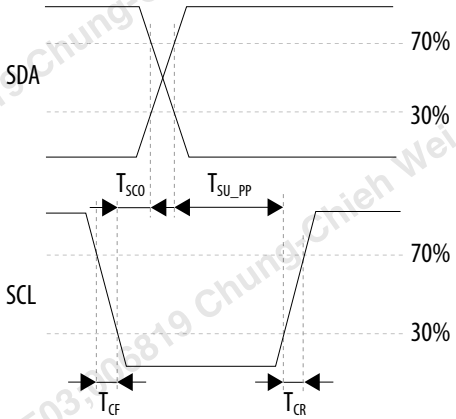
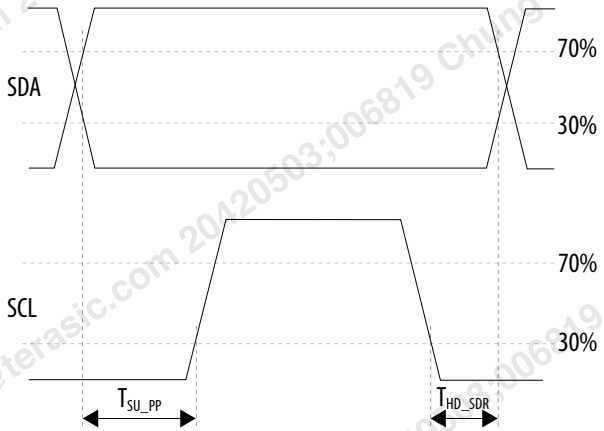


Figure 30. Master SDR Timing Diagram



Related Information

HPS Power Supply Operating Conditions on page 31

HPS NAND Timing Characteristics

Table 100. HPS NAND SDR Timing Requirements

Compatible with the ONFI 1.x and 2.x specifications. Compatible with the Toggle 1.x and 2.x specifications. HPS I/O supports SDR, NV-DDR protocols up to 200 MT/s.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{WP} (158)	Write enable pulse width	10	—	ns
T_{WH} (158)	Write enable hold time	7	—	ns
T_{RP} (158)	Read enable pulse width	10	—	ns
T_{REH} (158)	Read enable hold time	7	—	ns
T_{CLS} (158)	Command latch enable to write enable setup time	10	—	ns
T_{CLH} (158)	Command latch enable to write enable hold time	5	—	ns
T_{CS} (158)	Chip enable to write enable setup time	15	—	ns
T_{CH} (158)	Chip enable to write enable hold time	5	—	ns
T_{ALS} (158)	Address latch enable to write enable setup time	10	—	ns
T_{ALH} (158)	Address latch enable to write enable hold time	5	—	ns
T_{DS} (158)	Data to write enable setup time	7	—	ns
T_{DH} (158)	Data to write enable hold time	5	—	ns
T_{WB} (158)	Write enable high to R/B low	—	200	ns
T_{CEA}	Chip enable to data access time	—	100	ns

continued...

(158) This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

Symbol	Description	Min	Max	Unit
T_{REA}	Read enable to data access time	—	40	ns
T_{RHZ}	Read enable to data high impedance	—	200	ns
T_{RR}	Ready to read enable low	20	—	ns

Figure 31. NAND SDR Command Latch Timing Diagram

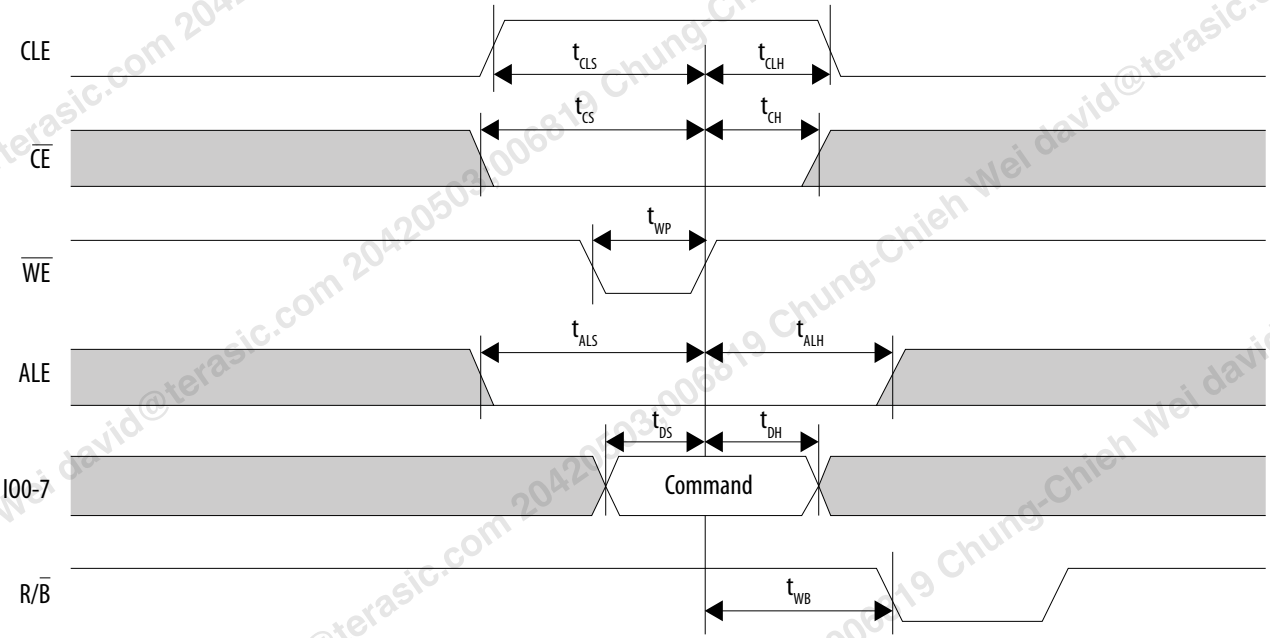


Figure 32. NAND SDR Address Latch Timing Diagram

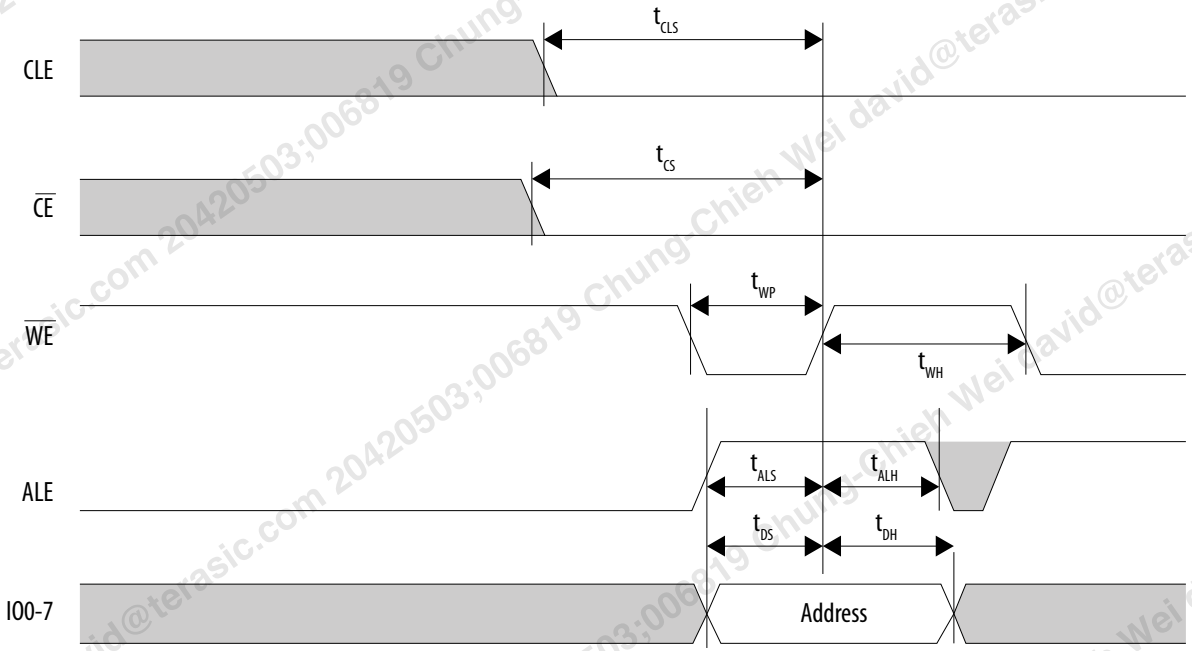


Figure 33. NAND SDR Data Output Cycle Timing Diagram

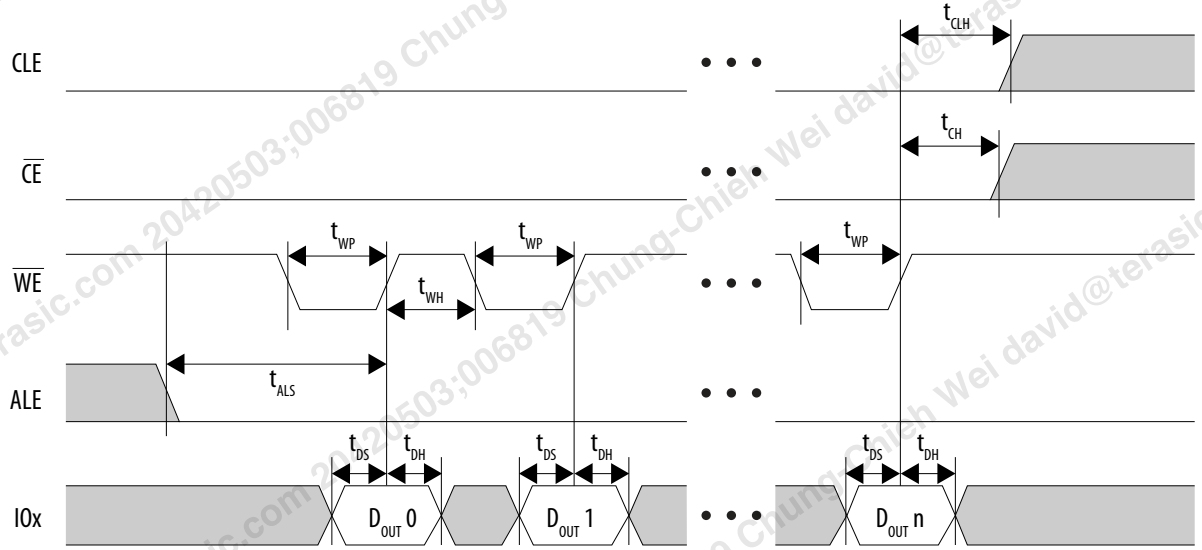


Figure 34. NAND SDR Data Input Cycle Timing Diagram

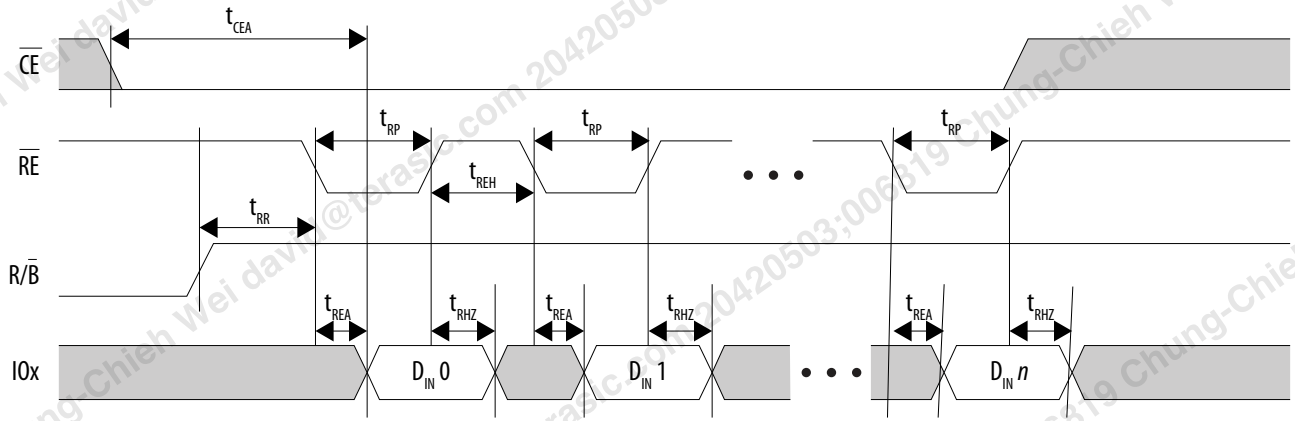


Figure 35. NAND SDR Data Input Timing Diagram for Extended Data Output (EDO) Cycle

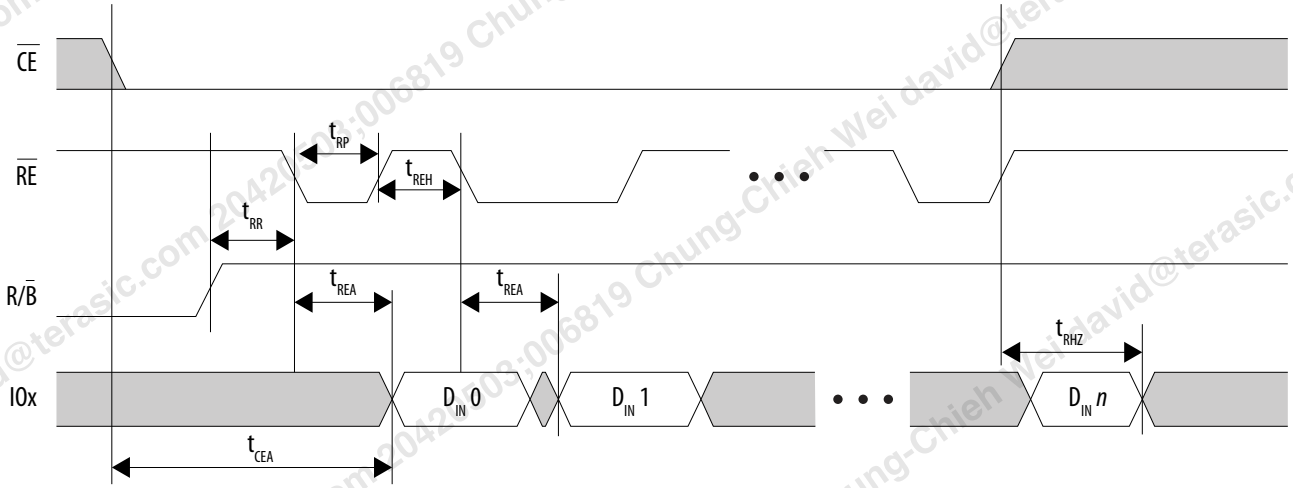


Figure 36. NAND SDR Read Status Timing Diagram

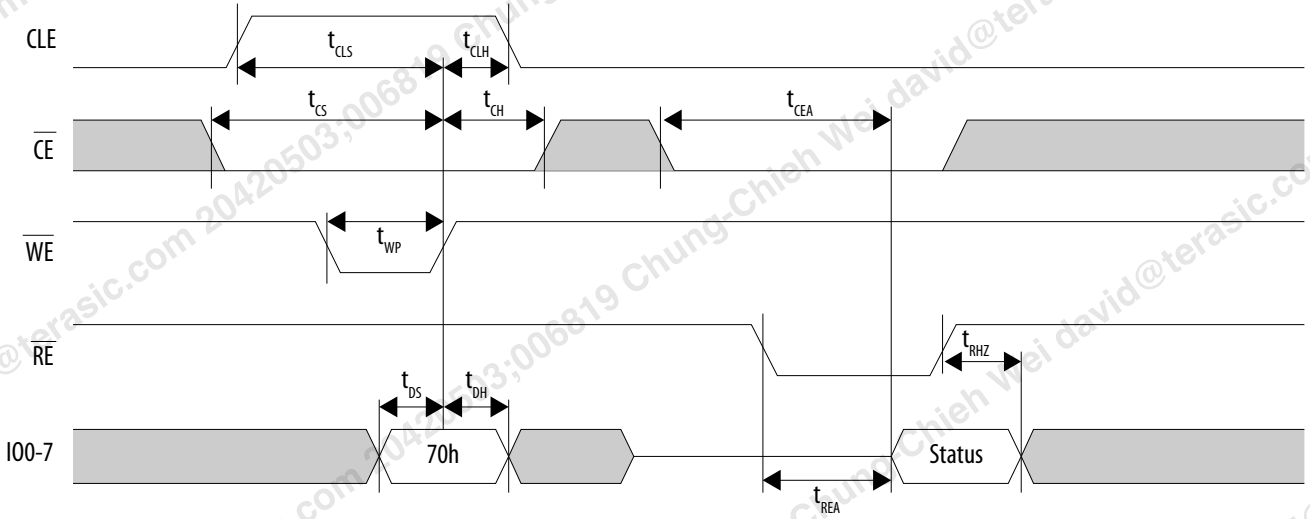


Figure 37. NAND SDR Read Status Enhanced Timing Diagram

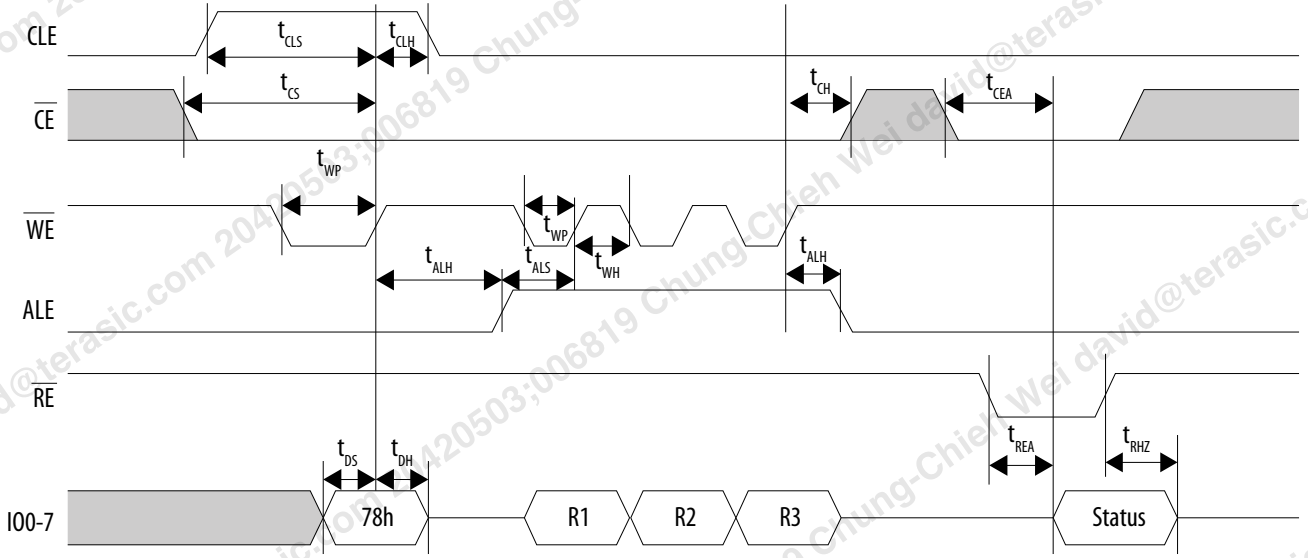


Table 101. HPS NAND DDR Timing Requirements

Compatible with the ONFI 1.x and 2.x specifications. Compatible with the Toggle 1.x and 2.x specifications. HPS I/O supports SDR, NV-DDR protocols up to 200 MT/s.

For specification status, see the *Data Sheet Status* table

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{AC}	Access window of DQ[7:0] from CLK	3	25	ns
t_{ADL}	Address cycle to data loading time	400	—	ns
t_{CADf}	Command, address, data delay (fast) (command to command, address to address, command to	25	—	ns

continued...

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
	address, address to command, command/address to start of data)			
t_{CADs}	Command, address, data delay (slow) (command to command, address to address, command to address, address to command, command/address to start of data)	45	—	ns
t_{CAH}	Command/address DQ hold time	2	—	ns
t_{CALH}	W/R_n, CLE, and ALE hold time	2	—	ns
t_{CALS}	W/R_n, CLE, and ALE setup time	2	—	ns
t_{CAS}	Command/address DQ setup time	2	—	ns
t_{CEH}	CE_n high hold time	20	—	ns
t_{CH}	CE_n hold time	2	—	ns
$t_{CK(avg)}$ or t_{CK} (159)	Average clock cycle time	10	—	ns
$t_{CK(abs)}$	Absolute clock period, measured from rising edge to the next consecutive rising edge	$t_{CK(avg)} + t_{JIT(per)\ min}$	$t_{CK(avg)} + t_{JIT(per)\ max}$	ns
$t_{CKH(abs)}$ (160)	Clock cycle high	0.43	0.57	t_{CK}
$t_{CKL(abs)}$ (160)	Clock cycle low	0.43	0.57	t_{CK}
t_{CKWR}	Data output end to W/R_n high	RoundUp{[$t_{DQSCK(max)} + t_{CK}$] / t_{CK}}	—	t_{CK}
t_{CS3}	CE_n setup time for data input and data output after CE_n has been high for greater than 1 µs	75	—	ns

continued...

(159) $t_{CK(avg)}$ is the average clock period over any consecutive 200 cycles window.

(160) $t_{CKH(abs)}$ and $t_{CKL(abs)}$ include static offset and duty cycle jitter.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{CS}	CE_n setup time	15	—	ns
t_{DH}	Data hold time	0.9	—	ns
t_{DPZ}	Data input pause setup time	1.5	—	t_{DSC}
t_{DQSCK}	Access window of DQS from CLK	3	25	ns
t_{DQSD}	W/R_n low to DQS/DQ driven by device	0	18	ns
t_{DQSH} (161)	DQS input high pulse width	0.4	0.6	t_{CK} or t_{DSC4}
t_{DQSHZ} (162)	W/R_n high to DQS/DQ tri-state by device	—	20	ns
t_{DQSL} (161)	DQS input low pulse width	0.4	0.6	t_{CK} or t_{DSC4}
t_{DQSQ}	DQS-DQ skew, DQS to last DQ valid, per access	—	0.85	ns
t_{DQSS}	Data input to first DQS latching transition	0.75	1.25	t_{CK}
t_{DS}	Data setup time	0.9	—	ns
t_{DSC}	DQS cycle time	10	—	ns
t_{DSH}	DQS falling edge to CLK rising – hold time	0.2	—	t_{CK}
t_{DSS}	DQS falling edge to CLK rising – setup time	0.2	—	t_{CK}
t_{DVW}	Output data valid window	$t_{DVW} = t_{QH} - t_{DQSQ}$		ns
t_{FEAT}	Busy time for Set Features and Get Features	—	1	µs
t_{HP}	Half-clock period	$t_{HP} = \min(t_{CKL}, t_{CKH})$		ns

continued...

(161) t_{DQSL} and t_{DQSH} are relative to t_{CK} when CLK is running. If CLK is stopped during data input, then t_{DQSL} and t_{DQSH} are relative to t_{DSC}.

(162) t_{DQSHZ} is not referenced to a specific voltage level, but specifies when the device output is no longer driving.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{ITC}	Interface and Timing Mode Change time	—	1	µs
$t_{JIT(per)}$	The deviation of a given $t_{CK(abs)}$ from $t_{CK(avg)}$	–0.5	0.5	ns
t_{QH}	DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH} = t_{HP} - t_{QHS}$		ns
t_{QHS}	Data hold skew factor	—	1	ns
t_{RHW}	Data output cycle to command, address, or data input cycle	100	—	ns
t_{RR}	Ready to data output cycle (data only)	20	—	ns
t_{RST} (raw NAND)	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n	—	15/30/500	µs
t_{RST} (EZ NAND)(163)	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n	—	150/150/500	µs
t_{WB}	(WE_n high or CLK rising edge) to SR[6] low	—	100	ns
t_{WHR}	Command, address, or data input cycle to data output cycle	80	—	ns
t_{WPRE}	DQS write preamble	1.5	—	t_{CK}
t_{WPST}	DQS write postamble	1.5	—	t_{CK}
t_{WRCK}	W/R_n low to data output cycle	20	—	ns
t_{WW}	WP_n transition to command cycle	100	—	ns

(163) If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using Synchronous Reset (FCh) or a Reset LUN (FAh) command then the values are as shown.

Figure 38. NAND DDR Command Cycle Timing Diagram

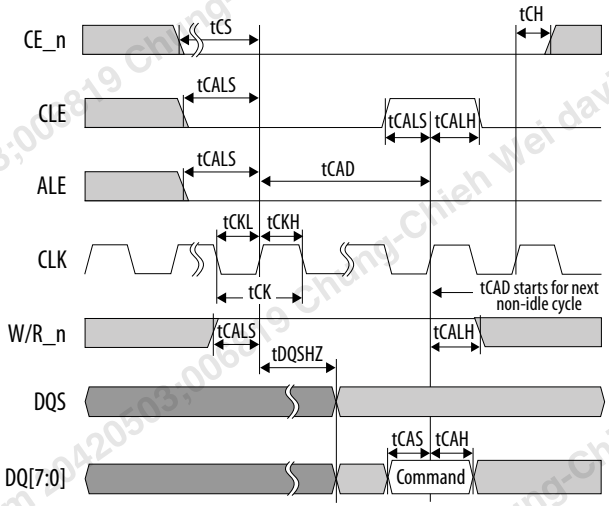


Figure 39. NAND DDR Address Cycle Timing Diagram

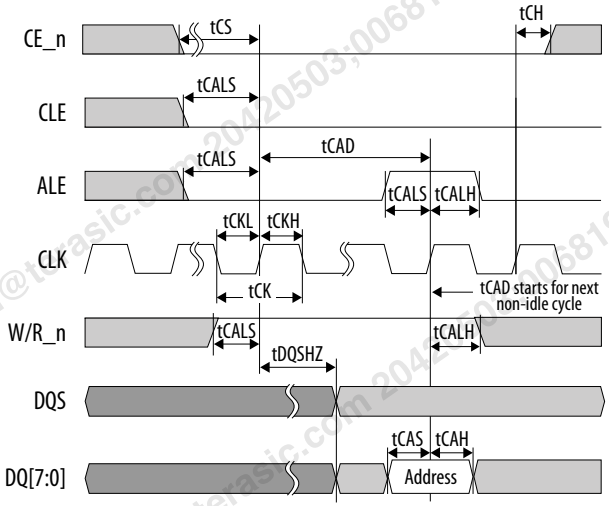


Figure 40. NAND DDR Data Input Cycle Timing Diagram

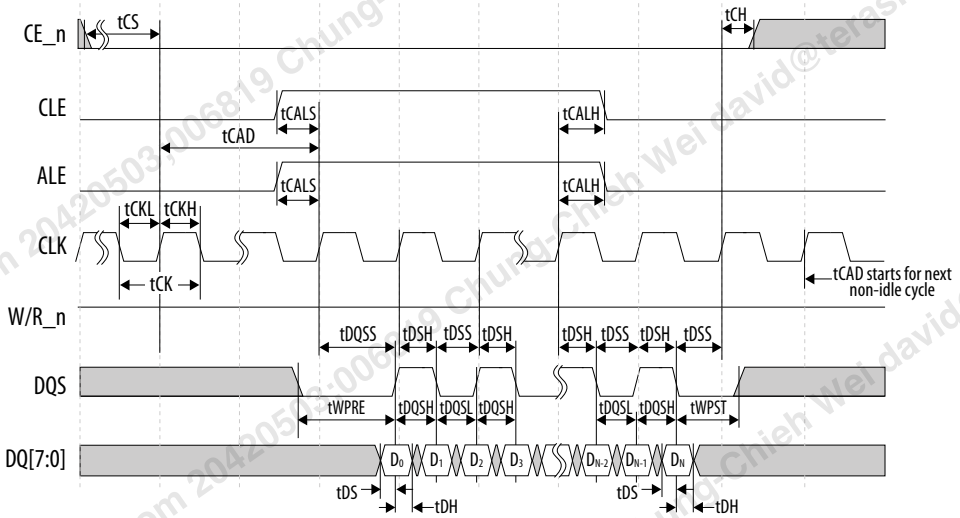


Figure 41. NAND DDR Data Input Cycle Timing Diagram (CLK Stopped)

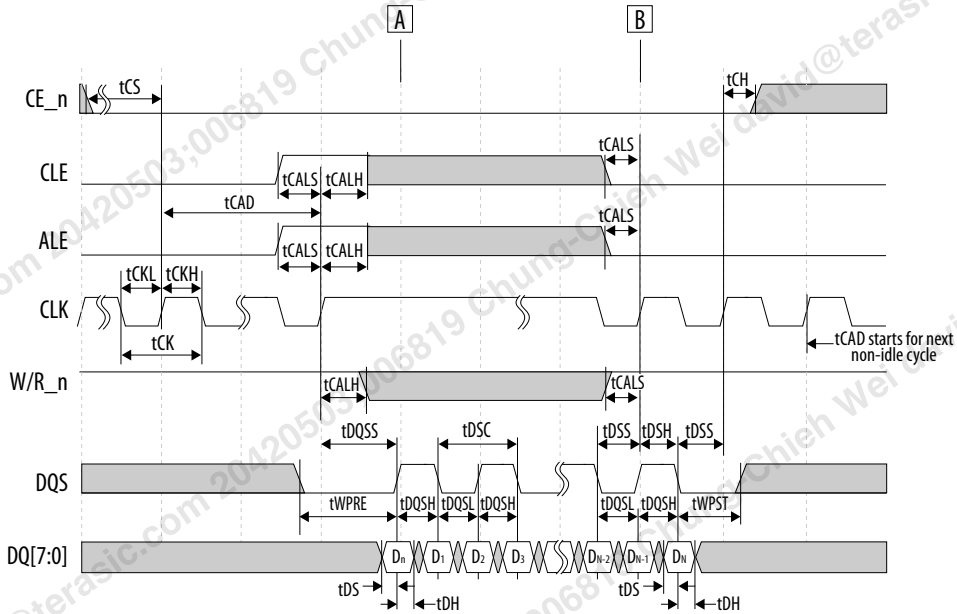


Figure 42. NAND DDR Data Input Cycle Timing Diagram (CLK Stopped with Data Pause)

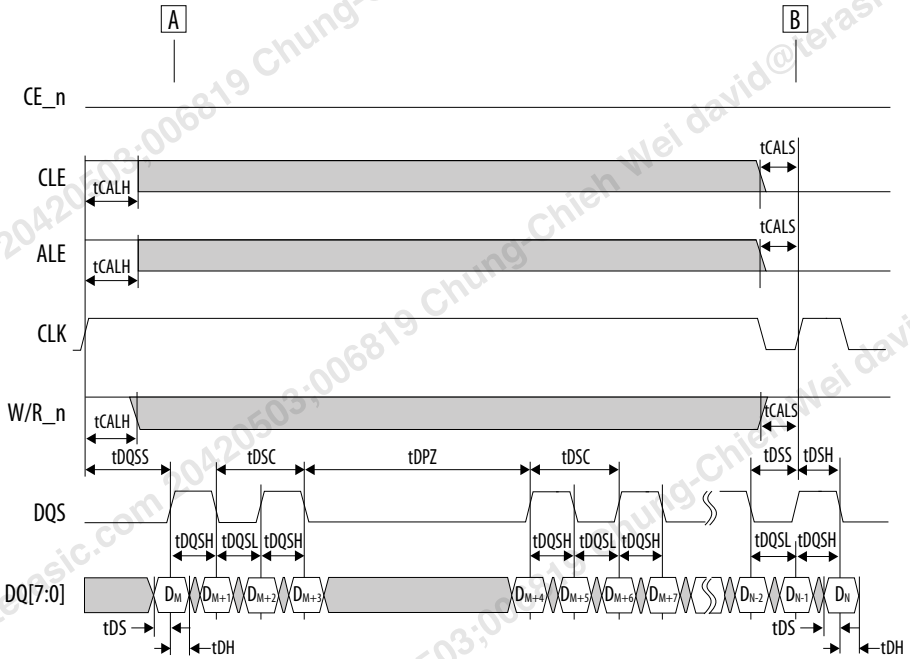


Figure 43. NAND DDR Data Output Cycle Timing Diagram

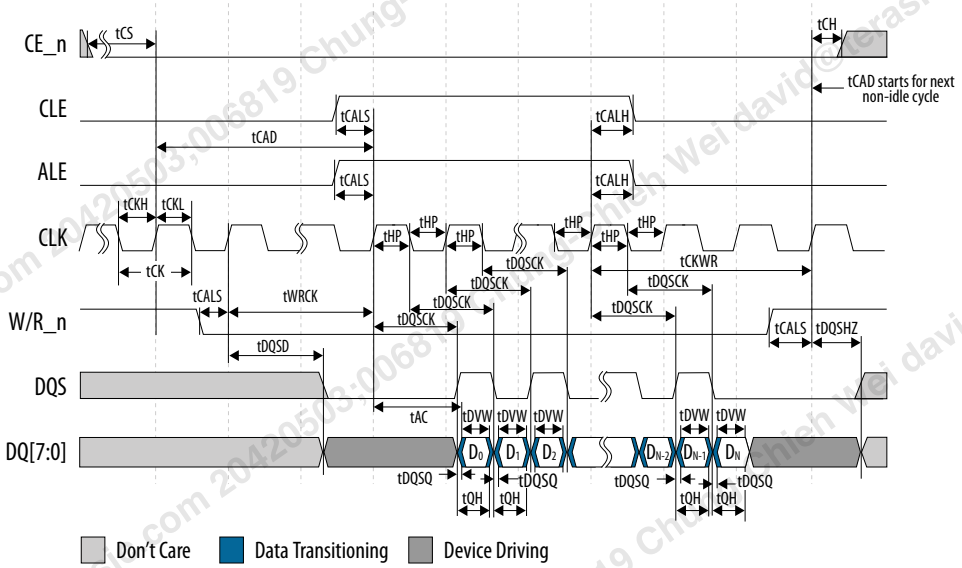


Figure 44. NAND DDR W/R_n Timing Diagram

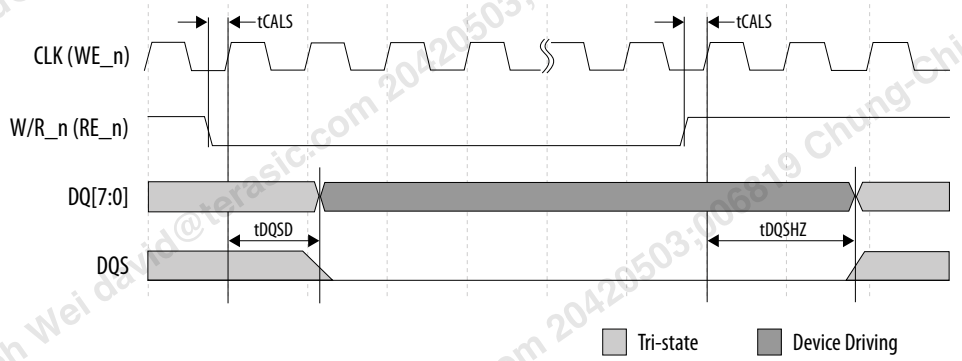
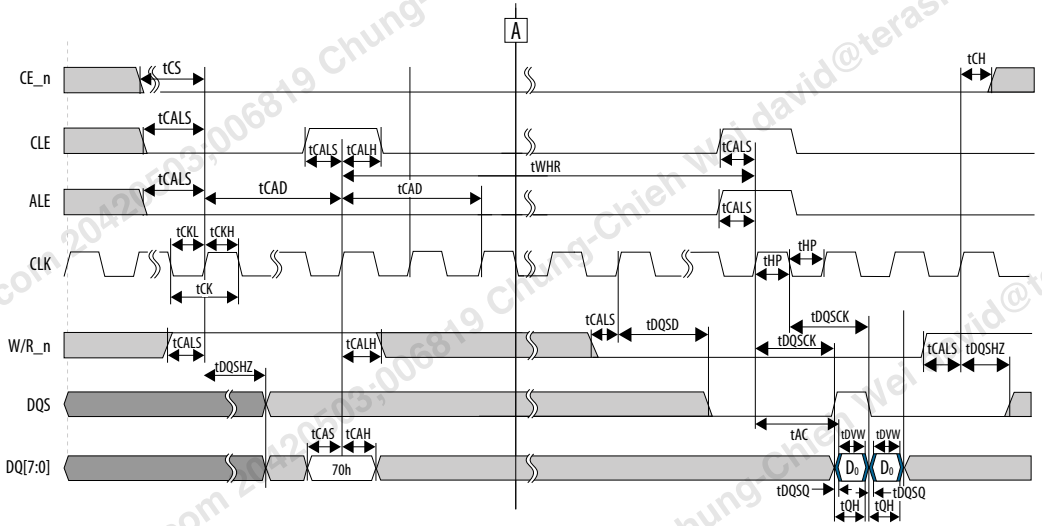


Figure 45. NAND DDR Read Status Including tWHR and tCAD Timing Diagram



HPS Trace Timing Characteristics

Table 102. Trace Timing Requirements

To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Platform Designer component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

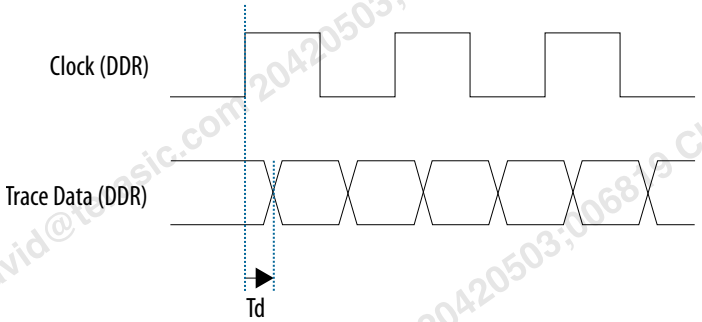
Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module data sheet for termination recommendations.

Most trace modules implement programmable clock and data skew to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	Trace clock period	6.667	—	—	ns
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	–0.5	—	1.3	ns

Figure 46. Trace Timing Diagram



HPS GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz).

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

The GPIO modules provided in the HPS include optional debounce capabilities. The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock, `gpio_db_clk`.

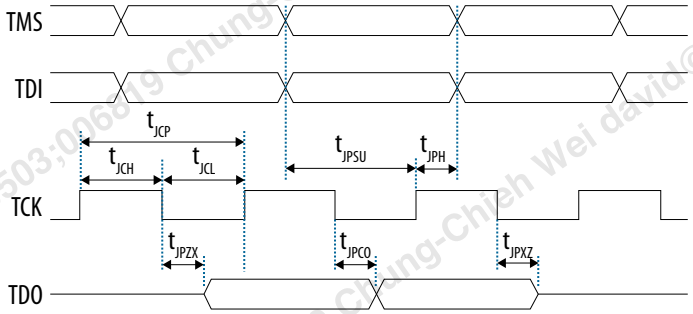
HPS JTAG Timing Characteristics

Table 103. HPS JTAG Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
t_{JCP}	TCK clock period	41.66	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	5	—	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0.5	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns

Figure 47. HPS JTAG Timing Diagram



HPS Programmable I/O Timing Characteristics

Table 104. HPS Programmable I/O Delay (Output Path)

For specification status, see the *Data Sheet Status* table

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	422	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	518	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	607	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	705	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	786	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	874	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	955	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	1,042	—	ps
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,126	—	ps
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,214	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,296	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,382	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,462	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,552	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,626	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,798	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	1,885	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	1,967	—	ps
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,054	—	ps
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,137	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,222	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,305	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,395	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,475	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,564	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	2,644	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	2,732	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	2,808	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	2,901	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	2,979	—	ps

Table 105. HPS Programmable I/O Delay (Input Path)

For specification status, see the *Data Sheet Status* table

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	422	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	518	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	607	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	705	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	786	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	874	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	955	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	1,042	—	ps
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,126	—	ps
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,214	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,296	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,382	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,462	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,552	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,626	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,798	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	1,885	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	1,967	—	ps
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,054	—	ps
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,137	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,222	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,305	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,395	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,475	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,564	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	2,644	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	2,732	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	2,808	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	2,901	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	2,979	—	ps

You can program the number of delay steps by adjusting the I/O Delay register (`io0_delay` through `io47_delay` for I/Os 0 through 47).

Configuration Specifications

General Configuration Timing Specifications

Table 106. General Configuration Timing Specifications

For specification status, see the *Data Sheet Status* table

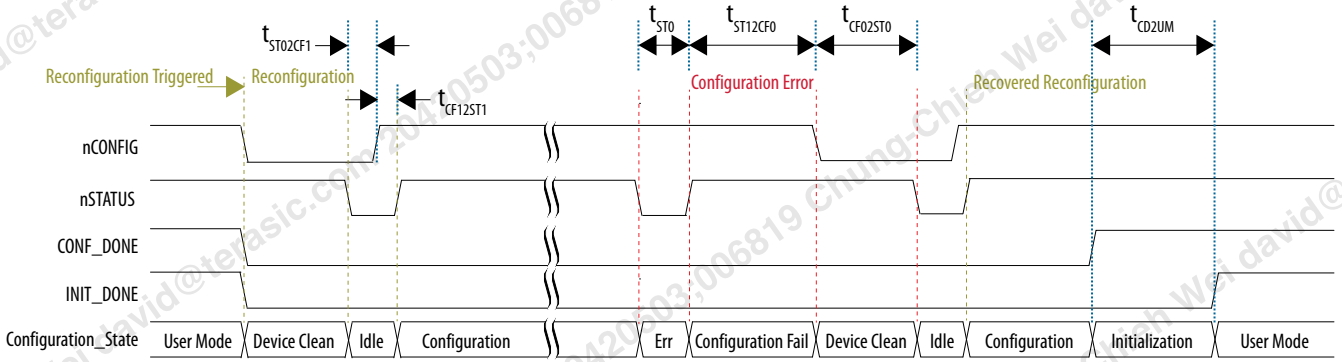
Symbol	Description	Requirement		Unit
		Min	Max	
$t_{CF12ST1}$	nCONFIG high to nSTATUS high	—	20	ms
$t_{CF02ST0}$ (164)	nCONFIG low to nSTATUS low	—	400	ms
t_{ST0}	nSTATUS low pulse during configuration error	0.5	10	ms

continued...

(164) You need to drive nCONFIG low pulse by referring to maximum value if nSTATUS cannot be monitored by host.

Symbol	Description	Requirement		Unit
		Min	Max	
t_{CD2UM} (165)	CONF_DONE high to user mode	—	5	ms
$t_{ST12CF0}$	Minimum time to drive nCONFIG from high to low after nSTATUS transitions from low to high	0	—	ms
$t_{ST02CF1}$	Minimum time to drive nCONFIG from low to high after nSTATUS transitions from high to low	0	—	ms

Figure 48. General Configuration Timing Diagram



POR Specifications

Power-on reset (POR) delay is defined as the delay between last power rail (V_{CCIO_SDM}) monitored by POR circuitry reached the minimum operating voltage to the time the device is ready to begin configuration.

(165) This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

Table 107. POR Delay Specifications

For specification status, see the *Data Sheet Status* table

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16	11.5	20.2	ms
AS (Fast mode)	1.5	7.6	ms

External Configuration Clock Source Requirements

Table 108. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements

For specification status, see the *Data Sheet Status* table

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency(166)	Powered by V_{CCIO_SDM}		25/100/125		MHz
Clock input peak-to-peak period jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

JTAG Configuration Timing

Table 109. JTAG Timing Parameters and Values

For specification status, see the *Data Sheet Status* table

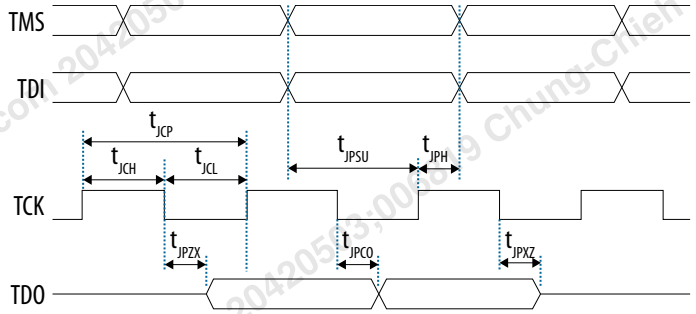
Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	10	—	ns
t_{JCH}	TCK clock high time	5	—	ns
t_{JCL}	TCK clock low time	5	—	ns

continued...

(166) The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. You must match the external configuration clock frequency on the OSC_CLK_1 pin to the configuration clock source assignment in the Intel Quartus Prime software. Other frequencies in the range are not supported.

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
$t_{JPSU\ (TDI)}$ (167)	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$ (167)	TMS JTAG port setup time	2	—	ns
t_{JPH} (167)	JTAG port hold time	1.5	—	ns
t_{JPCO}	JTAG port clock to output	—	5(168)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	5.5	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	2.1	ns

Figure 49. JTAG Timing Diagram



(167) For boundary-scan testing, the TMS and TDI JTAG ports minimum setup time and hold time are 7 ns.

(168) Capacitance loading at 10 pF.

AS Configuration Timing

Table 110. AS Timing Parameters

Intel recommends performing trace length matching for nCSO and AS_DATA pins to AS_CLK to minimize the skew.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk} (169)	AS_CLK clock period	—	6.02	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	8.5(170)	—	—	ns
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	6.8(170)	—	—	ns
T_{do} (171)	AS_DATA[3:0] output delay	–0.6	—	0.6	ns
T_{ext_delay} (172) (173) (174)	Total external propagation delay on AS signals	0	—	13.5	ns

continued...

(169) AS_CLK f_{MAX} has dependency on the maximum board loading. For AS single device configuration or AS using multiple serial flash devices configuration, use the equations in T_{do} and T_{ext_delay} notes to ensure your board has sufficient timing margin to meet flash setup/hold time specifications and AS timing specifications in this data sheet. For AS using multiple serial flash devices, refer to the *Configuration User Guide* for the recommended AS_CLK frequency and maximum board loading.

(170) AS operating at maximum clock frequency = 166 MHz. The delay is larger when operating at AS clock frequency lower than 166 MHz.

(171) Load capacitance for DCLK = 10 pF and AS_DATA = 18 pF. Intel recommends obtaining the T_{do} for a given link (including receiver, transmission lines, connectors, termination resistors, and other components) through IBIS or HSPIC simulation. To analyze flash setup time,

- $T_{su} = T_{clk}/2 - T_{do(max)} + T_{bd\_clk} - T_{bd\_data(max)}$
- $T_{ho} = T_{clk}/2 + T_{do(min)} - T_{bd\_clk} + T_{bd\_data(min)}$

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	62	—	—	ns
Skew (AS_CLK – AS_nCSO)	Maximum skew tolerance between nCSO and AS_CLK	$T_{su\_ncso} - T_{dcsfrs} < Skew\ (AS\_CLK - AS\_nCSO) < AS\_CLK/2 + T_{dcslst} - T_{ho\_ncso}$ (175)			ns
Skew (AS_CLK – AS_DATA)	Maximum skew tolerance between AS_CLK and AS_DATA	$-AS\_CLK/2 + T_{do(max)} + T_{su} < Skew\ (AS\_CLK - AS\_DATA) < AS\_CLK/2 + T_{do(min)} - T_{ho}$ (175)			ns

(172) $T_{ext\_delay} = T_{bd\_clk} + T_{co} + T_{bd\_data} + T_{add}$
- T_{bd_clk}: Propagation delay for AS_CLK between FPGA and flash device.
- T_{co}: Output hold time and clock low to output valid of flash device. This delay must be used to ensure T_{ext_delay} is within the minimum and maximum specification values.
- T_{bd_data}: Propagation delay for AS_DATA bus between FPGA and flash device.
- T_{add}: Propagation delay for active/passive components on AS_DATA interfaces.

(173) T_{ext_delay} specification is based on AS_CLK = 166 MHz. The value can be larger at lower AS_CLK frequency.

(174) Meeting T_{ext_delay} timing specifications indicates that the AS_DATA setup/hold timing is met.

(175)
- T_{su} = Data setup time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{ho} = Data hold time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{do} = AS_DATA[3:0] output delay. Refer to the specification in this table.
- AS_CLK = AS_CLK clock period.
- T_{su_ncso} = Chip select setup time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{ho_ncso} = Chip select hold time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{dcsfrs} = AS_nCSO[3:0] asserted to first AS_CLK edge. Refer to the specification in this table.
- T_{dcslst} = Last AS_CLK edge to AS_nCSO[3:0] deasserted. Refer to the specification in this table.

Figure 50. AS Configuration Serial Output Timing Diagram

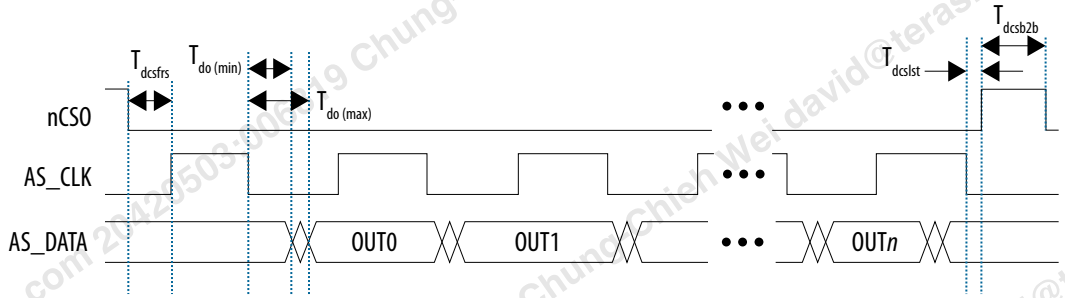
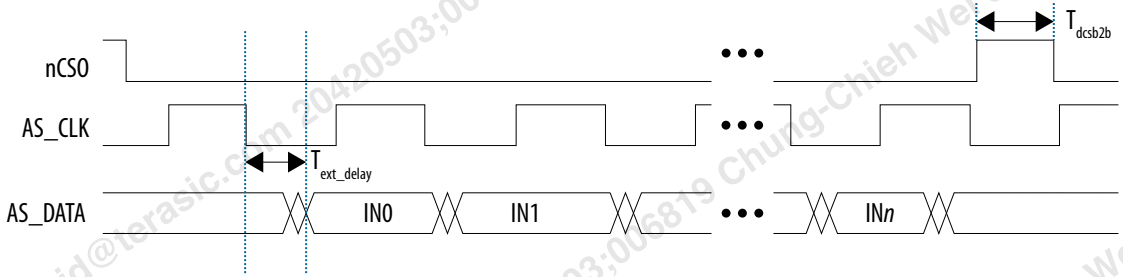


Figure 51. AS Configuration Serial Input Timing Diagram



Avalon Streaming Configuration Timing

Table 111. Avalon Streaming Timing Parameters for ×8 and ×16 Configurations

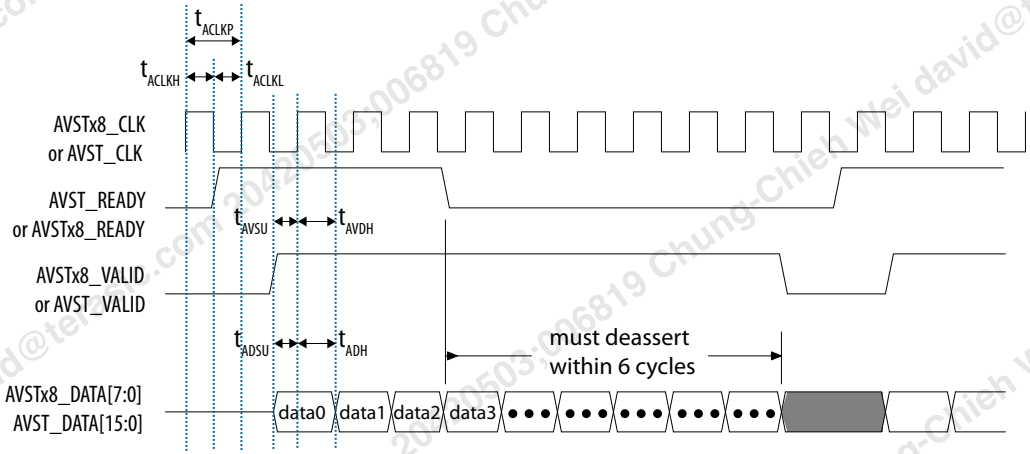
For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Unit
t_{ACLKH}	AVST_CLK high time	1.8	ns
t_{ACLKL}	AVST_CLK low time	1.8	ns
t_{ACLKP}	AVST_CLK period	4	ns
t_{ADSU} (176)	AVST_DATA setup time before rising edge of AVST_CLK	2.5	ns

continued...

Symbol	Description	Minimum	Unit
t_{ADH} (176)	AVST_DATA hold time after rising edge of AVST_CLK	0	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	2.5	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	ns

Figure 52. Avalon Streaming Configuration Timing Diagram



(176) Data sampled by the FPGA (sink) at the next rising clock edge.

Configuration Bit Stream Sizes

Table 112. Configuration Bit Stream Sizes

Configuration bit stream sizes shown in this table are based on worst-case scenarios. The sizes are typically substantially smaller because of the use of the Intel bit stream compression. The Intel bit stream compression efficiency has dependency on your design complexity.

For specification status, see the *Data Sheet Status* table

Variant	Compressed Configuration Bit Stream Size (Mbits)
A5E 065	268

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Programmable IOE Delay

Table 113. Programmable IOE Delay Specifications

For specification status, see the *Data Sheet Status* table

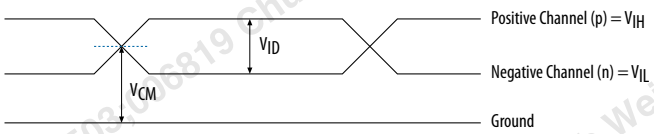
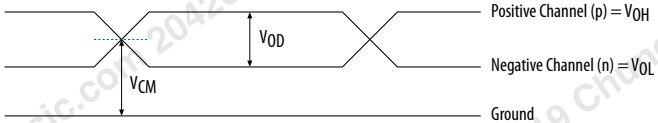
Parameter	Maximum Offset	Minimum Offset	Fast Model	Slow Model						Unit
				–E1V, –I1V	–E2V, –I2V	–E3V, –I3V	–E4S, –I4S	–E5S, –I5S	–E6S, –I6S, –E6X, –I6X	
Input Delay Chain (INPUT_DELAY_CHAIN)	63	0	0.062	7.095	7.100	7.105	7.110	7.115	7.120	ns
Output Delay Chain (OUTPUT_DELAY_CHAIN)	15	0	0.062	1.925	1.930	1.935	1.940	1.945	1.850	ns
Output Enable Delay Chain (OUTPUT_EENABLE_DELAY_CHAIN)	15	0	0.062	1.925	1.930	1.935	1.940	1.945	1.850	ns

Glossary

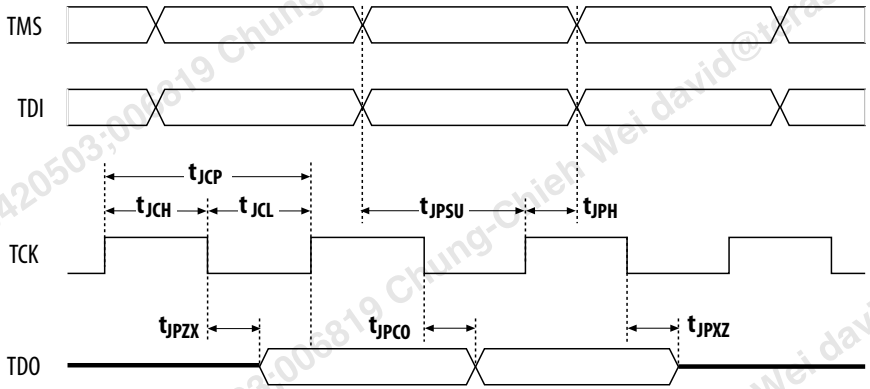
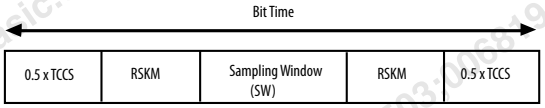
Table 114. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

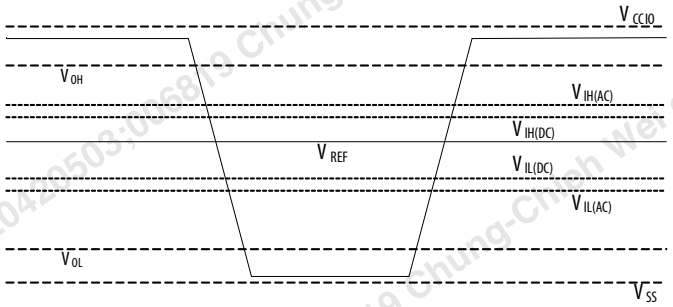
continued...

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	LVDS SERDES block—maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	LVDS SERDES block—maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J (SERDES factor)	LVDS SERDES block—deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

continued...

Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	LVDS SERDES block—duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—the common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage—minimum DC input differential voltage required for switching.

continued...

Term	Definition
V_{IH}	Voltage input high—the minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—the maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—the common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{OX}	Output differential cross point voltage.
$V_{IX(AC)}$	V_{IX} Input differential cross point voltage.
W	LVDS SERDES block—Clock Boost Factor.

Document Revision History for the Intel Agilex 5 FPGAs and SoCs Device Data Sheet

Document Version	Changes
2023.08.11	• Updated the *D-Series FPGAs Absolute Maximum Ratings* table. — Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. — Added V_{CCIO_PIO} specifications for V_{CCIO_PIO} = 1.0 V. — Updated V_I specifications and footnote. — Updated I_{OUT} specifications and added footnote. • Updated the *E-Series FPGAs Absolute Maximum Ratings* table. — Updated –6L to –6X speed grade. — Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. — Added V_{CCIO_PIO} specifications for V_{CCIO_PIO} = 1.0 V. — Updated V_I specifications and footnote. — Updated I_{OUT} specifications and added footnote. • Updated the description in the *Maximum Allowed Overshoot and Undershoot Voltage* section and added the following tables: — *Maximum Allowed Overshoot During Transitions for 1.0 V I/O in HSIO Bank* — *Maximum Allowed Overshoot During Transitions for 1.3 V I/O in HSIO Bank* • Updated the *D-Series FPGAs Recommended Operating Conditions* table. — Updated $V_{CCIO\_PIO\_SDM}$ specifications. — Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. — Updated V_{CCIO_PIO} specifications and footnote. — Updated V_I specifications and footnote. — Added V_O specifications for V_{CCIO_PIO} = 1.0 V. — Updated t_{RAMP} footnote. • Updated the *E-Series FPGAs Recommended Operating Conditions* table. — Updated –6L to –6X speed grade. — Updated V_{CCH_SDM}, $V_{CCIO\_PIO\_SDM}$, and $V_{CC\_IO\_SDM}$ specifications. — Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. — Updated V_{CCIO_PIO} specifications and footnote. — Updated V_I specifications and footnote. — Added V_O specifications for V_{CCIO_PIO} = 1.0 V. — Updated t_{RAMP} footnote. • Added footnote to maximum value column in the *D-Series FPGAs GTS Transceiver Power Supply Operating Conditions* table. • Updated the *E-Series FPGAs GTS Transceiver Power Supply Operating Conditions* table. — Added footnote to maximum value column. — Updated –6L to –6X speed grade.

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Document Version	Changes
	• Updated the *HSIO OCT Calibration Accuracy Specifications* table. — Removed 50-Ω R_S specification. — Added footnote to R_S and R_T. — Removed DPHY11 I/O standards support. • Updated the *HSIO OCT Without Calibration Resistance Tolerance Specifications* table. — Added 34-Ω and 40-Ω R_S specifications for 1.0 V LVCMOS and 1.3 V LVCMOS I/O standards. — Added footnote to R_S and R_T. • Added specifications for V_{CCIO_PIO} = 1.0 ±5% and V_{CCIO_PIO} = 1.3 ±5% in the *HSIO Internal Weak Pull-Up Resistor* table. • Updated I_I and I_{OZ} specifications for V_I = 0 V to V_{CCIO_HVIO} = 2.5 V in the *HVIO I/O Pin Leakage Current* table. • Updated C_{IO} specification in the *HVIO Pin Capacitance* table. • Updated V_{HYS} specification for V_{CCIO_HVIO} = 3.3 V in the *HVIO Hysteresis Specifications for Schmitt Trigger Input* table. • Added specifications for 1.0 V LVCMOS and 1.3 V LVCMOS I/O standards in the *HSIO Single-Ended I/O Standards Specifications* table. • Updated POD11 and POD12 specifications in the *HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications* table. • Updated LVSTL11, LVSTL105, and LVSTL700 specifications in the *HSIO Single-Ended LVSTL I/O Standards Specifications* table. • Added footnote to SSTL-12, HSTL-12, and HSUL-12 in the *HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications* table. • Updated POD11 and POD12 specifications in the *HSIO Differential POD I/O Standards Specifications* table. • Updated LVSTL11, LVSTL105, and LVSTL700 specifications in the *HSIO Differential LVSTL I/O Standards Specifications* table. • Updated f_{IN} specifications in the *D-Series FPGAs I/O PLL Specifications* table. • Updated the *E-Series FPGAs I/O PLL Specifications* table. — Updated f_{IN} specifications. — Updated –6L to –6X speed grade. • Updated Fixed-point complex multiplication mode to Fixed-point 18 x 19 complex multiplication mode in the *D-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks* table. • Updated –6L to –6X speed grade in the *E-Series FPGAs DSP Block Performance Specifications for Single DSP Block* table. • Updated the *E-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks* table. — Updated –6L to –6X speed grade. — Updated Fixed-point complex multiplication mode to Fixed-point 18 x 19 complex multiplication mode. • Updated –6L to –6X speed grade in the *E-Series FPGAs Memory Block Performance Specifications* table. • Updated the *Voltage Sensor Specifications* table. — Added external reference voltage specifications. — Updated footnote to voltage sensor accuracy, V_{in}. • Split the *LVDS SERDES Specifications* table into the following tables and updated specifications: — *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* — *E-Series Device Group B FPGAs LVDS SERDES Specifications* • Removed $T_{PP\text{-}JITTER\text{-}TOLERANCE}$ specifications in the *System PLL Reference Clock (Using HVIO) Specifications* table.

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Document Version	Changes
	• Updated the *Electrical Compliance List* table. — Updated specification for IEEE 802.3by 111/110 and CPRI V7.0. — Added footnote to PCIe BASE 4.0 / PIPE 4.4.1 specification. — Updated specification/clause and protocol for USB. • Removed the following RMII content: — *Reduced Media Independent Interface (RMII) Clock Timing Requirements* table — *RMII TX Timing Requirements* table — *RMII TX Timing Diagram* — *RMII RX Timing Requirements* table — *RMII RX Timing Diagram* • Removed ONFI 3.x, INFI 4.x, NV-DDR2, and NV-DDR3 in the table description of the following tables: — *HPS NAND SDR Timing Requirements* — *HPS NAND DDR Timing Requirements* • Updated t_{JCP}, t_{JCH}, t_{JCL}, $t_{JPSU\ (TMS)}$, t_{JPH}, t_{JPCO}, t_{JPZX}, and t_{JPXZ} specifications in the *JTAG Timing Parameters and Values* table. • Updated t_{ACLKH}, t_{ACLKL}, t_{ACLKP}, t_{ADSU}, t_{ADH}, and t_{AVSU} specifications in the *Avalon Streaming Timing Parameters for ×8 and ×16 Configurations* table. • Updated the *Programmable IOE Delay Specifications* table. — Added specifications for Output Enable Delay Chain (OUTPUT_EENABLE_DELAY_CHAIN). — Updated –6L to –6X speed grade.
2023.03.27	Initial release.