KSZ9031RNX

Gigabit Ethernet Transceiver with RGMII Support

Data Sheet Rev 1.0

General Description

The KSZ9031RNX is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9031RNX provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000 Mbps speed.

The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

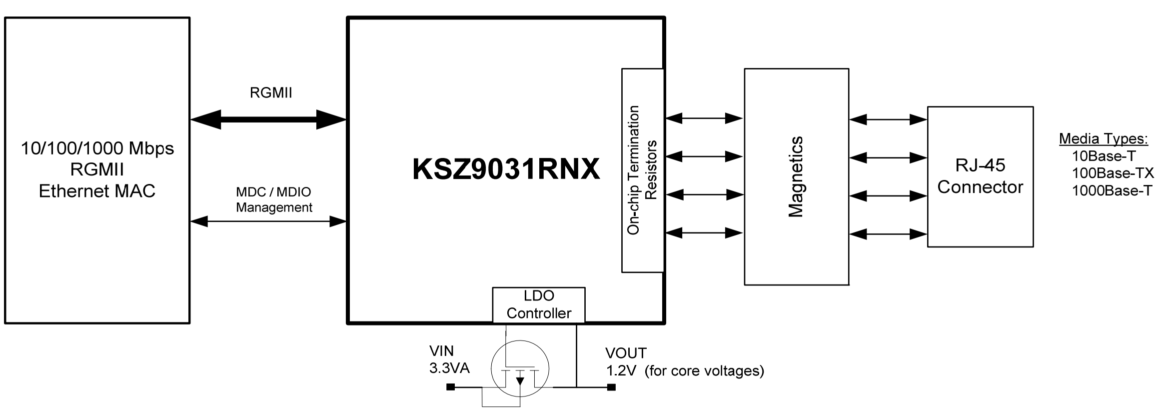
The KSZ9031RNX provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9031 I/Os and board. LinkMD® TDR-based cable diagnostic allows identification of faulty copper cabling. Remote and local loopback functions provide verification of analog and digital data paths.

The KSZ9031RNX is available in the 48-pin lead-free QFN package (See Ordering Information).

Features

- Single-chip 10/100/1000 Mbps IEEE 802.3 compliant Ethernet Transceiver
- RGMII timing supports on-chip delay per RGMII Version 2.0, with programming options for external delay and to make adjustment and correction to Tx and Rx timing paths
- RGMII I/Os with 3.3V/2.5V/1.8V tolerant
- Auto-Negotiation to automatically select the highest link up speed (10/100/1000 Mbps) and duplex (half/full)
- On-chip termination resistors for the differential pairs
- On-chip LDO controller to support single 3.3V supply operation – requires only external FET to generate 1.2V for the core
- Jumbo frame support up to 16KB
- 125 MHz Reference Clock Output
- Energy Detect Power Down Mode for reduced power consumption when cable not attached
- Energy Efficient Ethernet (EEE) support with Low Power Idle (LPI) mode and clock stoppage for 100Base-TX/1000Base-T and transmit amplitude reduction with 10Base-Te option
- Wake On LAN (WOL) Support with robust custom packet detection

Functional Diagram



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More Features

- Programmable LED outputs for link, activity and speed
- Baseline Wander Correction
- LinkMD® TDR-based cable diagnostic for identification of faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and board
- Loopback modes for diagnostics
- Automatic MDI/MDI-X crossover for detection and correction of pair swap at all speeds of operation
- Automatic detection and correction of pair swap, pair skew and pair polarity
- MDC/MDIO Management Interface for PHY register configuration
- Interrupt pin option
- Power down and power saving modes
- Operating Voltages
  - Core (DVDDL, AVDDL, AVDDL_PLL):
    - 1.2V (external FET or regulator)
  - VDD I/O (DVDDH):
    - 3.3V, 2.5V, or 1.8V
  - Transceiver (AVDDH):
    - 3.3V, or 2.5V (commercial temp)
- Available package
  - 48-pin QFN (7mm x 7mm)

Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Gigabit LAN on Motherboard (GLOM)
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-top Box
- Game Console
- Triple-play (data, voice, video) Media Center
- Media Converter

Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Wire Bonding	Description
KSZ9031RNXCA	0°C to 70°C	48-Pin QFN	Pb-Free	Gold	RGMII, Commercial Temperature, Gold Wire Bonding
KSZ9031RNXCC (1)	0°C to 70°C	48-Pin QFN	Pb-Free	Copper	RGMII, Commercial Temperature, Copper Wire Bonding
KSZ9031RNXIA (1)	–40°C to 85°C	48-Pin QFN	Pb-Free	Gold	RGMII, Industrial Temperature, Gold Wire Bonding
KSZ9031RNX-EVAL	0°C to 70°C	48-Pin QFN	Pb-Free		KSZ9031RNX Evaluation Board (Mounted with KSZ9031RNX device in commercial temperature)

Note:

1. Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
1.0	9/28/12	Data sheet created.

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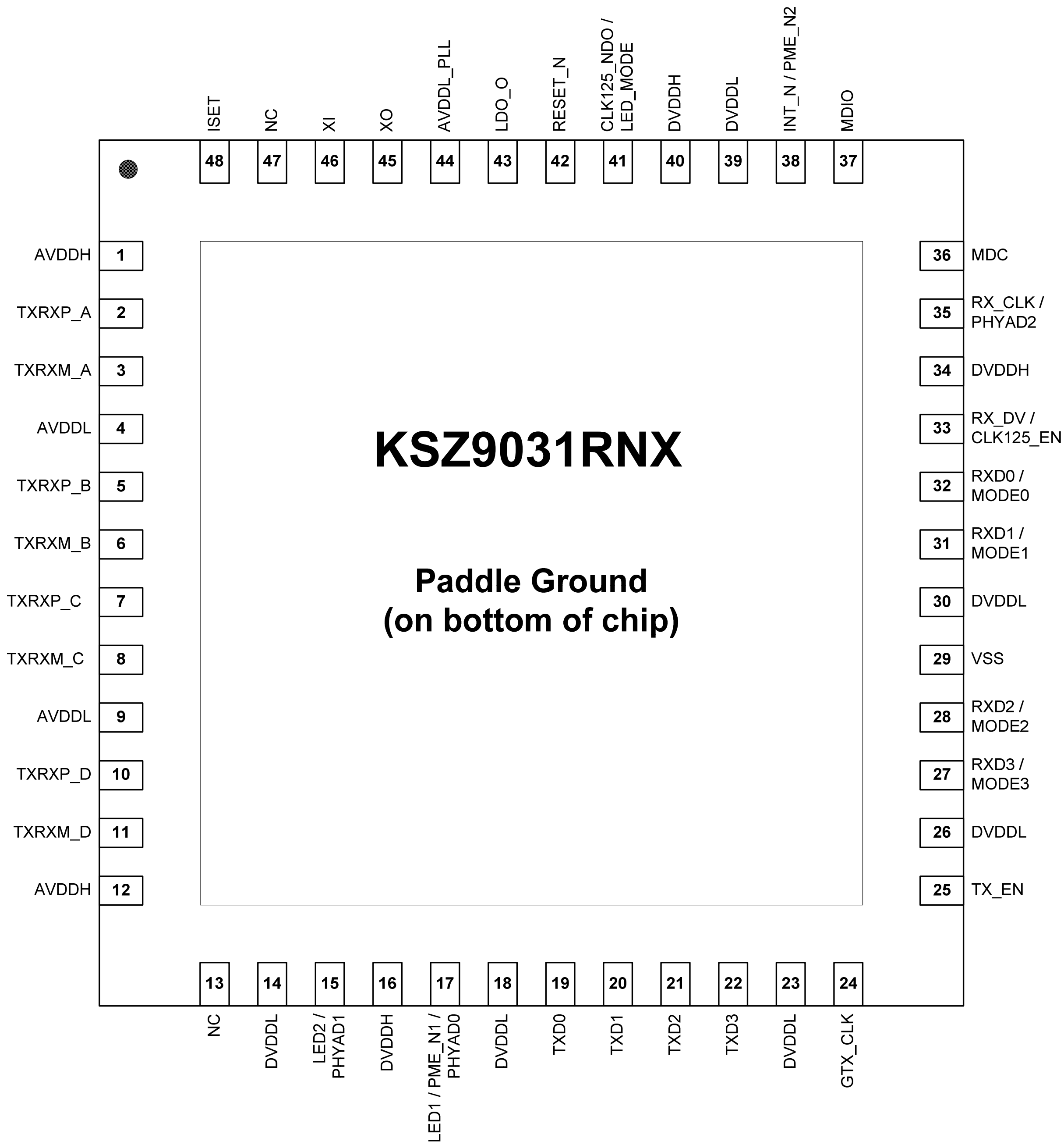
Pin Configuration



48-Pin QFN
(Top View)

Pin Description – KSZ9031RNX

Pin Number	Pin Name	Type[(1)]	Pin Function
1	AVDDH	P	3.3V / 2.5V (commercial temp only) analog V_{DD}
2	TXRXP_A	I/O	Media Dependent Interface[0], positive signal of differential pair 1000Base-T Mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
3	TXRXM_A	I/O	Media Dependent Interface[0], negative signal of differential pair 1000Base-T Mode: TXRXM_A corresponds to BI_DA- for MDI configuration and BI_DB- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively.
4	AVDDL	P	1.2V analog V_{DD}
5	TXRXP_B	I/O	Media Dependent Interface[1], positive signal of differential pair 1000Base-T Mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
6	TXRXM_B	I/O	Media Dependent Interface[1], negative signal of differential pair 1000Base-T Mode: TXRXM_B corresponds to BI_DB- for MDI configuration and BI_DA- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively.
7	TXRXP_C	I/O	Media Dependent Interface[2], positive signal of differential pair 1000Base-T Mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_C is not used.
8	TXRXM_C	I/O	Media Dependent Interface[2], negative signal of differential pair 1000Base-T Mode: TXRXM_C corresponds to BI_DC- for MDI configuration and BI_DD- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_C is not used.
9	AVDDL	P	1.2V analog V_{DD}

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>10</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair
1000Base-T Mode:
TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.
10Base-T / 100Base-TX Mode:
TXRXP_D is not used.</td></tr>
<tr><td>11</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair
1000Base-T Mode:
TXRXM_D corresponds to BI_DD- for MDI configuration and BI_DC- for MDI-X configuration, respectively.
10Base-T / 100Base-TX Mode:
TXRXM_D is not used.</td></tr>
<tr><td>12</td><td>AVDDH</td><td>P</td><td>3.3V / 2.5V (commercial temp only) analog V_{DD}</td></tr>
<tr><td>13</td><td>NC</td><td>-</td><td>No connect – This pin is not bonded and can be connected to digital ground for footprint compatibility with the Micrel KSZ9021RN Gigabit PHY.</td></tr>
<tr><td>14</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>15</td><td>LED2 /
PHYAD1</td><td>I/O</td><td>LED Output: Programmable LED2 Output
Config Mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up / reset. See “Strapping Options” section for details.
The LED2 pin is programmed by the LED_MODE strapping option (pin 41), and is defined as follows.

Single LED Mode
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link on (any speed)</td><td>L</td><td>ON</td></tr>
</table>

Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>

For Tri-color Dual LED Mode, LED2 works in conjunction with LED1 (pin 17) to indicate 10 Mbps Link and Activity.</td></tr>
</table>

Pin Number	Pin Name	Type[1]	Pin Function
16	DVDDH	P	3.3V / 2.5V / 1.8V digital $V_{DD\_I/O}$
17	LED1 / PHYAD0 / PME_N1	I/O	LED1 Output: Programmable LED1 Output Config Mode: The voltage on this pin is sampled and latched during the power-up / reset process to determine the value of PHYAD[0]. See “Strapping Options” section for details. PME_N Output: Programmable PME_N Output (pin option 1). This pin function requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0KΩ to 4.7KΩ. When asserted low, this pin signals a WOL event has occurred. The LED1 pin is programmed by the LED_MODE strapping option (pin 41), and is defined as follows.

Single LED Mode

Activity	Pin State	LED Definition
No Activity	H	OFF
Activity (RX, TX)	Toggle	Blinking

Tri-color Dual LED Mode

Link / Activity	Pin State		LED Definition	
	LED2	LED1	LED2	LED1
Link off	H	H	OFF	OFF
1000 Link / No Activity	L	H	ON	OFF
1000 Link / Activity (RX, TX)	Toggle	H	Blinking	OFF
100 Link / No Activity	H	L	OFF	ON
100 Link / Activity (RX, TX)	H	Toggle	OFF	Blinking
10 Link / No Activity	L	L	ON	ON
10 Link / Activity (RX, TX)	Toggle	Toggle	Blinking	Blinking

For Tri-color Dual LED Mode, LED1 works in conjunction with LED2 (pin 15) to indicate 10 Mbps Link and Activity.

Pin Number	Pin Name	Type[1]	Pin Function
18	DVDDL	P	1.2V digital V_{DD}
19	TXD0	I	RGMII Mode: RGMII TD0 (Transmit Data 0) Input
20	TXD1	I	RGMII Mode: RGMII TD1 (Transmit Data 1) Input
21	TXD2	I	RGMII Mode: RGMII TD2 (Transmit Data 2) Input
22	TXD3	I	RGMII Mode: RGMII TD3 (Transmit Data 3) Input
23	DVDDL	P	1.2V digital V_{DD}
24	GTX_CLK	I	RGMII Mode: RGMII TXC (Transmit Reference Clock) Input
25	TX_EN	I	RGMII Mode: RGMII TX_CTL (Transmit Control) Input
26	DVDDL	P	1.2V digital V_{DD}
27	RXD3 / MODE3	I/O	RGMII Mode: RGMII RD3 (Receive Data 3) Output Config Mode: The pull-up/pull-down value is latched as MODE3 during power-up / reset. See “Strapping Options” section for details.
28	RXD2 / MODE2	I/O	RGMII Mode: RGMII RD2 (Receive Data 2) Output Config Mode: The pull-up/pull-down value is latched as MODE2 during

Pin Number	Pin Name	Type[1]	Pin Function
			power-up / reset. See “Strapping Options” section for details.
29	VSS	Gnd	Digital ground
30	DVDDL	P	1.2V digital V_{DD}
31	RXD1 / MODE1	I/O	RGMII Mode: RGMII RD1 (Receive Data 1) Output Config Mode: The pull-up/pull-down value is latched as MODE1 during power-up / reset. See “Strapping Options” section for details.
32	RXD0 / MODE0	I/O	RGMII Mode: RGMII RD0 (Receive Data 0) Output Config Mode: The pull-up/pull-down value is latched as MODE0 during power-up / reset. See “Strapping Options” section for details.
33	RX_DV / CLK125_EN	I/O	RGMII Mode: RGMII RX_CTL (Receive Control) Output Config Mode: Latched as CLK125_NDO Output Enable during power-up / reset. See “Strapping Options” section for details.
34	DVDDH	P	3.3V / 2.5V / 1.8V digital $V_{DD\_I/O}$
35	RX_CLK / PHYAD2	I/O	RGMII Mode: RGMII RXC (Receive Reference Clock) Output Config Mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up / reset. See “Strapping Options” section for details.
36	MDC	Ipu	Management Data Clock Input This pin is the input reference clock for MDIO (pin 37).
37	MDIO	Ipu/O	Management Data Input / Output This pin is synchronous to MDC (pin 36) and requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0KΩ to 4.7KΩ.
38	INT_N / PME_N2	O	Interrupt Output: Programmable Interrupt Output with register 1Bh as the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh, bit [14] sets the interrupt output to active low (default) or active high. PME_N Output: Programmable PME_N Output (pin option 2). When asserted low, this pin signals a WOL event has occurred. For Interrupt (when active low) and PME functions, this pin requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0KΩ to 4.7KΩ.
39	DVDDL	P	1.2V digital V_{DD}
40	DVDDH	P	3.3V / 2.5V / 1.8V digital $V_{DD\_I/O}$
41	CLK125_NDO / LED_MODE	I/O	125 MHz Clock Output This pin provides a 125 MHz reference clock output option for use by the MAC. Config Mode: The pull-up/pull-down value is latched as LED_MODE during power-up / reset. See “Strapping Options” section for details.
42	RESET_N	Ipu	Chip Reset (active low) Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See “Strapping Options” section for more details.
43	LDO_O	O	On-chip 1.2V LDO Controller Output This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip’s core voltages. If 1.2V is provided by the system and this pin is not used, it can be left floating.
44	AVDDL_PLL	P	1.2V analog V_{DD} for PLL
45	XO	O	25 MHz Crystal feedback This pin is a no connect if oscillator or external clock source is used.
46	XI	I	Crystal / Oscillator / External Clock Input 25 MHz +/-50ppm tolerance

Pin Number	Pin Name	Type[1]	Pin Function
47	NC	-	No connect – This pin is not bonded and can be connected to AVDDH power for footprint compatibility with the Micrel KSZ9021RN Gigabit PHY.
48	ISET	I/O	Set transmit output level Connect a 12.1KΩ 1% resistor to ground on this pin.
PADDLE	P_GND	Gnd	Exposed Paddle on bottom of chip Connect P_GND to ground.

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up (see Electrical Characteristics for value).
   Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) / Output.

Strapping Options – KSZ9031RNX

Pin Number	Pin Name	Type(1)	Pin Function
35 15 17	PHYAD2 PHYAD1 PHYAD0	I/O I/O I/O	The PHY Address, PHYAD[2:0], is sampled and latched at power-up / reset and is configurable to any value from 0 to 7. Each PHY address bit is configured as follows: Pull-up = 1 Pull-down = 0 PHY Address bits [4:3] are always set to ‘00’.
27 28 31 32	MODE3 MODE2 MODE1 MODE0	I/O I/O I/O I/O	The MODE[3:0] strap-in pins are latched at power-up / reset and are defined as follows:

MODE[3:0]	Mode
0000	Reserved – not used
0001	Reserved – not used
0010	Reserved – not used
0011	Reserved – not used
0100	NAND Tree Mode
0101	Reserved – not used
0110	Reserved – not used
0111	Chip Power Down Mode
1000	Reserved – not used
1001	Reserved – not used
1010	Reserved – not used
1011	Reserved – not used
1100	RGMII Mode – advertise 1000Base-T full-duplex only
1101	RGMII Mode – advertise 1000Base-T full and half-duplex only
1110	RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex),except 1000Base-T half-duplex
1111	RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex)

Pin Number	Pin Name	Type(1)	Pin Function
33	CLK125_EN	I/O	CLK125_EN is latched at power-up / reset and is defined as follows: Pull-up = Enable 125 MHz Clock Output Pull-down = Disable 125 MHz Clock Output Pin 41 (CLK125_NDO) provides the 125 MHz reference clock output option for use by the MAC.
41	LED_MODE	I/O	LED_MODE is latched at power-up / reset and is defined as follows: Pull-up = Single LED Mode Pull-down = Tri-color Dual LED Mode

Note:

1. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to the incorrect configuration. In this case, it is recommended to add external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

Functional Overview

The KSZ9031RNX is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver solution for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable. Its on-chip proprietary 1000Base-T transceiver and Manchester/MLT-3 signaling-based 10Base-T/100Base-TX transceivers are all IEEE 802.3 compliant.

The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9031RNX can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9031RNX provides the RGMII interface for a direct and seamless connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000 Mbps speed.

The following figure shows a high-level block diagram of the KSZ9031RNX.

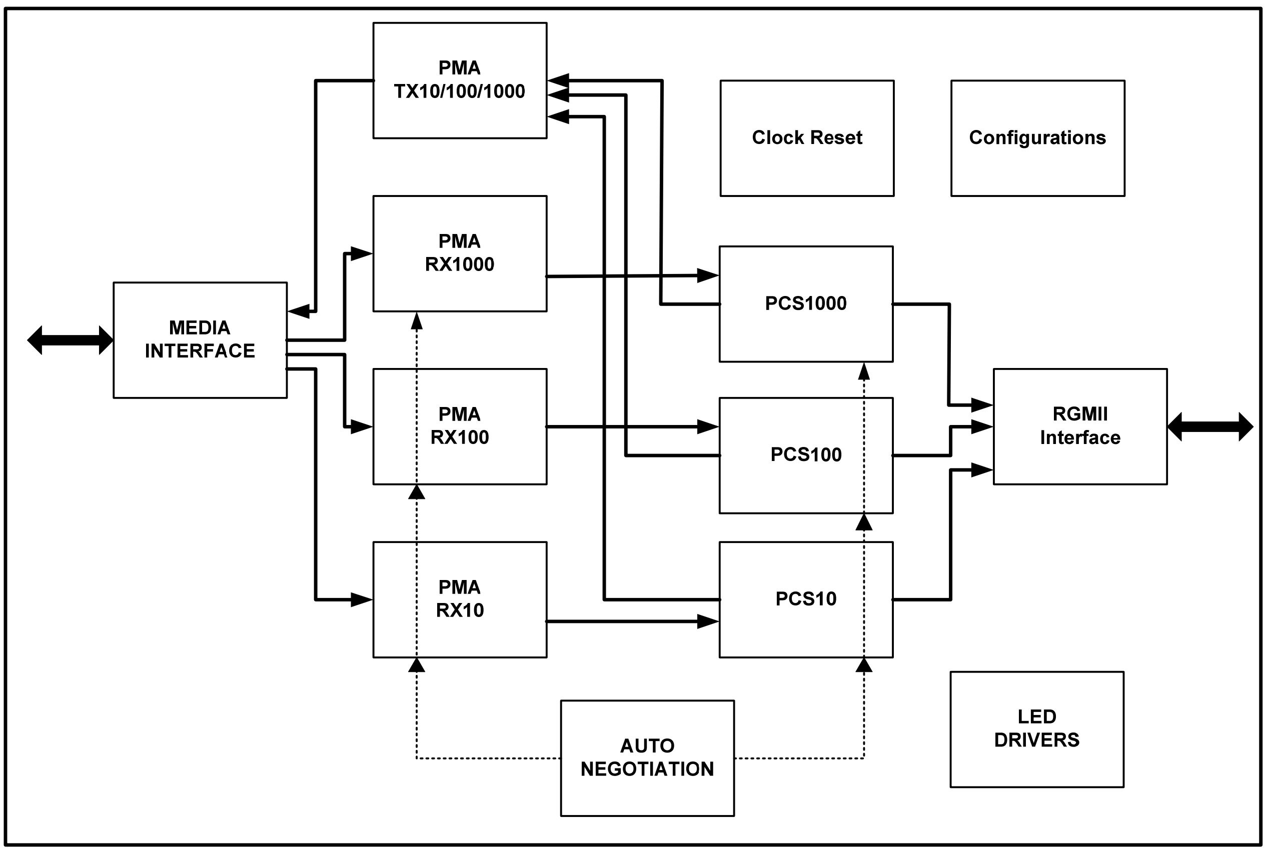


Figure 1. KSZ9031RNX Block Diagram

Functional Description: 10Base-T/100Base-TX Transceiver

100Base-TX Transmit

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the RGMII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 12.1KΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RGMII format and provided as the input data to the MAC.

Scrambler/De-scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

10Base-T Transmit

The 10Base-T output drivers are incorporated into the 100Base-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with a typical amplitude of 2.5V peak for standard 10Base-T mode and 1.75V peak for energy-efficient 10Base-Te mode. The 10Base-T/10Base-Te signals have harmonic contents that are at least 31dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9031RNX decodes a data frame. The receiver clock is maintained active during idle periods in between receiving data frames.

Auto-polarity correction is provided for receive differential pair to automatically swap and fix the incorrect +/- polarity wiring in the cabling.

Functional Description: 1000Base-T Transceiver

The 1000Base-T transceiver is based on a mixed-signal/digital signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancellers, cross-talk cancellers, precision clock recovery scheme, and power efficient line drivers.

The following figure shows a high-level block diagram of a single channel of the 1000Base-T transceiver for one of the four differential pairs.

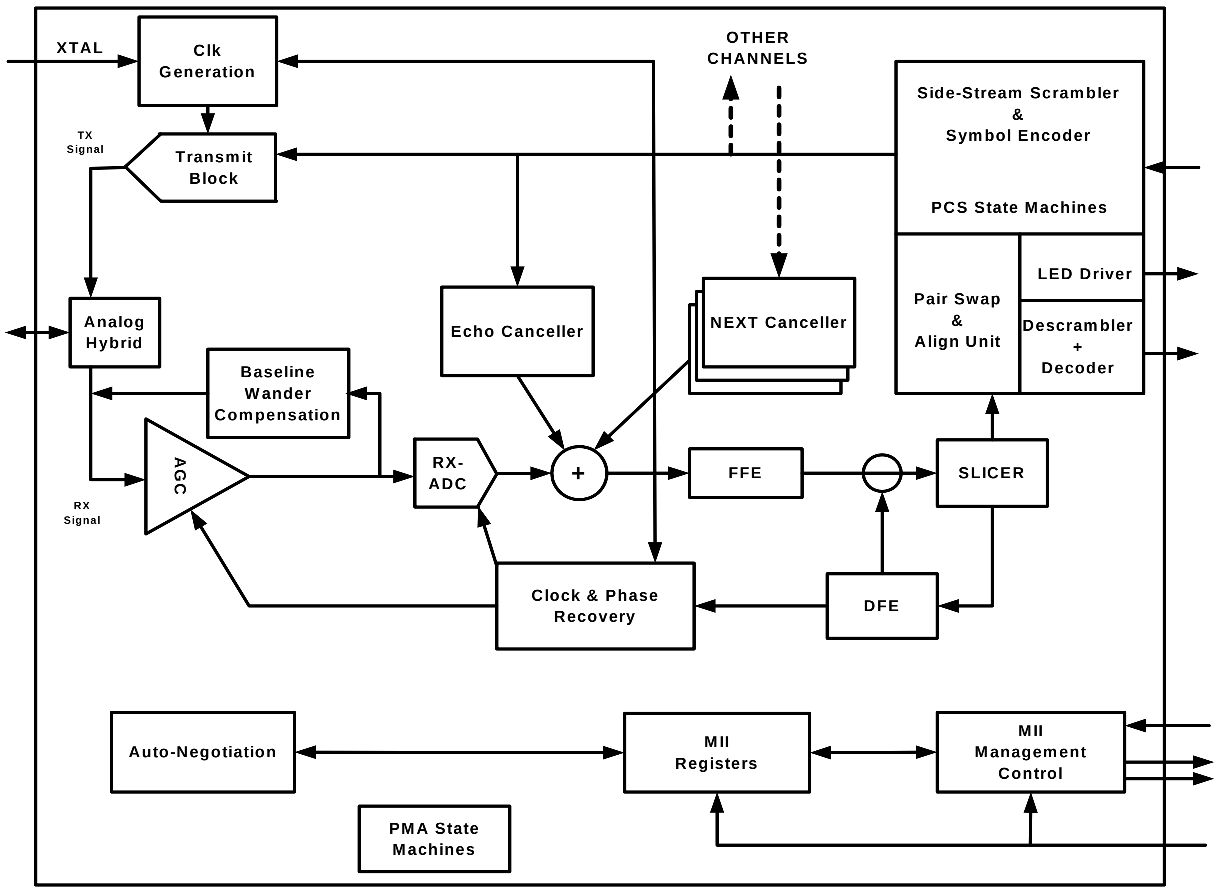


Figure 2. KSZ9031RNX 1000Base-T Transceiver Block Diagram – Single Channel

Analog Echo Cancellation Circuit

In 1000Base-T mode, the analog echo cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10Base-T/100Base-TX mode.

Automatic Gain Control (AGC)

In 1000Base-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

Analog-to-Digital Converter (ADC)

In 1000Base-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10Base-T/100Base-TX mode.

Timing Recovery Circuit

In 1000Base-T mode, the mixed-signal clock recovery circuit, together with the digital phase locked loop, is used to recover and track the incoming timing information from the received data. The digital phase locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000Base-T slave PHY is required to transmit the exact receive clock frequency recovered from the received data back to the 1000Base-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. Additionally, this helps to facilitate echo cancellation and NEXT removal.

Adaptive Equalizer

In 1000Base-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid due to impedance mismatch. The KSZ9031RNX employs a digital echo canceller to further reduce echo components on the receive signal.

In 1000Base-T mode, the data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high frequency cross-talk coming from adjacent wires. The KSZ9031RNX employs three NEXT cancellers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10Base-T/100Base-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

Trellis Encoder and Decoder

In 1000Base-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9031RNX is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order and polarity have to be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and then de-scrambled into 8-bit data.

Functional Description: 10/100/1000 Transceiver Features

Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9031RNX and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and then assigns the MDI/MDI-X pair mapping of the KSZ9031RNX accordingly.

The following table shows the KSZ9031RNX 10/100/1000 pin-out assignments for MDI/MDI-X pin mapping.

Pin (RJ-45 pair)	MDI			MDI-X		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
TXRXP/M_A (1,2)	A+/-	TX+/-	TX+/-	B+/-	RX+/-	RX+/-
TXRXP/M_B (3,6)	B+/-	RX+/-	RX+/-	A+/-	TX+/-	TX+/-
TXRXP/M_C (4,5)	C+/-	Not used	Not used	D+/-	Not used	Not used
TXRXP/M_D (7,8)	D+/-	Not used	Not used	C+/-	Not used	Not used

Table 1. MDI / MDI-X Pin Mapping

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 1Ch, bit [6]. MDI and MDI-X mode is set by register 1Ch, bit [7] if Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Pair- Swap, Alignment, and Polarity Check

In 1000Base-T mode, the KSZ9031RNX

- Detects incorrect channel order and automatically restore the pair order for the A, B, C, D pairs (four channels)
- Supports 50±10ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected 4-pairs of data symbols are synchronized

Incorrect pair polarities for receive differential signals are automatically corrected for all speeds.

Wave Shaping, Slew Rate Control and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000Base-T, a special partial response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100Base-TX, a simple slew rate control method is used to minimize EMI.
- For 10Base-T, pre-emphasis is used to extend the signal quality through the cable.

PLL Clock Synthesizer

The KSZ9031RNX generates 125 MHz, 25 MHz and 10 MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

Auto-Negotiation

The KSZ9031RNX conforms to the Auto-Negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-Negotiation allows UTP (Unshielded Twisted Pair) link partners to select the highest common mode of operation.

During Auto-Negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 1000Base-T, full-duplex
- Priority 2: 1000Base-T, half-duplex
- Priority 3: 100Base-TX, full-duplex
- Priority 4: 100Base-TX, half-duplex
- Priority 5: 10Base-T, full-duplex
- Priority 6: 10Base-T, half-duplex

If Auto-Negotiation is not supported or the KSZ9031RNX link partner is forced to bypass Auto-Negotiation for 10Base-T and 100Base-TX modes, then the KSZ9031RNX sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9031RNX to establish a link by listening for a fixed signal protocol in the absence of Auto-Negotiation advertisement protocol.

The Auto-Negotiation link up process is shown in the following flow chart.

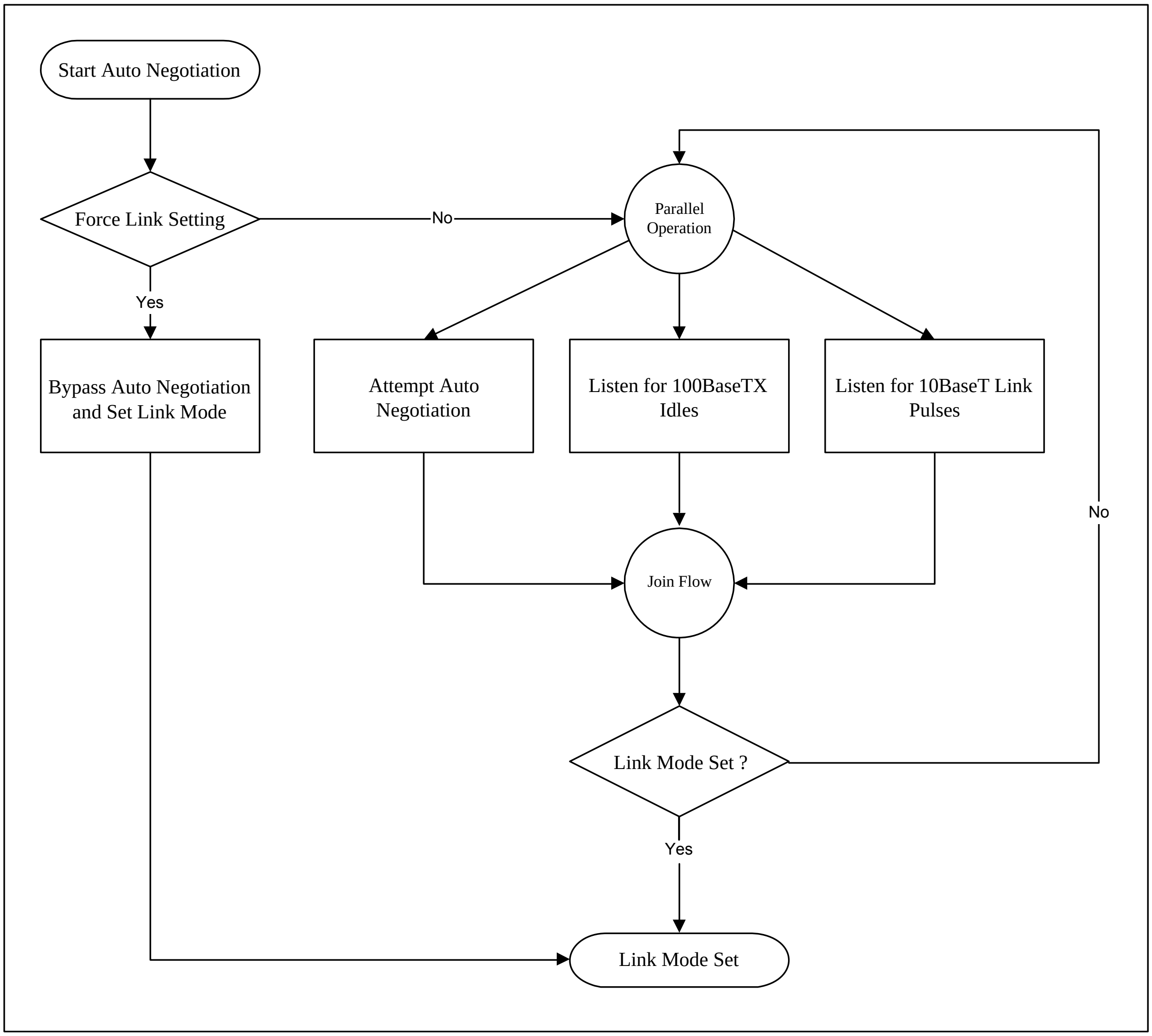


Figure 3. Auto-Negotiation Flow Chart

For 1000Base-T mode, Auto-Negotiation is always required to establish link. During 1000Base-T Auto-Negotiation, Master and Slave configuration is first resolved between link partners, and then link-up is established with the highest common capabilities between link partners.

Auto-Negotiation is enabled by default after power-up or hardware reset. Afterwards, Auto-Negotiation can be enabled or disabled through register 0h, bit [12]. If Auto-Negotiation is disabled, the speed is set by register 0h, bits [6, 13] and the duplex is set by register 0h, bit [8].

If the speed is changed on the fly, the link goes down, and then Auto-Negotiation and parallel detection will initiate until a common speed between KSZ9031RNX and its link partner is re-established for link-up.

If link is already established, and there is no change of speed on the fly, then the changes (e.g., duplex and PAUSE capabilities) will not take effect unless either Auto-Negotiation is restarted through register 0h, bit [9], or a link down to link up transition occurs (i.e., disconnecting and reconnecting the cable).

After Auto-Negotiation is completed, the link status is updated in register 1h, bit [2], and the link partner capabilities are updated in registers 5h, 6h, 8h and Ah.

The Auto-Negotiation finite state machines employ interval timers to manage the Auto-Negotiation process. The duration of these timers under normal operating conditions are summarized in the following table.

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst interval	16 ms
Transmit Pulse interval	68 us
FLP detect minimum time	17.2 us
FLP detect maximum time	185 us
Receive minimum Burst interval	6.8 ms
Receive maximum Burst interval	112 ms
Data detect minimum interval	35.4 us
Data detect maximum interval	95 us
NLP test minimum interval	4.5 ms
NLP test maximum interval	30 ms
Link Loss time	52 ms
Break Link time	1480 ms
Parallel Detection wait time	830 ms
Link Enable wait time	1000 ms

Table 2. Auto-Negotiation Timers

RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) supports on-chip data-to-clock delay timing per the RGMII Version 2.0 Specification, with programming options for external delay timing and to make adjustment and correction to Tx and Rx timing paths.

RGMII provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for the IEEE Gigabit Media Independent Interface (GMII) to 12 pins for RGMII.
- All speeds (10 Mbps, 100 Mbps, and 1000 Mbps) are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

In RGMII operation, the RGMII pins function as follow:

- The MAC sources the transmit reference clock, TXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, RXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- For 1000Base-T, the transmit data, TXD[3:0], is presented on both edges of TXC, and the received data, RXD[3:0], is clocked out on both edges of the recovered 125 MHz clock, RXC.
- For 10Base-T/100Base-TX, the MAC will hold TX_CTL low until both PHY and MAC operate at the same speed. During the speed transition, the receive clock will be stretched on either positive or negative pulse to ensure that no clock glitch is presented to the MAC at any time.
- TX_ER and RX_ER are combined with TX_EN and RX_DV, respectively, to form TX_CTL and RX_CTL. These two RGMII control signals are valid at the falling clock edge.

After power-up or reset, the KSZ9031RNX is configured to RGMII mode if the MODE[3:0] strap-in pins are set to one of the RGMII mode capability options. See Strapping Options section for available options.

The KSZ9031RNX has the option to output a 125 MHz reference clock on the CLK125_NDO pin. This clock provides a lower cost reference clock alternative for RGMII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

RGMII Signal Definition

The following table describes the RGMII signals. Refer to the RGMII Version 2.0 Specification for detailed information.

RGMII Signal Name (per spec)	RGMII Signal Name (per KSZ9031RNX)	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TXC	GTX_CLK	Input	Output	Transmit Reference Clock (125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
TX_CTL	TX_EN	Input	Output	Transmit Control
TXD[3:0]	TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	RX_CLK	Output	Input	Receive Reference Clock (125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
RX_CTL	RX_DV	Output	Input	Receive Control
RXD[3:0]	RXD[3:0]	Output	Input	Receive Data [3:0]

Table 3. RGMII Signal Definition

RGMII Signal Diagram

The KSZ9031RNX RGMII pin connections to the MAC are shown in the following figure.

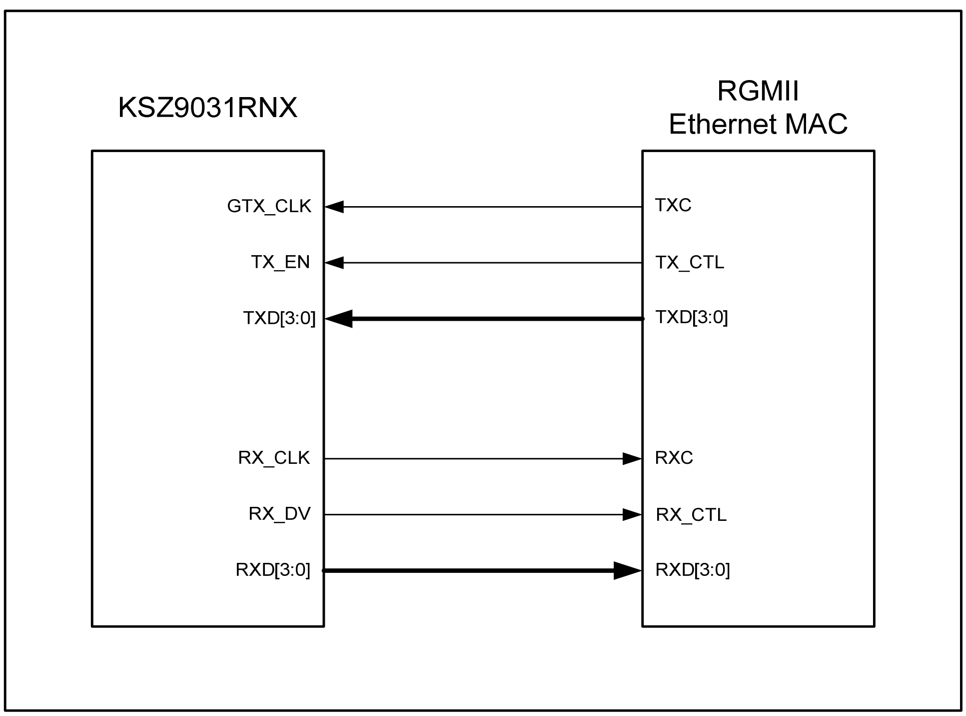


Figure 4. KSZ9031RNX RGMII Interface

RGMII Pad Skew Registers

Pad skew registers are available for all RGMII pins (clocks, control signals and data bits) to provide programming options to adjust or correct the timing relationship for each RGMII pin. With RGMII being a source synchronous bus interface, the timing relationship needs to be maintained only within the RGMII pin's respective timing group.

- RGMII transmit timing group pins: GTX_CLK, TX_EN, TXD[3:0]
- RGMII receive timing group pins: RX_CLK, RX_DV, RXD[3:0]

The following four registers located at MMD Address 2h are provided for pad skew programming.

Address	Name	Description	Mode	Default
MMD Address 2h, Register 4h – RGMII Control Signal Pad Skew				
2.4.15:8	Reserved	Reserved	RW	0000_0000
2.4.7:4	RX_DV pad skew	RGMII RX_CTL output pad skew control (0.06ns/step)	RW	0111
2.4.3:0	TX_EN pad skew	RGMII TX_CTL input pad skew control (0.06ns/step)	RW	0111
MMD Address 2h, Register 5h – RGMII RX Data Pad Skew				
2.5.15:12	RXD3 pad skew	RGMII RXD3 output pad skew control (0.06ns/step)	RW	0111
2.5.11:8	RXD2 pad skew	RGMII RXD2 output pad skew control (0.06ns/step)	RW	0111
2.5.7:4	RXD1 pad skew	RGMII RXD1 output pad skew control (0.06ns/step)	RW	0111
2.5.3:0	RXD0 pad skew	RGMII RXD0 output pad skew control (0.06ns/step)	RW	0111
MMD Address 2h, Register 6h – RGMII TX Data Pad Skew				
2.6.15:12	TXD3 pad skew	RGMII TXD3 output pad skew control (0.06ns/step)	RW	0111
2.6.11:8	TXD2 pad skew	RGMII TXD2 output pad skew control (0.06ns/step)	RW	0111
2.6.7:4	TXD1 pad skew	RGMII TXD1 output pad skew control (0.06ns/step)	RW	0111
2.6.3:0	TXD0 pad skew	RGMII TXD0 output pad skew control (0.06ns/step)	RW	0111
MMD Address 2h, Register 8h – RGMII Clock Pad Skew				
2.8.15:10	Reserved	Reserved	RW	0000_00
2.8.9:5	GTX_CLK pad skew	RGMII GTX_CLK input pad skew control (0.06ns/step)	RW	01_111
2.8.4:0	RX_CLK pad skew	RGMII RX_CLK output pad skew control (0.06ns/step)	RW	0_1111

Table 4. RGMII Pad Skew Registers

The RGMII control signals and data bits have 4-bit skew settings, while the RGMII clocks have 5-bit skew settings.

Each register bit is approximately a 0.06ns step change. A single bit decrement decreases the delay by approximately 0.06ns, while a single bit increment increases the delay by approximately 0.06ns.

The following two tables list the approximate absolute delay for each pad skew (value) setting.

Pad Skew (value)	Delay (ns)
0_0000	-0.90
0_0001	-0.84
0_0010	-0.78
0_0011	-0.72
0_0100	-0.66
0_0101	-0.60
0_0110	-0.54
0_0111	-0.48
0_1000	-0.42
0_1001	-0.36
0_1010	-0.30
0_1011	-0.24
0_1100	-0.18
0_1101	-0.12
0_1110	-0.06
0_1111	No delay adjustment (default value)
1_0000	+0.06
1_0001	+0.12
1_0010	+0.18
1_0011	+0.24
1_0100	+0.30
1_0101	+0.36
1_0110	+0.42
1_0111	+0.48
1_1000	+0.54
1_1001	+0.60
1_1010	+0.66
1_1011	+0.72
1_1100	+0.78
1_1101	+0.84
1_1110	+0.90
1_1111	+0.96

Table 5. Absolute Delay for 5-bit Pad Skew Setting

Pad Skew (value)	Delay (ns)
0000	-0.42
0001	-0.36
0010	-0.30
0011	-0.24
0100	-0.18
0101	-0.12
0110	-0.06
0111	No delay adjustment (default value)
1000	+0.06
1001	+0.12
1010	+0.18
1011	+0.24
1100	+0.30
1101	+0.36
1110	+0.42
1111	+0.48

Table 6. Absolute Delay for 4-bit Pad Skew Setting

When computing the RGMII timing relationships, delays along the entire data path need to be aggregated to determine the total delay to be used for comparison between RGMII pins within their respective timing group. For the transmit data path, total delay includes MAC output delay, MAC-to-PHY PCB routing delay, and PHY (KSZ9031RNX) input delay and skew setting (if any). For the receive data path, the total delay includes PHY (KSZ9031RNX) output delay, PHY-to-MAC PCB routing delay, and MAC input delay and skew setting (if any).

After power-up or reset, the KSZ9031RNX defaults to the following timings at its RGMII I/0 pins to support on-chip data-to-clock skew timing per the RGMII Version 2.0 Specification:

- Transmit Inputs: GTX_CLK clock is in sync within +/-500ps of TX_EN and TXD[3:0]
- Receive outputs: RX_CLK is delayed about 1.2ns with respect to RX_DV and RXD[3:0]

The above default RGMII timings imply:

- RX_CLK clock skew is set by the KSZ9031RNX default register settings.
- GTX_CLK clock skew is to be provided by the MAC.
- No PCB delay is required for GTX_CLK and RX_CLK clocks.

The following examples show how to read/write to MMD Address 2h, Register 8h for the RGMII GTX_CLK and RX_CLK skew settings. MMD register access is via the direct portal registers Dh and Eh. For more programming details, refer to MMD Registers – Description section.

- Read back value of MMD Address 2h, Register 8h.
  - Write register 0xd = 0x0002 // Select MMD Device Address 2h
  - Write register 0xe = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write register 0xd = 0x4002 // Select Register Data for MMD Device Address 2h, Register 8h
  - Read register 0xe // Read value of MMD Device Address 2h, Register 8h

- Write value 0x03ff (delay GTX_CLK and RX_CLK pad skews to their maximum values) to MMD Address 2h, Register 8h
  - Write register 0xd = 0x0002 // Select MMD Device Address 2h
  - Write register 0xe = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write register 0xd = 0x4002 // Select Register Data for MMD Device Address 2h, Register 8h
  - Write register 0xe = 0x03ff // Write value 0x03ff to MMD Device Address 2h, Register 8h

RGMII In-band Status

The KSZ9031RNX provides in-band status to the MAC during the inter-frame gap when RX_DV is de-asserted. RGMII in-band status is always enabled after power-up.

The in-band status is sent to the MAC using the RXD[3:0] data pins, and is described in the following table.

RX_DV	RXD3	RXD[2:1]	RXD0
0 (valid only when RX_DV is low)	Duplex Status 0 = half-duplex 1 = full-duplex	RX_CLK clock speed 00 =2.5 MHz (10Mbps) 01 =25 MHz (100Mbps) 10 =125 MHz (1000Mbps) 11 = reserved	Link Status 0 = Link down 1 = Link up

Table 7. RGMII In-Band Status

MII Management (MIIM) Interface

The KSZ9031RNX supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9031RNX. A external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further detail on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with one or more KSZ9031RNX device. Each KSZ9031RNX device is assigned a unique PHY address between 0h and 7h by the PHYAD[2:0] strapping pins.
- A 32-registers address space for direct access to IEEE Defined Registers and Vendor Specific Registers, and for indirect access to MMD Addresses and Registers. See Register Map section.

PHY address 0h is supported as the unique PHY address only; it is not supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (e.g., using PHY address 0h to set register 0h to a value of 0x1940 to set bit [11] to a value of one to enable Software Power Down). Instead, separate write commands are used to program each PHY device.

The following table shows the MII Management frame format for the KSZ9031RNX.

	Preamble	**Start of Frame**	**Read/Write OP Code**	**PHY Address Bits [4:0]**	**REG Address Bits [4:0]**	**TA**	**Data Bits [15:0]**	**Idle**
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 8. MII Management Frame Format – for KSZ9031RNX

Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9031RNX PHY register. Bits [15:8] of register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit [14] of register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9031RNX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

LED Mode

The KSZ9031RNX provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in pin. It is latched at power-up/reset and is defined as follows:

- Pull-up: Single LED Mode
- Pull-down: Tri-color Dual LED Mode

Single LED Mode

In Single LED Mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in the following table.

LED pin	Pin State	LED Definition	Link / Activity
LED2	H	OFF	Link off
	L	ON	Link on (any speed)
LED1	H	OFF	No Activity
	Toggle	Blinking	Activity (RX, TX)

Table 9. Single LED Mode – Pin Definition

Tri-color Dual LED Mode

In Tri-color Dual LED Mode, the Link and Activity status are indicated by the LED2 pin for 1000Base-T, by the LED1 pin for 100Base-TX, and by both LED2 and LED1 pin, working in conjunction, for 10Base-T. This is summarized in the following table.

LED Pin (State)		LED Pin (Definition)		Link / Activity
LED2	**LED1**	**LED2**	**LED1**	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link / No Activity
Toggle	Toggle	Blinking	Blinking	10 Link / Activity (RX, TX)

Table 10. Tri-color Dual LED Mode – Pin Definition

Each LED output pin can directly drive a LED with a series resistor (typically 220Ω to 470Ω).

Loopback Mode

The KSZ9031RNX supports the following loopback operations to verify analog and/or digital data paths.

- Local (Digital) Loopback
- Remote (Analog) Loopback

Local (Digital) Loopback

This loopback mode checks the RGMII transmit and receive data paths between KSZ9031RNX and external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

The loopback data path is shown in the following figure.

1) RGMII MAC transmits frames to KSZ9031RNX.
2) Frames are wrapped around inside KSZ9031RNX.
3) KSZ9031RNX transmits frames back to RGMII MAC.

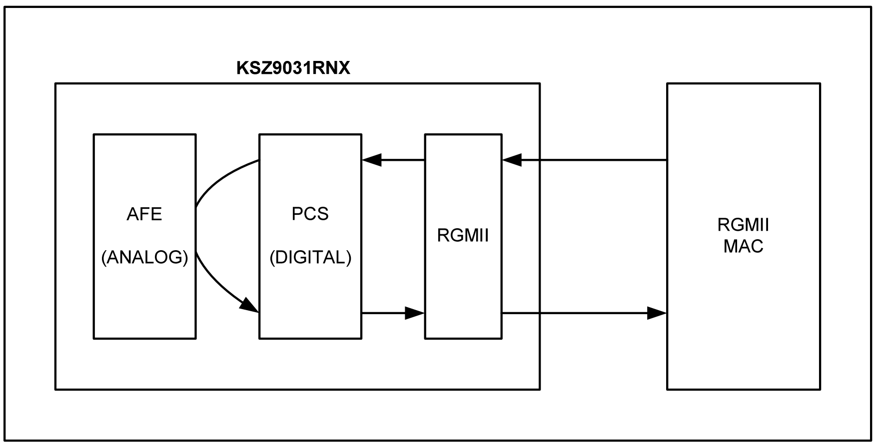


Figure 5. Local (Digital) Loopback

The following programming steps and register settings are used for Local Loopback mode.

For 1000 Mbps loopback,

1) Set Register 0h,
   - Bit [14] = 1 // Enable Local Loopback mode
   - Bits [6, 13] = 10 // Select 1000Mbps speed
   - Bit [12] = 0 // Disable Auto-Negotiation
   - Bit [8] = 1 // Select full-duplex mode
2) Set Register 9h,
   - Bit [12] = 1 // Enable Master-Slave manual configuration
   - Bit [11] = 0 // Select Slave configuration (must use for this loopback mode)

For 10/100 Mbps loopback,

1) Set Register 0h,
   - Bit [14] = 1 // Enable Local Loopback mode
   - Bits [6, 13] = 00 / 01 // Select 10Mbps / 100Mbps speed
   - Bit [12] = 0 // Disable Auto-Negotiation
   - Bit [8] = 1 // Select full-duplex mode

Remote (Analog) Loopback

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ9031RNX and its link partner, and is supported for 1000Base-T full-duplex mode only.

The loopback data path is shown in the following figure.

1) Gigabit PHY Link Partner transmits frames to KSZ9031RNX.
2) Frames are wrapped around inside KSZ9031RNX.
3) KSZ9031RNX transmits frames back to Gigabit PHY Link Partner.

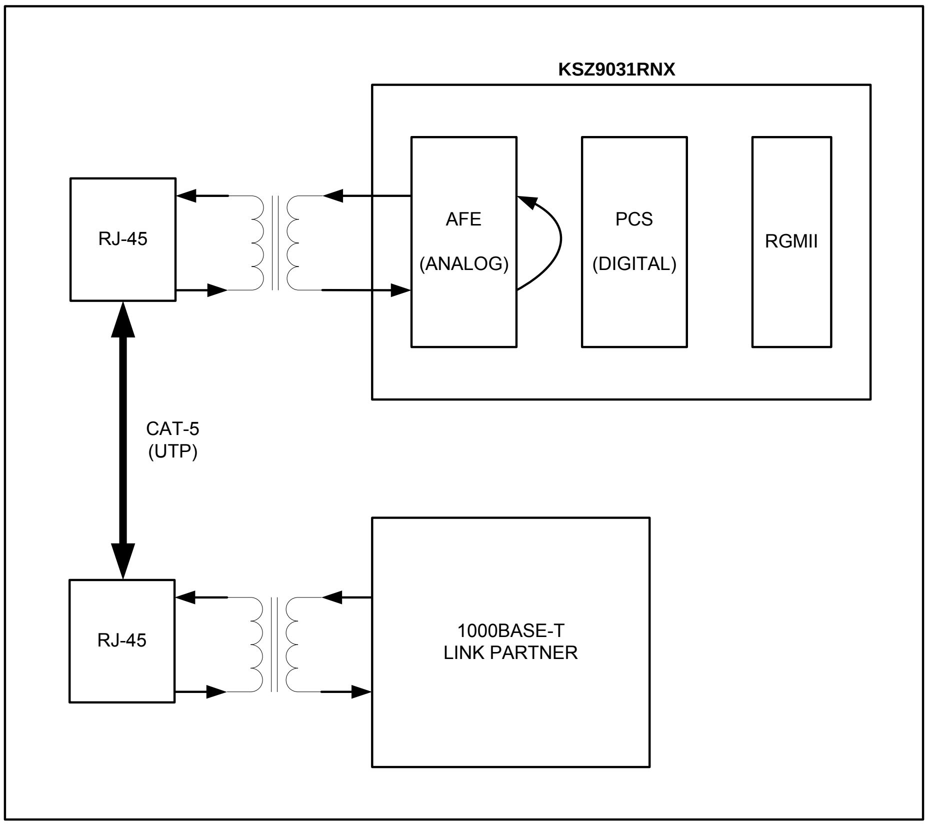


Figure 6. Remote (Analog) Loopback

The following programming steps and register settings are used for Remote Loopback mode.

1) Set Register 0h,
   - Bits [6, 13] = 10 // Select 1000Mbps speed
   - Bit [12] = 0 // Disable Auto-Negotiation
   - Bit [8] = 1 // Select full-duplex mode

   Or just simply auto-negotiate and link up at 1000Base-T full-duplex mode with link partner

2) Set Register 11h,
   - Bit [8] = 1 // Enable Remote Loopback mode

LinkMD® Cable Diagnostic

The LinkMD® function utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits and impedance mismatches.

LinkMD® operates by sending a pulse of known amplitude and duration down the selected differential pair, and then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD® function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD® is initiated by accessing register 12h, the LinkMD® - Cable Diagnostic Register, in conjunction with register 1Ch, the Auto MDI/MDI-X Register. The latter register is needed to disable the auto MDI/MDI-X function before executing the LinkMD® test. Additionally, a software reset (Reg. 0h, bit [15] = 1) should be performed before and after executing the LinkMD® test. The reset helps to ensure the KSZ9031RNX is in the normal operating state before and after the test.

NAND Tree Support

The KSZ9031RNX provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up / reset with the MODE[3:0] strap-in pins set to “0100”.

The following table lists the NAND tree pin order.

Pin	Description
LED2	Input
LED1	Input
TXD0	Input
TXD1	Input
TXD2	Input
TXD3	Input
GTX_CLK	Input
TX_EN	Input
RX_DV	Input
RX_CLK	Input
INT_N	Input
MDC	Input
MDIO	Input
CLK125_NDO	Output

Table 11. NAND Tree Test Pin Order – for KSZ9031RNX

Power Management

The KSZ9031RNX offers the following power management modes:

Energy Detect Power Down Mode

Energy Detect Power Down (EDPD) Mode is used to further reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a one to MMD address 1Ch, register 23h, bit [0], and is in effect when auto-negotiation mode is enabled and cable is disconnected (no link).

In EDPD Mode, the KSZ9031RNX shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Further power reduction is achieved by extending the time interval in between transmission of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure two link partners in the same low power state and with Auto MDI/MDI-X disabled can wake up when the cable is connected between them. By default, EDPD Mode is disabled after power-up.

Software Power Down Mode

This mode is used to power down the KSZ9031RNX device when it is not in use after power-up. Software Power Down (SPD) Mode is enabled by writing a one to register 0h, bit [11]. In the SPD state, the KSZ9031RNX disables all internal functions, except for the MII management interface. The KSZ9031RNX exits the SPD state after a zero is written to register 0h, bit [11].

Chip Power Down Mode

This mode provides the lowest power state for the KSZ9031RNX device when it is not in use and is mounted on the board. Chip Power Down (CPD) Mode is enabled after power-up / reset with the MODE[3:0] strap-in pins set to “0111”. The KSZ9031RNX exits CPD Mode after a hardware reset is applied to the RESET_N pin with the MODE[3:0] strap-in pins set to an operating mode other than CPD Mode.

Energy Efficient Ethernet (EEE)

The KSZ9031RNX implements Energy Efficient Ethernet (EEE) as described per IEEE Standard 802.3az for line signaling by the four differential pairs (analog side) and per Multisource Agreement (MSA) of collaborating Gigabit Ethernet chip vendors for the RGMII (digital side), which is based on the IEEE Standard’s EEE implementation for GMII (1000Mbps) and MII (100Mbps). The specification is defined around an EEE-compliant MAC on the host side and an EEE-compliant Link Partner on the line side that support special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak for as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as Low Power Idle (LPI) mode or state.

During LPI mode, the copper link will respond automatically upon receiving traffic and resume normal PHY operation immediately, without blockage of traffic or loss of packet – exiting LPI mode and returning to normal 100/1000Mbps operating mode. Wake-up times are <16us for 1000Base-T and <30us for 100Base-TX.

The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

The KSZ9031RNX has the EEE function disabled as the power-up default setting. The EEE function is enabled by setting the following EEE Advertisement bits at MMD address 7h, register 3Ch, and then followed by re-starting Auto-Negotiation (writing a ‘1’ to register 0h, bit [9]):

- Bit [2] = 1 // Enable 1000Mbps EEE mode
- Bit [1] = 1 // Enable 100Mbps EEE mode

For standard (non-EEE) 10Base-T mode, Normal Link Pulses (NLPs) with long durations of no AC signal transmission are used already to maintain link during the idle period when there is no traffic activity. For further power saving, the KSZ9031RNX provides the option to enable 10Base-Te mode which saves additional power by reducing the transmitted signal amplitude from 2.5V to 1.75V. To enable 10Base-Te mode, write a one to MMD address 1Ch, register 4h, bit [10].

During LPI mode, Refresh transmissions are used to maintain link and the Quiet periods are when the power savings take place. Approximately, every 20-22 milliseconds a Refresh transmission of 200-220 microseconds is sent to the link partner. The Refresh transmissions and Quiet periods are shown in the following figure.

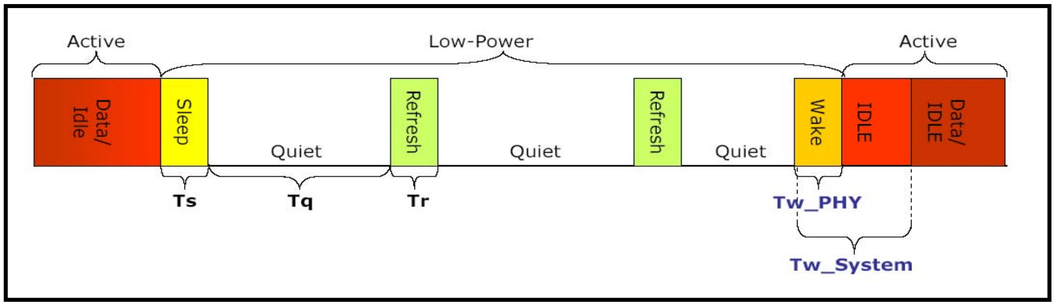


Figure 7. LPI Mode (Refresh transmissions and Quiet periods)

Transmit Direction Control (MAC-to-PHY)

For RGMII – 1000Mbps transmission from MAC-to-PHY, both rising and falling edges of the GTX_CLK clock are used. The KSZ9031RNX uses the TX_EN pin as the RGMII transmit control signal (TX_CTL) to clock in the TX_EN signal on the rising edge and the TX_ER signal on the falling edge, and also uses the TXD[3:0] pins to clock in the TX data low nibble bits [3:0] on the rising edge and the TX data high nibble bits [7:4] on the falling edge.

The KSZ9031RNX enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts TX_EN signal (TX_CTL pin outputs low on rising edge), asserts TX_ER signal (TX_CTL pin outputs high on falling edge), and sets TX data bits [7:0] to “0000_0001” (TXD[3:0] pins output “0001” on rising edge and “0000” on falling edge). The KSZ9031RNX will remain in the 1000Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the TX_EN, TX_ER, or TX data signals from their LPI state values, the KSZ9031RNX will exit the LPI transmit state.

For additional power saving, the GTX_CLK clock can be stopped by the MAC after the RGMII signals for the LPI state have been asserted for 10 or more GTX_CLK clock cycles.

The following figure shows the LPI transition for RGMII transmit in 1000Mbps speed mode.

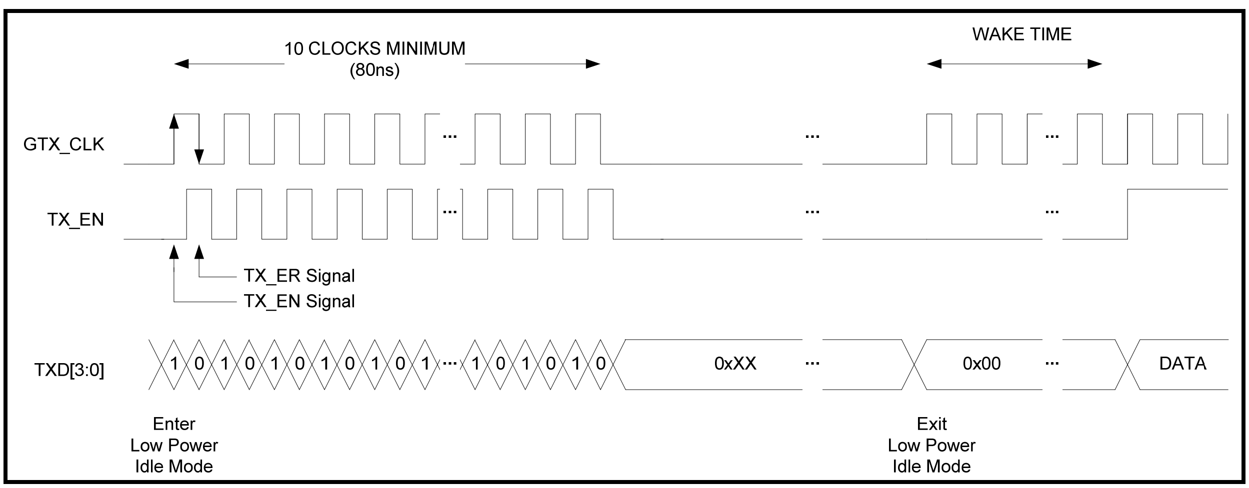


Figure 8. LPI Transition – RGMII (1000Mbps) Transmit

For RGMII – 100Mbps transmission from MAC-to-PHY, both rising and falling edges of the GTX_CLK clock are used. The KSZ9031RNX uses the TX_EN pin as the RGMII transmit control signal (TX_CTL) to clock in the TX_EN signal on the rising edge and the TX_ER signal on the falling edge, and also uses the TXD[3:0] pins to clock in the TX data bits [3:0] on the rising edge.

The KSZ9031RNX enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts TX_EN signal (TX_CTL pin outputs low on rising edge), asserts TX_ER signal (TX_CTL pin outputs high on falling edge), and sets TX data bits [3:0] to “0001” (TXD[3:0] pins output “0001”). The KSZ9031RNX will remain in the 100Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the TX_EN, TX_ER, or TX data signals from their LPI state values, the KSZ9031RNX will exit the LPI transmit state.

For additional power saving, the GTX_CLK clock can be stopped by the MAC after the RGMII signals for the LPI state have been asserted for 10 or more GTX_CLK clock cycles.

The following figure shows the LPI transition for RGMII transmit in 100Mbps speed mode.

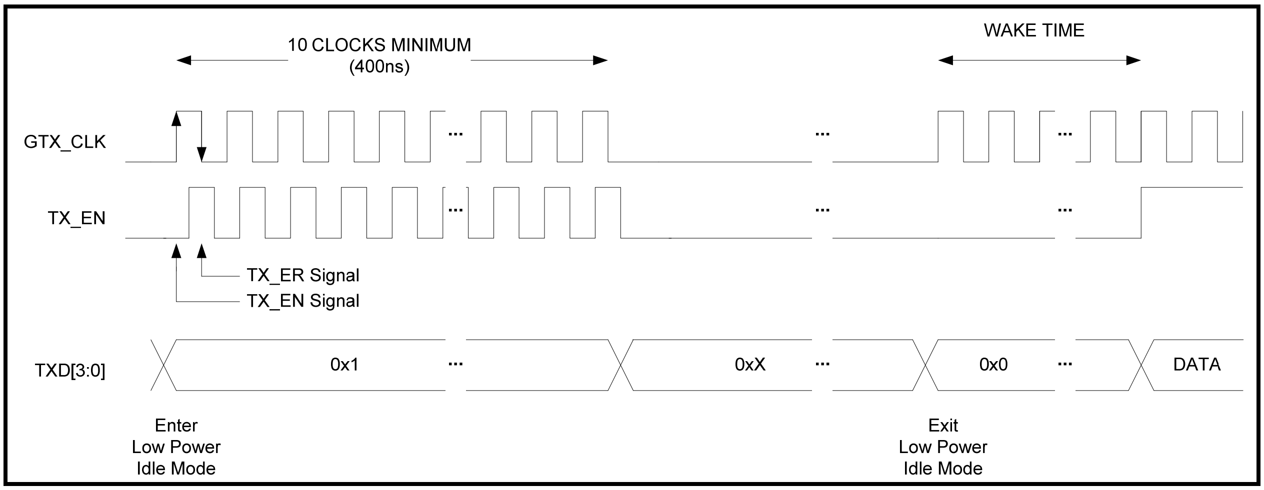


Figure 9. LPI Transition – RGMII (100Mbps) Transmit

Receive Direction Control (PHY-to-MAC)

For RGMII – 1000Mbps transmission from PHY-to-MAC, both rising and falling edges of the RX_CLK clock are used. The KSZ9031RNX uses the RX_DV pin as the RGMII receive control signal (RX_CTL) to clock out the RX_DV signal on the rising edge and the RX_ER signal on the falling edge, and also uses the RXD[3:0] pins to clock out the RX data low nibble bits [3:0] on the rising edge and the RX data high nibble bits [7:4] on the falling edge.

The KSZ9031RNX enters LPI mode for the receive direction upon receiving the /P/ code bit pattern (Sleep/Refresh) from its EEE-compliant link partner, and then will drive RX_DV pin low on rising clock edge and high on falling clock edge to de-assert RX_DV signal and assert RX_ER signal, respectively to the MAC. Also, the RXD[3:0] pins are driven to “0001” on rising clock edge and “0000” on falling clock edge to set the RX data bits [7:0] to “0000_0001”. The KSZ9031RNX will remain in the 1000Mbps receive LPI state while it continues to receive the Refresh from its link partner, and thus will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the KSZ9031RNX receives a non /P/ code bit pattern (non Refresh), it exits the receive LPI state and sets the RX_DV and RXD[3:0] output pins accordingly for a normal frame or normal idle.

The KSZ9031RNX stops the RX_CLK clock output to the MAC after 10 or more RX_CLK clock cycles have occurred in the receive LPI state to provide further power saving.

The following figure shows the LPI transition for RGMII receive in 1000Mbps speed mode.

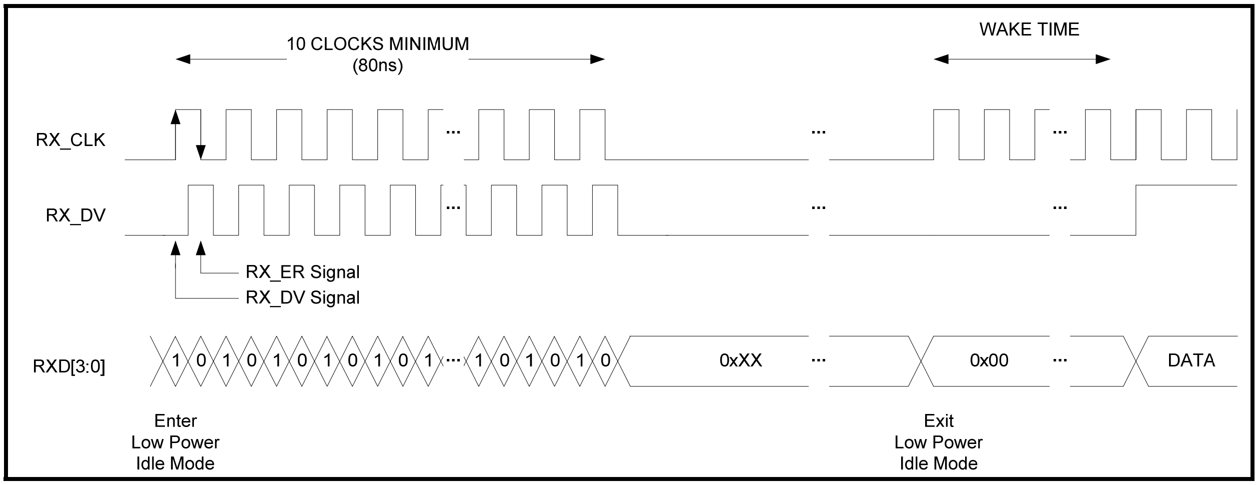


Figure 10. LPI Transition – RGMII (1000Mbps) Receive

For RGMII – 100Mbps transmission from PHY-to-MAC, both rising and falling edges of the RX_CLK clock are used. The KSZ9031RNX uses the RX_DV pin as the RGMII receive control signal (RX_CTL) to clock out the RX_DV signal on the rising edge and the RX_ER signal on the falling edge, and also uses the RXD[3:0] pins to clock out the RX data bits [3:0] on the rising edge.

The KSZ9031RNX enters LPI mode for the receive direction upon receiving the /P/ code bit pattern (Sleep/Refresh) from its EEE-compliant link partner, and then will drive RX_DV pin low on rising clock edge and high on falling clock edge to de-assert RX_DV signal and assert RX_ER signal, respectively to the MAC. Also, the RXD[3:0] pins are driven to “0001”. The KSZ9031RNX will remain in the 100Mbps receive LPI state while it continues to receive the Refresh from its link partner, and thus will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the KSZ9031RNX receives a non /P/ code bit pattern (non Refresh), it exits the receive LPI state and sets the RX_DV and RXD[3:0] output pins accordingly for a normal frame or normal idle.

The KSZ9031RNX stops the RX_CLK clock output to the MAC after 10 or more RX_CLK clock cycles have occurred in the receive LPI state to provide further power saving.

The following figure shows the LPI transition for RGMII receive in 100Mbps speed mode.

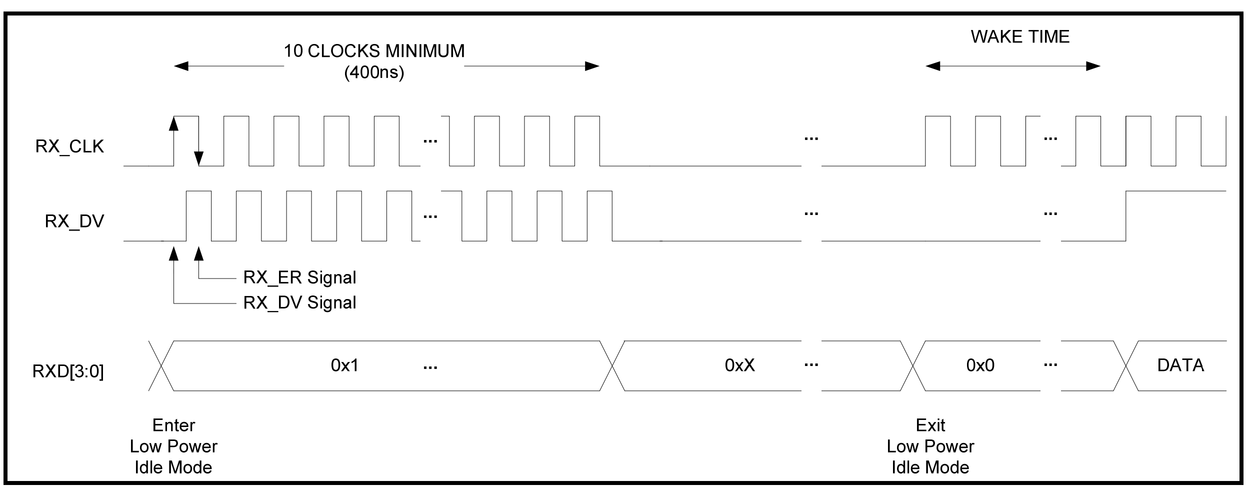


Figure 11. LPI Transition – RGMII (100Mbps) Receive

Registers Associated with EEE

The following MMD registers are provided for EEE configuration and management:

- MMD address 3h, register 0h - PCS EEE – Control Register
- MMD address 3h, register 1h - PCS EEE – Status Register
- MMD address 7h, register 3Ch - EEE Advertisement Register
- MMD address 7h, register 3Dh - EEE Link Partner Advertisement Register

Wake-on-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the “Magic Packet”) that is sent by the remote link partner. The KSZ9031RNX can perform the same WOL function if the MAC address of its associated MAC device is entered into the KSZ9031RNX PHY registers for Magic Packet detection. Upon detection of the Magic Packet, the KSZ9031RNX wakes up the host by driving its Power Management Event (PME) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected PME wake-up detection method.

The KSZ9031RNX provides three methods to trigger a PME wake-up:

- Magic Packet Detection
- Customized Packet Detection
- Link Status Change Detection

Magic Packet Detection

The Magic Packet’s frame format starts with 6-bytes of 0xFFh and is followed by 16 repetitions of the MAC address of its associated MAC device (local MAC device).

When the Magic Packet is detected from its link partner, the KSZ9031RNX asserts its PME output pin low.

The following MMD address 2h registers are provided for Magic Packet detection:

- Magic Packet detection is enabled by writing a one to MMD address 2h, register 10h, bit [6]
- MAC address (for local MAC device) is written to and stored in MMD address 2h, registers 11h – 13h

The KSZ9031RNX does not generate the Magic Packet. The Magic Packet must be provided by the external system.

Customized Packet Detection

The Customized Packet has associated register/bit masks to select which byte or bytes of the first 64-bytes of the packet to utilize in the CRC calculation. As the KSZ9031RNX receives the packet from its link partner, the selected byte(s) for the received packet is/are used to calculate the CRC. The calculated CRC is compared with the expected CRC value written to and stored in the KSZ9031RNX PHY registers in advance. If there is a match, the KSZ9031RNX asserts its PME output pin low.

Four Customized Packets are provided to support four types of wake-up scenarios. A dedicated set of registers is used to configure and enable each Customized Packet.

The following MMD registers are provided for Customized Packet detection:

- Each of the four Customized Packets is enabled via MMD address 2h, register 10h,
  - bit [2] // for Customized Packets, type 0
  - bit [3] // for Customized Packets, type 1
  - bit [4] // for Customized Packets, type 2
  - bit [5] // for Customized Packets, type 3
- 32-bit expected CRCs are written to and stored in:
  - MMD address 2h, registers 14h – 15h // for Customized Packets, type 0
  - MMD address 2h, registers 16h – 17h // for Customized Packets, type 1
  - MMD address 2h, registers 18h – 19h // for Customized Packets, type 2
  - MMD address 2h, registers 1Ah – 1Bh // for Customized Packets, type 3
- Masks to indicate which of the first 64-bytes to utilize in the CRC calculation are set in:
  - MMD address 2h, registers 1Ch – 1Fh // for Customized Packets, type 0
  - MMD address 2h, registers 20h – 23h // for Customized Packets, type 1
  - MMD address 2h, registers 24h – 27h // for Customized Packets, type 2
  - MMD address 2h, registers 28h – 2Bh // for Customized Packets, type 3

- 32-bit calculated CRCs (of receive packet) are stored in:
  - MMD address 2h, registers 30h – 31h // for Customized Packets, type 0
  - MMD address 2h, registers 32h – 33h // for Customized Packets, type 1
  - MMD address 2h, registers 34h – 35h // for Customized Packets, type 2
  - MMD address 2h, registers 36h – 37h // for Customized Packets, type 3

Link Status Change Detection

If Link Status Change Detection is enabled, the KSZ9031RNX asserts its PME output pin low whenever there is a link status change per the following MMD address 2h register bits and their enabled(1) or disabled (0) settings:

- MMD address 2h, register 10h, bit [0] // for link-up detection
- MMD address 2h, register 10h, bit [1] // for link-down detection

The PME output signal is available on either LED1/PME_N1 (pin 17) or INT_N/PME_N2 (pin 38), and is selected and enabled via MMD address 2h, register 2h, bits [8] and [10], respectively. Additionally, MMD address 2h, register 10h, bits [15:14] defines the output function(s) for pins 17 and 38.

The PME output is active low and requires a 1K pull-up to the VDDIO supply. When asserted, the PME output is cleared by disabling the register bit that enabled the PME trigger source (Magic Packet, Customized Packet, Link Status Change).

Typical Current / Power Consumption

The following tables show the typical current consumption by the core (DVDDL, AVDDL, AVDDL_PLL), transceiver (AVDDH) and digital I/Os (DVDDH) supply pins, and the total typical power for the entire KSZ9031RNX device for various nominal operating voltages combinations.

Transceiver (3.3V), Digital I/Os (3.3V)

Condition	1.2V Core (DVDDL, AVDDL, AVDDL_PLL)	3.3V Transceiver (AVDDH)	3.3V Digital I/Os (DVDDH)	Total Chip Power
	mA	mA	mA	mW
1000Base-T Link-up (no traffic)	210	67.4	19.5	538
1000Base-T Full-duplex @ 100% utilization	221	66.3	41.5	621
100Base-TX Link-up (no traffic)	63.6	28.7	13.9	217
100Base-TX Full-duplex @ 100% utilization	63.8	28.6	17.2	228
10Base-T Link-up (no traffic)	7.1	15.9	11.5	99
10Base-T Full-duplex @ 100% utilization	7.7	28.6	13.7	149
EEE Mode – 1000Mbps	43.5	5.7	30.6	172
EEE Mode – 100Mbps (Tx and Rx in LPI)	25.6	5.3	18.1	108
Software Power Down Mode (Reg. 0h.11 =1)	1.0	4.2	9.3	46

Table 12. Typical Current / Power Consumption – Transceiver (3.3V), Digital I/Os (3.3V)

Transceiver (3.3V), Digital I/Os (1.8V)

Condition	1.2V Core (DVDDL, AVDDL, AVDDL_PLL)	3.3V Transceiver (AVDDH)	1.8V Digital I/Os (DVDDH)	Total Chip Power
	mA	mA	mA	mW
1000Base-T Link-up (no traffic)	210	67.4	11.2	494
1000Base-T Full-duplex @ 100% utilization	221	66.3	23.6	526
100Base-TX Link-up (no traffic)	63.6	28.7	8.4	186
100Base-TX Full-duplex @ 100% utilization	63.8	28.6	9.8	189
10Base-T Link-up (no traffic)	7.1	15.9	3.6	67
10Base-T Full-duplex @ 100% utilization	7.7	28.6	5.6	114
EEE Mode – 1000Mbps	43.5	5.7	15.9	100
EEE Mode – 100Mbps (Tx and Rx in LPI)	25.6	5.3	9.1	65
Software Power Down Mode (Reg. 0h.11 =1)	1.0	4.2	5.5	25

Table 13. Typical Current / Power Consumption – Transceiver (3.3V), Digital I/Os (1.8V)

Transceiver (2.5V), Digital I/Os (2.5V)

Condition	1.2V Core (DVDDL, AVDDL, AVDDL_PLL)	2.5V Transceiver (AVDDH – commercial temp only) *	2.5V Digital I/Os (DVDDH)	Total Chip Power
	mA	mA	mA	mW
1000Base-T Link-up (no traffic)	210	58.8	14.7	435
1000Base-T Full-duplex @ 100% utilization	221	57.9	31.5	488
100Base-TX Link-up (no traffic)	63.6	24.9	10.5	165
100Base-TX Full-duplex @ 100% utilization	63.8	24.9	13.0	171
10Base-T Link-up (no traffic)	7.1	11.5	6.3	53
10Base-T Full-duplex @ 100% utilization	7.7	25.3	9.0	95
EEE Mode – 1000Mbps	43.5	4.5	23.6	122
EEE Mode – 100Mbps (Tx and Rx in LPI)	25.6	4.1	13.8	75
Software Power Down Mode (Reg. 0h.11 =1)	1.0	3.1	6.7	26

Note: * 2.5V AVDDH is recommended for commercial temperature range (0°C to +70°C) operation only.

Table 14. Typical Current / Power Consumption – Transceiver (2.5V), Digital I/Os (2.5V)

Transceiver (2.5V), Digital I/Os (1.8V)

Condition	1.2V Core (DVDDL, AVDDL, AVDDL_PLL)	2.5V Transceiver (AVDDH – commercial temp only) *	1.8V Digital I/Os (DVDDH)	Total Chip Power
	mA	mA	mA	mW
1000Base-T Link-up (no traffic)	210	58.8	11.2	419
1000Base-T Full-duplex @ 100% utilization	221	57.9	23.6	452
100Base-TX Link-up (no traffic)	63.6	24.9	8.4	154
100Base-TX Full-duplex @ 100% utilization	63.8	24.9	9.8	156
10Base-T Link-up (no traffic)	7.1	11.5	3.6	44
10Base-T Full-duplex @ 100% utilization	7.7	25.3	5.6	83
EEE Mode – 1000Mbps	43.5	4.5	15.9	92
EEE Mode – 100Mbps (Tx and Rx in LPI)	25.6	4.1	9.1	57
Software Power Down Mode (Reg. 0h.11 =1)	1.0	3.1	5.5	19

Note: * 2.5V AVDDH is recommended for commercial temperature range (0°C to +70°C) operation only.

Table 15. Typical Current / Power Consumption – Transceiver (2.5V), Digital I/Os (1.8V)

Register Map

The register space within the KSZ9013RNX is comprised of two distinct areas.

- Standard Registers // direct register access
- MDIO Manageable Device (MMD) Registers // indirect register access

The KSZ9031RNX supports the following Standard Registers.

Register Number (Hex)	Description
IEEE Defined Registers	
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Auto-Negotiation Link Partner Next Page Ability
9h	1000Base-T Control
Ah	1000Base-T Status
Bh – Ch	Reserved
Dh	MMD Access – Control
Eh	MMD Access – Register/Data
Fh	Extended Status
Vendor Specific Registers	
10h	Reserved
11h	Remote Loopback
12h	LinkMD® Cable Diagnostic
13h	Digital PMA/PCS Status
14h	Reserved
15h	RXER Counter
16h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch	Auto MDI/MDI-X
1Dh – 1Eh	Reserved
1Fh	PHY Control

Table 16. Standard Registers – supported by KSZ9031RNX

The KSZ9031RNX supports the following MMD Device Addresses and their associated Register Addresses, which makes up the indirect MMD Registers.

Device Address (Hex)	Register Address (Hex)	Description
1h	5Ah	1000Base-T Link-up Time Control
2h	0h	Common Control
	1h	Strap Status
	2h	Operation Mode Strap Override
	3h	Operation Mode Strap Status
	4h	RGMII Control Signal Pad Skew
	5h	RGMII RX Data Pad Skew
	6h	RGMII TX Data Pad Skew
	8h	RGMII Clock Pad Skew
	10h	Wake-On-LAN – Control
	11h	Wake-On-LAN – Magic Packet, MAC-DA-0
	12h	Wake-On-LAN – Magic Packet, MAC-DA-1
	13h	Wake-On-LAN – Magic Packet, MAC-DA-2
	14h	Wake-On-LAN – Customized Packet, Type-0, Expected-CRC-0
	15h	Wake-On-LAN – Customized Packet, Type-0, Expected-CRC-1
	16h	Wake-On-LAN – Customized Packet, Type-1, Expected-CRC-0
	17h	Wake-On-LAN – Customized Packet, Type-1, Expected-CRC-1
	18h	Wake-On-LAN – Customized Packet, Type-2, Expected-CRC-0
	19h	Wake-On-LAN – Customized Packet, Type-2, Expected-CRC-1
	1Ah	Wake-On-LAN – Customized Packet, Type-3, Expected-CRC-0
	1Bh	Wake-On-LAN – Customized Packet, Type-3, Expected-CRC-1
	1Ch	Wake-On-LAN – Customized Packet, Type-0, Mask-0
	1Dh	Wake-On-LAN – Customized Packet, Type-0, Mask-1
	1Eh	Wake-On-LAN – Customized Packet, Type-0, Mask-2
	1Fh	Wake-On-LAN – Customized Packet, Type-0, Mask-3
	20h	Wake-On-LAN – Customized Packet, Type-1, Mask-0
	21h	Wake-On-LAN – Customized Packet, Type-1, Mask-1
	22h	Wake-On-LAN – Customized Packet, Type-1, Mask-2
	23h	Wake-On-LAN – Customized Packet, Type-1, Mask-3
	24h	Wake-On-LAN – Customized Packet, Type-2, Mask-0
	25h	Wake-On-LAN – Customized Packet, Type-2, Mask-1
	26h	Wake-On-LAN – Customized Packet, Type-2, Mask-2
	27h	Wake-On-LAN – Customized Packet, Type-2, Mask-3
	28h	Wake-On-LAN – Customized Packet, Type-3, Mask-0
	29h	Wake-On-LAN – Customized Packet, Type-3, Mask-1
	2Ah	Wake-On-LAN – Customized Packet, Type-3, Mask-2
	2Bh	Wake-On-LAN – Customized Packet, Type-3, Mask-3
3h	0h	PCS EEE – Control
	1h	PCS EEE – Status

Device Address (Hex)	Register Address (Hex)	Description
7h	3Ch	EEE Advertisement
	3Dh	EEE Link Partner Advertisement
1Ch	4h	Analog Control 4
	23h	EDPD Control

Table 17. MMD Registers – supported by KSZ9031RNX

Standard Registers

Standard Registers provide direct read/write access to a 32-register address space, as defined per Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16-registers (registers 0h to Fh) are defined per the IEEE specification, while the remaining 16-registers (registers 10h to 1Fh) are defined specific to the PHY vendor.

IEEE Defined Registers – Descriptions

Address	Name	Description	Mode(1)	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software PHY reset 0 = Normal operation This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.14	Loop-back	1 = Loop-back mode 0 = Normal operation	RW	0
0.13	Speed Select (LSB)	[0.6, 0.13] [1,1] = Reserved [1,0] = 1000 Mbps [0,1] = 100 Mbps [0,0] = 10 Mbps This bit is ignored if Auto-Negotiation is enabled (Reg. 0.12 = 1).	RW	0
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation process 0 = Disable Auto-Negotiation process If enabled, Auto-Negotiation result overrides settings in Reg. 0.13, 0.8 and 0.6.	RW	1
0.11	Power Down	1 = Power down mode 0 = Normal operation	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from RGMII 0 = Normal operation	RW	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Normal operation. This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	1
0.7	Reserved	Reserved	RW	0

Address	Name	Description	Mode(1)	Default
0.6	Speed Select (MSB)	[0.6, 0.13] [1,1] = Reserved [1,0] = 1000 Mbps [0,1] = 100 Mbps [0,0] = 10 Mbps This bit is ignored if Auto-Negotiation is enabled (Reg. 0.12 = 1).	RW	Set by MODE[3:0] strapping pins. See "Strapping Options" section for details.
0.5:0	Reserved	Reserved	RO	00_0000
Register 1h – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full-Duplex	1 = Capable of 100 Mbps full-duplex 0 = Not capable of 100 Mbps full-duplex	RO	1
1.13	100Base-TX Half-Duplex	1 = Capable of 100 Mbps half-duplex 0 = Not capable of 100 Mbps half-duplex	RO	1
1.12	10Base-T Full-Duplex	1 = Capable of 10 Mbps full-duplex 0 = Not capable of 10 Mbps full-duplex	RO	1
1.11	10Base-T Half-Duplex	1 = Capable of 10 Mbps half-duplex 0 = Not capable of 10 Mbps half-duplex	RO	1
1.10:9	Reserved	Reserved	RO	00
1.8	Extended Status	1 = Extended Status Info in Reg. 15h. 0 = No Extended Status Info in Reg. 15h.	RO	1
1.7	Reserved	Reserved	RO	0
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform Auto-Negotiation 0 = Not capable to perform Auto-Negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capability registers	RO	1
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1h	RO	0022h

Address	Name	Description	Mode(1)	Default
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1h	RO	0001_01
3.9:4	Model Number	Six-bit manufacturer's model number	RO	10_0010
3.3:0	Revision Number	Four-bit manufacturer's revision number	RO	Indicates silicon revision
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability.	RW	0
4.14	Reserved	Reserved	RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved	Reserved	RO	0
4.11:10	Pause	[4.11, 4.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device)	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100Base-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	1
4.7	100Base-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RW	1
4.6	10Base-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved		RO	0

Address	Name	Description	Mode[1]	Default
5.11:10	Pause	[5.11, 5.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device)	RW	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100 Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0000
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved	Reserved	RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has Auto-Negotiation capability 0 = Link partner does not have Auto-Negotiation capability	RO	0
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved	Reserved	RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0

Address	Name	Description	Mode(1)	Default
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8h – Auto-Negotiation Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field		RO	000_0000_0000
Register 9h – 1000Base-T Control				
9.15:13	Test Mode Bits	Transmitter test mode operations [9.15:13] Mode [000] Normal Operation [001] Test mode 1 –Transmit waveform test [010] Test mode 2 –Transmit jitter test in Master mode [011] Test mode 3 –Transmit jitter test in Slave mode [100] Test mode 4 –Transmitter distortion test [101] Reserved, operations not identified [110] Reserved, operations not identified [111] Reserved, operations not identified	RW	000
9.12	MASTER-SLAVE Manual Config Enable	1 = Enable MASTER-SLAVE Manual configuration value 0 = Disable MASTER-SLAVE Manual configuration value	RW	0
9.11	MASTER-SLAVE Manual Config Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation This bit is ignored if MASTER-SLAVE Manual Config is disabled (Reg. 9.12 = 0).	RW	0

Address	Name	Description	Mode(1)	Default
9.10	Port Type	1 = Indicate the preference to operate as multiport device **(MASTER)** 0 = Indicate the preference to operate as single-port device (**SLAVE**) This bit is valid only if the MASTER-SLAVE Manual Config Enable bit is disabled (Reg. 9.12 = 0).	RW	0
9.9	1000Base-T Full-Duplex	1 = Advertise PHY is 1000Base-T full-duplex capable 0 = Advertise PHY is not 1000Base-T full-duplex capable	RW	1
9.8	1000Base-T Half-Duplex	1 = Advertise PHY is 1000Base-T half-duplex capable 0 = Advertise PHY is not 1000Base-T half-duplex capable	RW	Set by MODE[3:0] strapping pins. See "Strapping Options" section for details.
9.7:0	Reserved	Write as 0, ignore on read	RO	
Register Ah – 1000Base-T Status				
A.15	MASTER-SLAVE configuration fault	1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	RO/LH/SC	0
A.14	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO	0
A.13	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status = 1) 0 = Local Receiver not OK (loc_rcvr_status = 0)	RO	0
A.12	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status = 1) 0 = Remote Receiver not OK (rem_rcvr_status = 0)	RO	0
A.11	Link Partner 1000Base-T Full-duplex capability	1 = Link Partner is capable of 1000Base-T full-duplex 0 = Link Partner is not capable of 1000Base-T full-duplex	RO	0
A.10	Link Partner 1000Base-T Half-duplex capability	1 = Link Partner is capable of 1000Base-T half-duplex 0 = Link Partner is not capable of 1000Base-T half-duplex	RO	0
A.9:8	Reserved	Reserved	RO	00
A.7:0	Idle Error Count	Cumulative count of errors detected when receiver is receiving idles and PMA_TXMODE.indicate = SEND_N. The counter is incremented every symbol period that rxerror_status = ERROR.	RO/SC	0000_0000

Address	Name	Description	Mode[1]	Default
Register Dh – MMD Access – Control				
D.15:14	MMD – Operation Mode	For the selected MMD – Device Address (bits [4:0] of this register), these two bits select one of the following Register or Data operations and the usage for MMD Access – Register/Data (Reg. Eh). 00 = Register 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	RW	00
D.13:5	Reserved	Reserved	RW	00_0000_000
D.4:0	MMD – Device Address	The MMD – Device Address is set by these five bits.	RW	0_0000
Register Eh – MMD Access – Register/Data				
E.15:0	MMD – Register / Data	For the selected MMD – Device Address (Reg. Dh, bits [4:0]), When Reg. Dh, bits [15:14] = 00, this register contains the read/write register address for the MMD – Device Address. Otherwise, this register contains the read/write data value for the MMD – Device Address and its selected Register Address. See also Reg. Dh, bits [15:14] descriptions for post increment reads and writes of this register for Data operation.	RW	0000_0000_0000_0000
Register Fh – Extended Status				
F.15	1000Base-X Full-duplex	1 = PHY able to perform 1000Base-X Full-duplex 0 = PHY not able to perform 1000Base-X Full-duplex	RO	0
F.14	1000Base-X Half-duplex	1 = PHY able to perform 1000Base-X Half-duplex 0 = PHY not able to perform 1000Base-X Half-duplex	RO	0
F.13	1000Base-T Full-duplex	1 = PHY able to perform 1000Base-T Full-duplex 0 = PHY not able to perform 1000Base-T Full-duplex	RO	1
F.12	1000Base-T Half-duplex	1 = PHY able to perform 1000Base-T Half-duplex 0 = PHY not able to perform 1000Base-T Half-duplex	RO	1
F.11:0	Reserved	Ignore when read	RO	-

Note:

1. RW = Read/Write.
   RO = Read only.

SC = Self-cleared.

LH = Latch high.

LL = Latch low.

Vendor Specific Registers – Descriptions

Address	Name	Description	Mode[1]	Default
Register 11h – Remote Loopback				
11.15:9	Reserved	Reserved	RW	0000_000
11.8	Remote Loopback	1 = Enable Remote Loopback 0 = Disable Remote Loopback	RW	0
11.7:1	Reserved	Reserved	RW	1111_010
11.0	Reserved	Reserved	RO	0
Register 12h – LinkMD® – Cable Diagnostic				
12.15	Cable Diagnostic Test Enable	Write value: 1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Disable cable diagnostic test. Read value: 1 = Cable diagnostic test is in progress. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0
12.14	Reserved	This bit should always be set to ‘0’.	RW	0
12.13:12	Cable Diagnostic Test Pair	These two bits select the differential pair for testing: 00 = Differential pair A (pins 2, 3) 01 = Differential pair B (pins 5, 6) 10 = Differential pair C (pins 7, 8) 11 = Differential pair D (pins 10, 11)	RW	00
12.11:10	Reserved	These two bits should always be set to ‘00’.	RW	00
12.9:8	Cable Diagnostic Status	These two bits represent the test result for the selected differential pair in bits [13:12] of this register. 00 = Normal cable condition (no fault detected) 01 = Open cable fault detected 10 = Short cable fault detected 11 = Reserved	RO	00
12.7:0	Cable Diagnostic Fault Data	For the open or short cable fault detected in bits [9:8] of this register, this 8-bit value represents the distance to the cable fault.	RO	0000_0000
Register 13h – Digital PMA/PCS Status				
13.15:3	Reserved	Reserved	RO/LH	0000_0000_0000_0

Address	Name	Description	Mode(1)	Default
13.2	1000Base-T Link Status	1000Base-T Link Status 1 = Link status is OK 0 = Link status is not OK	RO	0
13.1	100Base-TX Link Status	100Base-TX Link Status 1 = Link status is OK 0 = Link status is not OK	RO	0
13.0	Reserved	Reserved	RO	0
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for Symbol Error frames	RO/RC	0000_0000_0000_0000
Register 1Bh – Interrupt Control/Status				
1B.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
1B.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
1B.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
1B.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
1B.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
1B.10	Link Down Interrupt Enable	1 = Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
1B.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
1B.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
1B.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occurred	RO/RC	0
1B.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occurred	RO/RC	0
1B.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occurred	RO/RC	0
1B.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occurred	RO/RC	0
1B.3	Link Partner Acknowledge Interrupt	1 = Link Partner Acknowledge occurred 0 = Link Partner Acknowledge did not occurred	RO/RC	0

Address	Name	Description	Mode(1)	Default
1B.2	Link Down Interrupt	1 = Link Down occurred 0 = Link Down did not occurred	RO/RC	0
1B.1	Remote Fault Interrupt	1 = Remote Fault occurred 0 = Remote Fault did not occurred	RO/RC	0
1B.0	Link Up Interrupt	1 = Link Up occurred 0 = Link Up did not occurred	RO/RC	0
Register 1Ch – Auto MDI/MDI-X				
1C.15:8	Reserved	Reserved	RW	0000_0000
1C.7	MDI-set	When Swap-off (bit [6] of this register) is asserted (1), 1 = PHY is set to operate as MDI mode. 0 = PHY is set to operate as MDI-X mode. This bit has no function when Swap-off is de-asserted (0).	RW	0
1C.6	Swap-off	1 = Disable Auto MDI/MDI-X function 0 = Enable Auto MDI/MDI-X function	RW	0
1C.5:0	Reserved	Reserved	RW	00_0000
Register 1Fh – PHY Control				
1F.15	Reserved	Reserved	RW	0
1F.14	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1F.13:12	Reserved	Reserved	RW	00
1F.11:10	Reserved	Reserved	RO/LH/RC	00
1F.9	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1F.8:7	Reserved	Reserved	RW	00
1F.6	Speed status 1000Base-T	1 = Indicate chip final speed status at 1000Base-T	RO	0
1F.5	Speed status 100Base-TX	1 = Indicate chip final speed status at 100Base-TX	RO	0
1F.4	Speed status 10Base-T	1 = Indicate chip final speed status at 10Base-T	RO	0
1F.3	Duplex status	Indicate chip duplex status 1 = Full-duplex 0 = Half-duplex	RO	0
1F.2	1000Base-T Mater/Slave status	Indicate chip Master/Slave status 1 = 1000Base-T Master mode 0 = 1000Base-T Slave mode	RO	0
1F.1	Reserved	Reserved	RW	0
1F.0	Link Status Check Fail	1 = Fail 0 = Not Failing	RO	0

Note:

1. RW = Read/Write.
   RC = Read-cleared

RO = Read only.

SC = Self-cleared.

LH = Latch high.

MMD Registers

MMD Registers provide indirect read/write access up to 32 MMD Device Addresses with each device supporting up to 65,536 16-bit registers, as defined per Clause 22 of the IEEE 802.3 Specification. The KSZ9031RNX, however, uses only a small fraction of the available registers. See Register Map section for a list of supported MMD Device Addresses and their associated Register Addresses.

The following two Standard Registers serve as the portal registers to access the indirect MMD Registers.

- Standard Register Dh – MMD Access – Control
- Standard Register Eh – MMD Access – Register/Data

Register Dh – MMD Access – Control				
D.15:14	MMD – Operation Mode	For the selected MMD – Device Address (bits [4:0] of this register), these two bits select one of the following Register or Data operations and the usage for MMD Access – Register/Data (Reg. Eh). 00 = Register 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	RW	00
D.13:5	Reserved	Reserved	RW	00_0000_000
D.4:0	MMD – Device Address	The MMD – Device Address is set by these five bits.	RW	0_0000
Register Eh – MMD Access – Register/Data				
E.15:0	MMD – Register / Data	For the selected MMD – Device Address (Reg. Dh, bits [4:0]), When Reg. Dh, bits [15:14] = 00, this register contains the read/write register address for the MMD – Device Address. Otherwise, this register contains the read/write data value for the MMD – Device Address and its selected Register Address. See also Reg. Dh, bits [15:14] descriptions for post increment reads and writes of this register for Data operation.	RW	0000_0000_0000_0000

Table 18. Portal Registers (Access to indirect MMD Registers)

Examples:

- **MMD Register Write**

  Write MMD – Device Address 2h, Register 10h = 0001h to enable link-up detection to trigger PME for WOL.

  1. Write register Dh with 0002h // Setup Register Address for MMD – Device Address 2h.
  2. Write register Eh with 0010h // Select Register 10h of MMD – Device Address 2h.
  3. Write register Dh with 4002h // Select Register Data for MMD – Device Address 2h, Register 10h.
  4. Write register Eh with 0001h // Write value 0001h to MMD – Device Address 2h, Register 10h.

- **MMD Register Read**

  Read MMD – Device Address 2h, Register 11h – 13h for the Magic Packet's MAC Address

  1. Write register Dh with 0002h // Setup Register Address for MMD – Device Address 2h.
  2. Write register Eh with 0011h // Select Register 11h of MMD – Device Address 2h.
  3. Write register Dh with 8002h // Select Register Data for MMD – Device Address 2h, Register 11h.
  4. Read register Eh // Read data in MMD – Device Address 2h, Register 11h.
  5. Read register Eh // Read data in MMD – Device Address 2h, Register 12h.
  6. Read register Eh // Read data in MMD – Device Address 2h, Register 13h.

MMD Registers – Descriptions

Address	Name	Description	Mode[(1)]	Default
MMD Address 1h, Register 5Ah – 1000Base-T Link-up Time Control				
1.5A.15:9	Reserved	Reserved	RO	0000_000
1.5A.8:4	Reserved	Reserved	RW	1_0000
1.5A.3:1	1000Base-T Link-up Time	When the Link Partner is another KSZ9031 device, the 1000Base-T link-up time can be long. These three bits provides an optional setting to reduce the 1000Base-T link-up time. 100 = Default power-up setting 011 = Optional setting to reduce link-up time when Link Partner is KSZ9031 device. All other settings are reserved and should not be used. The optional setting is safe to use with any Link Partner. Note: Read/Write access to this register bit is available only when Reg. 0h is set to 0x2100 for Auto-Negotiation disable and force 100Base-TX mode.	RW	100
1.5A.0	Reserved	Reserved	RW	0
MMD Address 2h, Register 0h – Common Control				
2.0.15:4	Reserved	Reserved	RW	0000_0000_0000
2.0.3	LED Mode	Override strap-in for LED_MODE 1 = Single LED Mode 0 = Bi-color Dual LED Mode	RW	Set by LED_MODE strapping pin. See "Strapping Options" section for details.
2.0.2	Reserved	Reserved	RW	0

Address	Name	Description	Mode[1]	Default
2.0.1	CLK125_EN Status	Override strap-in for CLK125_EN 1 = CLK125_EN strap-in is enabled 0 = CLK125_EN strap-in is disabled	RW	Set by CLK125_EN strapping pin. See “Strapping Options” section for details.
2.0.0	Reserved	Reserved	RW	0
MMD Address 2h, Register 1h – Strap Status				
2.1.15:8	Reserved	Reserved	RO	0000_0000
2.1.7	LED_MODE strap-in status	Strap to 1 = Single LED Mode 0 = Bi-color Dual LED Mode	RO	Set by LED_MODE strapping pin. See “Strapping Options” section for details.
2.1.6	Reserved	Reserved	RO	0
2.1.5	CLK125_EN strap-in status	Strap to 1 = CLK125_EN strap-in is enabled 0 = CLK125_EN strap-in is disabled	RO	Set by CLK125_EN strapping pin. See “Strapping Options” section for details.
2.1.4:3	Reserved	Reserved	RO	00
2.1.2:0	PHYAD[2:0] strap-in value	Strap-in value for PHY Address Bits [4:3] of PHY Address are always set to ‘00’.	RO	Set by PHYAD[2:0] strapping pin. See “Strapping Options” section for details.
MMD Address 2h, Register 2h – Operation Mode Strap Override				
2.2.15	RGMII all capabilities override	1 = Override strap-in for RGMII advertise all capabilities	RW	Set by MODE[3:0] strapping pin. See “Strapping Options” section for details.
2.2.14	RGMII no 1000BT_HD override	1 = Override strap-in for RGMII advertise all capabilities except 1000Base-T half-duplex	RW	
2.2.13	RGMII 1000BT_H/FD only override	1 = Override strap-in for RGMII advertise 1000Base-T full and half-duplex only	RW	
2.2.12	RGMII 1000BT_FD only override	1 = Override strap-in for RGMII advertise 1000Base-T full-duplex only	RW	
2.2.11	Reserved	Reserved	RW	0
2.2.10	PME_N2 Output Enable	For INT_N / PME_N2 (pin 38), 1 = Enable PME Output 0 = Disable PME Output This bit works in conjunction with MMD Address 2h, Reg. 10h, Bits [15:14] to define the output for pin 38.	RW	0
2.2.9	Reserved	Reserved	RW	0
2.2.8	PME_N1 Output Enable	For LED1 / PME_N1 (pin 17), 1 = Enable PME Output 0 = Disable PME Output This bit works in conjunction with MMD Address 2h, Reg. 10h, Bits [15:14] to define the output for pin 17.	RW	0

Address	Name	Description	Mode[1]	Default
2.2.7	Chip Power Down override	1 = Override strap-in for Chip Power Down mode	RW	Set by MODE[3:0] strapping pin. See “Strapping Options” section for details.
2.2.6:5	Reserved	Reserved	RW	00
2.2.4	NAND Tree override	1 = Override strap-in for NAND Tree mode	RW	Set by MODE[3:0] strapping pin. See “Strapping Options” section for details.
2.2.3:0	Reserved	Reserved	RW	0000
MMD Address 2h, Register 3h – Operation Mode Strap Status				
2.3.15	RGMII all capabilities strap-in status	1 = Strap to RGMII advertise all capabilities	RO	Set by MODE[3:0] strapping pin. See “Strapping Options” section for details.
2.3.14	RGMII no 1000BT_HD strap-in status	1 = Strap to RGMII advertise all capabilities except 1000Base-T half-duplex	RO	
2.3.13	RGMII only 1000BT_H/FD strap-in status	1 = Strap to RGMII advertise 1000Base-T full and half-duplex only	RO	
2.3.12	RGMII only 1000BT_FD strap-in status	1 = Strap to RGMII advertise 1000Base-T full-duplex only	RO	
2.3.11:8	Reserved	Reserved	RO	0000
2.3.7	Chip Power Down strap-in status	1 = Strap to Chip Power Down mode	RO	Set by MODE[3:0] strapping pin. See “Strapping Options” section for details.
2.3.6:5	Reserved	Reserved	RO	00
2.3.4	NAND Tree strap-in status	1 = Strap to NAND Tree mode	RO	Set by MODE[3:0] strapping pin. See “Strapping Options” section for details.
2.3.3:0	Reserved	Reserved	RO	0000
MMD Address 2h, Register 4h – RGMII Control Signal Pad Skew				
2.4.15:8	Reserved	Reserved	RW	0000_0000
2.4.7:4	RX_DV pad skew	RGMII RX_CTL output pad skew control (0.06ns/step)	RW	0111
2.4.3:0	TX_EN pad skew	RGMII TX_CTL input pad skew control (0.06ns/step)	RW	0111
MMD Address 2h, Register 5h – RGMII RX Data Pad Skew				
2.5.15:12	RXD3 pad skew	RGMII RXD3 output pad skew control (0.06ns/step)	RW	0111
2.5.11:8	RXD2 pad skew	RGMII RXD2 output pad skew control (0.06ns/step)	RW	0111
2.5.7:4	RXD1 pad skew	RGMII RXD1 output pad skew control (0.06ns/step)	RW	0111
2.5.3:0	RXD0 pad skew	RGMII RXD0 output pad skew control (0.06ns/step)	RW	0111

Address	Name	Description	Mode(1)	Default
MMD Address 2h, Register 6h – RGMII TX Data Pad Skew				
2.6.15:12	TXD3 pad skew	RGMII TXD3 output pad skew control (0.06ns/step)	RW	0111
2.6.11:8	TXD2 pad skew	RGMII TXD2 output pad skew control (0.06ns/step)	RW	0111
2.6.7:4	TXD1 pad skew	RGMII TXD1 output pad skew control (0.06ns/step)	RW	0111
2.6.3:0	TXD0 pad skew	RGMII TXD0 output pad skew control (0.06ns/step)	RW	0111
MMD Address 2h, Register 8h – RGMII Clock Pad Skew				
2.8.15:10	Reserved	Reserved	RW	0000_00
2.8.9:5	GTX_CLK pad skew	RGMII GTX_CLK input pad skew control (0.06ns/step)	RW	01_111
2.8.4:0	RX_CLK pad skew	RGMII RX_CLK output pad skew control (0.06ns/step)	RW	0_1111
MMD Address 2h, Register 10h – Wake-On-LAN – Control				
2.10.15:14	PME Output Select	These two bits work in conjunction with MMD Address 2h, Reg. 2h, Bits [8] and [10] for PME_N1 and PME_N2 enable to define the output for pins 17 and 38, respectively. LED1 / PME_N1 (pin 17) 00 = PME_N1 output only 01 = LED1 output only 10 = LED1 and PME_N1 output 11 = Reserved INT_N / PME_N2 (pin 38) 00 = PME_N2 output only 01 = INT_N output only 10 = INT_N and PME_N2 output 11 = Reserved	RW	00
2.10.13:7	Reserved	Reserved	RW	00_0000_0
2.10.6	Magic Packet Detect Enable	1 = Enable Magic Packet detection 0 = Disable Magic Packet detection	RW	0
2.10.5	Custom Packet Type-3 Detect Enable	1 = Enable Custom Packet, Type-3 detection 0 = Disable Custom Packet, Type-3 detection	RW	0
2.10.4	Custom Packet Type-2 Detect Enable	1 = Enable Custom Packet, Type-2 detection 0 = Disable Custom Packet, Type-2 detection	RW	0
2.10.3	Custom Packet Type-1 Detect Enable	1 = Enable Custom Packet, Type-1 detection 0 = Disable Custom Packet, Type-1 detection	RW	0
2.10.2	Custom Packet Type-0 Detect Enable	1 = Enable Custom Packet, Type-0 detection 0 = Disable Custom Packet, Type-0 detection	RW	0

Address	Name	Description	Mode[1]	Default
2.10.1	Link-down Detect Enable	1 = Enable Link-down detection 0 = Disable Link-down detection	RW	0
2.10.0	Link-up Detect Enable	1 = Enable Link-up detection 0 = Disable Link-up detection	RW	0
MMD Address 2h, Register 11h – Wake-On-LAN – Magic Packet, MAC-DA-0				
2.11.15:0	Magic Packet MAC-DA-0	This register stores the lower 2 bytes of the Destination MAC Address for the Magic Packet Bit [15:8] = byte-2 (MAC Address [15:8]) Bit [7:0] = byte-1 (MAC Address [7:0]) The upper 4 bytes of the Destination MAC Address are stored in the following two registers.	RW	0000_0000_0000_0000
MMD Address 2h, Register 12h – Wake-On-LAN – Magic Packet, MAC-DA-1				
2.12.15:0	Magic Packet MAC-DA-1	This register stores the middle 2 bytes of the Destination MAC Address for the Magic Packet Bit [15:8] = byte-4 (MAC Address [31:24]) Bit [7:0] = byte-3 (MAC Address [23:16]) The lower 2 bytes and upper 2 bytes of the Destination MAC Address are stored in the previous and following registers, respectively.	RW	0000_0000_0000_0000
MMD Address 2h, Register 13h – Wake-On-LAN – Magic Packet, MAC-DA-2				
2.13.15:0	Magic Packet MAC-DA-2	This register stores the upper 2 bytes of the Destination MAC Address for the Magic Packet Bit [15:8] = byte-6 (MAC Address [47:40]) Bit [7:0] = byte-5 (MAC Address [39:32]) The lower 4 bytes of the Destination MAC Address are stored in the previous two registers.	RW	0000_0000_0000_0000
MMD Address 2h, Register 14h – Wake-On-LAN – Customized Packet, Type-0, Expected-CRC-0 **MMD Address 2h, Register 16h – Wake-On-LAN – Customized Packet, Type-1, Expected-CRC-0** **MMD Address 2h, Register 18h – Wake-On-LAN – Customized Packet, Type-2, Expected-CRC-0** **MMD Address 2h, Register 1Ah – Wake-On-LAN – Customized Packet, Type-3, Expected-CRC-0**				
2.14.15:0 2.16.15:0 2.18.15:0 2.1A.15:0	Custom Packet Type-X CRC-0	This register stores the lower 2 bytes for the expected CRC Bit [15:8] = byte-2 (CRC [15:8]) Bit [7:0] = byte-1 (CRC [7:0]) The upper 2 bytes for the expected CRC is stored in the following register.	RW	0000_0000_0000_0000

Address	Name	Description	Mode(1)	Default
MMD Address 2h, Register 15h – Wake-On-LAN – Customized Packet, Type-0, Expected-CRC-1 **MMD Address 2h, Register 17h – Wake-On-LAN – Customized Packet, Type-1, Expected-CRC-1** **MMD Address 2h, Register 19h – Wake-On-LAN – Customized Packet, Type-2, Expected-CRC-1** **MMD Address 2h, Register 1Bh – Wake-On-LAN – Customized Packet, Type-3, Expected-CRC-1**				
2.15.15:0 2.17.15:0 2.19.15:0 2.1B.15:0	Custom Packet Type-X CRC-1	This register stores the upper 2 bytes for the expected CRC Bit [15:8] = byte-4 (CRC [31:24]) Bit [7:0] = byte-3 (CRC [23:16]) The lower 2 bytes for the expected CRC is stored in the previous register.	RW	0000_0000_0000_0000
MMD Address 2h, Register 1Ch – Wake-On-LAN – Customized Packet, Type-0, Mask-0 **MMD Address 2h, Register 20h – Wake-On-LAN – Customized Packet, Type-1, Mask-0** **MMD Address 2h, Register 24h – Wake-On-LAN – Customized Packet, Type-2, Mask-0** **MMD Address 2h, Register 28h – Wake-On-LAN – Customized Packet, Type-3, Mask-0**				
2.1C.15:0 2.20.15:0 2.24.15:0 2.28.15:0	Custom Packet Type-X Mask-0	This register selects the byte(s) in the first 16 bytes of the packet (bytes 1 thru 16) that will be used for the CRC calculation. For each bit in this register, 1 = byte is selected for CRC calculation 0 = byte is not selected for CRC calculation The register-bit to packet-byte mapping is as follows: Bit [15] : byte-16 … : … Bit [2] : byte-2 Bit [0] : byte-1	RW	0000_0000_0000_0000

Address	Name	Description	Mode(1)	Default
MMD Address 2h, Register 1Dh – Wake-On-LAN – Customized Packet, Type-0, Mask-1 **MMD Address 2h, Register 21h – Wake-On-LAN – Customized Packet, Type-1, Mask-1** **MMD Address 2h, Register 25h – Wake-On-LAN – Customized Packet, Type-2, Mask-1** **MMD Address 2h, Register 29h – Wake-On-LAN – Customized Packet, Type-3, Mask-1**				
2.1D.15:0 2.21.15:0 2.25.15:0 2.29.15:0	Custom Packet Type-X Mask-1	This register selects the byte(s) in the second 16 bytes of the packet (bytes 17 thru 32) that will be used for the CRC calculation. For each bit in this register, 1 = byte is selected for CRC calculation 0 = byte is not selected for CRC calculation The register-bit to packet-byte mapping is as follows: Bit [15] : byte-32 … : … Bit [2] : byte-18 Bit [0] : byte-17	RW	0000_0000_0000_0000
MMD Address 2h, Register 1Eh – Wake-On-LAN – Customized Packet, Type-0, Mask-2 **MMD Address 2h, Register 22h – Wake-On-LAN – Customized Packet, Type-1, Mask-2** **MMD Address 2h, Register 26h – Wake-On-LAN – Customized Packet, Type-2, Mask-2** **MMD Address 2h, Register 2Ah – Wake-On-LAN – Customized Packet, Type-3, Mask-2**				
2.1E.15:0 2.22.15:0 2.26.15:0 2.2A.15:0	Custom Packet Type-X Mask-2	This register selects the byte(s) in the third 16 bytes of the packet (bytes 33 thru 48) that will be used for the CRC calculation. For each bit in this register, 1 = byte is selected for CRC calculation 0 = byte is not selected for CRC calculation The register-bit to packet-byte mapping is as follows: Bit [15] : byte-48 … : … Bit [2] : byte-34 Bit [0] : byte-33	RW	0000_0000_0000_0000

Address	Name	Description	Mode(1)	Default
MMD Address 2h, Register 1Fh – Wake-On-LAN – Customized Packet, Type-0, Mask-3 **MMD Address 2h, Register 23h – Wake-On-LAN – Customized Packet, Type-1, Mask-3** **MMD Address 2h, Register 27h – Wake-On-LAN – Customized Packet, Type-2, Mask-3** **MMD Address 2h, Register 2Bh – Wake-On-LAN – Customized Packet, Type-3, Mask-3**				
2.1F.15:0 2.23.15:0 2.27.15:0 2.2B.15:0	Custom Packet Type-X Mask-3	This register selects the byte(s) in the fourth 16 bytes of the packet (bytes 49 thru 64) that will be used for the CRC calculation. For each bit in this register, 1 = byte is selected for CRC calculation 0 = byte is not selected for CRC calculation The register-bit to packet-byte mapping is as follows: Bit [15] : byte-64 … : … Bit [2] : byte-50 Bit [0] : byte-49	RW	0000_0000_0000_0000
MMD Address 3h, Register 0h – PCS EEE – Control				
3.0.15:12	Reserved	Reserved	RW	0000
3.0.11	1000Base-T Force LPI	1 = Force 1000Base-T Low Power Idle transmission 0 = Normal operation	RW	0
3.0.10	100Base-TX RX_CLK Stoppable	During receive Lower Power Idle mode, 1 = RX_CLK stoppable for 100Base-TX 0 = RX_CLK not stoppable for 100Base-TX	RW	0
3.0.9:0	Reserved	Reserved	RW	00_0000_0000
MMD Address 3h, Register 1h – PCS EEE – Status				
3.1.15:12	Reserved	Reserved	RO	0000
3.1.11	Transmit Low Power Idle received	1 = Transmit PCS has received Low Power Idle 0 = Low Power Idle not received	RO/LH	0
3.1.10	Receive Low Power Idle received	1 = Receive PCS has received Low Power Idle 0 = Low Power Idle not received	RO/LH	0
3.1.9	Transmit Low Power Idle Indication	1 = Transmit PCS is currently receiving Low Power Idle 0 = Transmit PCS is not currently receiving Low Power Idle	RO	
3.1.8	Receive Low Power Idle Indication	1 = Receive PCS is currently receiving Low Power Idle 0 = Receive PCS is not currently receiving Low Power Idle	RO	
3.1.7:0	Reserved	Reserved	RO	0000_0000
MMD Address 7h, Register 3Ch – EEE Advertisement				
7.3C.15:3	Reserved	Reserved	RW	0000_0000_0000_0

Address	Name	Description	Mode[1]	Default
7.3C.2	1000Base-T EEE	1 = 1000Mbps EEE capable 0 = No 1000Mbps EEE capability This bit is set to '0' as the default after power-up or reset. Set this bit to '1' to enable 1000Mbps EEE mode.	RW	0
7.3C.1	100Base-TX EEE	1 = 100Mbps EEE capable 0 = No 100Mbps EEE capability This bit is set to '0' as the default after power-up or reset. Set this bit to '1' to enable 100Mbps EEE mode.	RW	0
7.3C.0	Reserved	Reserved	RW	0
MMD Address 7h, Register 3Dh – EEE Link Partner Advertisement				
7.3D.15:3	Reserved	Reserved	RO	0000_0000_0000_0
7.3D.2	1000Base-T EEE	1 = 1000Mbps EEE capable 0 = No 1000Mbps EEE capability	RO	0
7.3D.1	100Base-TX EEE	1 = 100Mbps EEE capable 0 = No 100Mbps EEE capability	RO	0
7.3D.0	Reserved	Reserved	RO	0
MMD Address 1Ch, Register 4h – Analog Control 4				
1C.4.15:11	Reserved	Reserved	RW	0000_0
1C.4.10	10Base-Te Mode	1 = EEE 10Base-Te (1.75V TX amplitude) 0 = Standard 10Base-T (2.5V TX amplitude)	RW	0
1C.4.9:0	Reserved	Reserved	RW	00_1111_1111
MMD Address 1Ch, Register 23h – EDPD Control				
1C.23.15:1	Reserved	Reserved	RW	0000_0000_0000_000
1C.23.0	EDPD Mode Enable	Energy Detect Power Down mode 1 = Enable 0 = Disable	RW	0

Note:

1. RW = Read/Write.
   RO = Read only.
   LH = Latch high.

Absolute Maximum Ratings[1]

Supply Voltage
- (DVDDL, AVDDL, AVDDL_PLL) .... -0.5V to +1.8V
- (AVDDH) .... -0.5V to +5.0V
- (DVDDH) .... -0.5V to +5.0V

Input Voltage (all inputs) .... -0.5V to +5.0V
Output Voltage (all outputs) .... -0.5V to +5.0V
Lead Temperature (soldering, 10sec.) .... 260°C
Storage Temperature (T_s) .... -55°C to +150°C

Operating Ratings[2]

Supply Voltage
- (DVDDL, AVDDL, AVDDL_PLL).... +1.140V to +1.260V
- (AVDDH @ 3.3V) .... +3.135V to +3.465V
- (AVDDH @ 2.5V, C-temp) .... +2.375V to +2.625V
- (DVDDH @ 3.3V) .... +3.135V to +3.465V
- (DVDDH @ 2.5V) .... +2.375V to +2.625V
- (DVDDH @ 1.8V) .... +1.710V to +1.890V

Ambient Temperature
- (T_A Commercial: KSZ9031RNXC) .... 0°C to +70°C
- (T_A Industrial: KSZ9031RNXI) .... -40°C to +85°C

Maximum Junction Temperature (T_J Max) .... 125°C
Thermal Resistance (θ_{JA}) .... 36.34°C/W
Thermal Resistance (θ_{JC}) .... 9.47°C/W

Electrical Characteristics[3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current – Core / Digital I/Os						
I_{CORE}	1.2V total of:	1000Base-T Link-up (no traffic)		210		mA
	DVDDL (digital core) +	1000Base-T Full-duplex @ 100% utilization		221		mA
	AVDDL (analog core) +	100Base-TX Link-up (no traffic)		63.6		mA
	AVDDL_PLL (PLL)	100Base-TX Full-duplex @ 100% utilization		63.8		mA
		10Base-T Link-up (no traffic)		7.1		mA
		10Base-T Full-duplex @ 100% utilization		7.7		mA
		Software Power Down Mode (Reg. 0h.11 =1)		1.0		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		0.7		mA
$I_{DVDDH\_1.8}$	1.8V for digital I/Os	1000Base-T Link-up (no traffic)		11.2		mA
		1000Base-T Full-duplex @ 100% utilization		23.6		mA
	(RGMII operating @ 1.8V)	100Base-TX Link-up (no traffic)		8.4		mA
		100Base-TX Full-duplex @ 100% utilization		9.8		mA
		10Base-T Link-up (no traffic)		3.6		mA
		10Base-T Full-duplex @ 100% utilization		5.6		mA
		Software Power Down Mode (Reg. 0h.11 =1)		5.5		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		0.3		mA
$I_{DVDDH\_2.5}$	2.5V for digital I/Os	1000Base-T Link-up (no traffic)		14.7		mA
		1000Base-T Full-duplex @ 100% utilization		31.5		mA
	(RGMII operating @ 2.5V)	100Base-TX Link-up (no traffic)		10.5		mA
		100Base-TX Full-duplex @ 100% utilization		13.0		mA
		10Base-T Link-up (no traffic)		6.3		mA
		10Base-T Full-duplex @ 100% utilization		9.0		mA
		Software Power Down Mode (Reg. 0h.11 =1)		6.7		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		0.7		mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{DVDDH\_3.3}$	3.3V for digital I/Os	1000Base-T Link-up (no traffic)		19.5		mA
		1000Base-T Full-duplex @ 100% utilization		41.5		mA
	(RGMII operating @ 3.3V)	100Base-TX Link-up (no traffic)		13.9		mA
		100Base-TX Full-duplex @ 100% utilization		17.2		mA
		10Base-T Link-up (no traffic)		11.5		mA
		10Base-T Full-duplex @ 100% utilization		13.7		mA
		Software Power Down Mode (Reg. 0h.11 =1)		9.3		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		2.2		mA
Supply Current – Transceiver (equivalent to current draw through external transformer center taps for PHY transceivers with current-mode transmit drivers)						
$I_{AVDDH\_2.5}$	2.5V for transceiver	1000Base-T Link-up (no traffic)		58.8		mA
		1000Base-T Full-duplex @ 100% utilization		57.9		mA
	(Recommended for commerical temperature range operation only)	100Base-TX Link-up (no traffic)		24.9		mA
		100Base-TX Full-duplex @ 100% utilization		24.9		mA
		10Base-T Link-up (no traffic)		11.5		mA
		10Base-T Full-duplex @ 100% utilization		25.3		mA
		Software Power Down Mode (Reg. h0.11 =1)		3.1		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		0.02		mA
$I_{AVDDH\_3.3}$	3.3V for transceiver	1000Base-T Link-up (no traffic)		67.4		mA
		1000Base-T Full-duplex @ 100% utilization		66.3		mA
		100Base-TX Link-up (no traffic)		28.7		mA
		100Base-TX Full-duplex @ 100% utilization		28.6		mA
		10Base-T Link-up (no traffic)		15.9		mA
		10Base-T Full-duplex @ 100% utilization		28.6		mA
		Software Power Down Mode (Reg. h0.11 =1)		4.2		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		0.02		mA
CMOS Inputs						
V_{IH}	Input High Voltage	DVDDH (digital I/Os) = 3.3V	2.0			V
		DVDDH (digital I/Os) = 2.5V	1.5			V
		DVDDH (digital I/Os) = 1.8V	1.1			V
V_{IL}	Input Low Voltage	DVDDH (digital I/Os) = 3.3V			1.3	V
		DVDDH (digital I/Os) = 2.5V			1.0	V
		DVDDH (digital I/Os) = 1.8V			0.7	V
I_{IN}	Input Current	V_{IN} = GND ~ V_{DDIO}		-10	10	µA
CMOS Outputs						
V_{OH}	Output High Voltage	DVDDH (digital I/Os) = 3.3V	2.7			V
		DVDDH (digital I/Os) = 2.5V	2.0			V
		DVDDH (digital I/Os) = 1.8V	1.5			V
V_{OL}	Output Low Voltage	DVDDH (digital I/Os) = 3.3V			0.3	V
		DVDDH (digital I/Os) = 2.5V			0.3	V

Symbol	Parameter	Condition	Min	Typ	Max	Units
		DVDDH (digital I/Os) = 1.8V			0.3	V
$\lvert I_{oz} \rvert$	Output Tri-State Leakage				10	µA
LED Outputs						
I_{LED}	Output Drive Current	Each LED pin (LED1, LED2)		8		mA
Pull-Up Pins						
pu	Internal Pull-up Resistance (MDC, MDIO, RESET_N pins)	DVDDH (digital I/Os) = 3.3V	13	22	31	KΩ
		DVDDH (digital I/Os) = 2.5V	16	28	39	KΩ
		DVDDH (digital I/Os) = 1.8V	26	44	62	KΩ
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				± 0.25	ns
	Overshoot				5	%
	Output Jitter	Peak-to-peak		0.7		ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
	Harmonic Rejection	Transmit all-one signal sequence		-31		dB
10Base-T Receive						
V_{SQ}	Squelch Threshold	5 MHz square wave	300	400		mV
Transmitter – Drive Setting						
V_{SET}	Reference Voltage of I_{SET}	$R(I_{SET})$ = 12.1K		1.2		V
LDO Controller – Drive Range						
V_{LDO_O}	Output drive range for LDO_O (pin 43) to gate input of P-channel MOSFET	AVDDH = 3.3V for MOSFET source voltage	0.85		2.8	V
		AVDDH = 2.5V for MOSFET source voltage (recommended for commerical temperature range operation only)	0.85		2.0	V

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. The device is not guaranteed to function outside its operating rating.
3. T_A = 25°C. Specification is for packaged product only.

Timing Diagrams

RGMII Timing

The KSZ9031RNX RGMII timing conforms to the timing requirements per the RGMII Version 2.0 Specification.

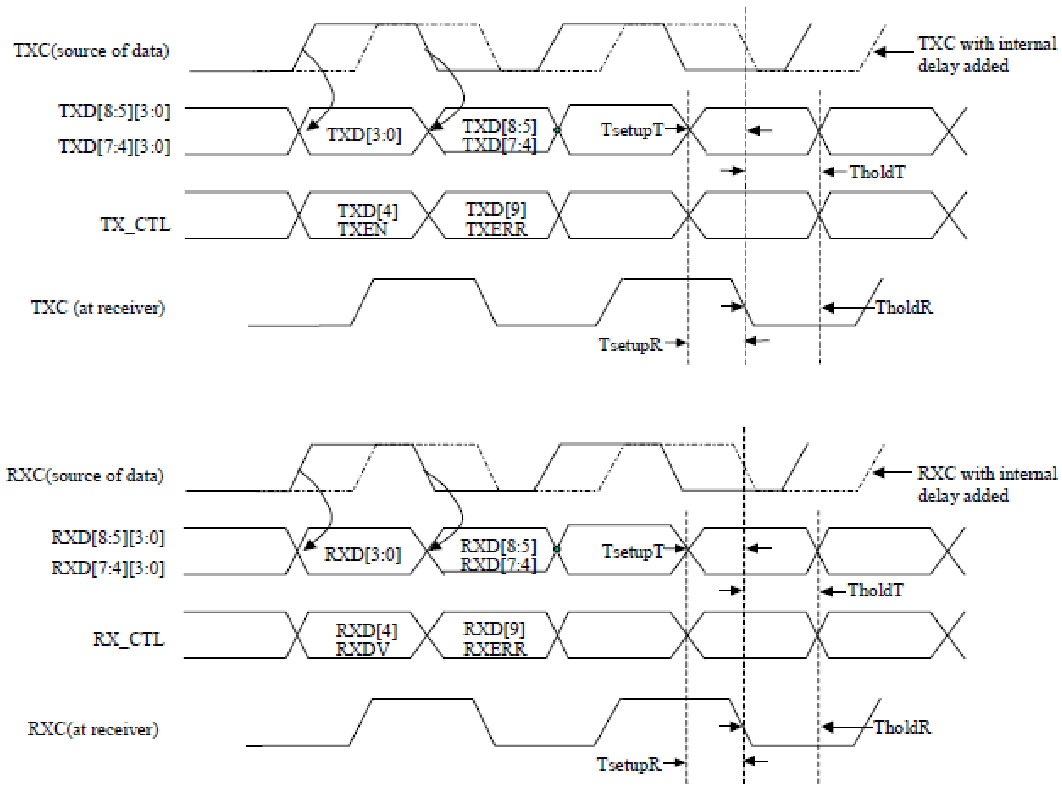


Figure 12. RGMII v2.0 Specification (Figure 3 – Multiplexing and Timing Diagram)

Timing Parameter	Description	Min	Typ	Max	Unit
TskewT	Data to Clock output Skew (at Transmitter)	-500		500	ps
TskewR	Data to Clock input Skew (at Receiver)	1.0		2.6	ns
Tcyc (1000Base-T)	Clock Cycle Duration for 1000Base-T	7.2	8	8.8	ns
Tcyc (100Base-TX)	Clock Cycle Duration for 100Base-TX	36	40	44	ns
Tcyc (10Base-T)	Clock Cycle Duration for 10Base-T	360	400	440	ns

Table 19. RGMII v2.0 Specification (Timing Specifics from Table 2)

Auto-Negotiation Timing

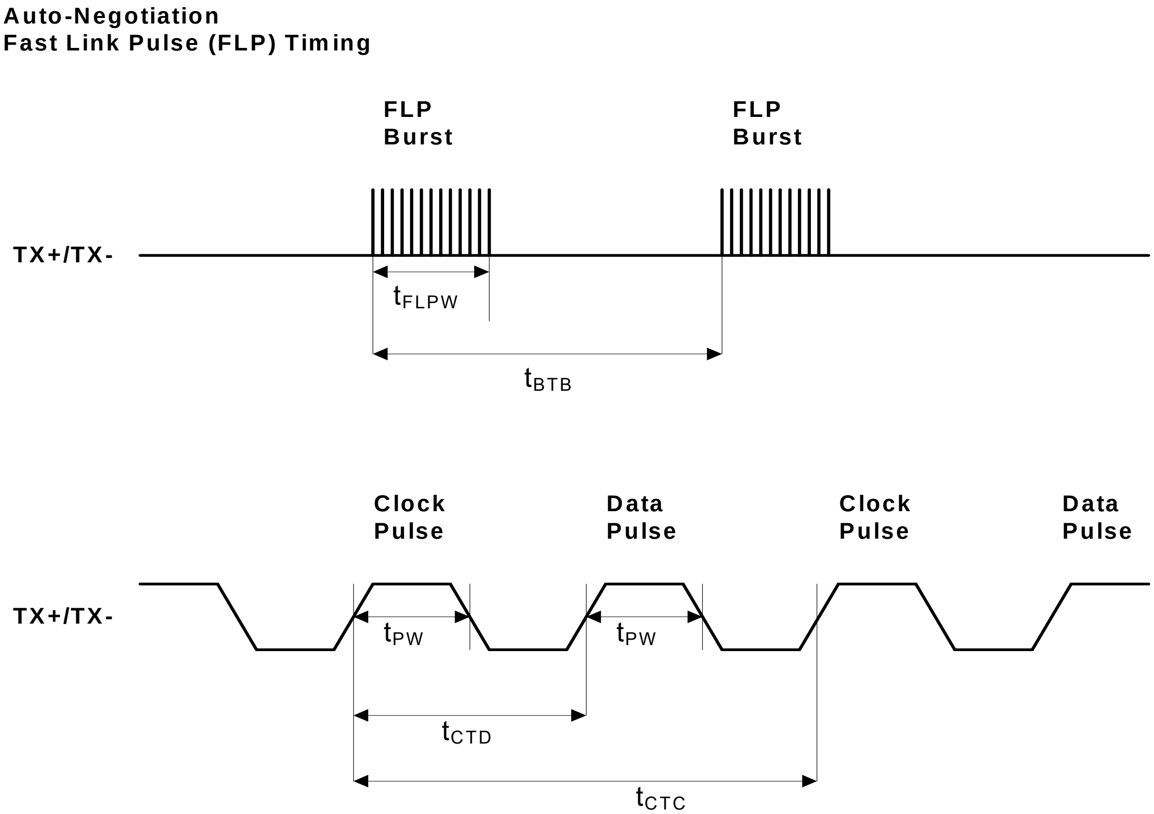


Figure 13. Auto-Negotiation Fast Link Pulse (FLP) Timing

Timing Parameter	Description	Min	Typ	Max	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst width		2		ms
t_{PW}	Clock/Data Pulse width		100		ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
	Number of Clock/Data Pulse per FLP Burst	17		33	

Table 20. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing

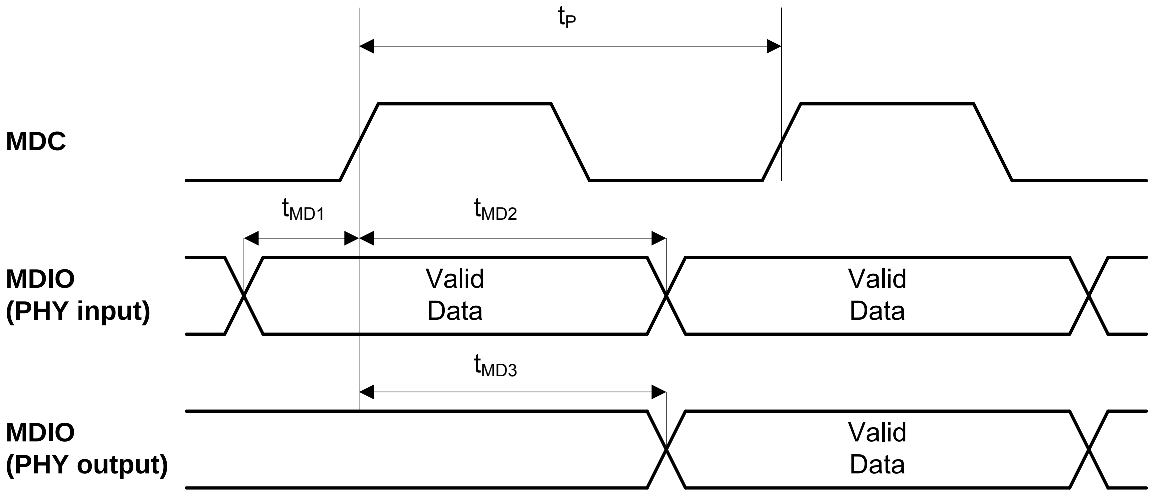


Figure 14. MDC/MDIO Timing

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	MDC period		400		ns
t_{1MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	10			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	0			ns

Table 21. MDC/MDIO Timing Parameters

Power-up / Power-down / Reset Timing

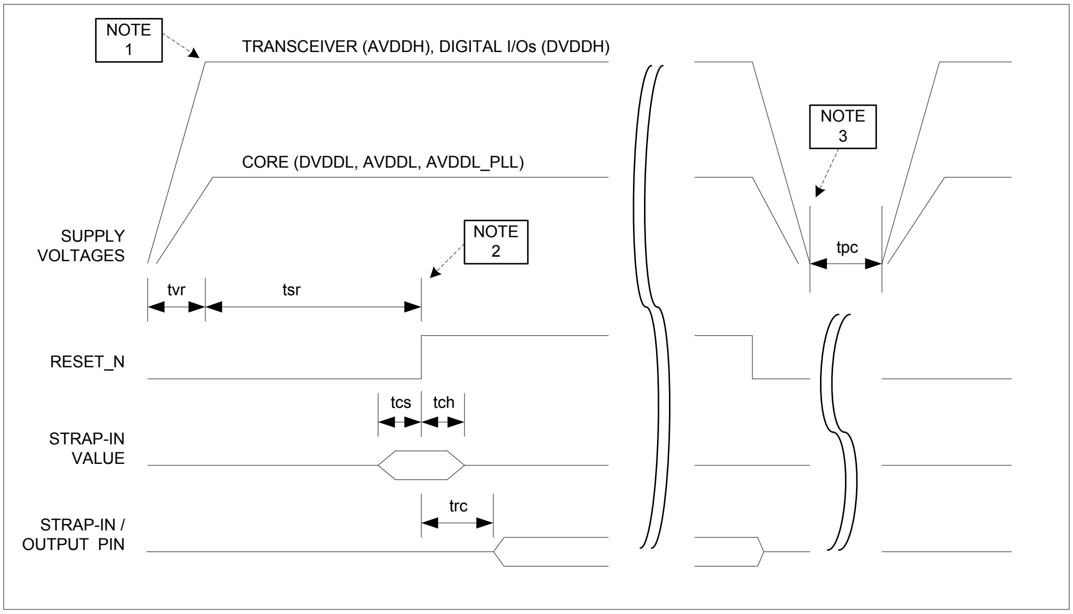


Figure 15. Power-up / Power-down / Reset Timing

Parameter	Description	Min	Max	Units
t_{vr}	Supply voltages rise time (must be monotonic)	200		µs
t_{sr}	Stable supply voltages to de-assertion of reset	10		ms
t_{cs}	Strap-in pin configuration setup time	5		ns
t_{ch}	Strap-in pin configuration hold time	5		ns
t_{rc}	De-assertion of reset to strap-in pin output	6		ns
t_{pc}	Supply voltages cycle off-to-on time	150		ms

Table 22. Power-up / Power-down / Reset Timing Parameters

NOTE 1: The recommended power-up sequence is to have the transceiver (AVDDH) and digital I/Os (DVDDH) voltages power up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL) voltage. If the 1.2V core must power-up first, the maximum lead time for the 1.2V core voltage with respect to the transceiver and digital I/O voltages should be 200µs.

There is no power sequence requirement between transceiver (AVDDH) and digital I/Os (DVDDH) power rails.

The power-up waveforms should be monotonic for all supply voltages to the KSZ9031RNX.

NOTE 2: After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) Interface.

NOTE 3: The recommended power-down sequence is to have the 1.2V core voltage power down first before powering down the transceiver and digital I/O voltages.

Before the next power-up cycle, all supply voltages to the KSZ9031RNX should reach 0V and there should be a minimum wait time of 150ms from power-off to power-on.

Reset Circuit

The following reset circuit is recommended for powering up the KSZ9031RNX if reset is triggered by the power supply.

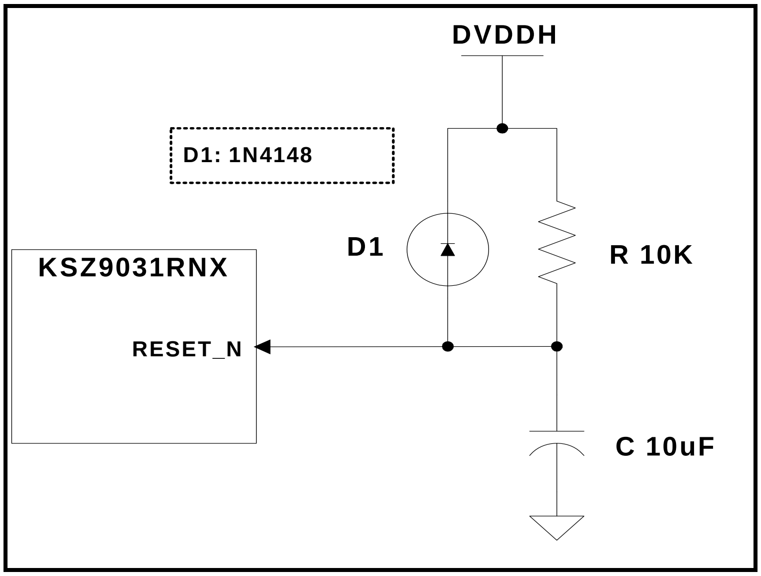


Figure 16. Recommended Reset Circuit

The following reset circuit is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ9031RNX device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

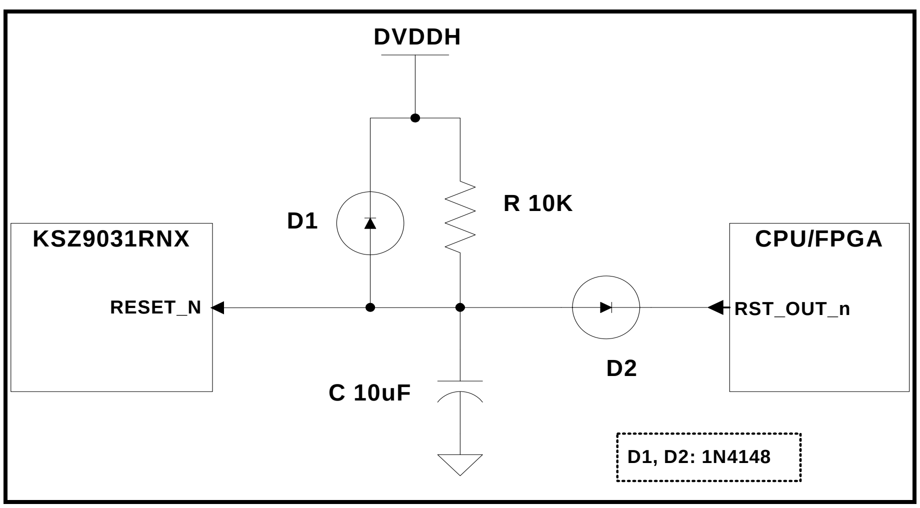


Figure 17. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output

Reference Circuits – LED Strap-in Pins

The pull-up and pull-down reference circuits for the LED2/PHYAD1 and LED1/PHYAD0 strapping pins are shown in the following figure for 3.3V and 2.5V DVDDH.

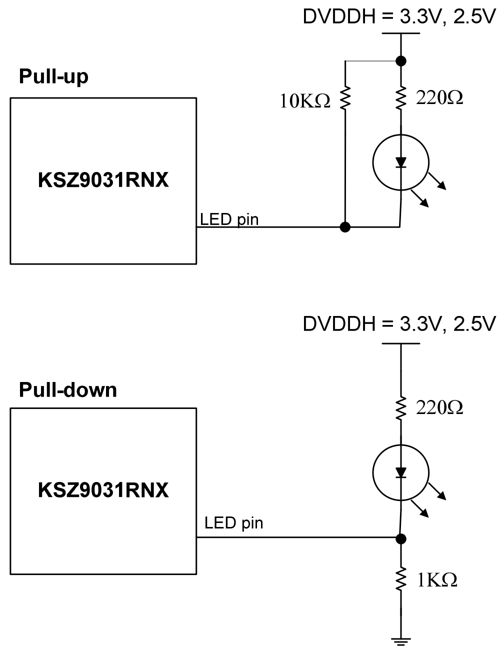


Figure 18. Reference Circuits for LED Strapping Pins

For 1.8V DVDDH, LED indication support is not recommended due to the low voltage. Without the LED indicator, the PHYAD1 and PHYAD0 strapping pins are functional with 10K pull-up to 1.8V DVDDH for a value of ‘1’, and with 1.0K pull-down to ground for a value of ‘0’.

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ9031RNX. The reference clock is 25 MHz for all operating modes of the KSZ9031RNX.

The following figure and table shows the reference clock connection to pins XI and XO of the KSZ9031RNX, and the reference clock selection criteria.

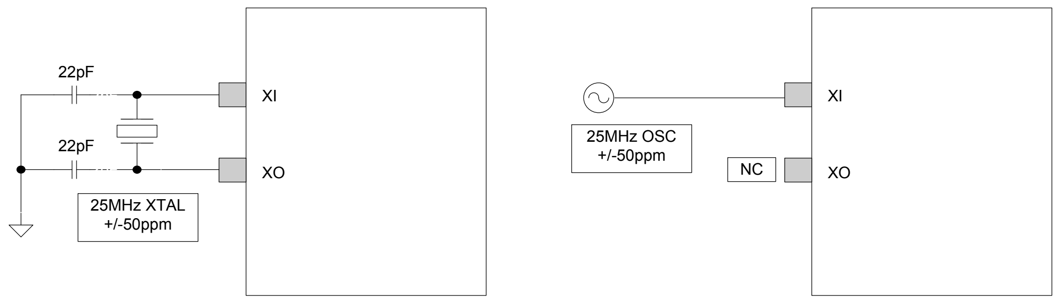


Figure 19. 25 MHz Crystal / Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm

Table 23. Reference Crystal/Clock Selection Criteria

Magnetic – Connection and Selection

A 1:1 isolation transformer is required at the line interface. One with integrated common-mode chokes is recommended for exceeding FCC requirements. An optional auto-transformer stage following the chokes provides additional common-mode noise and signal attenuation.

The KSZ9031RNX design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the four differential pairs. Therefore, the four transformer center tap pins on the KSZ9031RNX side should not be connected to any power supply source on the board, but rather, the center tap pins should be separated from one another and connected through separate 0.1uF common-mode capacitors to ground. Separation is required because the common-mode voltage could be different between the four differential pairs, depending on the connected speed mode.

The following figure shows the typical gigabit magnetic interface circuit for the KSZ9031RNX.

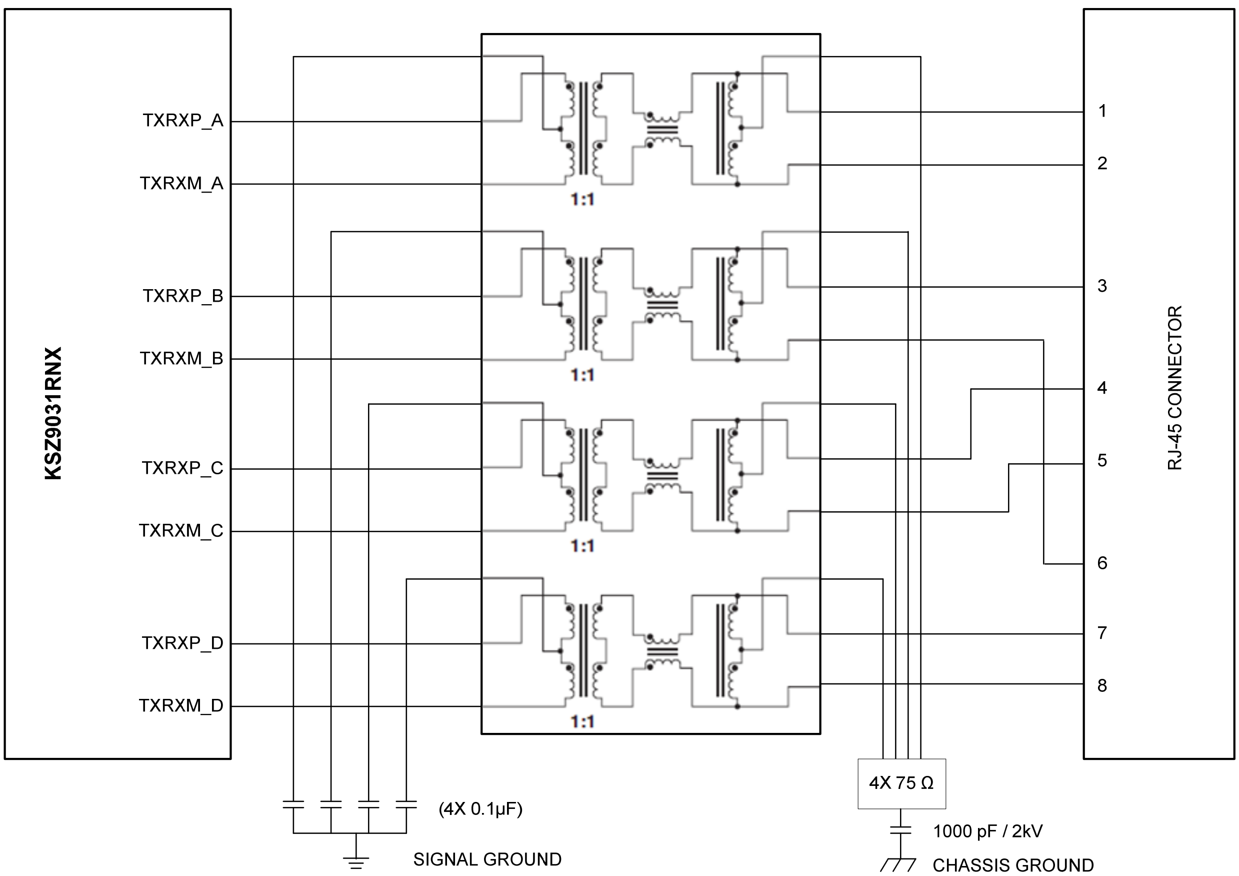


Figure 20. Typical Gigabit Magnetic Interface Circuit

The following table lists recommended magnetic characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350μH	100mV, 100kHz, 8mA
Insertion loss (max.)	1.0dB	0MHz – 100MHz
HIPOT (min.)	1500Vrms	

Table 24. Magnetics Selection Criteria

The following is a list of compatible single-port magnetics with separated transformer center tap pins on the G-PHY chip side that can be used with the KSZ9031RNX.

Manufacturer	Part Number	Auto-transformer	Temperature Range	Magnetic + RJ-45
Bel Fuse	0826-1G1T-23-F	Yes	0°C to 70°C	Yes
HALO	TG1G-E001NZRL	No	-40°C to 85°C	No
HALO	TG1G-S001NZRL	No	0°C to 70°C	No
HALO	TG1G-S002NZRL	Yes	0°C to 70°C	No
Pulse	H5007NL	Yes	0°C to 70°C	No
Pulse	H5062NL	Yes	0°C to 70°C	No
Pulse	HX5008NL	Yes	-40°C to 85°C	No
Pulse	JK0654219NL	Yes	0°C to 70°C	Yes
Pulse	JK0-0136NL	No	0°C to 70°C	Yes
TDK	TLA-7T101LF	No	0°C to 70°C	No
Wurth / Midcom	000-7093-37R-LF1	Yes	0°C to 70°C	No

Table 25. Compatible Single-port 10/100/1000 Magnetics

Recommended Land Pattern

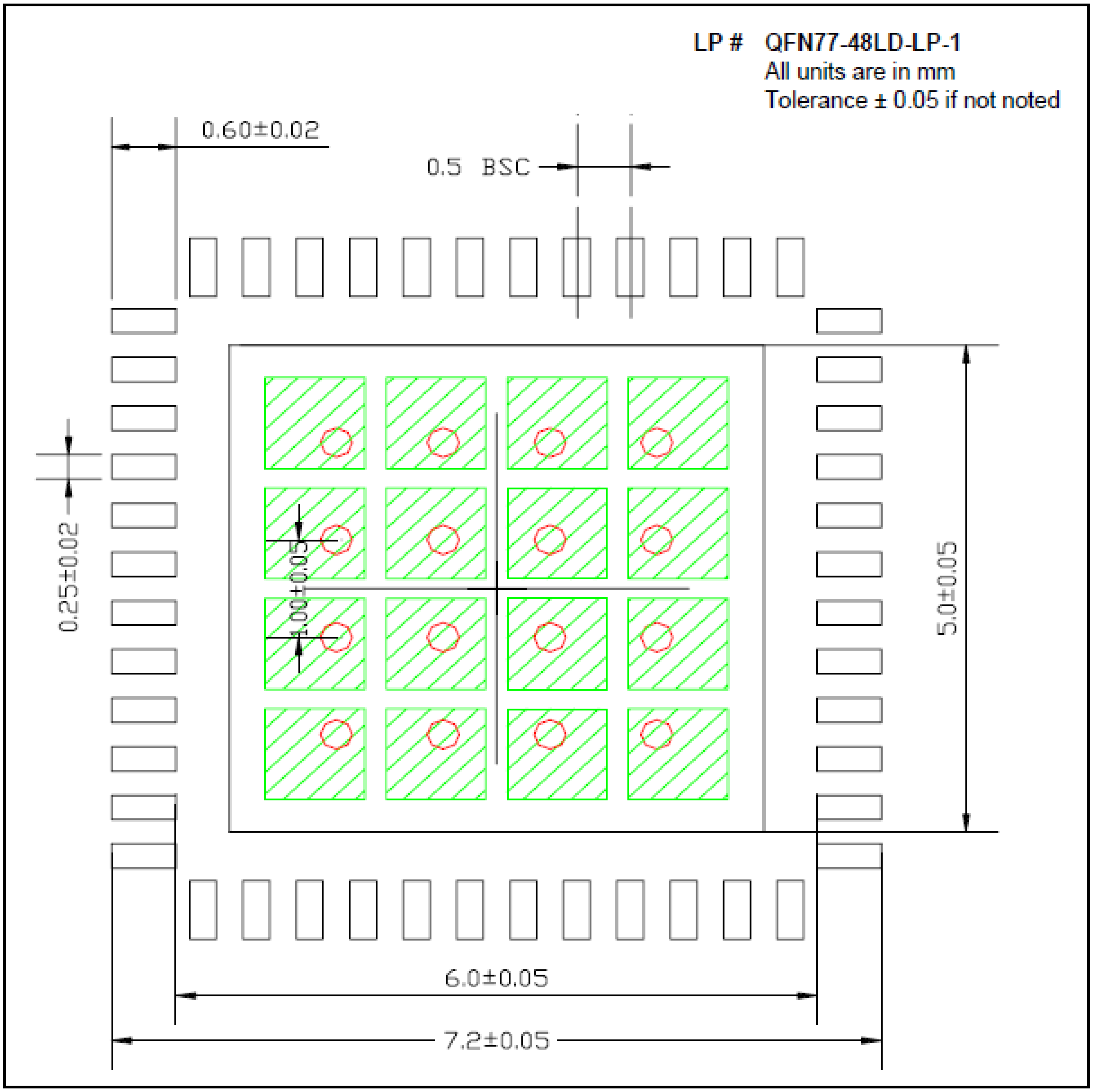
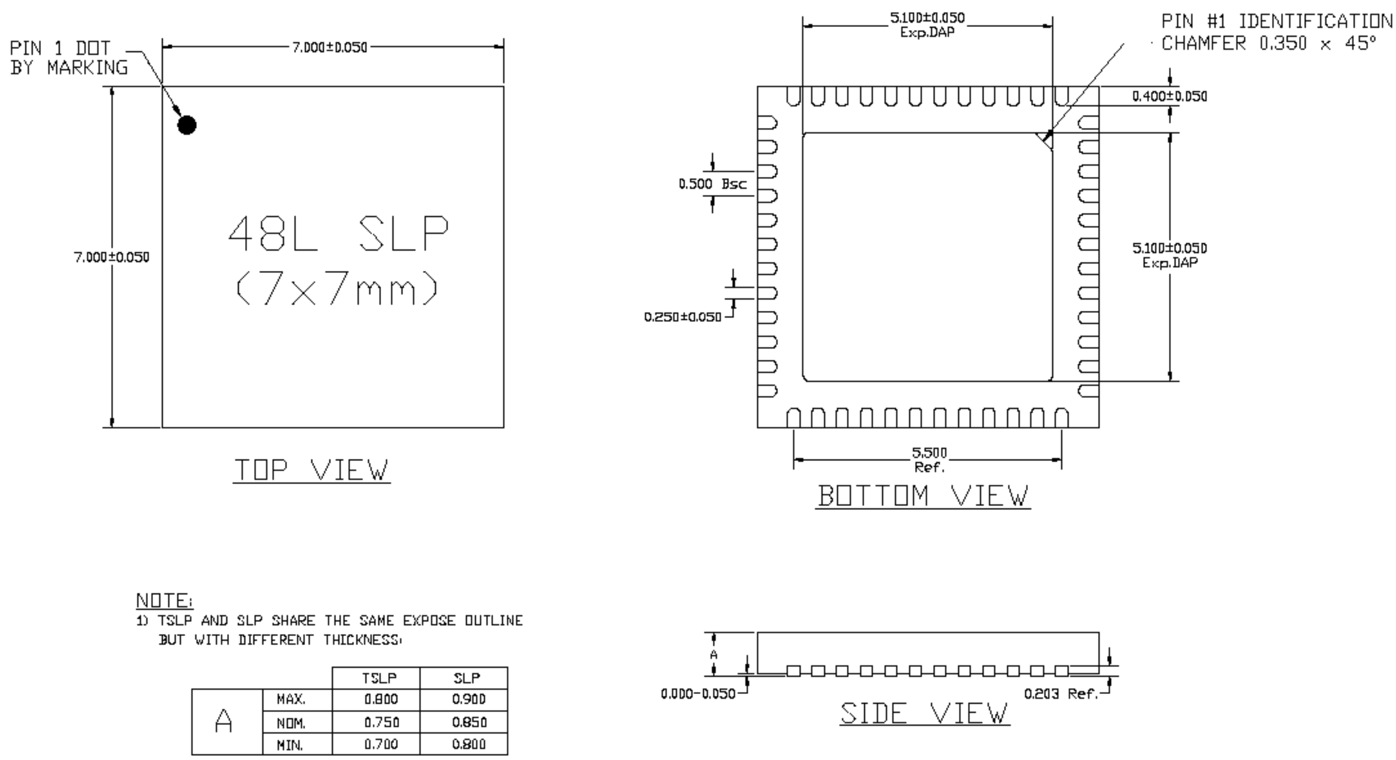


Figure 21. Recommended Land Pattern, 48-Pin (7mm x 7mm) QFN

Red circle indicates Thermal Via. Size should be 0.350 mm in diameter and it should be connected to GND plane for maximum thermal performance.

Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Size should be 0.93x0.93 mm in size, 1.13 mm pitch.

Package Information



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

48-Pin (7mm x 7mm) QFN

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