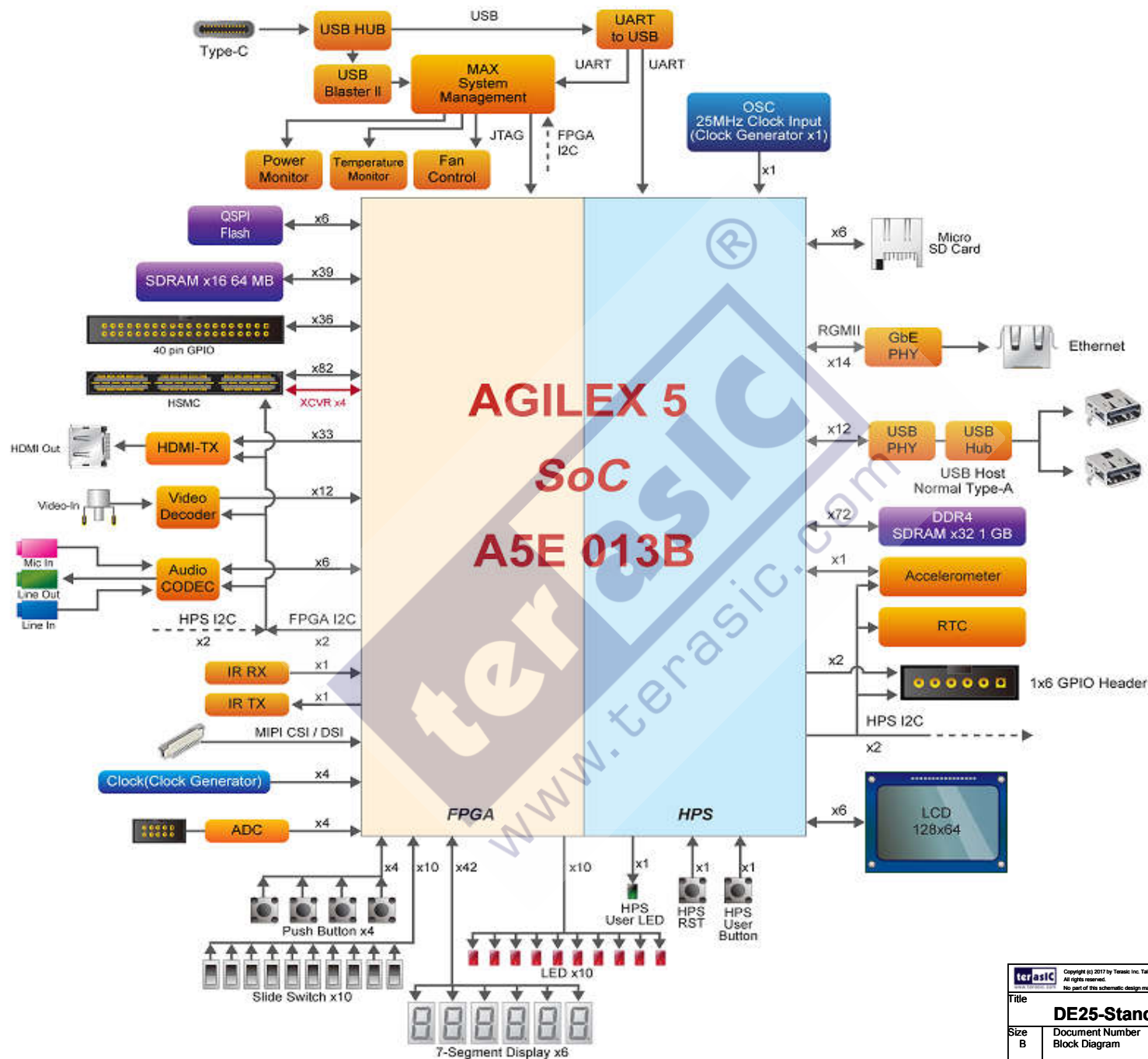
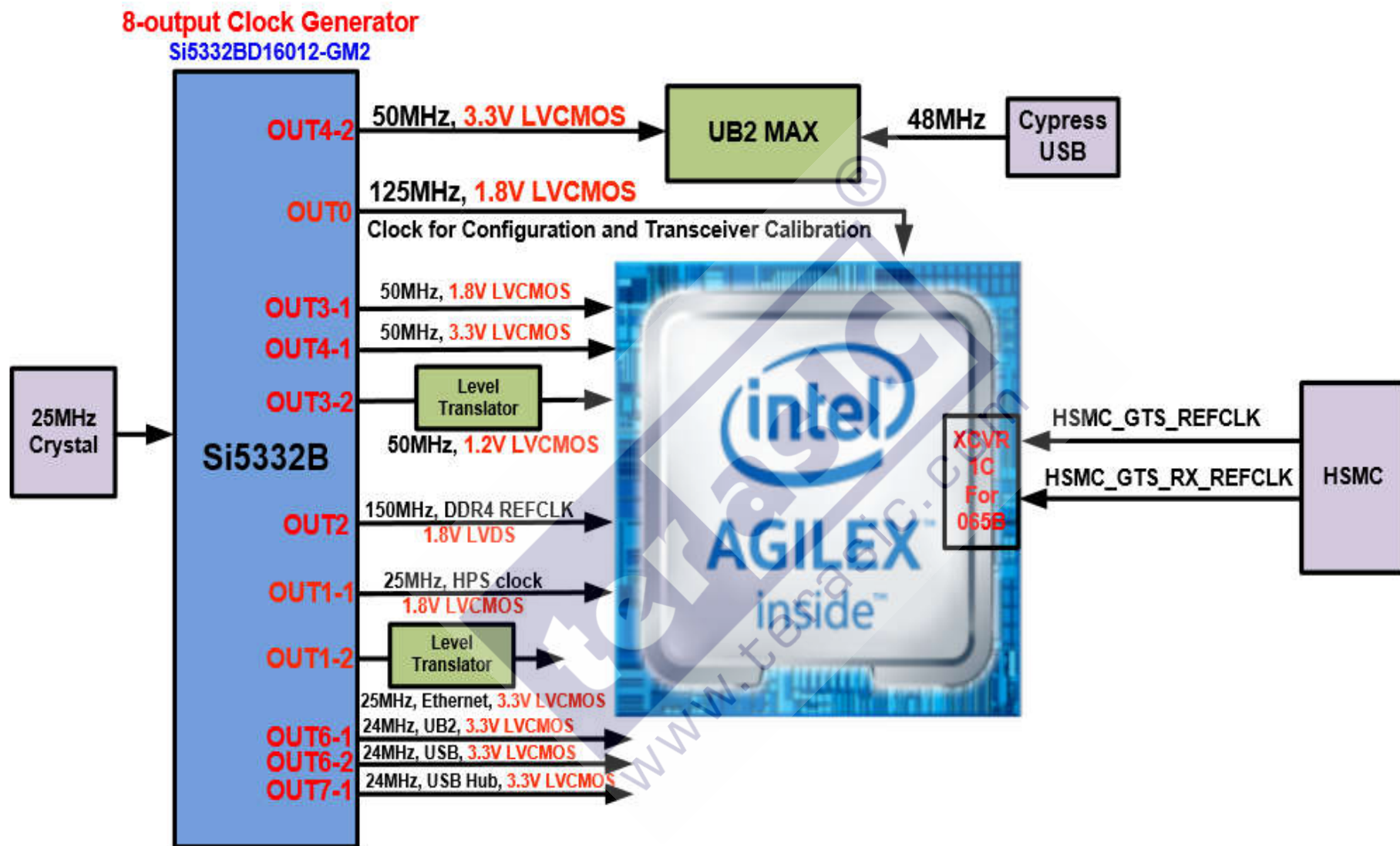
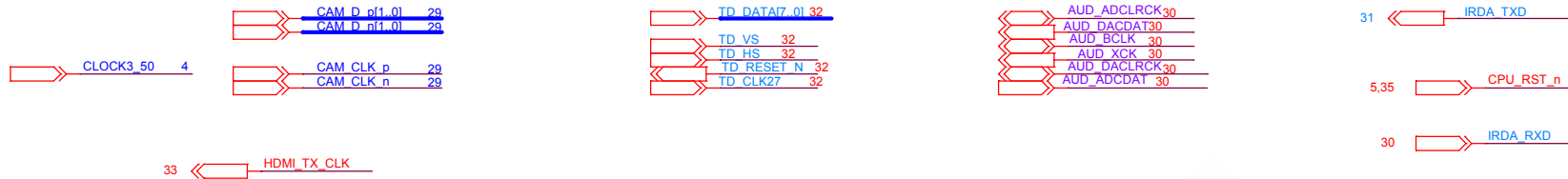


# Block Diagram



# Clock Tree



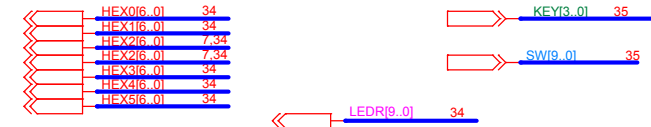


U30C

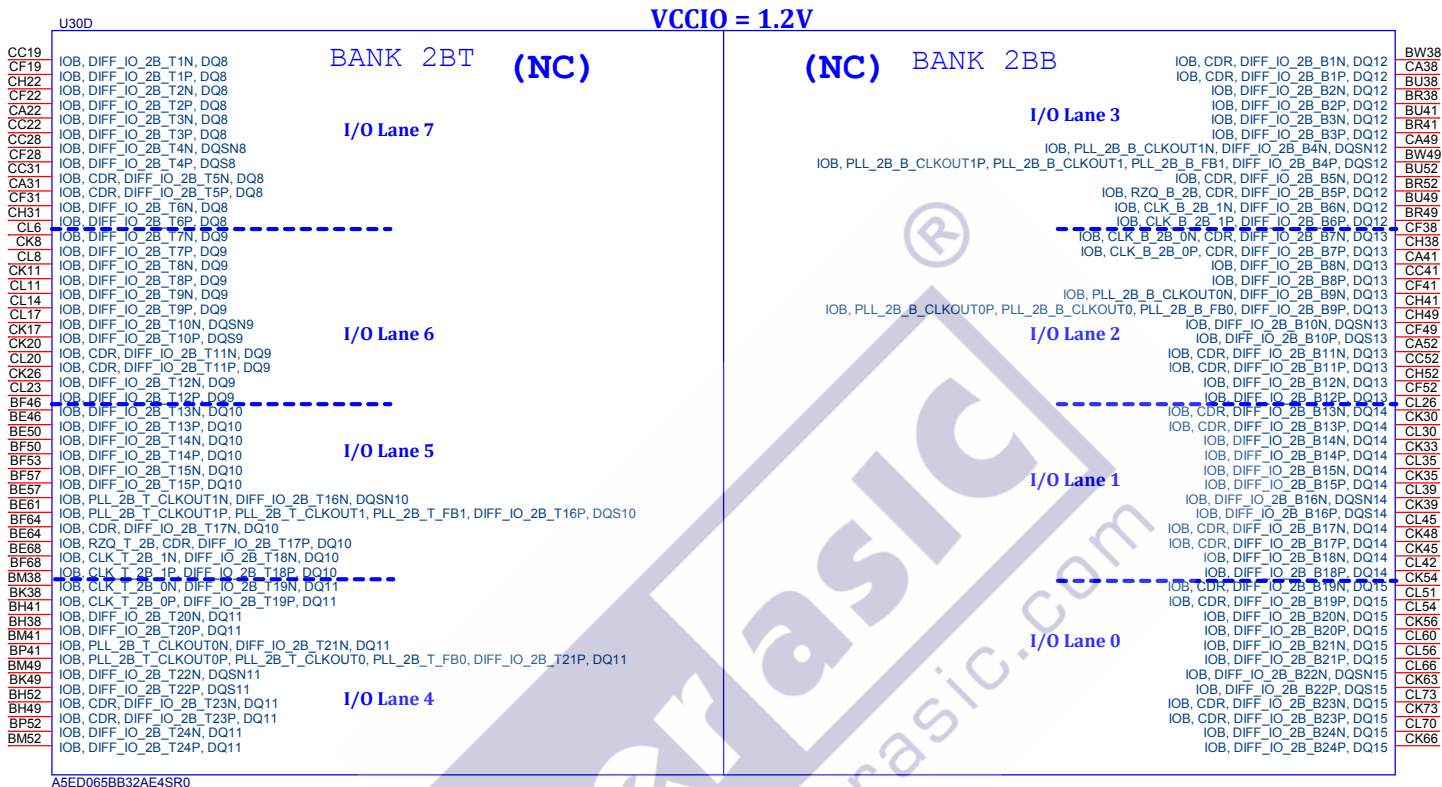
VCCIO = 1.2V




A5ED065BB32A4SR0



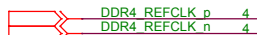
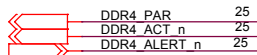
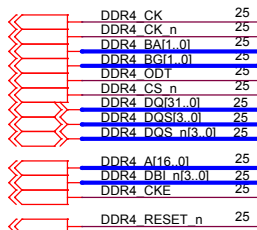
Title		
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Size	Document Number	
	FPGA Bank 2A	
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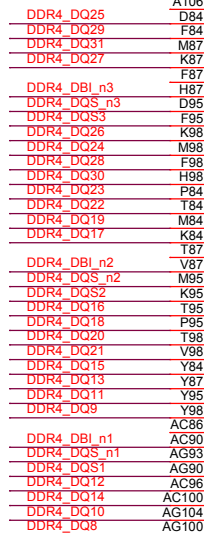
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Title <b>DE25-Standard Board</b>		
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## DDR4



RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14



U30E

BANK 3AT

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

VCCIO = 1.2V

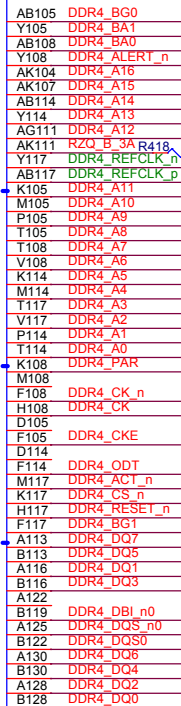
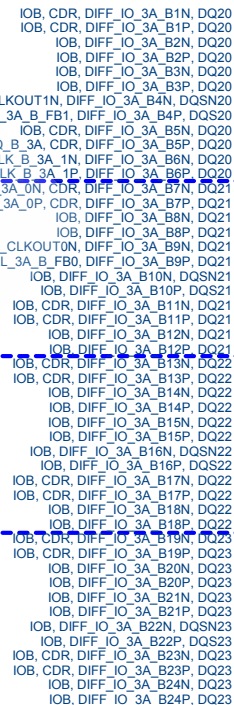
BANK 3AB

I/O Lane 3


I/O Lane 2

I/O Lane 1

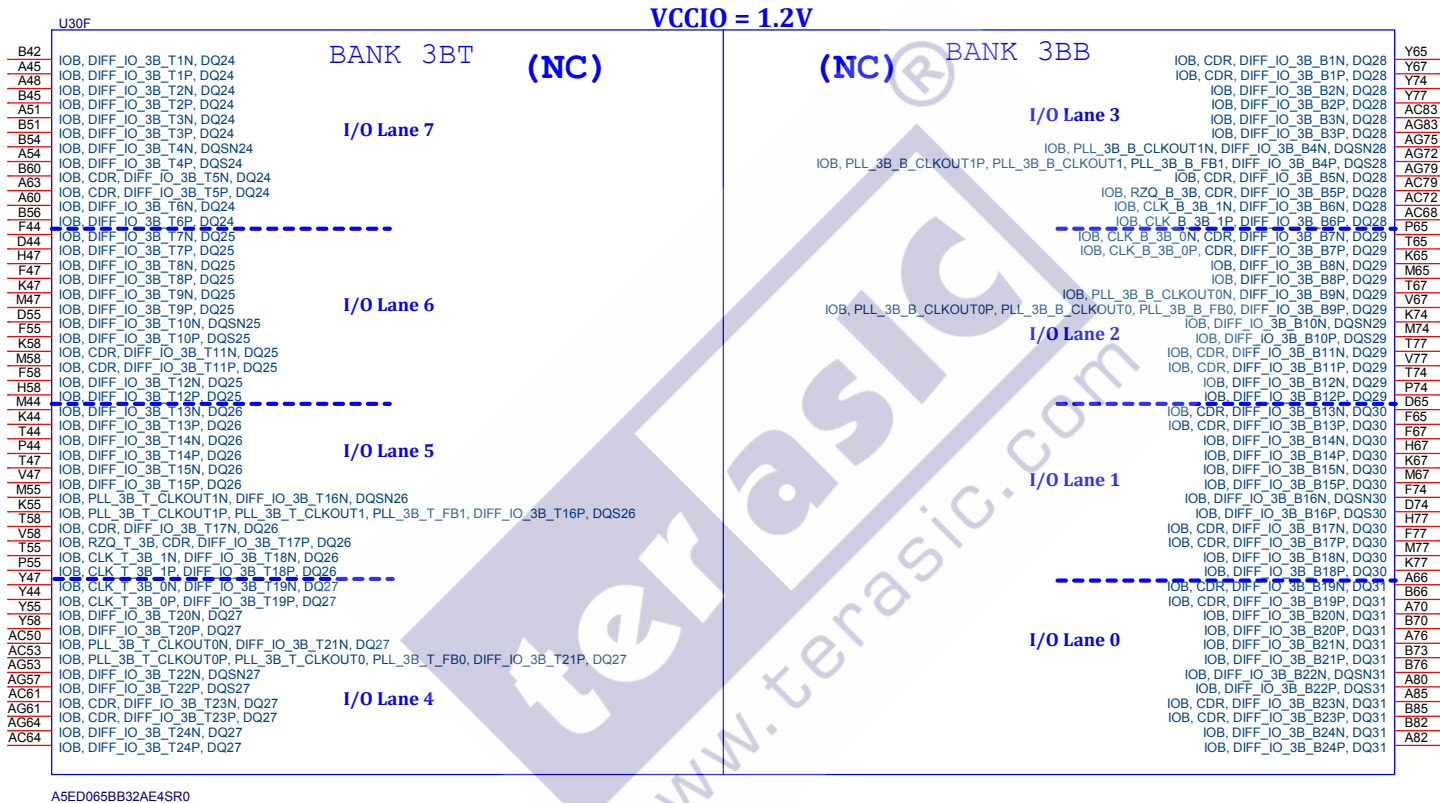
I/O Lane 0



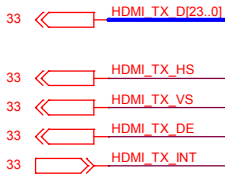
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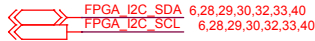




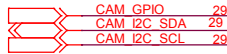
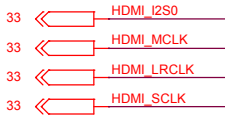
HDMI TX



FPGA I2C Interface



HDMI Audio Interface



VCCIO = 3.3V

HDMI_TX_D0	CD134
HDMI_TX_D1	CD135
HDMI_TX_D2	CG134
HDMI_TX_D3	CG135
HDMI_TX_D4	CH132
HDMI_TX_D5	CF132
HDMI_TX_D6	CF128
HDMI_TX_D7	CK134
CLOCK_50	CH128
HDMI_TX_D8	CL125
HDMI_TX_D9	CF121
HDMI_TX_D11	BU118
HDMI_TX_D12	BR118
HDMI_TX_D13	CA118
HDMI_TX_D14	BW118
HDMI_TX_D15	CL128
HDMI_TX_D16	CL130
HDMI_TX_D17	CK125
HDMI_TX_D18	CK128

U30G

HVIO\_5A\_1, SYSPLLREFCLK\_L1A\_0, TXCLK1, DATA\_CTRL1  
HVIO\_5A\_2, SYSPLLREFCLK\_L1A\_1, TXCLK2, DATA\_CTRL2  
HVIO\_5A\_3, SYSPLLREFCLK\_L1B\_0, TXCLK3, DATA\_CTRL3  
HVIO\_5A\_4, SYSPLLREFCLK\_L1B\_1, TXCLK4, DATA\_CTRL4  
HVIO\_5A\_5, PIN\_PERST\_N\_CVP\_L1A\_0, TXCLK5, DATA\_CTRL5  
HVIO\_5A\_6, PIN\_PERST\_N\_CVP\_L1B\_0, TXCLK6, DATA\_CTRL6  
HVIO\_5A\_7, PIN\_PERST\_N\_CVP\_L1C\_0, TXCLK7, DATA\_CTRL7  
HVIO\_5A\_8, TXCLK8, DATA\_CTRL8  
HVIO\_5A\_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA\_CTRL9  
HVIO\_5A\_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA\_CTRL10  
HVIO\_5A\_11, SOURCE\_SYNC\_CLK1, TXCLK11, RXCLK3, DATA\_CTRL11  
HVIO\_5A\_12, SOURCE\_SYNC\_CLK2, TXCLK12, RXCLK4, DATA\_CTRL12  
HVIO\_5A\_13, TXCLK13, DATA\_CTRL13  
HVIO\_5A\_14, TXCLK14, DATA\_CTRL14  
HVIO\_5A\_15, TXCLK15, DATA\_CTRL15  
HVIO\_5A\_16, TXCLK16, DATA\_CTRL16  
HVIO\_5A\_17, TXCLK17, DATA\_CTRL17  
HVIO\_5A\_18, TXCLK18, DATA\_CTRL18  
HVIO\_5A\_19, SYSPLLREFCLK\_L1C\_0, TXCLK19, DATA\_CTRL19  
HVIO\_5A\_20, TXCLK20, DATA\_CTRL20


BANK 5A

HVIO\_5B\_1, SYSPLLREFCLK\_L1A\_2, TXCLK1, DATA\_CTRL1  
HVIO\_5B\_2, SYSPLLREFCLK\_L1A\_3, TXCLK2, DATA\_CTRL2  
HVIO\_5B\_3, SYSPLLREFCLK\_L1B\_2, TXCLK3, DATA\_CTRL3  
HVIO\_5B\_4, SYSPLLREFCLK\_L1B\_3, TXCLK4, DATA\_CTRL4  
HVIO\_5B\_5, PIN\_PERST\_N\_CVP\_L1A\_1, TXCLK5, DATA\_CTRL5  
HVIO\_5B\_6, PIN\_PERST\_N\_CVP\_L1B\_1, TXCLK6, DATA\_CTRL6  
HVIO\_5B\_7, PIN\_PERST\_N\_CVP\_L1C\_1, TXCLK7, DATA\_CTRL7  
HVIO\_5B\_8, TXCLK8, DATA\_CTRL8  
HVIO\_5B\_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA\_CTRL9  
HVIO\_5B\_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA\_CTRL10  
HVIO\_5B\_11, SOURCE\_SYNC\_CLK1, TXCLK11, RXCLK3, DATA\_CTRL11  
HVIO\_5B\_12, SOURCE\_SYNC\_CLK2, TXCLK12, RXCLK4, DATA\_CTRL12  
HVIO\_5B\_13, TXCLK13, DATA\_CTRL13  
HVIO\_5B\_14, TXCLK14, DATA\_CTRL14  
HVIO\_5B\_15, TXCLK15, DATA\_CTRL15  
HVIO\_5B\_16, TXCLK16, DATA\_CTRL16  
HVIO\_5B\_17, TXCLK17, DATA\_CTRL17  
HVIO\_5B\_18, TXCLK18, DATA\_CTRL18  
HVIO\_5B\_19, SYSPLLREFCLK\_L1C\_1, TXCLK19, DATA\_CTRL19  
HVIO\_5B\_20, TXCLK20, DATA\_CTRL20

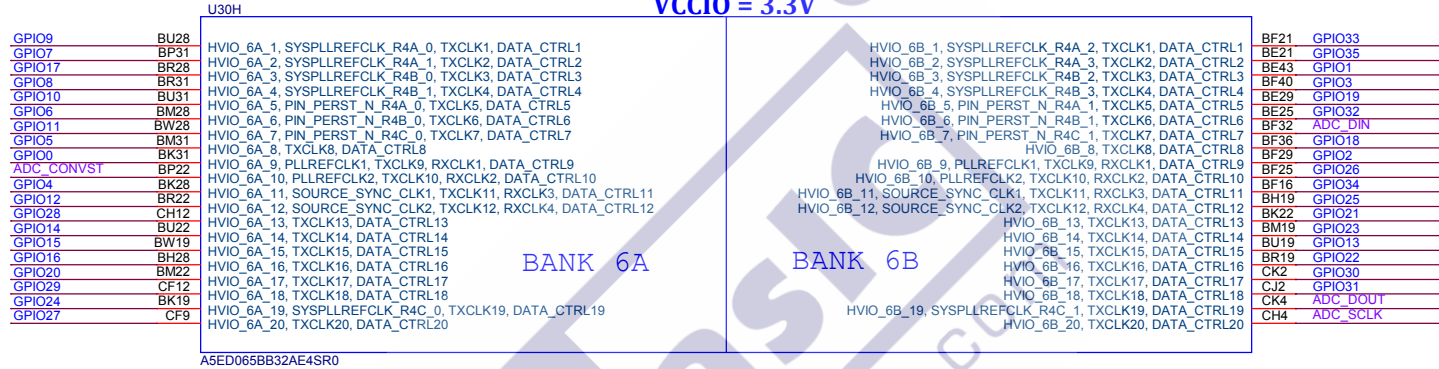
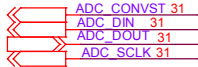
BANK 5B

BF111	HDMI_TX_D19
BH109	HDMI_TX_D20
BE115	HDMI_TX_D21
BF115	HDMI_TX_D22
BF107	HSMC_B5B_D0_E (Reset input in PCIe)
BU109	HDMI_TX_D23
BF104	HSMC_B5B_D1_E
BR109	HDMI_TX_HS
BE107	HDMI_TX_VS
BK109	HDMI_TX_DE
BE111	HDMI_TX_INT
BM109	FPGA_I2C_SDA
BR112	FPGA_I2C_SCL
BK113	HDMI_I2S0
BM118	HDMI_MCLK
BP112	HDMI_LRCLK
BM112	HDMI_SCLK
BK112	CAM_GPIO
BH118	CAM_I2C_SDA
BF120	CAM_I2C_SCL

A5ED065BB32AE4SR0

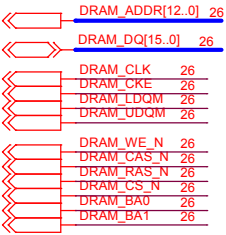
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Title <b>DE25-Standard Board</b>		
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GPIO

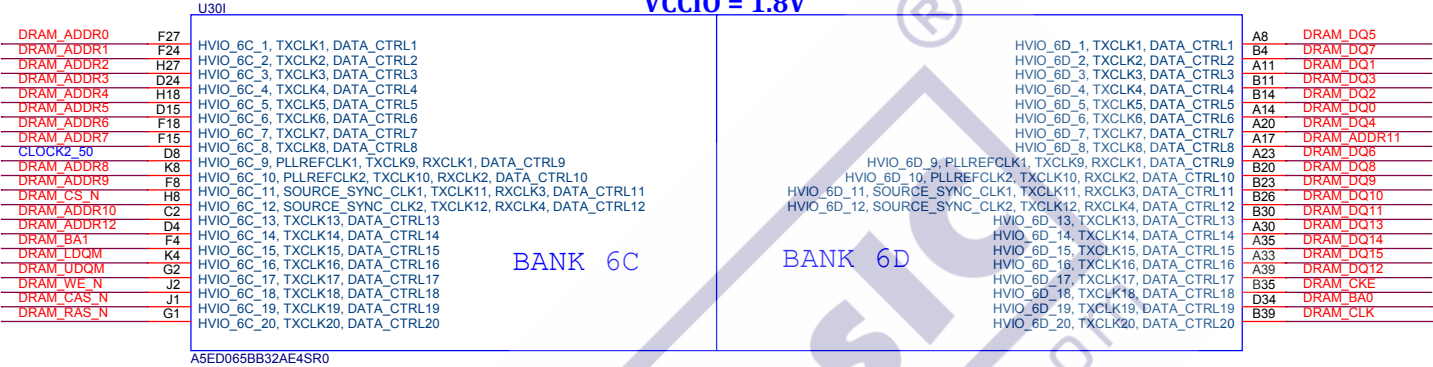




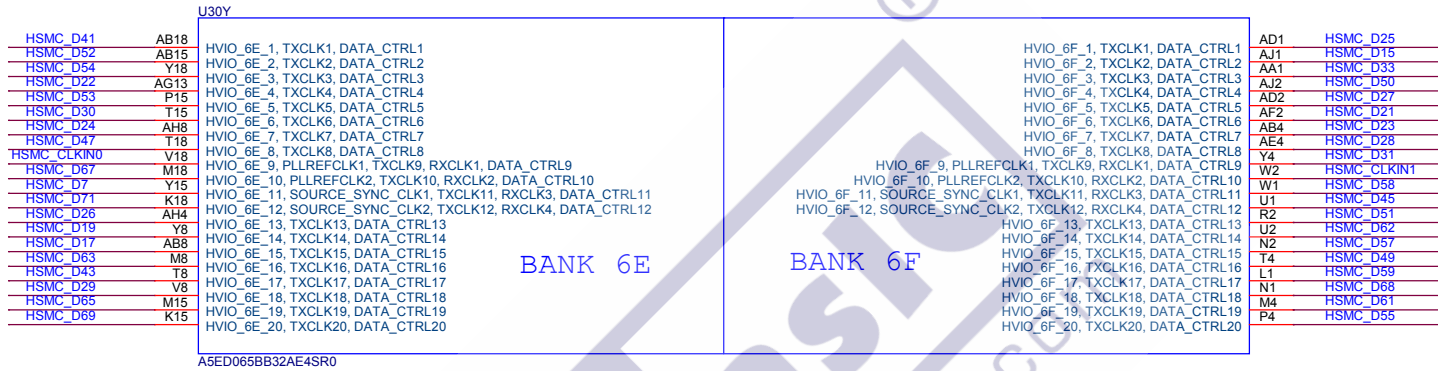
SDRAM




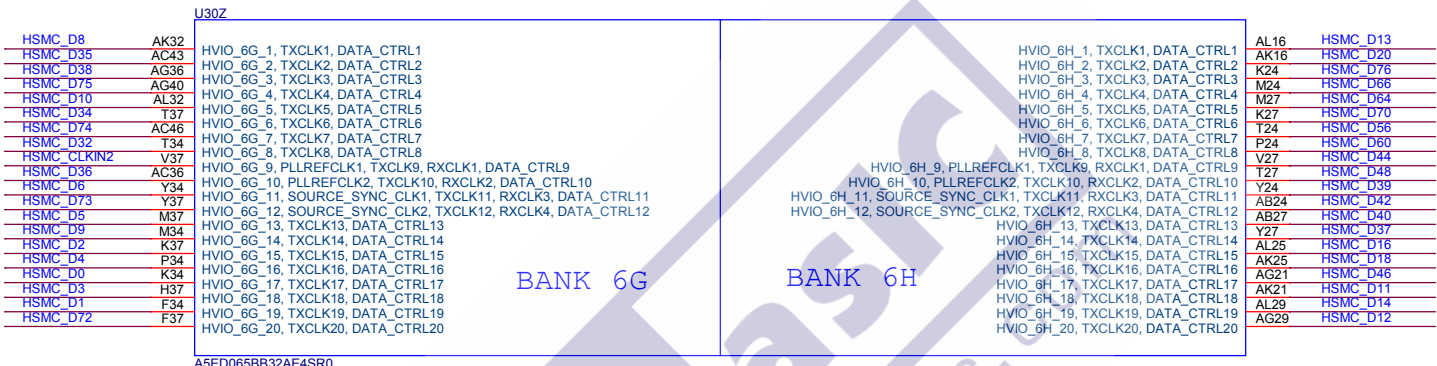
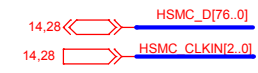
VCCIO = 1.8V



15,28 << HSMC\_D[76..0]  
15,28 << HSMC\_CLKIN[2..0]

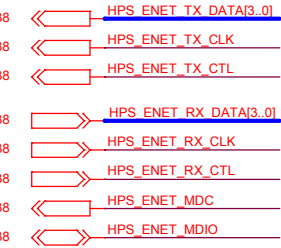


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Title	
DE25-Standard Board	
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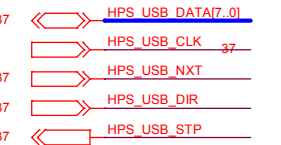


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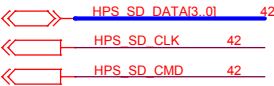
Ethernet PHY Interface (RGMII)



UBS PHY Interface (ULPI)



SD Card



HPS 25MHz Clock



HPS GPIO



HPS I2C Interface



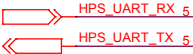
HPS User Button



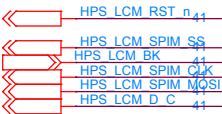
HPS User LED



UART Interface



HPS LCD



HPS_USB_CLK	W135
HPS_USB_STP	U135
HPS_USB_DIR	W134
HPS_USB_DATA0	AK115
HPS_USB_DATA1	U134
HPS_USB_NXT	AL120
HPS_USB_DATA2	R134
HPS_USB_DATA3	AG115
HPS_USB_DATA4	N135
HPS_USB_DATA5	AK120
HPS_USB_DATA6	N134
HPS_USB_DATA7	T132
HPS_ENET_TX_CTL	P132
HPS_ENET_TX_CLK	L135
HPS_ENET_RX_CLK	J135
HPS_ENET_RX_CTL	AD135
HPS_ENET_TX_DATA0	M132
HPS_ENET_TX_DATA1	AD134
HPS_ENET_RX_DATA0	K132
HPS_ENET_RX_DATA1	AG129
HPS_ENET_TX_DATA2	J134
HPS_ENET_TX_DATA3	G134
HPS_ENET_RX_DATA2	G135
HPS_ENET_RX_DATA3	G135

HPS_SD_DATA0	E135
HPS_SD_DATA1	F132
HPS_SD_CLK	D132
HPS_CLK_25	AG123
HPS_GSENSOR_INT	B134
HPS_SD_DATA2	AA135
HPS_SD_DATA3	V127
HPS_SD_CMD	AB132
HPS_GPIO0	T127
HPS_GPIO1	T124
HPS_LCM_RST_n	P124
HPS_LCM_D_C	P124
HPS_I2C_SDA	M127
HPS_I2C_SCL	K127
HPS_UART_TX	M124
HPS_UART_RX	AB127
HPS_KEY	K124
HPS_LED	Y127
HPS_LCM_BK	H127
HPS_LCM_SPIM_SS	AB124
HPS_LCM_SPIM_CLK	F127
HPS_LCM_SPIM_MOSI	Y124
HPS_ENET_MDIO	F124
HPS_ENET_MDC	D124


U30B

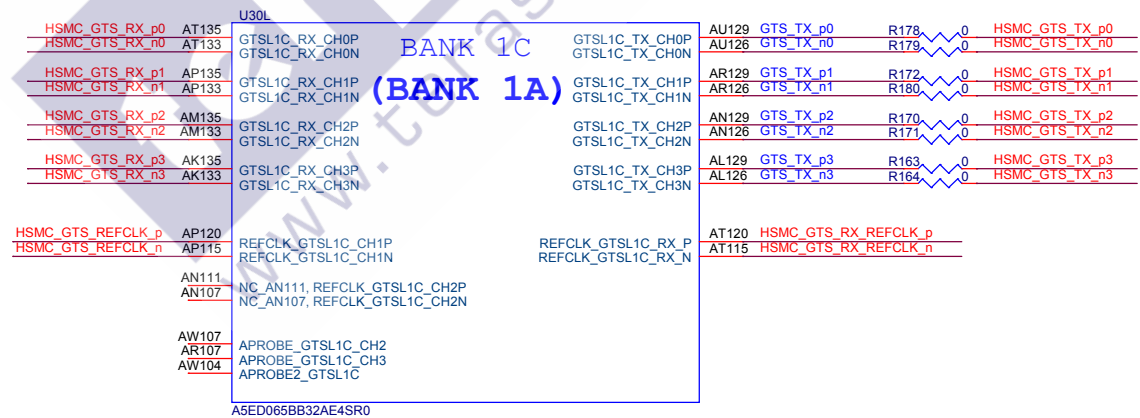
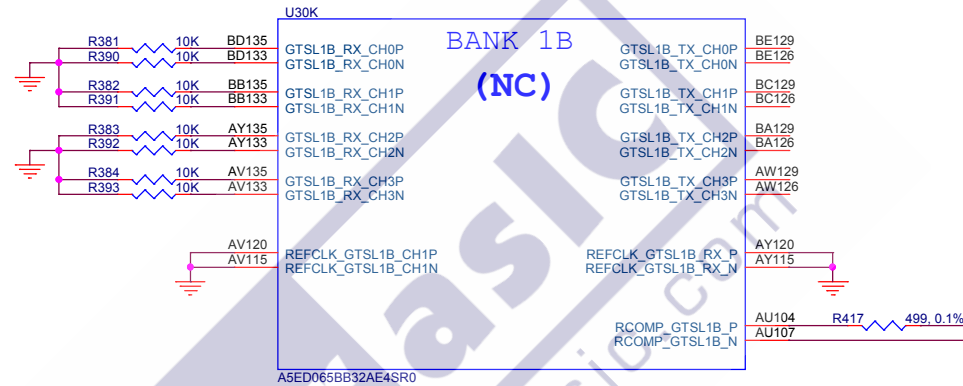
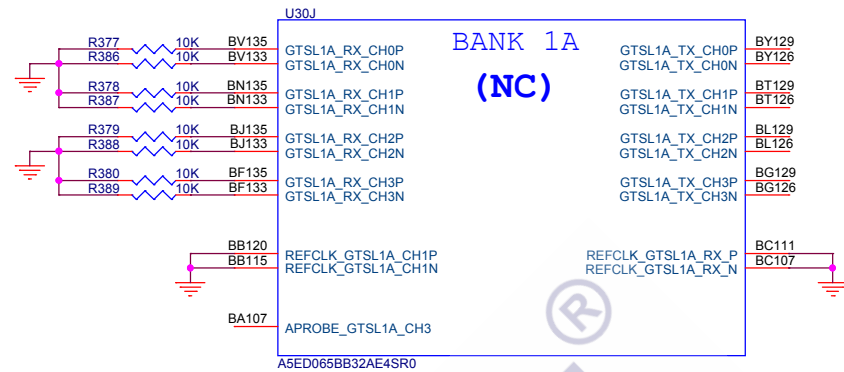
HPS\_IOA\_1, GPIO0\_IO0, SPIM0\_SS1\_N, SPIS0\_CLK, UART0\_CTS\_N, NAND\_ADQ0, SDMMC\_DATA0, USB0\_CLK, EMAC0\_PPS0, TRACE\_D10  
HPS\_IOA\_2, GPIO0\_IO1, SPIM1\_SS1\_N, SPIS0\_MOSI, UART0\_RTS\_N, NAND\_ADQ1, SDMMC\_DATA1, USB0\_STP, EMAC0\_PPSTRIG0, TRACE\_D9  
HPS\_IOA\_3, GPIO0\_IO2, SPIS0\_SS0\_N, UART0\_TX, I2C1\_SDA, NAND\_WE\_N, SDMMC\_CLK, USB0\_DIR, EMAC1\_PPS1, TRACE\_D8  
HPS\_IOA\_4, GPIO0\_IO3, SPIS0\_MISO, UART0\_RX, I2C1\_SCL, NAND\_RE\_N, USB0\_DATA0, EMAC1\_PPSTRIG1, TRACE\_D7  
HPS\_IOA\_5, GPIO0\_IO4, SPIM0\_CLK, UART1\_CTS\_N, I2C0\_SDA, NAND\_WP\_N, SDMMC\_WRITE\_PROTECT, USB0\_DATA1, EMAC2\_PPS2, TRACE\_D6  
HPS\_IOA\_6, GPIO0\_IO5, SPIM0\_MOSI, UART1\_RTS\_N, I2C0\_SCL, NAND\_ADQ2, SDMMC\_DATA2, USB0\_NXT, EMAC2\_PPSTRIG2, TRACE\_D5  
HPS\_IOA\_7, GPIO0\_IO6, SPIM0\_MISO, MDIO2\_MDIO, UART1\_TX, I2C\_EMAC2\_SDA, NAND\_ADQ3, SDMMC\_DATA3, USB0\_DATA2, TRACE\_D4  
HPS\_IOA\_8, GPIO0\_IO7, SPIM0\_SS0\_N, MDIO2\_MDC, UART1\_RX, I2C\_EMAC2\_SCL, NAND\_CLE, SDMMC\_CMD, USB0\_DATA3, TRACE\_D15  
HPS\_IOA\_9, GPIO0\_IO8, SPIM1\_CLK, SPIS1\_CLK, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ4, SDMMC\_DATA4, USB0\_DATA4, I3C1\_SCL, TRACE\_D14  
HPS\_IOA\_10, GPIO0\_IO9, SPIM1\_MOSI, SPIS1\_MOSI, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ5, SDMMC\_DATA5, USB0\_DATA5, I3C1\_SCL, TRACE\_D13  
HPS\_IOA\_11, GPIO0\_IO10, SPIM1\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, SDMMC\_DATA6, USB0\_DATA6, I3C0\_SDA, TRACE\_D12  
HPS\_IOA\_12, GPIO0\_IO11, SPIM1\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ7, SDMMC\_DATA7, USB0\_DATA7, I3C0\_SCL, TRACE\_D11  
HPS\_IOA\_13, GPIO0\_IO12, NAND\_ALE, SDMMC\_PU\_PD\_DATA2, USB1\_CLK, EMAC0\_TX\_CLK, TRACE\_D10  
HPS\_IOA\_14, GPIO0\_IO13, NAND\_RB\_N, SDMMC\_BUS\_PWR, USB1\_STP, EMAC0\_TX\_CTL, TRACE\_D9  
HPS\_IOA\_15, GPIO0\_IO14, NAND\_CE\_N, USB1\_DIR, EMAC0\_RX\_CLK, TRACE\_D8  
HPS\_IOA\_16, GPIO0\_IO15, NAND\_DQS, SDMMC\_DATA\_STROBE, USB1\_DATA0, EMAC0\_RX\_CTL, TRACE\_D7  
HPS\_IOA\_17, GPIO0\_IO16, I3C1\_SDA, NAND\_ADQ8, USB1\_NXT, EMAC0\_TXD0, TRACE\_D6  
HPS\_IOA\_18, GPIO0\_IO17, I3C1\_SCL, NAND\_ADQ9, USB1\_NXT, EMAC0\_TXD1, TRACE\_D5  
HPS\_IOA\_19, GPIO0\_IO18, I3C0\_SDA, NAND\_ADQ10, USB1\_DATA2, EMAC0\_RXD0, TRACE\_D4  
HPS\_IOA\_20, GPIO0\_IO19, SPIM1\_SS1\_N, I3C0\_SCL, NAND\_ADQ11, USB1\_DATA3, EMAC0\_RXD1, TRACE\_CLK  
HPS\_IOA\_21, GPIO0\_IO20, SPIM1\_CLK, SPIS0\_CLK, UART0\_CTS\_N, I2C1\_SDA, NAND\_ADQ12, USB1\_DATA4, EMAC0\_TXD2, TRACE\_D0  
HPS\_IOA\_22, GPIO0\_IO21, SPIM1\_MOSI, SPIS0\_MOSI, UART0\_RTS\_N, I2C1\_SCL, NAND\_ADQ13, USB1\_DATA5, EMAC0\_TXD3, TRACE\_D1  
HPS\_IOA\_23, GPIO0\_IO22, SPIM1\_MISO, SPIS0\_SS0\_N, UART0\_TX, I2C0\_SDA, NAND\_ADQ14, USB1\_DATA6, EMAC0\_RXD2, TRACE\_D2  
HPS\_IOA\_24, GPIO0\_IO23, SPIM1\_SS0\_N, SPIS0\_MISO, UART0\_RX, I2C0\_SCL, NAND\_ADQ15, USB1\_DATA7, EMAC0\_RXD3, TRACE\_D3

HPS\_IOB\_1, GPIO1\_IO0, SPIM1\_CLK, CM\_PLL\_CLK0, UART0\_CTS\_N, EMAC0\_PPS0, NAND\_ADQ0, SDMMC\_DATA0, EMAC1\_TX\_CLK, TRACE\_D10  
HPS\_IOB\_2, GPIO1\_IO1, SPIM1\_MOSI, CM\_PLL\_CLK1, UART0\_RTS\_N, EMAC0\_PPSTRIG0, NAND\_ADQ1, SDMMC\_DATA1, EMAC1\_TX\_CTL, TRACE\_D9  
HPS\_IOB\_3, GPIO1\_IO2, SPIM1\_MISO, CM\_PLL\_CLK2, UART0\_TX, I2C0\_SDA, NAND\_WE\_N, SDMMC\_CLK, EMAC1\_RX\_CLK, TRACE\_D8  
HPS\_IOB\_4, GPIO1\_IO3, SPIM1\_SS0\_N, CM\_PLL\_CLK3, UART0\_RX, I2C0\_SCL, NAND\_RE\_N, EMAC1\_RX\_CTL, TRACE\_D7  
HPS\_IOB\_5, GPIO1\_IO4, SPIM1\_SS1\_N, SPIS1\_CLK, UART1\_CTS\_N, EMAC2\_PPS2, NAND\_WP\_N, SDMMC\_WRITE\_PROTECT, I3C1\_SDA, EMAC1\_TXD0, TRACE\_D6  
HPS\_IOB\_6, GPIO1\_IO5, SPIS1\_MOSI, UART1\_RTS\_N, EMAC2\_PPSTRIG2, NAND\_ADQ2, SDMMC\_DATA2, I3C1\_SCL, EMAC1\_TXD1, TRACE\_D5  
HPS\_IOB\_7, GPIO1\_IO6, SPIS1\_SS0\_N, UART1\_TX, I2C1\_SDA, NAND\_ADQ3, SDMMC\_DATA3, I3C0\_SDA, EMAC1\_RXD0, TRACE\_D4  
HPS\_IOB\_8, GPIO1\_IO7, SPIS1\_MISO, UART1\_RX, I2C1\_SCL, NAND\_CLE, SDMMC\_CMD, I3C0\_SCL, EMAC1\_RXD1, TRACE\_D15  
HPS\_IOB\_9, GPIO1\_IO8, JTAG\_TCK, SPIS0\_CLK, MDIO2\_MDIO, I2C\_EMAC2\_SDA, NAND\_ADQ4, SDMMC\_DATA4, EMAC1\_TXD2, TRACE\_D14  
HPS\_IOB\_10, GPIO1\_IO9, JTAG\_TMS, SPIS0\_MOSI, MDIO2\_MDC, I2C\_EMAC2\_SCL, NAND\_ADQ5, SDMMC\_DATA5, EMAC1\_TXD3, TRACE\_D13  
HPS\_IOB\_11, GPIO1\_IO10, JTAG\_TDO, SPIS0\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, SDMMC\_DATA6, EMAC1\_RXD2, TRACE\_D12  
HPS\_IOB\_12, GPIO1\_IO11, JTAG\_TDI, SPIS0\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ7, SDMMC\_DATA7, EMAC1\_RXD3, TRACE\_D11  
HPS\_IOB\_13, GPIO1\_IO12, I2C1\_SDA, NAND\_ALE, SDMMC\_PU\_PD\_DATA2, EMAC2\_TX\_CLK, TRACE\_D10  
HPS\_IOB\_14, GPIO1\_IO13, I2C1\_SCL, NAND\_RB\_N, SDMMC\_BUS\_PWR, EMAC2\_TX\_CTL, TRACE\_D9  
HPS\_IOB\_15, GPIO1\_IO14, UART1\_TX, NAND\_CE\_N, I3C1\_SDA, EMAC2\_RX\_CLK, TRACE\_D8  
HPS\_IOB\_16, GPIO1\_IO15, UART1\_RX, NAND\_DQS, SDMMC\_DATA\_STROBE, I3C1\_SCL, EMAC2\_RX\_CTL, TRACE\_D7  
HPS\_IOB\_17, GPIO1\_IO16, UART1\_CTS\_N, NAND\_ADQ8, I3C0\_SDA, EMAC2\_TXD0, TRACE\_D6  
HPS\_IOB\_18, GPIO1\_IO17, SPIM0\_SS1\_N, UART1\_RTS\_N, NAND\_ADQ9, I3C0\_SCL, EMAC2\_TXD1, TRACE\_D5  
HPS\_IOB\_19, GPIO1\_IO18, SPIM0\_MISO, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ10, EMAC2\_RXD0, TRACE\_D4  
HPS\_IOB\_20, GPIO1\_IO19, SPIM0\_SS0\_N, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ11, EMAC2\_RXD1, TRACE\_CLK  
HPS\_IOB\_21, GPIO1\_IO20, SPIM0\_CLK, SPIS1\_CLK, I2C\_EMAC2\_SDA, NAND\_ADQ12, EMAC2\_TXD2, TRACE\_D0  
HPS\_IOB\_22, GPIO1\_IO21, SPIM0\_MOSI, SPIS1\_MOSI, I2C\_EMAC2\_SCL, NAND\_ADQ13, EMAC2\_TXD3, TRACE\_D1  
HPS\_IOB\_23, GPIO1\_IO22, SPIM0\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ14, EMAC2\_RXD2, TRACE\_D2  
HPS\_IOB\_24, GPIO1\_IO23, SPIM0\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ15, EMAC2\_RXD3, TRACE\_D3

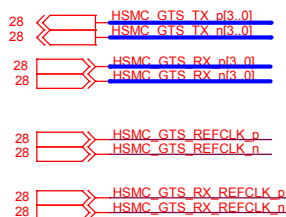
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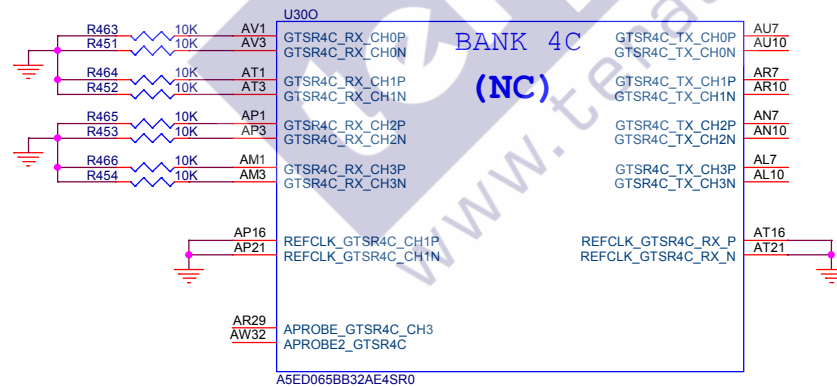
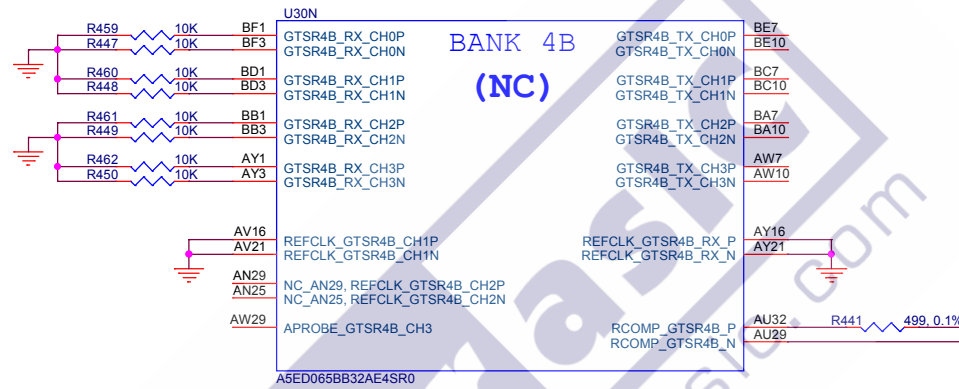
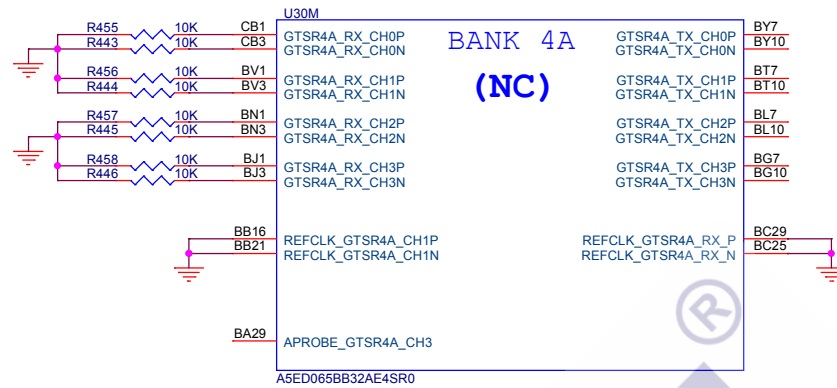
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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	FPGA Bank HPS	B
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### HSMC Transceivers

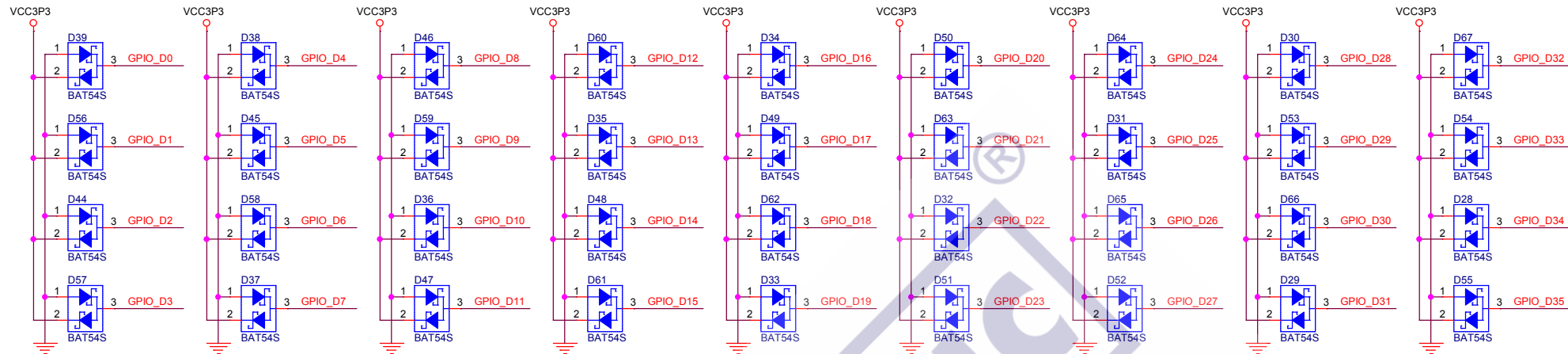


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DE25-Standard Board		
Size	Document Number	Rev
B	FPGA XCVR Bank 1A (NC) · 1B (NC) · 1C	B
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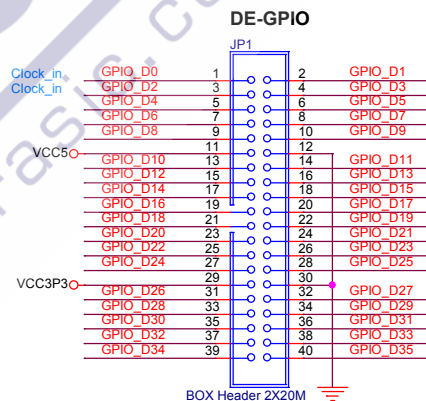
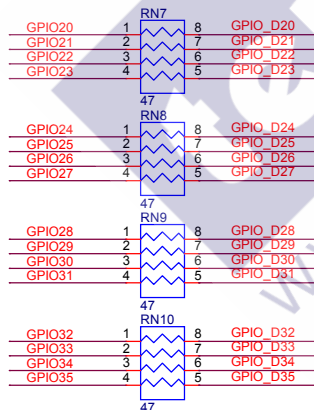
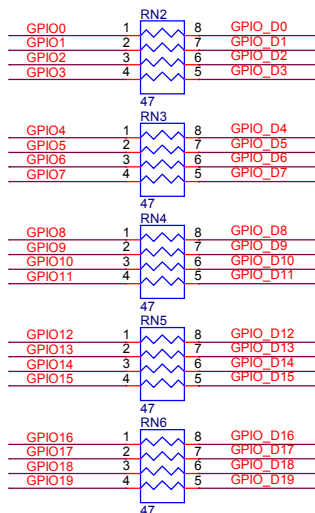


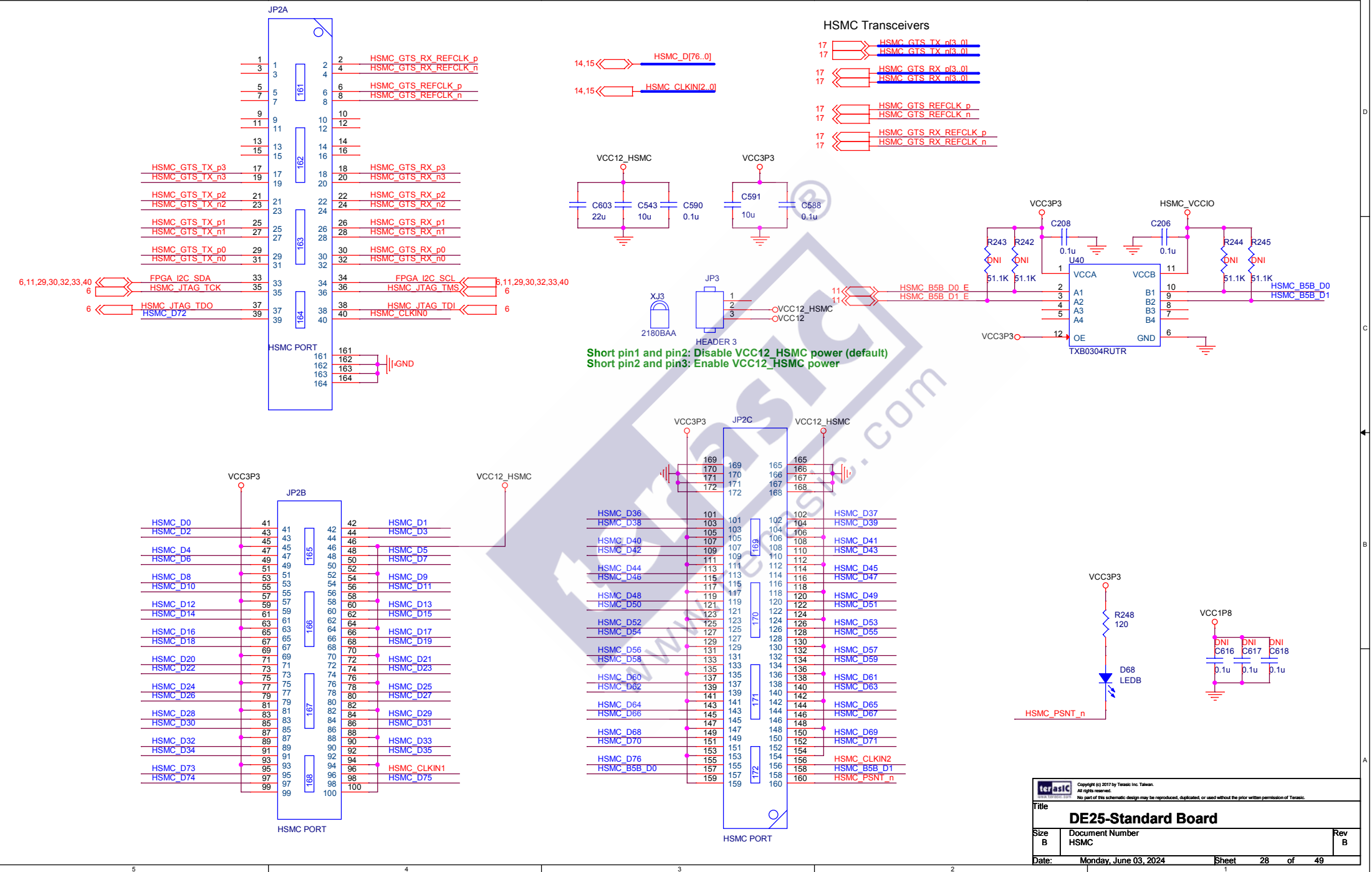
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Title			
DE25-Standard Board			
Size	Document Number		Rev
B	FPGA XCVR Bank 4A · 4B · 4C		B
Date:	Monday, June 03, 2024	Sheet	18 of 49

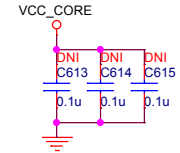
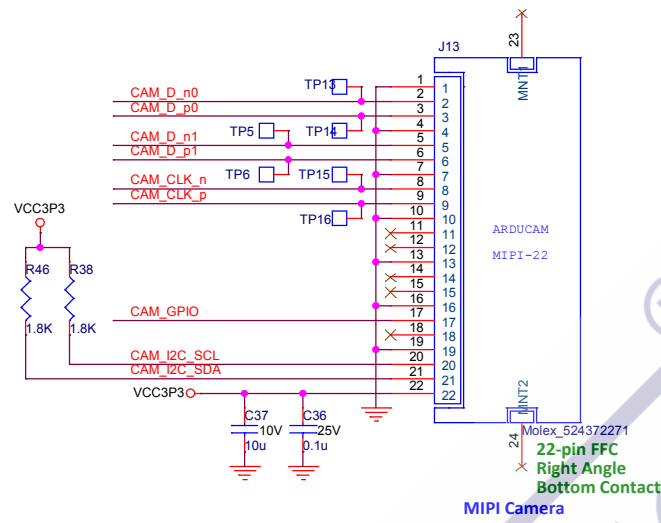
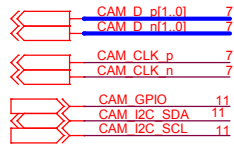




# GPIO



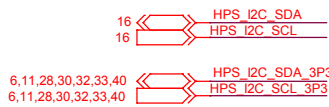




FPGA I2C Interface



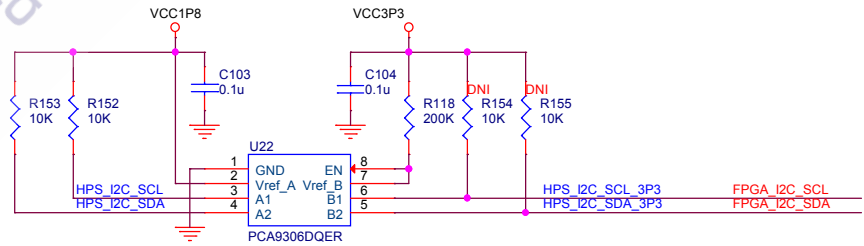
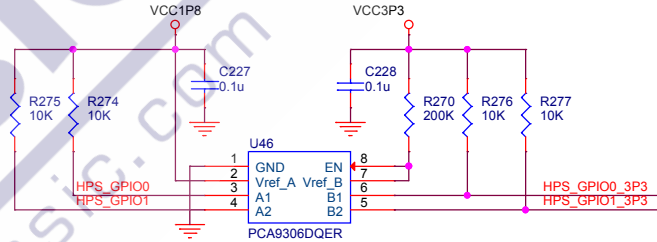
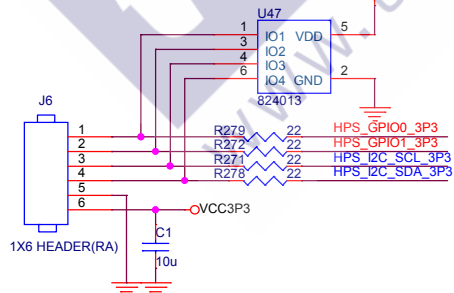
HPS I2C Interface



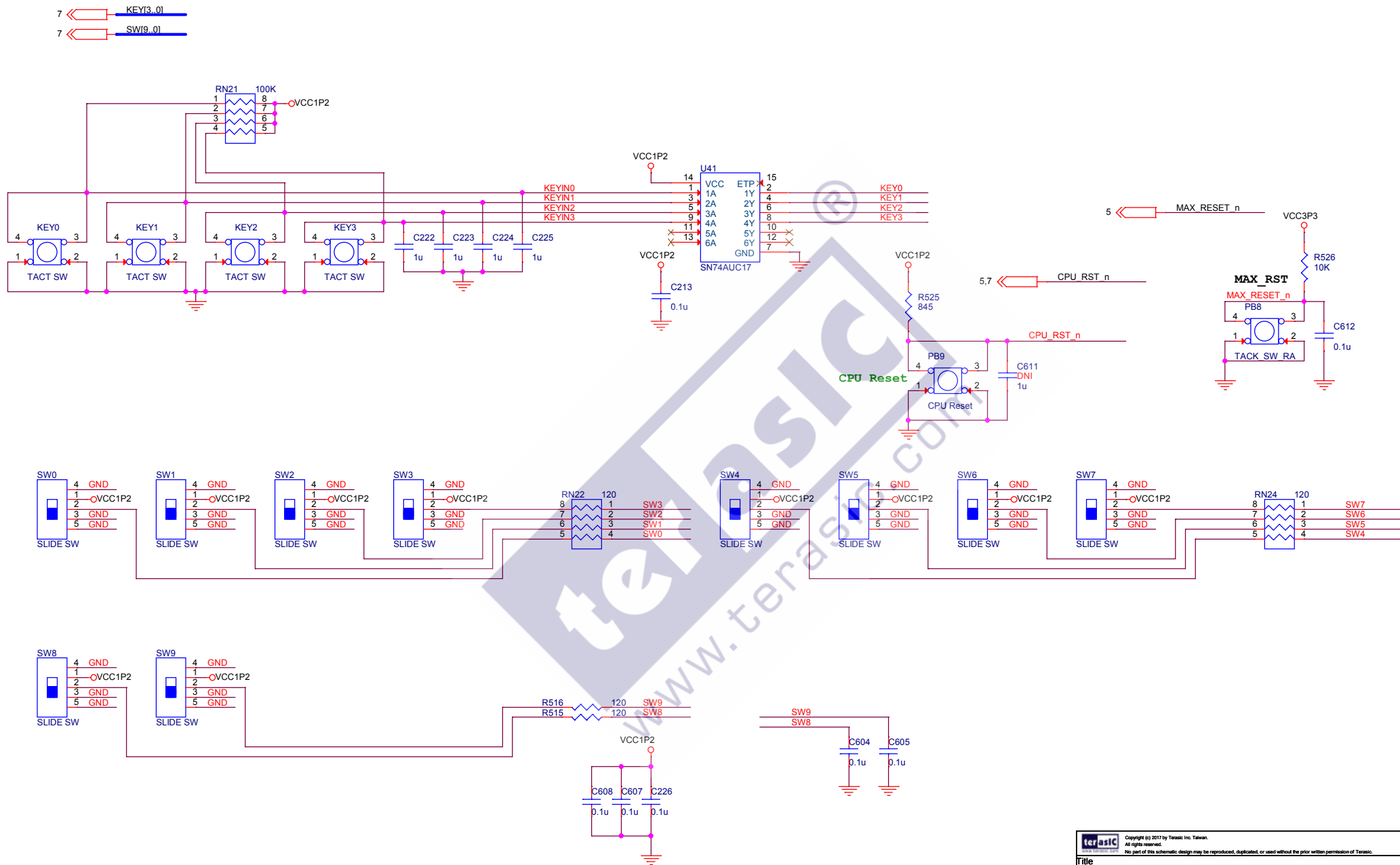
HPS GPIO

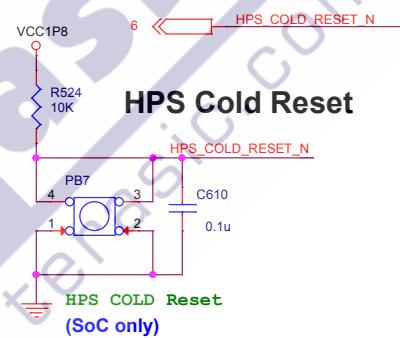
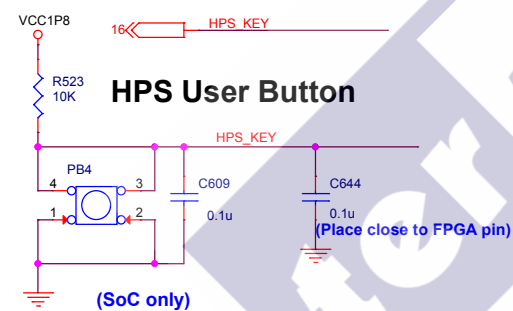
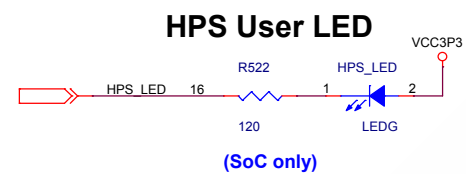



HPS 1x6 GPIO Header



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B	MIPI Connectors, HPS 2x3 GPIO	B	
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Title		
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B	HPS BUTTON, HPS LED	B
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