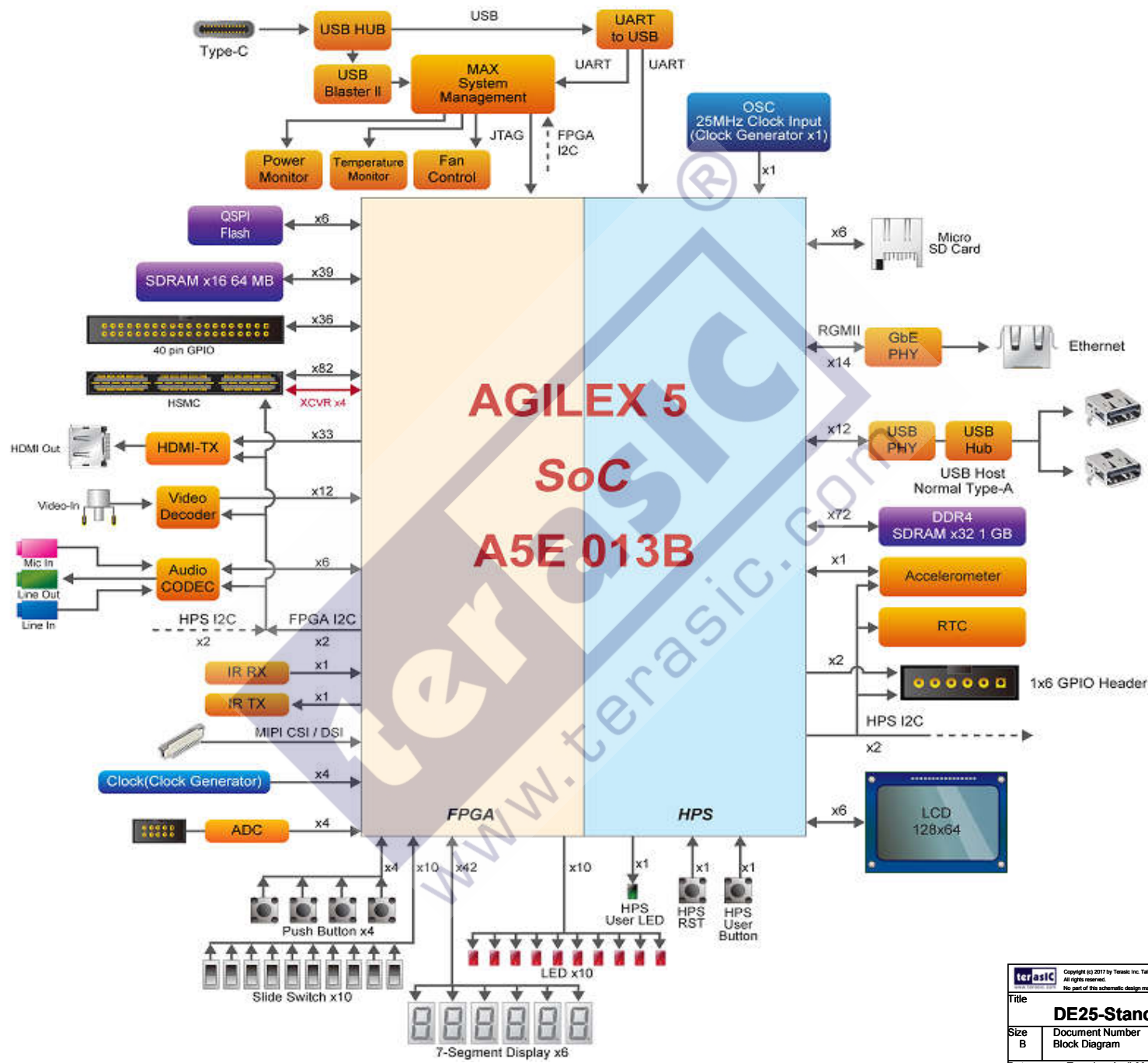


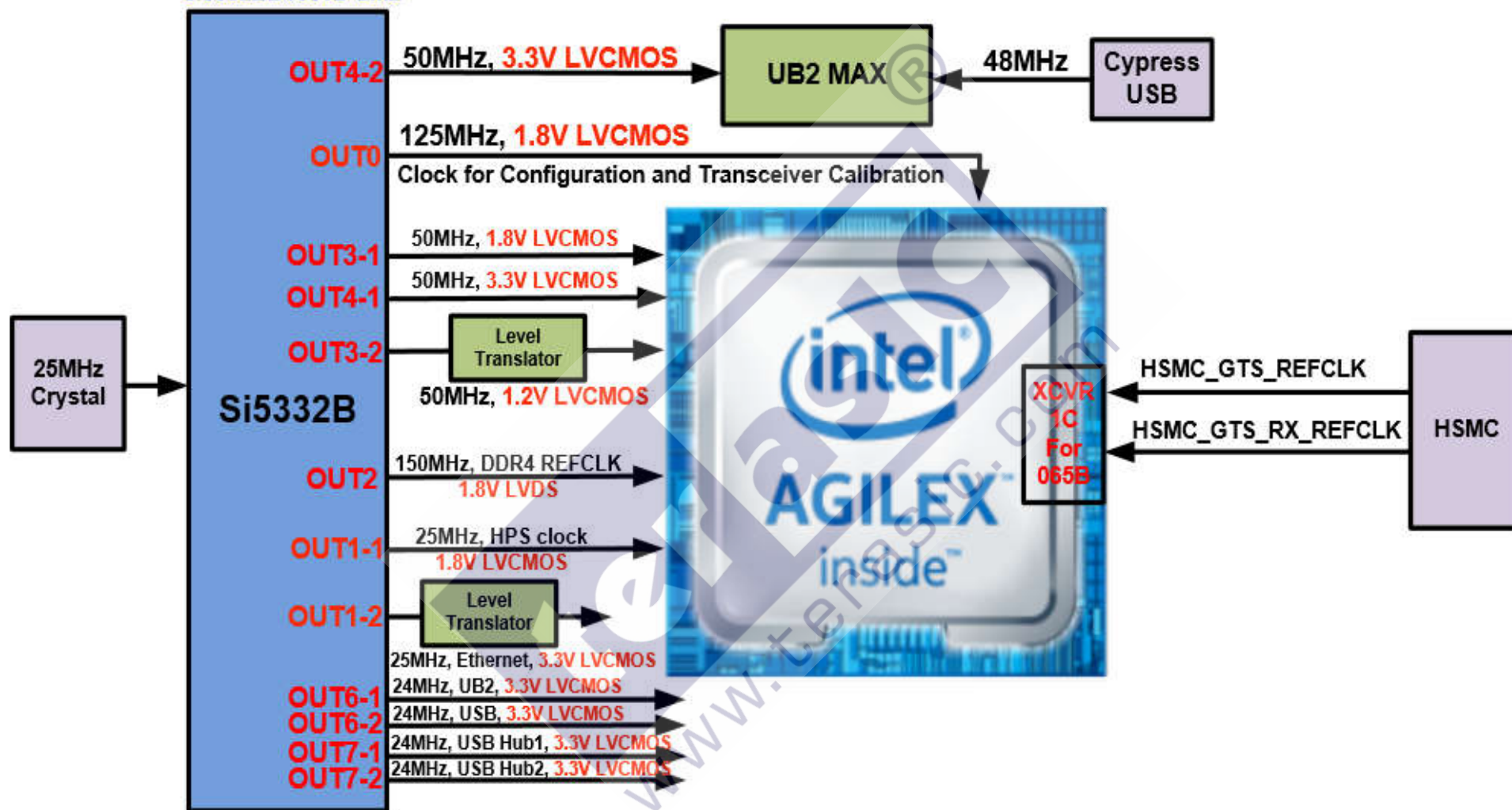
# Block Diagram

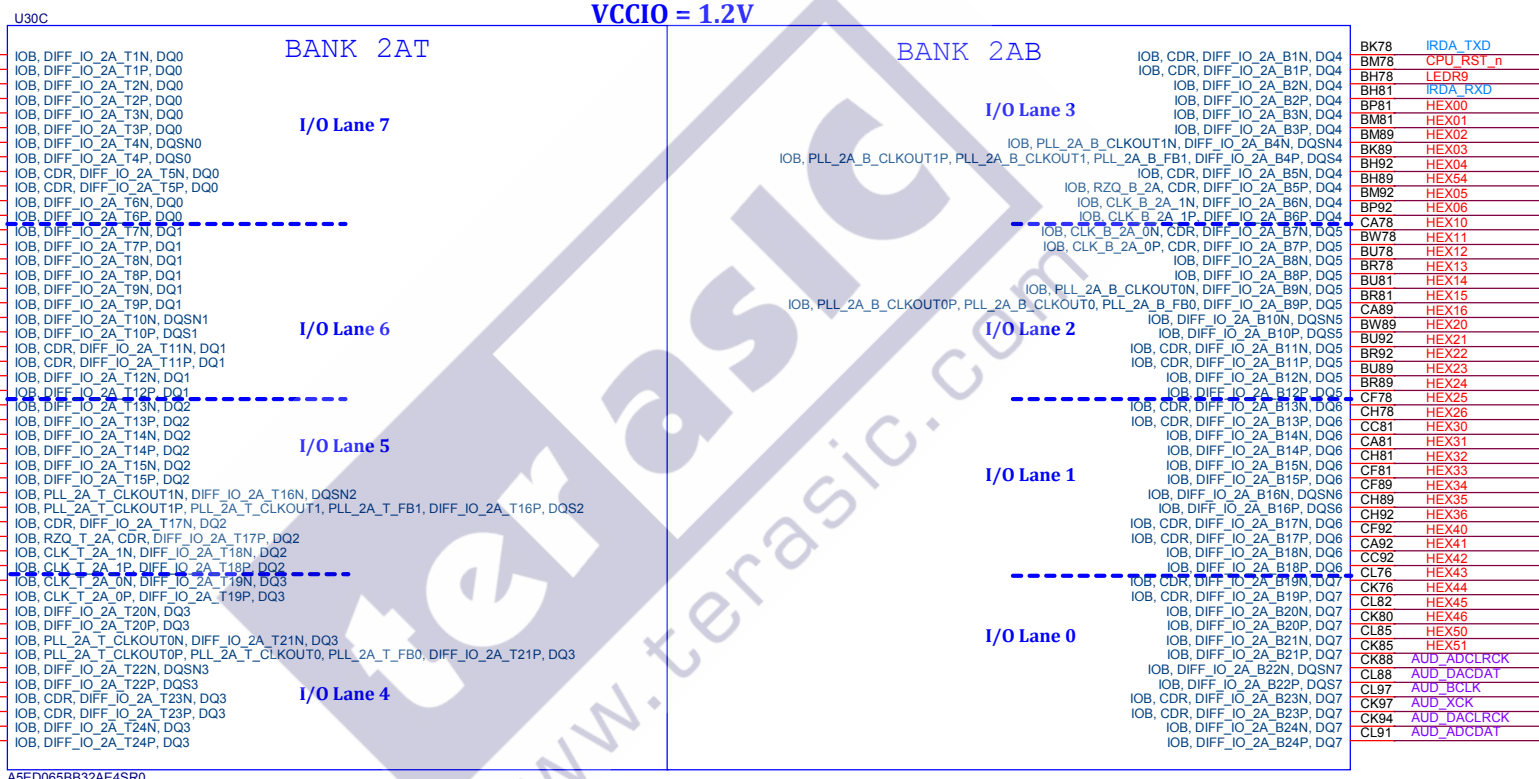
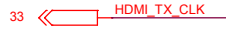
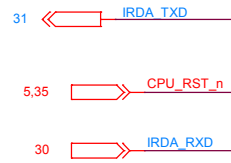
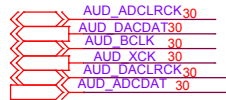
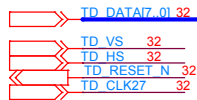


# Clock Tree

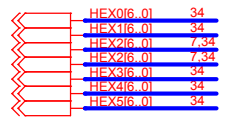
## 8-output Clock Generator

Si5332BD16012-GM2

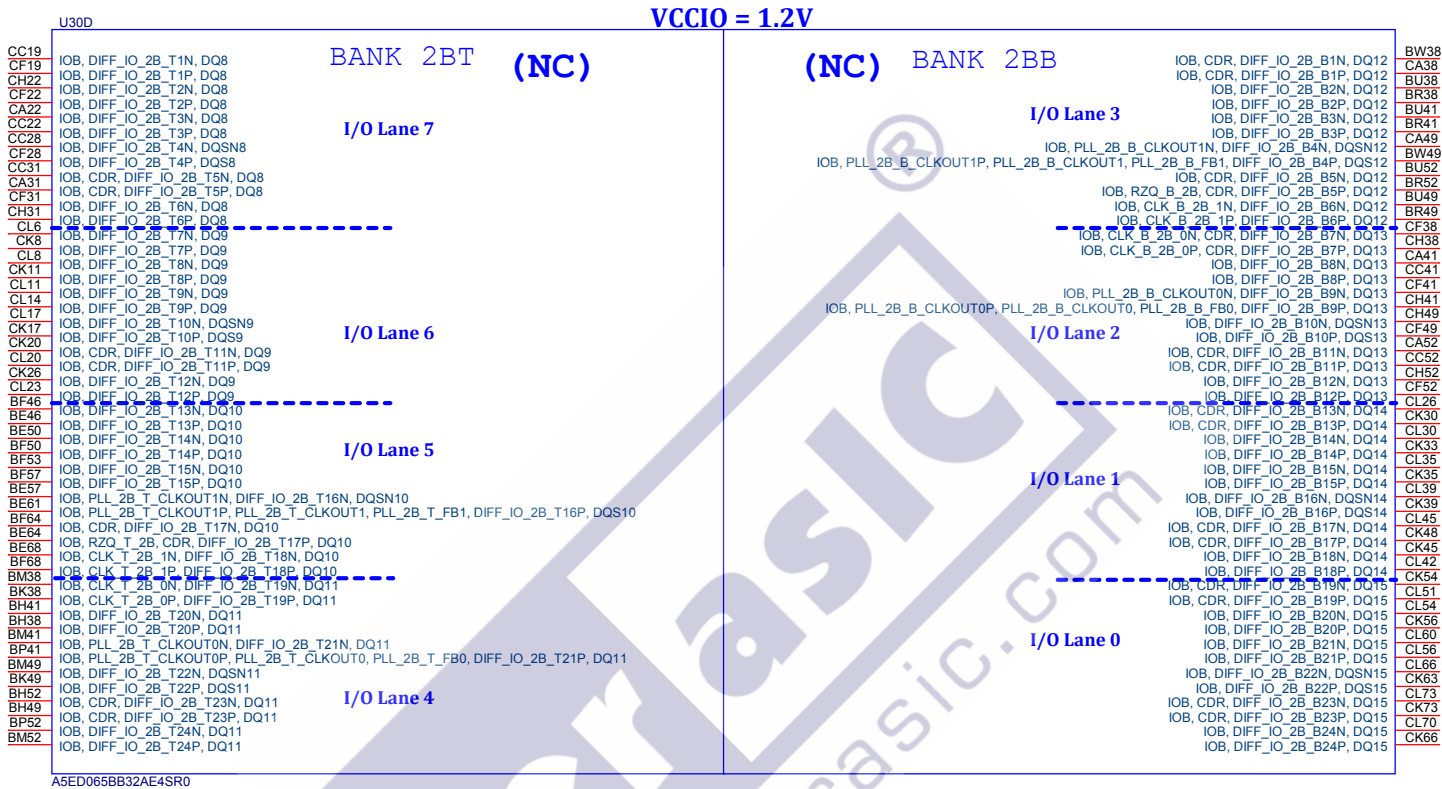




A5ED065BB32A4SR0



Title		
DE25-Standard Board		
Size B	Document Number	Rev A
	FPGA Bank 2A	
Date:	Friday, April 12, 2024	Sheet 7 of 49





DDR4 CK	25
DDR4 CK n	25
DDR4 BA[1..0]	25
DDR4 BG[1..0]	25
DDR4 OD1	25
DDR4 CS n	25
DDR4 DO[31..0]	25
DDR4 DOS[3..0]	25
DDR4 DQS n[3..0]	25
DDR4 A[16..0]	25
DDR4 DBI n[3..0]	25
DDR4 CKE	25
DDR4 RESET n	25

DDR4 PAR	25
DDR4 ACT <sub>n</sub>	25
DDR4 ALERT <sub>n</sub>	25

DDR4 REFCLK p	4
DDR4 REFCLK n	4

RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14

DDR4\_DQ25  
DDR4\_DQ29  
DDR4\_DQ31  
DDR4\_DQ27

DDR4\_DBI\_n3  
DDR4\_QQS\_n3  
DDR4\_QQS3  
DDR4\_DQ26  
DDR4\_DQ24  
DDR4\_DQ28  
DDR4\_DQ30  
DDR4\_DQ23  
DDR4\_DQ22  
DDR4\_DQ19  
DDR4\_DQ17

DDR4\_DBI\_n2  
DDR4\_QQS\_n2  
DDR4\_QQS2  
DDR4\_DQ16  
DDR4\_DQ18  
DDR4\_DQ20  
DDR4\_DQ21  
DDR4\_DQ15  
DDR4\_DQ13  
DDR4\_DQ11  
DDR4\_DQ9

DDR4\_DBI\_n1  
DDR4\_DQS\_n1  
DDR4\_DQS1  
DDR4\_DQ12  
DDR4\_DQ14  
DDR4\_DQ10  
DDR4\_DQ8

U30E

BANK 3AT

### I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

A5ED065BB32AE4SR0

**VCCIO = 1.2V**

BANK 3AB

I/O Lane 3

**I/O Lane 2**

**I/O Lane 1**

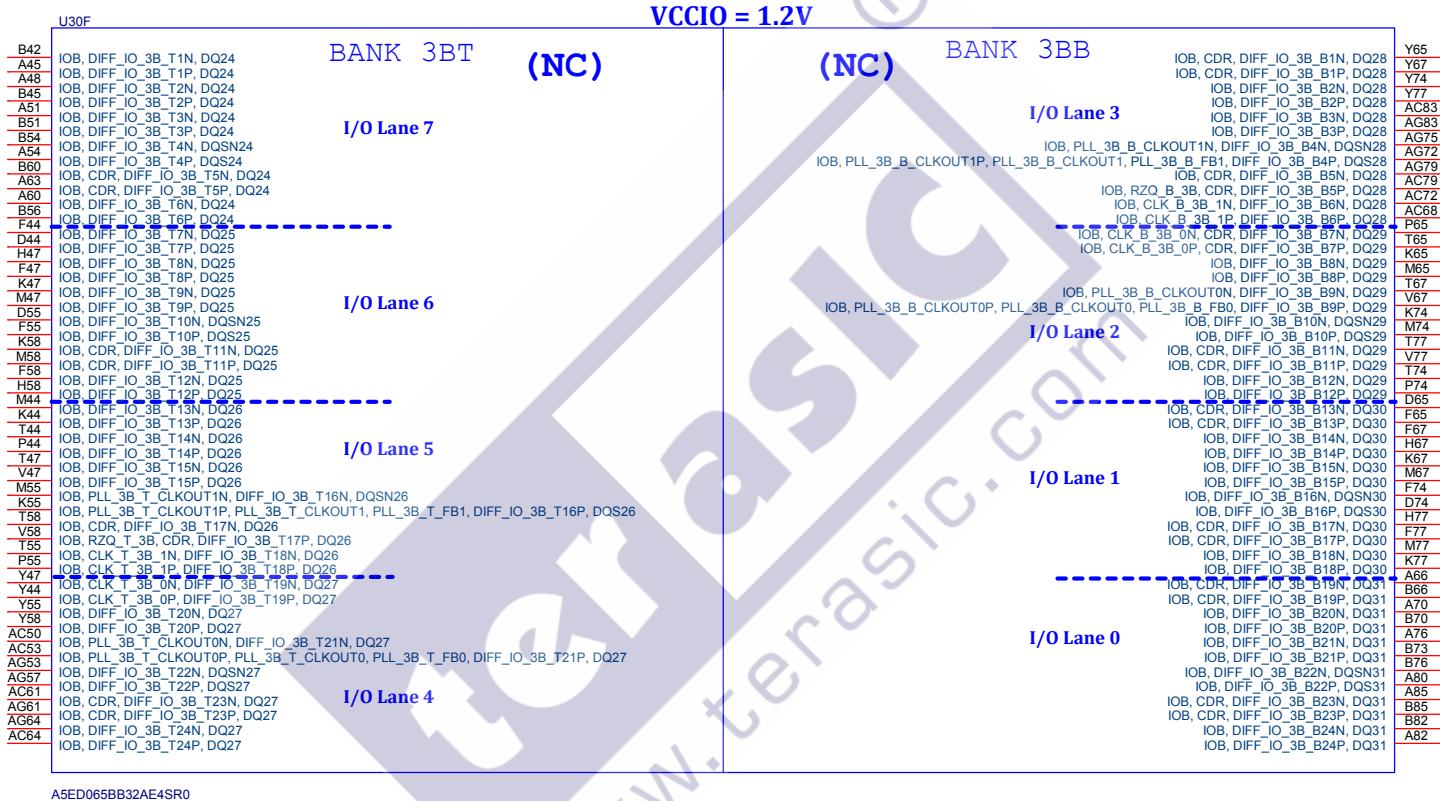
### I/O Lane 0

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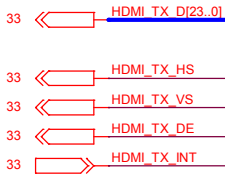
IOB, CDR, DIFF, IO_3A, B1N, DQ20
IOB, CDR, DIFF, IO_3A, B1P, DQ20
IOB, DIFF, IO_3A, B2N, DQ20
IOB, DIFF, IO_3A, B2P, DQ20
IOB, DIFF, IO_3A, B3N, DQ20
IOB, DIFF, IO_3A, B3P, DQ20
LKOUT1N, DIFF, IO_3A, B4N, DQS20
IOB, B_FBI, DIFF, IO_3A, B4P, DQS20
IOB, CDR, DIFF, IO_3A, B5N, DQ21
IOB, DIFF, IO_3A, B5P, DQ21
IOB, CDR, DIFF, IO_3A, B6N, DQ21
IOB, DIFF, IO_3A, B6P, DQ21
IOB, CDR, DIFF, IO_3A, B7N, DQ21
IOB, DIFF, IO_3A, B7P, DQ21
IOB, CDR, DIFF, IO_3A, B8N, DQ21
IOB, DIFF, IO_3A, B8P, DQ21
IOB, CDR, DIFF, IO_3A, B9N, DQ21
IOB, DIFF, IO_3A, B9P, DQ21
IOB, DIFF, IO_3A, B10N, DQS21
IOB, DIFF, IO_3A, B10P, DQS21
IOB, CDR, DIFF, IO_3A, B11N, DQ22
IOB, DIFF, IO_3A, B11P, DQ22
IOB, CDR, DIFF, IO_3A, B12N, DQ22
IOB, DIFF, IO_3A, B12P, DQ22
IOB, CDR, DIFF, IO_3A, B13N, DQ22
IOB, DIFF, IO_3A, B13P, DQ22
IOB, DIFF, IO_3A, B14N, DQ22
IOB, DIFF, IO_3A, B14P, DQ22
IOB, DIFF, IO_3A, B15N, DQ22
IOB, DIFF, IO_3A, B15P, DQ22
IOB, DIFF, IO_3A, B16N, DQS22
IOB, DIFF, IO_3A, B16P, DQS22
IOB, CDR, DIFF, IO_3A, B17N, DQ22
IOB, CDR, DIFF, IO_3A, B17P, DQ22
IOB, DIFF, IO_3A, B18N, DQ22
IOB, DIFF, IO_3A, B18P, DQ22
IOB, CDR, DIFF, IO_3A, B19N, DQ23
IOB, CDR, DIFF, IO_3A, B19P, DQ23
IOB, DIFF, IO_3A, B20N, DQ23
IOB, DIFF, IO_3A, B20P, DQ23
IOB, DIFF, IO_3A, B21N, DQ23
IOB, DIFF, IO_3A, B21P, DQ23
IOB, CDR, DIFF, IO_3A, B22N, DQS23
IOB, DIFF, IO_3A, B22P, DQS23
IOB, CDR, DIFF, IO_3A, B23N, DQ23
IOB, CDR, DIFF, IO_3A, B23P, DQ23
IOB, DIFF, IO_3A, B24N, DQ23
IOB, DIFF, IO_3A, B24P, DQ23

```

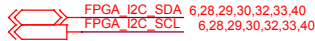
AB105	DDR4 B60
Y105	DDR4 BA1
AB108	DDR4 BA0
Y108	DDR4 ALERT_n
AK104	DDR4 A15
AK107	DDR4 A16
AB114	DDR4 A14
Y114	DDR4 A13
AK117	DDR4 A12
AK111	KZ0 B 3A R418
AB117	DDR4 REFCLK_p
K105	DDR4 A11
M105	DDR4 A10
P105	DDR4 A9
T105	DDR4 A8
T108	DDR4 A7
V108	DDR4 A6
K114	DDR4 A5
M114	DDR4 A4
P117	DDR4 A3
V117	DDR4 A2
P114	DDR4 A1
T114	DDR4 A0
K108	DDR4 PAR
M108	
F108	DDR4 CK_n
H108	DDR4 CK
D105	
F105	DDR4_CKE
D114	
F114	DDR4 ODT
M117	DDR4 ACT_n
K117	DDR4 CS_n
H117	DDR4 RESET_n
F117	DDR4 BG1
A113	DDR4 D07
B113	DDR4 D05
A116	DDR4 D01
B116	DDR4 D03
A122	
B119	DDR4 DBI_n0
A125	DDR4 D0S0
B122	DDR4 D0S2
A130	DDR4 D06
B130	DDR4 D04
A128	DDR4 D02
B128	DDR4 D00



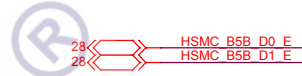
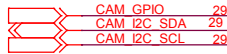
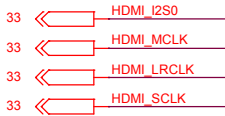
HDMI TX



FPGA I2C Interface



HDMI Audio Interface



VCCIO = 3.3V

HDMI\_TX\_D0 CD134

HDMI\_TX\_D1 CD135

HDMI\_TX\_D2 CG134

HDMI\_TX\_D3 CG135

HDMI\_TX\_D4 CH132

HDMI\_TX\_D5 CF132

HDMI\_TX\_D6 CF128

HDMI\_TX\_D7 CK134

CLOCK\_50 CH128

HDMI\_TX\_D8 CL125

HDMI\_TX\_D9 CF121

HDMI\_TX\_D10 BU118

HDMI\_TX\_D11 BR118

HDMI\_TX\_D12 CA118

HDMI\_TX\_D13 BW118

HDMI\_TX\_D15 CL128

HDMI\_TX\_D16 CL130

HDMI\_TX\_D17 CK125

HDMI\_TX\_D18 CK128

U30G

HVIO\_5A\_1, SYSPLLREFCLK\_L1A\_0, TXCLK1, DATA\_CTRL1

HVIO\_5A\_2, SYSPLLREFCLK\_L1A\_1, TXCLK2, DATA\_CTRL2

HVIO\_5A\_3, SYSPLLREFCLK\_L1B\_0, TXCLK3, DATA\_CTRL3

HVIO\_5A\_4, SYSPLLREFCLK\_L1B\_1, TXCLK4, DATA\_CTRL4

HVIO\_5A\_5, PIN\_PERST\_N\_CVP\_L1A\_0, TXCLK5, DATA\_CTRL5

HVIO\_5A\_6, PIN\_PERST\_N\_CVP\_L1B\_0, TXCLK6, DATA\_CTRL6

HVIO\_5A\_7, PIN\_PERST\_N\_CVP\_L1C\_0, TXCLK7, DATA\_CTRL7

HVIO\_5A\_8, TXCLK8, DATA\_CTRL8

HVIO\_5A\_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA\_CTRL9

HVIO\_5A\_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA\_CTRL10

HVIO\_5A\_11, SOURCE\_SYNC\_CLK1, TXCLK11, RXCLK3, DATA\_CTRL11

HVIO\_5A\_12, SOURCE\_SYNC\_CLK2, TXCLK12, RXCLK4, DATA\_CTRL12

HVIO\_5A\_13, TXCLK13, DATA\_CTRL13

HVIO\_5A\_14, TXCLK14, DATA\_CTRL14

HVIO\_5A\_15, TXCLK15, DATA\_CTRL15

HVIO\_5A\_16, TXCLK16, DATA\_CTRL16

HVIO\_5A\_17, TXCLK17, DATA\_CTRL17

HVIO\_5A\_18, TXCLK18, DATA\_CTRL18

HVIO\_5A\_19, SYSPLLREFCLK\_L1C\_0, TXCLK19, DATA\_CTRL19

HVIO\_5A\_20, TXCLK20, DATA\_CTRL20

BANK 5A

BANK 5B

HVIO\_5B\_1, SYSPLLREFCLK\_L1A\_2, TXCLK1, DATA\_CTRL1

HVIO\_5B\_2, SYSPLLREFCLK\_L1A\_3, TXCLK2, DATA\_CTRL2

HVIO\_5B\_3, SYSPLLREFCLK\_L1B\_2, TXCLK3, DATA\_CTRL3

HVIO\_5B\_4, SYSPLLREFCLK\_L1B\_3, TXCLK4, DATA\_CTRL4

HVIO\_5B\_5, PIN\_PERST\_N\_CVP\_L1A\_1, TXCLK5, DATA\_CTRL5

HVIO\_5B\_6, PIN\_PERST\_N\_CVP\_L1B\_1, TXCLK6, DATA\_CTRL6

HVIO\_5B\_7, PIN\_PERST\_N\_CVP\_L1C\_1, TXCLK7, DATA\_CTRL7

HVIO\_5B\_8, TXCLK8, DATA\_CTRL8

HVIO\_5B\_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA\_CTRL9

HVIO\_5B\_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA\_CTRL10

HVIO\_5B\_11, SOURCE\_SYNC\_CLK1, TXCLK11, RXCLK3, DATA\_CTRL11

HVIO\_5B\_12, SOURCE\_SYNC\_CLK2, TXCLK12, RXCLK4, DATA\_CTRL12

HVIO\_5B\_13, TXCLK13, DATA\_CTRL13

HVIO\_5B\_14, TXCLK14, DATA\_CTRL14

HVIO\_5B\_15, TXCLK15, DATA\_CTRL15

HVIO\_5B\_16, TXCLK16, DATA\_CTRL16

HVIO\_5B\_17, TXCLK17, DATA\_CTRL17

HVIO\_5B\_18, TXCLK18, DATA\_CTRL18

HVIO\_5B\_19, SYSPLLREFCLK\_L1C\_1, TXCLK19, DATA\_CTRL19

HVIO\_5B\_20, TXCLK20, DATA\_CTRL20

BF111 HDMI\_TX\_D19

BH109 HDMI\_TX\_D20

BE115 HDMI\_TX\_D21

BF115 HDMI\_TX\_D22

BF107 HSMC\_B5B\_D0\_E (Reset input in PCIE)

BU109 HDMI\_TX\_D23

BF104 HSMC\_B5B\_D1\_E

BR109 HDMI\_TX\_HS

BE107 HDMI\_TX\_VS

BK109 HDMI\_TX\_DE

BE111 HDMI\_TX\_INT

BM109 FPGA\_I2C\_SDA

BR112 FPGA\_I2C\_SCL

BK113 HDMI\_I2S0

BM118 HDMI\_MCLK

BP112 HDMI\_LRCLK


BM112 HDMI\_SCLK

BK112 CAM\_GPIO

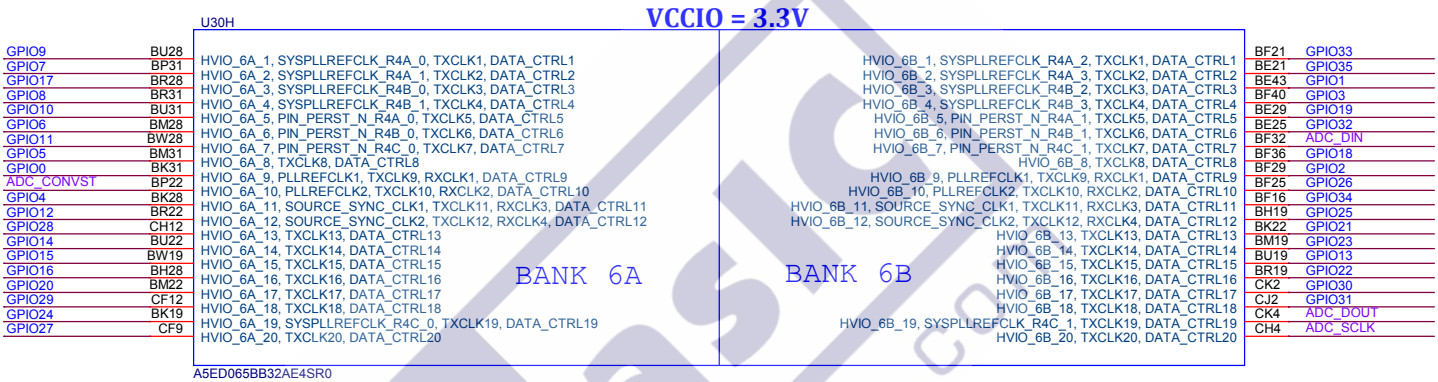
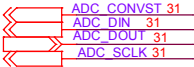
BH118 CAM\_I2C\_SDA

BF120 CAM\_I2C\_SCL

A5ED065BB32AE4SR0

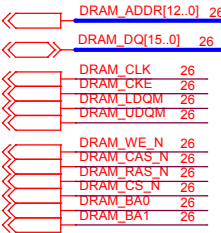
 Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title <b>DE25-Standard Board</b>		
Size B	Document Number FPGA Bank 5A - 5B	Rev A
Date:	Wednesday, April 10, 2024	Sheet 11 of 49

GPIO





SDRAM



U30I

VCCIO = 1.8V

DRAM_ADDR0	F27
DRAM_ADDR1	F24
DRAM_ADDR2	H27
DRAM_ADDR3	D24
DRAM_ADDR4	H18
DRAM_ADDR5	D16
DRAM_ADDR6	F18
DRAM_ADDR7	F15
CLOCK2_50	D8
DRAM_ADDR8	K8
DRAM_ADDR9	F8
DRAM_CS_N	H8
DRAM_ADDR10	C2
DRAM_ADDR12	D4
DRAM_BA1	F4
DRAM_LDQM	K4
DRAM_UDQM	G2
DRAM_WE_N	J2
DRAM_CAS_N	J1
DRAM_RAS_N	G1

HVIO_6C_1, TXCLK1, DATA_CTRL1
HVIO_6C_2, TXCLK2, DATA_CTRL2
HVIO_6C_3, TXCLK3, DATA_CTRL3
HVIO_6C_4, TXCLK4, DATA_CTRL4
HVIO_6C_5, TXCLK5, DATA_CTRL5
HVIO_6C_6, TXCLK6, DATA_CTRL6
HVIO_6C_7, TXCLK7, DATA_CTRL7
HVIO_6C_8, TXCLK8, DATA_CTRL8
HVIO_6C_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6C_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6C_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6C_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6C_13, TXCLK13, DATA_CTRL13
HVIO_6C_14, TXCLK14, DATA_CTRL14
HVIO_6C_15, TXCLK15, DATA_CTRL15
HVIO_6C_16, TXCLK16, DATA_CTRL16
HVIO_6C_17, TXCLK17, DATA_CTRL17
HVIO_6C_18, TXCLK18, DATA_CTRL18
HVIO_6C_19, TXCLK19, DATA_CTRL19
HVIO_6C_20, TXCLK20, DATA_CTRL20

BANK 6C

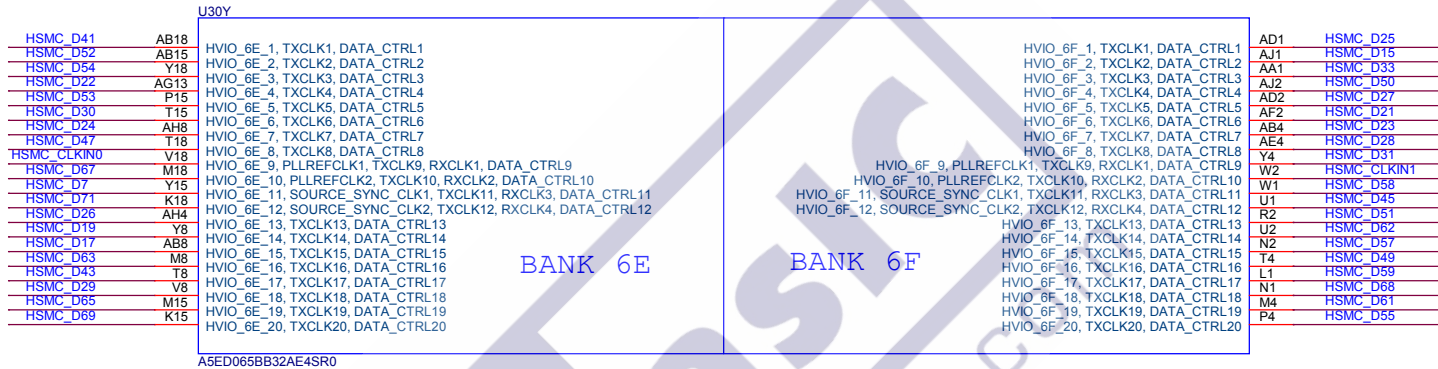
BANK 6D

HVIO_6D_1, TXCLK1, DATA_CTRL1
HVIO_6D_2, TXCLK2, DATA_CTRL2
HVIO_6D_3, TXCLK3, DATA_CTRL3
HVIO_6D_4, TXCLK4, DATA_CTRL4
HVIO_6D_5, TXCLK5, DATA_CTRL5
HVIO_6D_6, TXCLK6, DATA_CTRL6
HVIO_6D_7, TXCLK7, DATA_CTRL7
HVIO_6D_8, TXCLK8, DATA_CTRL8
HVIO_6D_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6D_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6D_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6D_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6D_13, TXCLK13, DATA_CTRL13
HVIO_6D_14, TXCLK14, DATA_CTRL14
HVIO_6D_15, TXCLK15, DATA_CTRL15
HVIO_6D_16, TXCLK16, DATA_CTRL16
HVIO_6D_17, TXCLK17, DATA_CTRL17
HVIO_6D_18, TXCLK18, DATA_CTRL18
HVIO_6D_19, TXCLK19, DATA_CTRL19
HVIO_6D_20, TXCLK20, DATA_CTRL20

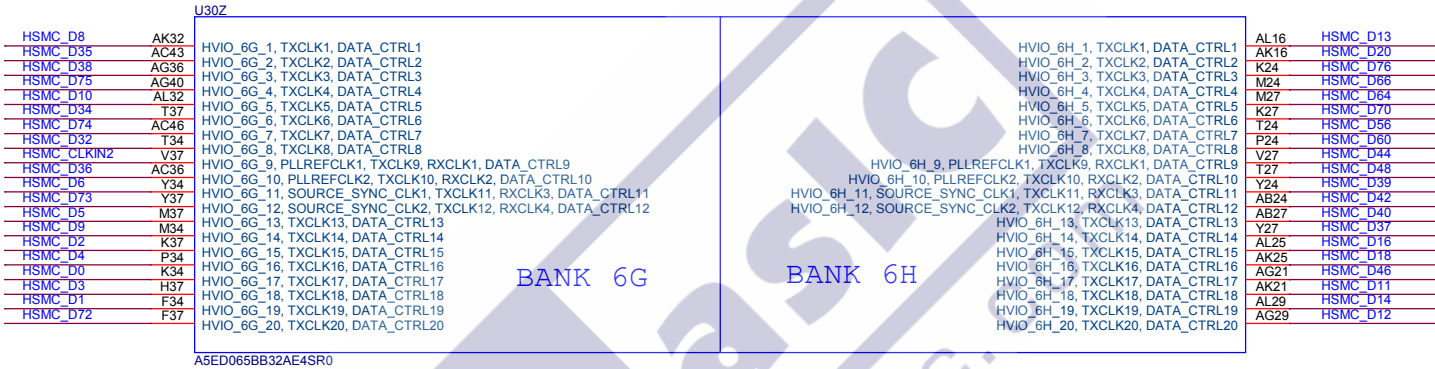
A8	DRAM_DQ5
B4	DRAM_DQ7
A11	DRAM_DQ1
B11	DRAM_DQ3
B14	DRAM_DQ2
A14	DRAM_DQ0
A20	DRAM_DQ4
A17	DRAM_ADDR11
A23	DRAM_DQ6
B20	DRAM_DQ8
B23	DRAM_DQ9
B26	DRAM_DQ10
B30	DRAM_DQ11
A30	DRAM_DQ13
A35	DRAM_DQ14
A33	DRAM_DQ15
A39	DRAM_DQ12
B35	DRAM_CKE
D34	DRAM_BA0
B39	DRAM_CLK

A5ED065BB32AE4SR0

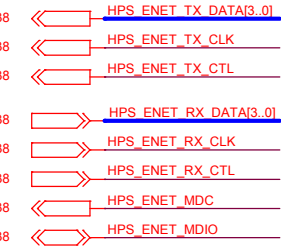
15,28 << HSMC\_D[76..0]  
15,28 << HSMC\_CLKIN[2..0]



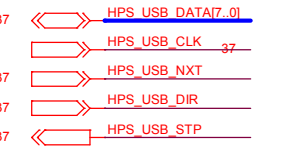
14,28 << HSMC\_D[76..0]  
14,28 << HSMC\_CLKIN[2..0]



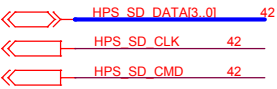
Ethernet PHY Interface (RGMII)



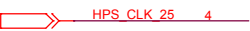
UBS PHY Interface (ULPI)



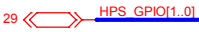
SD Card



HPS 25MHz Clock



HPS GPIO



HPS I2C Interface



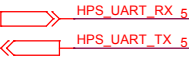
HPS User Button



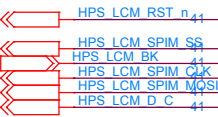
HPS User LED



UART Interface



HPS LCD



HPS_USB_CLK	W135
HPS_USB_STP	U135
HPS_USB_DIR	W134
HPS_USB_DATA0	AK115
HPS_USB_DATA1	U134
HPS_USB_NXT	AL120
HPS_USB_DATA2	R134
HPS_USB_DATA3	AG115
HPS_USB_DATA4	N135
HPS_USB_DATA5	AK120
HPS_USB_DATA6	N134
HPS_USB_DATA7	T132
HPS_ENET_TX_CTL	P132
HPS_ENET_TX_CLK	L135
HPS_ENET_RX_CLK	J135
HPS_ENET_RX_CTL	AD135
HPS_ENET_TX_DATA0	M132
HPS_ENET_TX_DATA1	AD134
HPS_ENET_RX_DATA0	K132
HPS_ENET_RX_DATA1	AG129
HPS_ENET_TX_DATA2	J134
HPS_ENET_TX_DATA3	AG120
HPS_ENET_RX_DATA2	G134
HPS_ENET_RX_DATA3	G135

HPS_SD_DATA0	E135
HPS_SD_DATA1	F132
HPS_SD_CLK	D132
HPS_CLK_25	AG123
HPS_GSENSOR_INT	B134
HPS_SD_DATA2	AA135
HPS_SD_DATA3	V127
HPS_SD_CMD	AB132
HPS_GPIO0	T127
HPS_GPIO1	Y132
HPS_LCM_RST_n	T124
HPS_LCM_D_C	P124
HPS_I2C_SDA	M127
HPS_I2C_SCL	K127
HPS_UART_TX	M124
HPS_UART_RX	AB127
HPS_KEY	K124
HPS_LED	Y127
HPS_LCM_BK	H127
HPS_LCM_SPIM_SS	AB124
HPS_LCM_SPIM_CLK	F127
HPS_LCM_SPIM_MOSI	Y124
HPS_ENET_MDIO	F124
HPS_ENET_MDC	D124

U30B

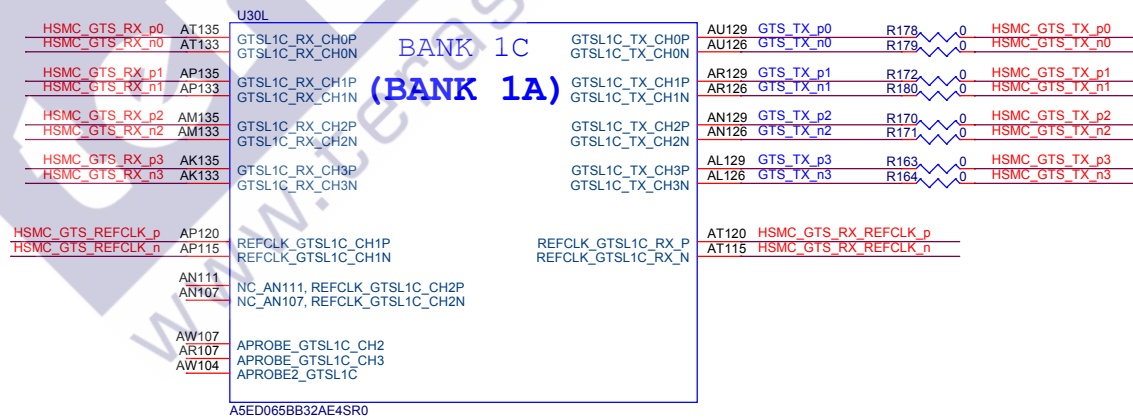
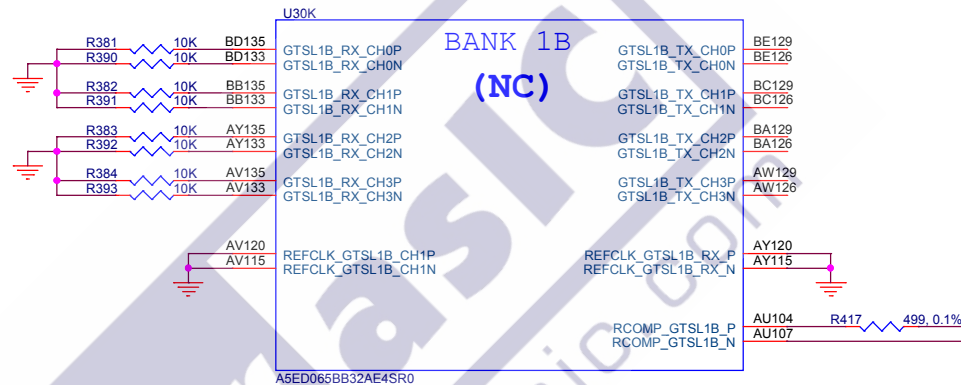
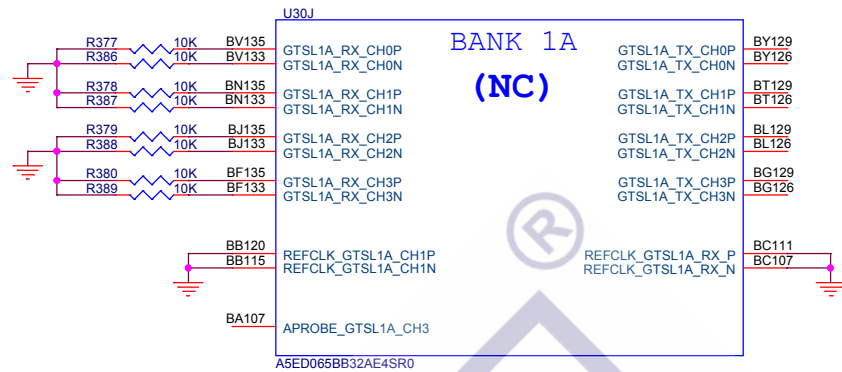
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HPS\_IOA\_2, GPIO0\_IO1, SPIM1\_SS1\_N, SPIS0\_MOSI, UART0\_RTS\_N, NAND\_ADQ1, SDMMC\_DATA1, USB0\_STP, EMAC0\_PPSTRIG0, TRACE\_D9  
HPS\_IOA\_3, GPIO0\_IO2, SPIS0\_SS0\_N, UART0\_TX, I2C1\_SDA, NAND\_WE\_N, SDMMC\_CLK, USB0\_DIR, EMAC1\_PPS1, TRACE\_D8  
HPS\_IOA\_4, GPIO0\_IO3, SPIS0\_MISO, UART0\_RX, I2C1\_SCL, NAND\_RE\_N, USB0\_DATA0, EMAC1\_PPSTRIG1, TRACE\_D7  
HPS\_IOA\_5, GPIO0\_IO4, SPIM0\_CLK, UART1\_CTS\_N, I2C0\_SDA, NAND\_WP\_N, SDMMC\_WRITE\_PROTECT, USB0\_DATA1, EMAC2\_PPS2, TRACE\_D6  
HPS\_IOA\_6, GPIO0\_IO5, SPIM0\_MOSI, UART1\_RTS\_N, I2C0\_SCL, NAND\_ADQ2, SDMMC\_DATA2, USB0\_NXT, EMAC2\_PPSTRIG2, TRACE\_D5  
HPS\_IOA\_7, GPIO0\_IO6, SPIM0\_MISO, MDIO2\_MDIO, UART1\_TX, I2C\_EMAC2\_SDA, NAND\_ADQ3, SDMMC\_DATA3, USB0\_DATA2, TRACE\_D4  
HPS\_IOA\_8, GPIO0\_IO7, SPIM0\_SS0\_N, MDIO2\_MDC, UART1\_RX, I2C\_EMAC2\_SCL, NAND\_CLE, SDMMC\_CMD, USB0\_DATA3, TRACE\_D15  
HPS\_IOA\_9, GPIO0\_IO8, SPIM1\_CLK, SPIS1\_CLK, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ4, SDMMC\_DATA4, USB0\_DATA4, I3C1\_SDA, TRACE\_D14  
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HPS\_IOA\_13, GPIO0\_IO12, NAND\_ALE, SDMMC\_PU\_PD\_DATA2, USB1\_CLK, EMAC0\_TX\_CLK, TRACE\_D10  
HPS\_IOA\_14, GPIO0\_IO13, NAND\_RB\_N, SDMMC\_BUS\_PWR, USB1\_STP, EMAC0\_TX\_CTL, TRACE\_D9  
HPS\_IOA\_15, GPIO0\_IO14, NAND\_CE\_N, USB1\_DIR, EMAC0\_RX\_CLK, TRACE\_D8  
HPS\_IOA\_16, GPIO0\_IO15, NAND\_DQS, SDMMC\_DATA\_STROBE, USB1\_DATA0, EMAC0\_RX\_CTL, TRACE\_D7  
HPS\_IOA\_17, GPIO0\_IO16, I3C1\_SDA, NAND\_ADQ8, USB1\_NXT, EMAC0\_TXD0, TRACE\_D6  
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HPS\_IOB\_20, GPIO1\_IO19, SPIM0\_SS0\_N, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ11, EMAC2\_RXD1, TRACE\_CLK  
HPS\_IOB\_21, GPIO1\_IO20, SPIM0\_CLK, SPIS1\_CLK, I2C\_EMAC2\_SDA, NAND\_ADQ12, EMAC2\_TXD2, TRACE\_D0  
HPS\_IOB\_22, GPIO1\_IO21, SPIM0\_MOSI, SPIS1\_MOSI, I2C\_EMAC2\_SCL, NAND\_ADQ13, EMAC2\_TXD3, TRACE\_D1  
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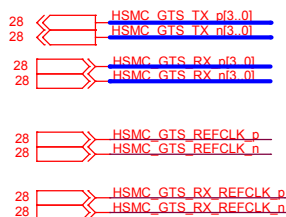
HPS


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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	FPGA Bank HPS	A
Date:	Thursday, April 11, 2024	Sheet 16 of 49

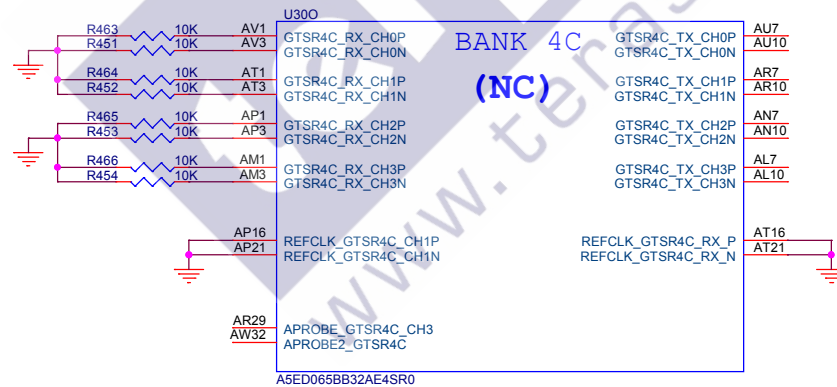
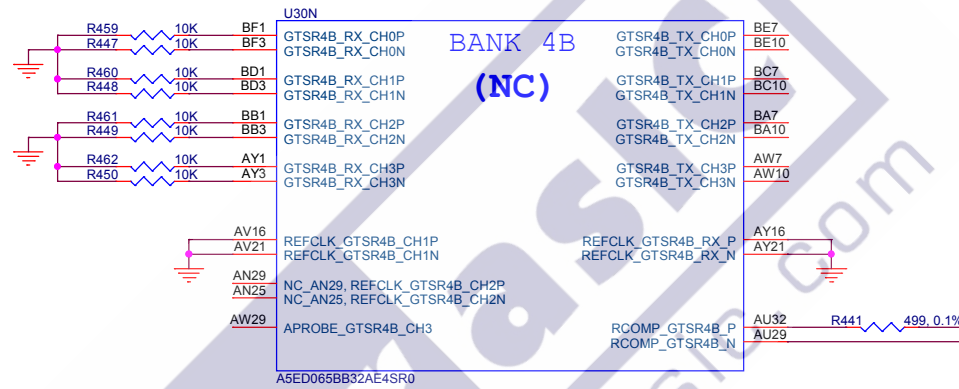
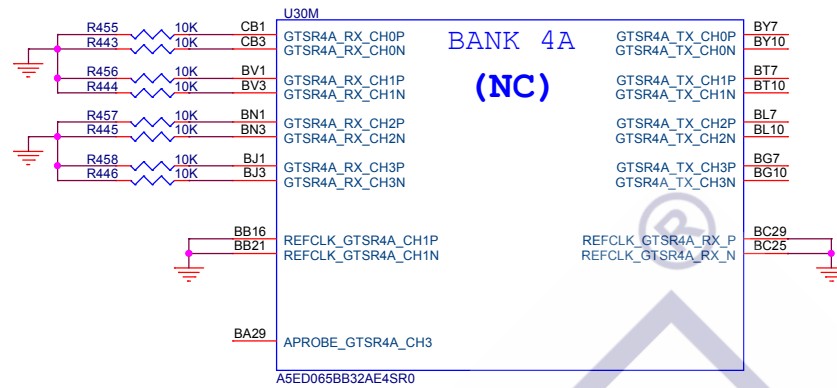



### HSMC Transceivers

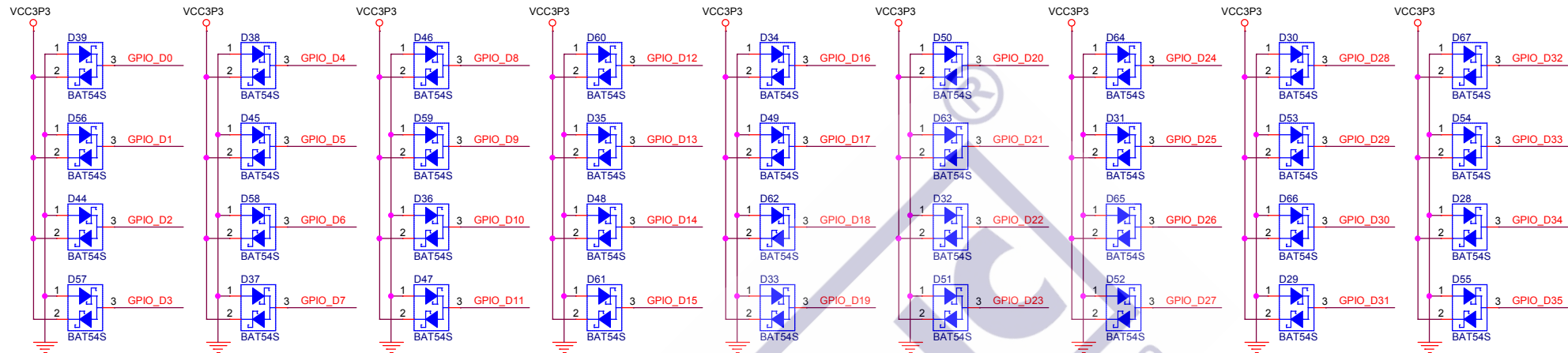


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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	FPGA XCVR Bank 1A (NC) · 1B (NC) · 1C	A
Date:	Wednesday, April 10, 2024	Sheet 17 of 49

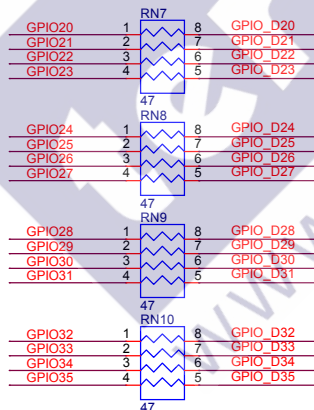
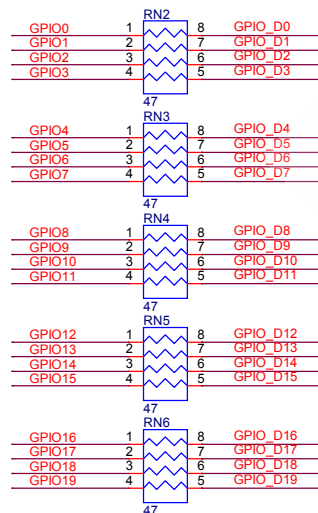




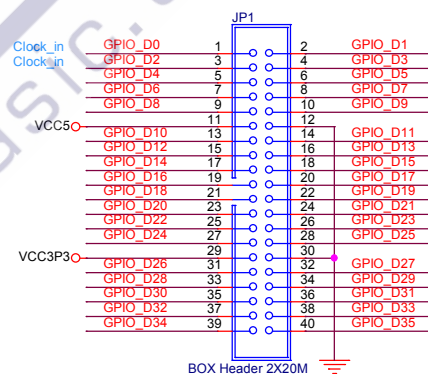
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Title			
DE25-Standard Board			
Size	Document Number		Rev
B	FPGA XCVR Bank 4A · 4B · 4C		A
Date:	Wednesday, April 10, 2024	Sheet	18 of 49

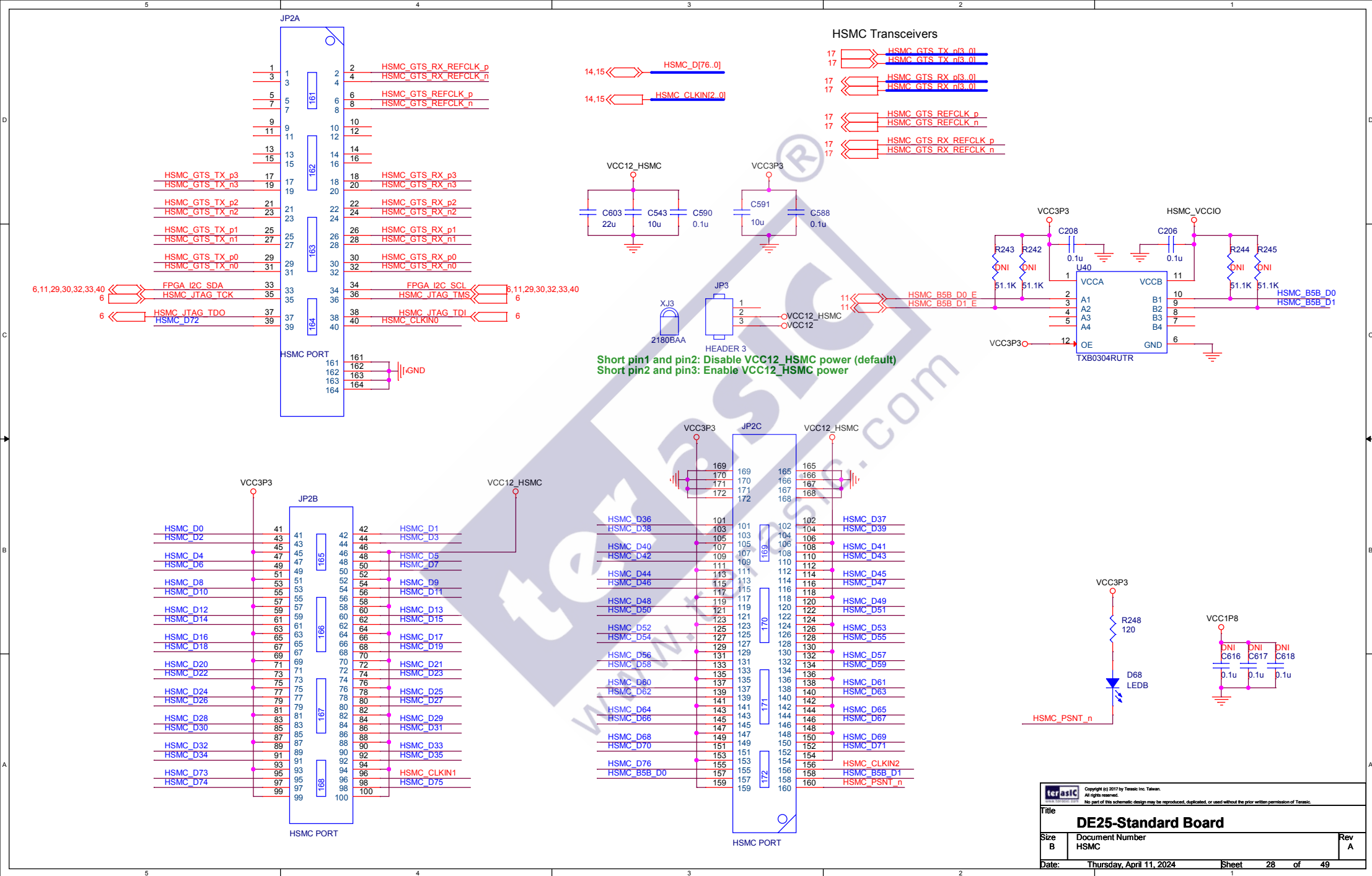


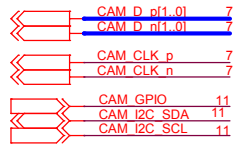
## GPIO



## DE-GPIO



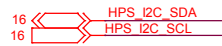




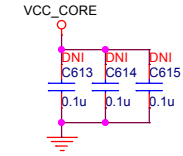
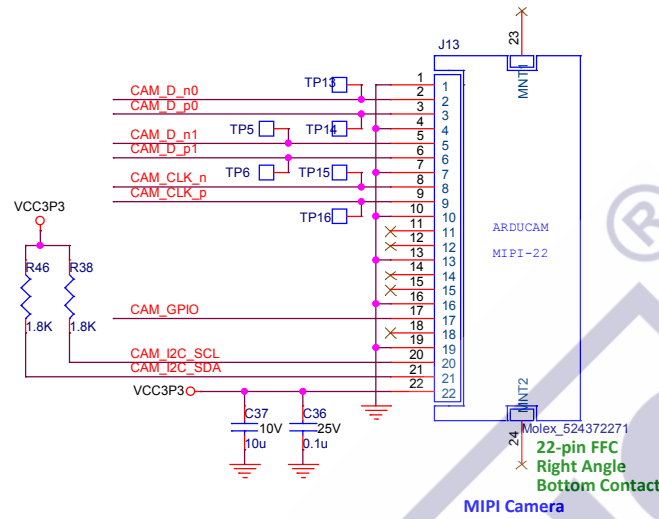
### FPGA I2C Interface



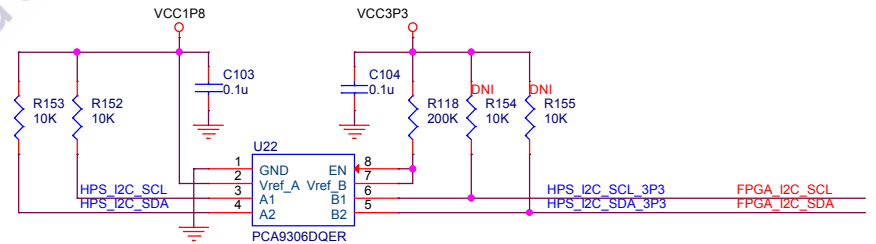
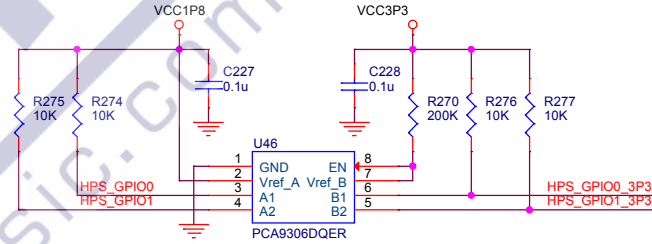
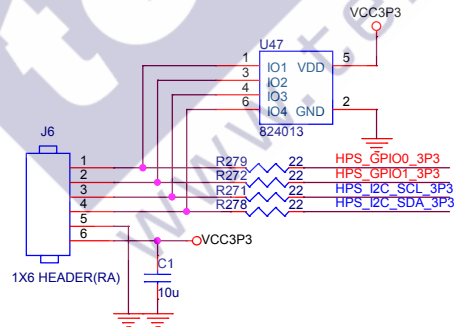
### HPS I2C Interface



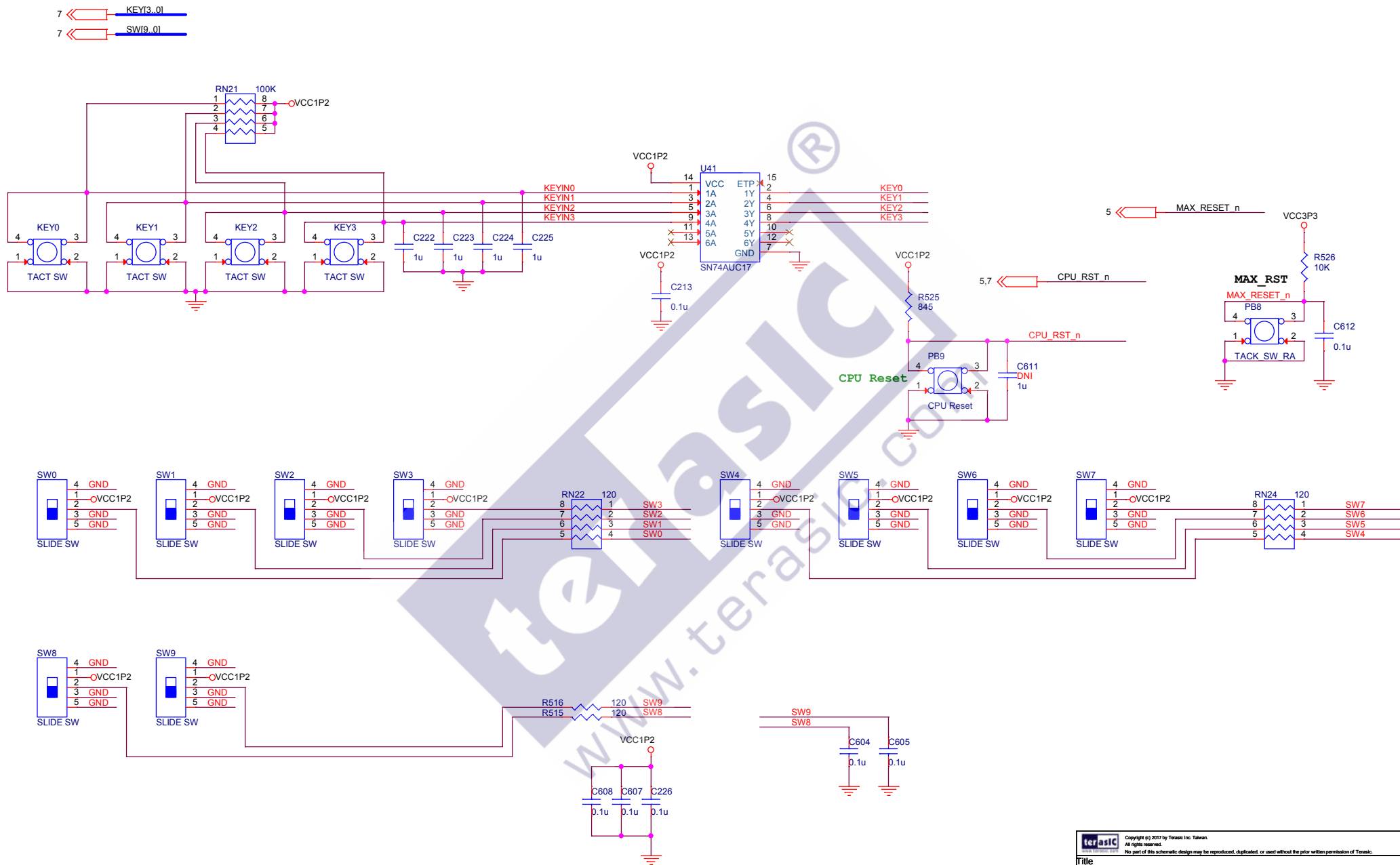
### HPS GPIO



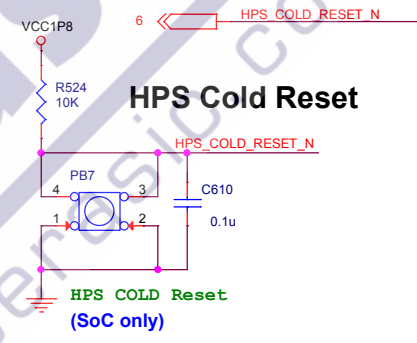
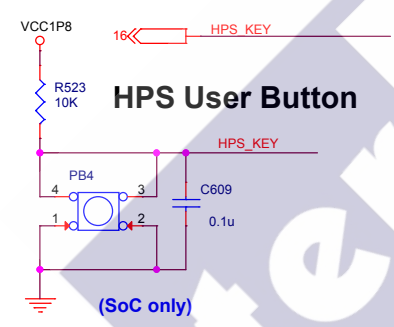
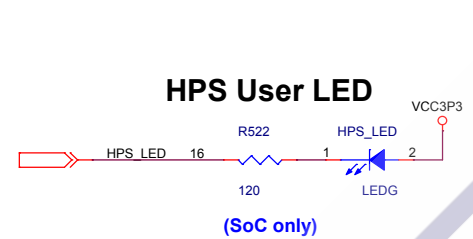
### HPS 1x6 GPIO Header




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Title		
DE25-Standard Board		
Size	Document Number	Rev
B	MIPI Connectors, HPS 2x3 GPIO	A
Date:	Thursday, April 11, 2024	Sheet 29 of 49







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Title					
DE25-Standard Board					
Size	Document Number		Rev		
B	HPS BUTTON, HPS LED		A		
Date:	Wednesday, April 10, 2024	Sheet	36 of 49		