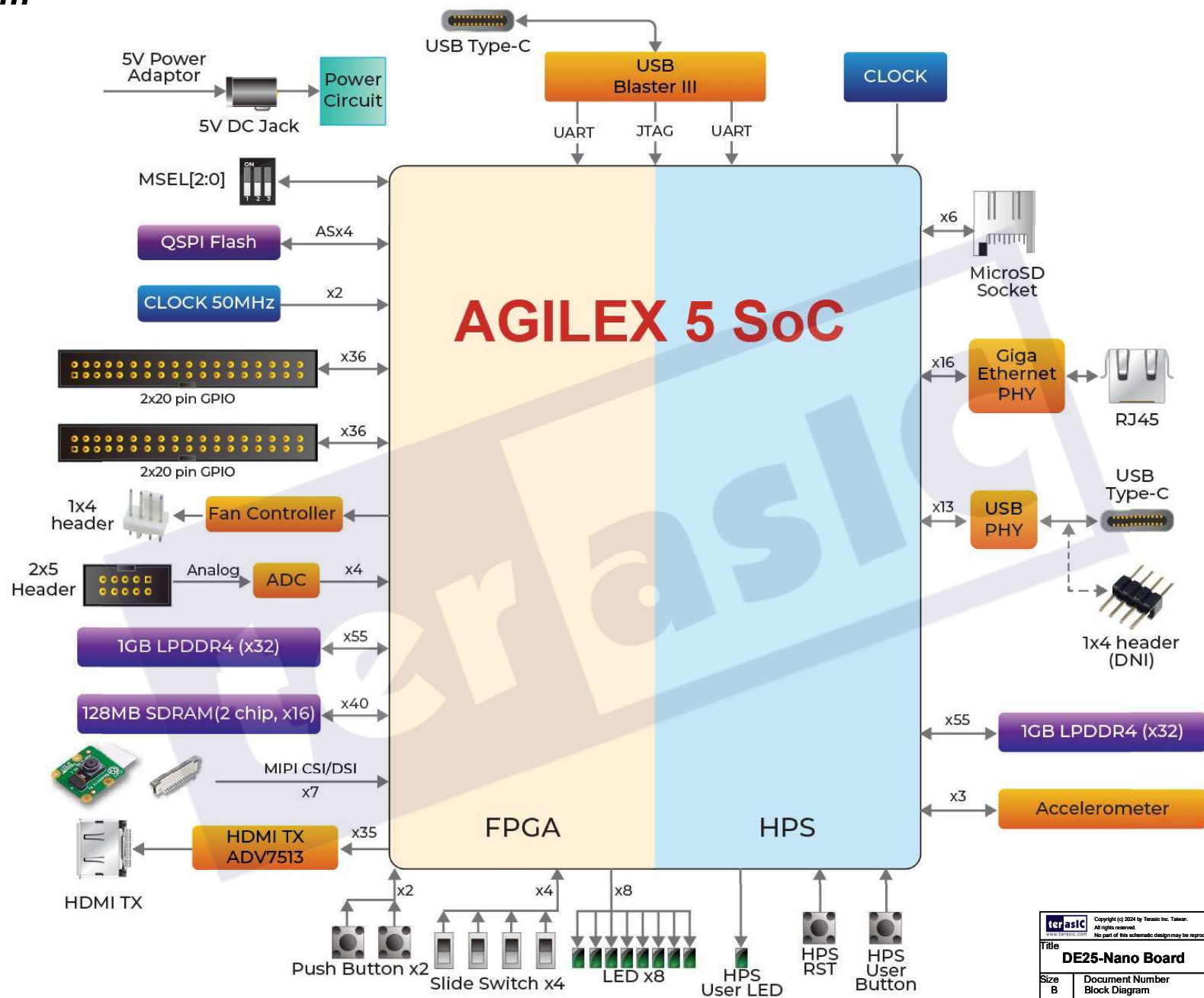


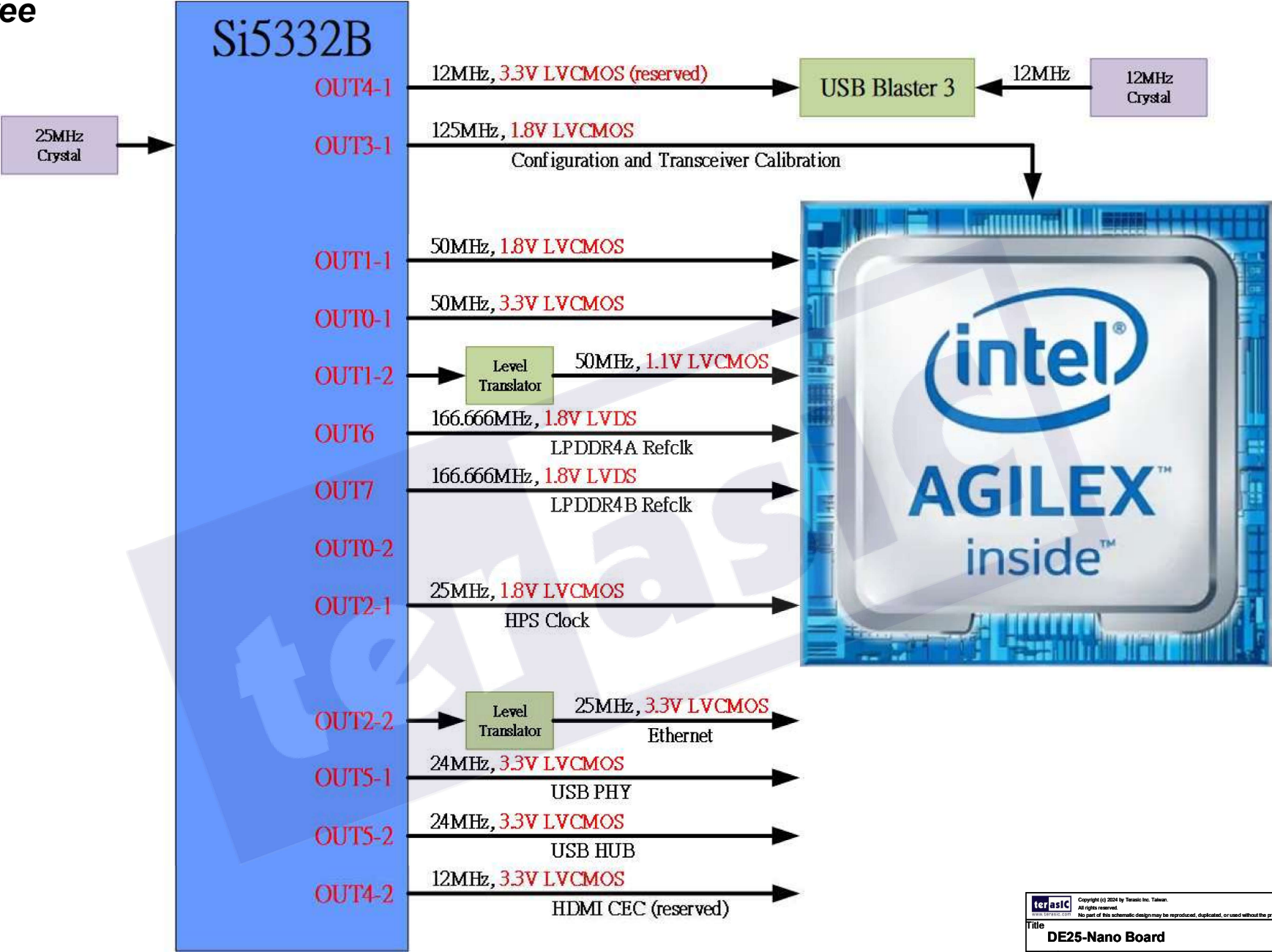
DE25-Nano

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5	USB Blaster	34	Power - 1.1V, 1.2V, 1.8V and VCCIO
6	FPGA Bank 2A (HSIO)	35	USB Hub, USB to Dual UART
7	FPGA Bank 3A (HSIO)		
8	FPGA Bank 6A6B (HVIO)		
9	FPGA Bank 6C6D (HVIO)		
10	FPGA Bank 6E6F (HVIO)		
11	FPGA Bank 6G6H (HVIO)		
12	FPGA Bank HPS		
13	FPGA Configuration		
14	FPGA Power		
15	FPGA GND & DNU & NC		
16	FPGA Decoupling 1		
17	FPGA Decoupling 2		
18	FPGA : LPDDR4-B		
19	FPGA : SDRAM, QSPI Flash		
20	FPGA : ADC - TLA2518		
21	FPGA : HDMI TX		
22	FPGA : GPIO x2, MIPI		
23	FPGA : Button, Switch, LEDs		
24	HPS : LPDDR4-A		
25	HPS : GigaBit Ethernet		
26	HPS : USB PHY		
27	HPS : Accelerometer		
28	HPS : SD Card		
29	HPS : Button, LED		

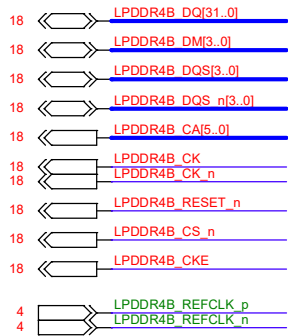
# Block Diagram



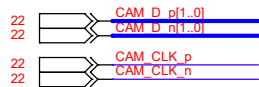
Clock Tree



## LPDDR4 B Interface (FPGA)



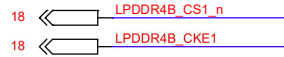
## Camera MIPI Interface



## Clock



## HDMI TX Interface



## SWITCH



## LED



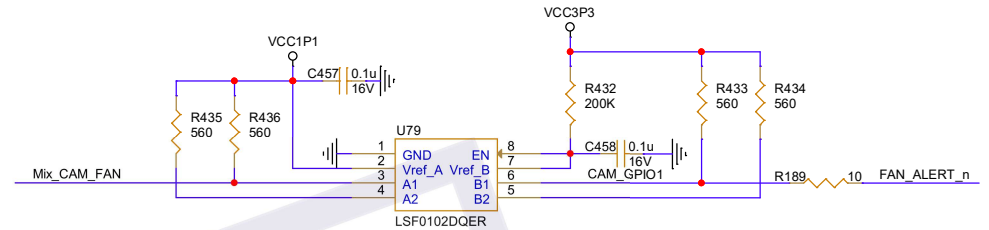
## Camera Control Interface



## FAN Interrupter



# HSIO Banks 2AT and 2AB



VCCIO = 1.1V

## BANK 2AT

LPDDR4B_DQ30	DJ9	IO_2A_T/IOB/DIFF_IO_2A_T1N/DQ0/95
LPDDR4B_DQ31	DK9	IO_2A_T/IOB/DIFF_IO_2A_T1P/DQ0/94
LPDDR4B_DQ24	DD9	IO_2A_T/IOB/DIFF_IO_2A_T2N/DQ0/93
LPDDR4B_DQ25	DD12	IO_2A_T/IOB/DIFF_IO_2A_T2P/DQ0/92
LPDDR4B_DM3	DF12	IO_2A_T/IOB/DIFF_IO_2A_T3N/DQ0/91
LPDDR4B_DQS_n3	DJ12	IO_2A_T/IOB/DIFF_IO_2A_T3P/DQ0/90
LPDDR4B_DQS3	DK18	IO_2A_T/IOB/DIFF_IO_2A_T4N/DQ0/89
LPDDR4B_DQ29	DD18	IO_2A_T/IOB/DIFF_IO_2A_T4P/DQ0/88
LPDDR4B_DQ27	DD21	IO_2A_T/IOB/DIFF_IO_2A_T5N/DQ0/87
LPDDR4B_DQ28	DF21	IO_2A_T/IOB/DIFF_IO_2A_T5P/DQ0/86
LPDDR4B_DQ26	DJ21	IO_2A_T/IOB/DIFF_IO_2A_T6N/DQ0/85
LPDDR4B_DQ23	DN7	IO_2A_T/IOB/DIFF_IO_2A_T6P/DQ0/84
LPDDR4B_DQ22	DN3	IO_2A_T/IOB/DIFF_IO_2A_T7N/DQ1/83
LPDDR4B_DQ16	DN10	IO_2A_T/IOB/DIFF_IO_2A_T7P/DQ1/82
LPDDR4B_DQ20	DP7	IO_2A_T/IOB/DIFF_IO_2A_T8N/DQ1/81
LPDDR4B_DQ13	DP13	IO_2A_T/IOB/DIFF_IO_2A_T8P/DQ1/80
LPDDR4B_DM2	DP10	IO_2A_T/IOB/DIFF_IO_2A_T9N/DQ1/79
LPDDR4B_DQS2_n2	DN15	IO_2A_T/IOB/DIFF_IO_2A_T9P/DQ1/78
LPDDR4B_DQS2	DP15	IO_2A_T/IOB/DIFF_IO_2A_T10N/DQ0/1/77
LPDDR4B_DQ19	DN20	IO_2A_T/IOB/DIFF_IO_2A_T10P/DQ0/1/76
LPDDR4B_DQ21	DP22	IO_2A_T/IOB/DIFF_IO_2A_T11N/DQ1/75
LPDDR4B_DQ17	DN17	IO_2A_T/IOB/DIFF_IO_2A_T11P/DQ1/74
LPDDR4B_DQ18	DP20	IO_2A_T/IOB/DIFF_IO_2A_T12N/DQ1/73
HDMI_TX_CLK	DJ24	IO_2A_T/IOB/DIFF_IO_2A_T12P/DQ1/72
SW0	DK24	IO_2A_T/IOB/DIFF_IO_2A_T13N/DQ2/71
SW1	DD24	IO_2A_T/IOB/DIFF_IO_2A_T13P/DQ2/70
SW2	DD27	IO_2A_T/IOB/DIFF_IO_2A_T14N/DQ2/69
SW3	DF27	IO_2A_T/IOB/DIFF_IO_2A_T14P/DQ2/68
LED6	DJ27	IO_2A_T/IOB/DIFF_IO_2A_T15N/DQ2/67
LED1	DJ32	IO_2A_T/IOB/DIFF_IO_2A_T15P/DQ2/66
Mix_CAM_FAN	DK32	IO_2A_T/IOB/PLL_2A_T_CLKOUT1N/DIFF_IO_2A_T16N/DQ0/2/65
CAM_RZQ1	DP35	IO_2A_T/IOB/PLL_2A_T_CLKOUT1P,PLL_2A_T_CLKOUT1,PLL_2A_T_FB1/DIFF_IO_2A_T16P/DQ0/2/64
LED0	DF35	IO_2A_T/IOB/DIFF_IO_2A_T17N/DQ2/63
CLOCK0_50	DJ35	IO_2A_T/IOB/RZQ_T_2A/DIFF_IO_2A_T17P/DQ2/62
LED2	DN22	IO_2A_T/IOB/CLK_T_2A_1N/DIFF_IO_2A_T18N/DQ2/61
LED3	DP23	IO_2A_T/IOB/CLK_T_2A_1P/DIFF_IO_2A_T18P/DQ2/60
LED4	DN25	IO_2A_T/IOB/CLK_T_2A_0N/DIFF_IO_2A_T19N/DQ3/59
LED5	DP25	IO_2A_T/IOB/CLK_T_2A_0P/DIFF_IO_2A_T19P/DQ3/58
DN28	DN28	IO_2A_T/IOB/DIFF_IO_2A_T20N/DQ3/57
LED7	DP30	IO_2A_T/IOB/DIFF_IO_2A_T20P/DQ3/56
CAM_CLK_n	DN30	IO_2A_T/IOB/PLL_2A_T_CLKOUT0N/DIFF_IO_2A_T21N/DQ3/55
CAM_CLK_p	DP33	IO_2A_T/IOB/PLL_2A_T_CLKOUT0P,PLL_2A_T_CLKOUT0,PLL_2A_T_FB0/DIFF_IO_2A_T21P/DQ3/54
CAM_D_n1	DP38	IO_2A_T/IOB/DIFF_IO_2A_T22N/DQ0/3/53
CAM_D_p1	DP38	IO_2A_T/IOB/DIFF_IO_2A_T22P/DQ0/3/52
CAM_D_n0	DN33	IO_2A_T/IOB/DIFF_IO_2A_T23N/DQ3/51
CAM_D_p0	DP36	IO_2A_T/IOB/DIFF_IO_2A_T23P/DQ3/50
		IO_2A_T/IOB/DIFF_IO_2A_T24N/DQ3/49
		IO_2A_T/IOB/DIFF_IO_2A_T24P/DQ3/48

A5EB013BB23BE4S

## BANK 2AB

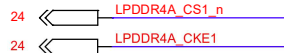
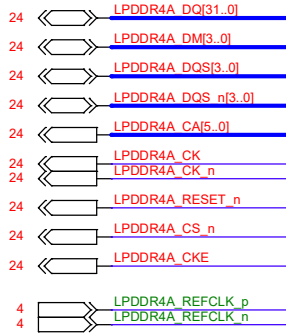
IO_2A_B/IOB/DIFF_IO_2A_B1N/DQ4/47	DN41
IO_2A_B/IOB/DIFF_IO_2A_B1P/DQ4/46	DP43
IO_2A_B/IOB/DIFF_IO_2A_B2N/DQ4/45	DN43
IO_2A_B/IOB/DIFF_IO_2A_B2P/DQ4/44	DP45
IO_2A_B/IOB/DIFF_IO_2A_B3N/DQ4/43	DN45
IO_2A_B/IOB/DIFF_IO_2A_B3P/DQ4/42	DP47
IO_2A_B/IOB/PLL_2A_B_CLKOUT1N/DIFF_IO_2A_B4N/DQ0/4/41	DN50
IO_2A_B/IOB/PLL_2A_B_CLKOUT1,PLL_2A_B_CLKOUT1,PLL_2A_B_FB1/DIFF_IO_2A_B4P/DQ0/4/40	DP50
IO_2A_B/IOB/DIFF_IO_2A_B5N/DQ4/39	DN55
IO_2A_B/IOB/RZQ_B_2A/DIFF_IO_2A_B5P/DQ4/38	DP58
IO_2A_B/IOB/CLK_B_2A_1N/DIFF_IO_2A_B6N/DQ4/37	DN53
IO_2A_B/IOB/CLK_B_2A_1P/DIFF_IO_2A_B6P/DQ4/36	DP55
IO_2A_B/IOB/CLK_B_2A_0N/DIFF_IO_2A_B7N/DQ5/35	DJ39
IO_2A_B/IOB/CLK_B_2A_0P/DIFF_IO_2A_B7P/DQ5/34	DK39
IO_2A_B/IOB/DIFF_IO_2A_B8N/DQ5/33	DP39
IO_2A_B/IOB/DIFF_IO_2A_B8P/DQ5/32	DP48
IO_2A_B/IOB/PLL_2A_B_CLKOUT0N/DIFF_IO_2A_B9N/DQ5/31	DF42
IO_2A_B/IOB/PLL_2A_B_CLKOUT0P,PLL_2A_B_CLKOUT0,PLL_2A_B_FB0/DIFF_IO_2A_B9P/DQ5/30	DJ42
IO_2A_B/IOB/DIFF_IO_2A_B10N/DQ0/5/29	DK48
IO_2A_B/IOB/DIFF_IO_2A_B10P/DQ0/5/28	DP48
IO_2A_B/IOB/DIFF_IO_2A_B11N/DQ5/27	DK48
IO_2A_B/IOB/DIFF_IO_2A_B11P/DQ5/26	DP48
IO_2A_B/IOB/DIFF_IO_2A_B12N/DQ5/25	DF51
IO_2A_B/IOB/DIFF_IO_2A_B12P/DQ5/24	DJ51
IO_2A_B/IOB/DIFF_IO_2A_B13N/DQ6/23	DN58
IO_2A_B/IOB/DIFF_IO_2A_B13P/DQ6/22	DP60
IO_2A_B/IOB/DIFF_IO_2A_B14N/DQ6/21	DN61
IO_2A_B/IOB/DIFF_IO_2A_B14P/DQ6/20	DP61
IO_2A_B/IOB/DIFF_IO_2A_B15N/DQ6/19	DN63
IO_2A_B/IOB/DIFF_IO_2A_B15P/DQ6/18	DP66
IO_2A_B/IOB/DIFF_IO_2A_B16N/DQ0/6/17	DN66
IO_2A_B/IOB/DIFF_IO_2A_B16P/DQ0/6/16	DP68
IO_2A_B/IOB/DIFF_IO_2A_B17N/DQ6/15	DN74
IO_2A_B/IOB/DIFF_IO_2A_B17P/DQ6/14	DP73
IO_2A_B/IOB/DIFF_IO_2A_B18N/DQ6/13	DN68
IO_2A_B/IOB/DIFF_IO_2A_B18P/DQ6/12	DP70
IO_2A_B/IOB/DIFF_IO_2A_B19N/DQ7/11	DJ56
IO_2A_B/IOB/DIFF_IO_2A_B19P/DQ7/10	DK56
IO_2A_B/IOB/DIFF_IO_2A_B20N/DQ7/9	DP56
IO_2A_B/IOB/DIFF_IO_2A_B20P/DQ7/8	DP59
IO_2A_B/IOB/DIFF_IO_2A_B21N/DQ7/7	DF59
IO_2A_B/IOB/DIFF_IO_2A_B21P/DQ7/6	DJ59
IO_2A_B/IOB/DIFF_IO_2A_B22N/DQ0/7/5	DJ62
IO_2A_B/IOB/DIFF_IO_2A_B22P/DQ0/7/4	DK62
IO_2A_B/IOB/DIFF_IO_2A_B23N/DQ7/3	DP62
IO_2A_B/IOB/DIFF_IO_2A_B23P/DQ7/2	DP65
IO_2A_B/IOB/DIFF_IO_2A_B24N/DQ7/1	DF65
IO_2A_B/IOB/DIFF_IO_2A_B24P/DQ7/0	DJ65

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<b>Title</b> DE25-Nano Board	
<b>Size</b> B	<b>Document Number</b> FPGA Bank 2A
<b>Date:</b> Tuesday, July 29, 2025	<b>Rev</b> A0
<b>Sheet</b> 6 of 35	

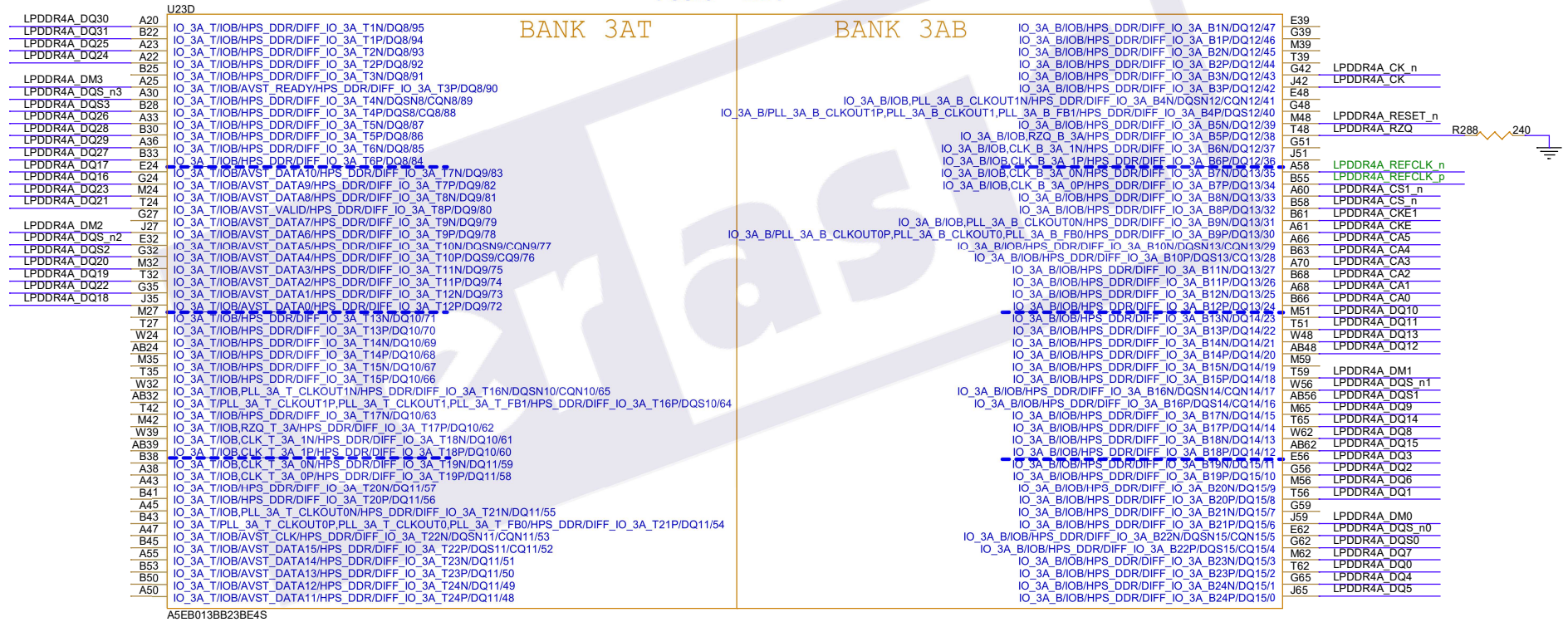


# HSIO Banks 3AT and 3AB

## LPDDR4 A Interface (HPS)



VCCIO = 1.1V



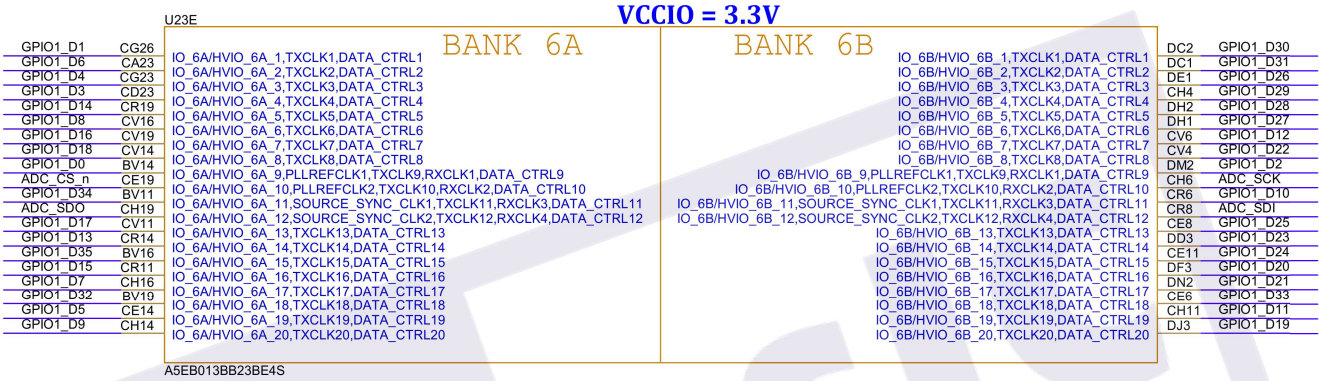
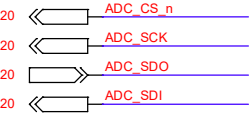
terasic		Copyright (c) 2024 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title <b>DE25-Nano Board</b>			
Size B	Document Number FPGA Bank 3A		Rev A0
Date:	Tuesday, July 29, 2025		Sheet 7 of 35

HVIO Banks 6A and 6B

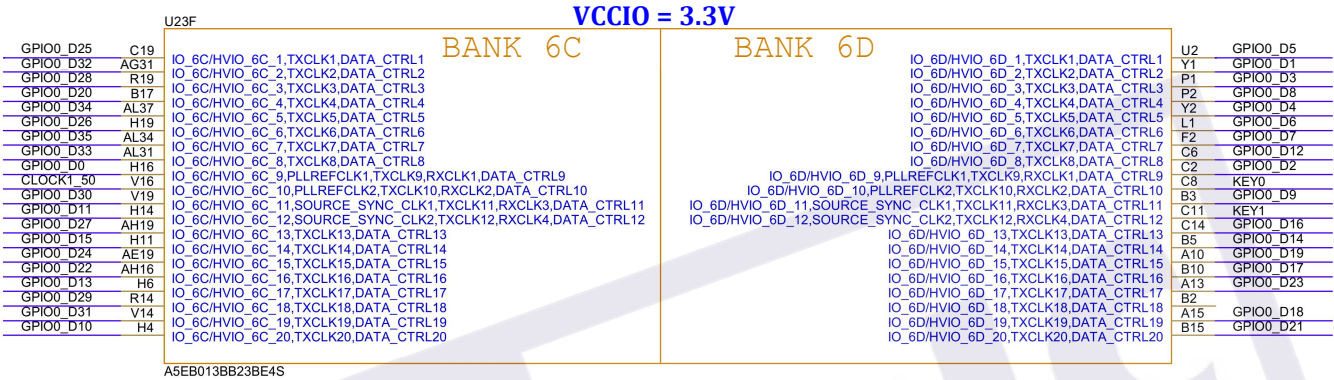
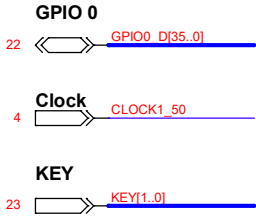
GPIO 1



ADC

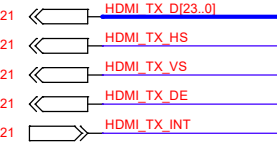


# HVIO Banks 6C and 6D

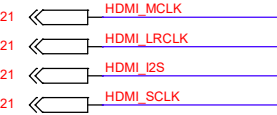


HVIO Banks 6E and 6F

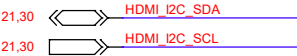
HDMI TX Interface



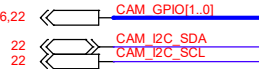
HDMI Audio Interface



HDMI I2C Interface



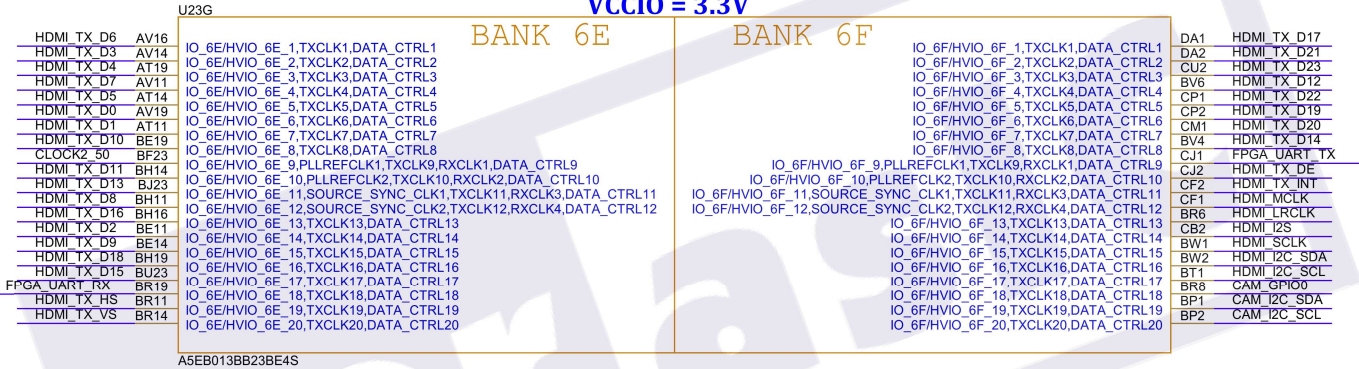
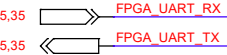
Camera Control Interface



Clock



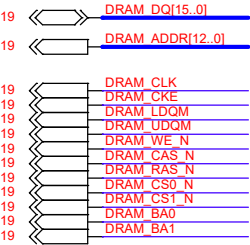
FPGA UART Interface



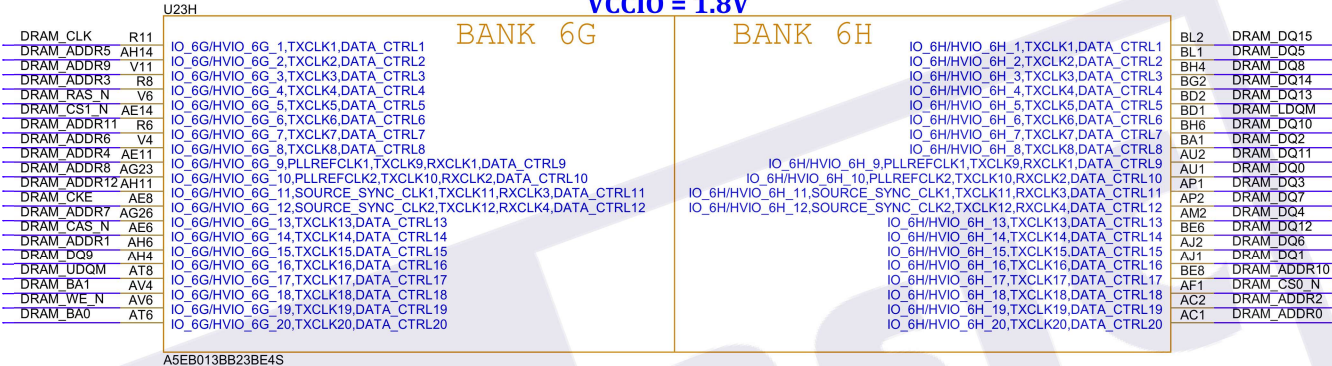


HVIO Banks 6G and 6H

SDRAM Interface (FPGA)

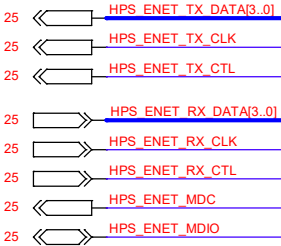


VCCIO = 1.8V

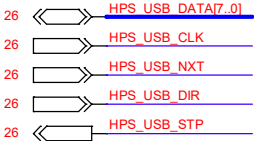


HPS

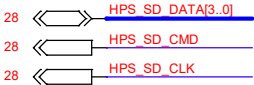
Ethernet PHY Interface (RGMII)



UBS PHY Interface (ULPI)



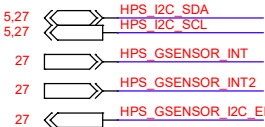
SD Card Interface



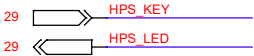
HPS 25MHz Clock



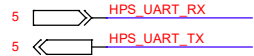
HPS I2C Interface



HPS User Button amd LED



HPS UART Interface



U23B

VCCIO = 1.8V

HPS


HPS_USB_CLK	BC64
HPS_USB_STP	BC67
HPS_USB_DIR	AY67
HPS_USB_DATA0	AN72
HPS_USB_DATA1	AY69
HPS_USB_NXT	BA75
HPS_USB_DATA2	BC71
HPS_USB_DATA3	AJ74
HPS_USB_DATA4	AY71
HPS_USB_DATA5	AJ75
HPS_USB_DATA6	BC72
HPS_USB_DATA7	BP74
HPS_ENET_TX_CLK	BP75
HPS_ENET_TX_CTL	BL74
HPS_ENET_RX_CLK	BL75
HPS_ENET_RX_CTL	AP74
HPS_ENET_TX_DATA0	BG74
HPS_ENET_TX_DATA1	AP75
HPS_ENET_RX_DATA0	BD74
HPS_ENET_RX_DATA1	BN71
HPS_ENET_TX_DATA2	AM74
HPS_ENET_RX_DATA2	AJ74
HPS_ENET_RX_DATA3	AJ75

HPS_SD_DATA0	AF75
HPS_SD_DATA1	AC75
HPS_SD_CLK	AC74
HPS_CLK_25	AN67
HPS_GSENSOR_INT	Y75
HPS_SD_DATA2	AN64
HPS_SD_DATA3	Y74
HPS_SD_CMD	AK69
	U74
HPS_GSENSOR_INT2	AK67
HPS_GSENSOR_I2C_EN	P75
	P74
HPS_I2C_SDA	L75
HPS_I2C_SCL	N72
HPS_UART_TX	N71
HPS_UART_RX	AD72
HPS_KEY	F75
HPS_LED	AD71
	IK71
	AK71
	F74
	AA71
HPS_ENET_MDIO	C74
HPS_ENET_MDC	D71

HPS\_IOA\_1/GPIO0\_I00,SPIM0\_SS1\_N,SPIS0\_CLK,UART0\_CTS\_N,NAND\_ADQ0,SDMMC\_DATA0,USB0\_CLK,EMAC0\_PPS0,TRACE\_D10/HPS\_IOA\_1  
HPS\_IOA\_2/GPIO0\_I01,SPIM1\_SS1\_N,SPIS0\_MOSI,UART0\_RTS\_N,NAND\_ADQ1,SDMMC\_DATA1,USB0\_STP,EMAC0\_PPSTRIG0,TRACE\_D9/HPS\_IOA\_2  
HPS\_IOA\_3/GPIO0\_I02,SPIS0\_SS0\_N,UART0\_TX,I2C1\_SDA,NAND\_WE,N,SDMMC\_CLK,USB0\_DIR,EMAC1\_PPS1,TRACE\_D8/HPS\_IOA\_3  
HPS\_IOA\_4/GPIO0\_I03,SPIS0\_MISO,UART0\_RX,I2C1\_SCL,NAND\_RE,N,USB0\_DATA0,EMAC1\_PPSTRIG1,TRACE\_D7/HPS\_IOA\_4  
HPS\_IOA\_5/GPIO0\_I04,SPIM0\_CLK,UART1\_CTS\_N,I2C0\_SDA,NAND\_WP,N,SDMMC\_WRITE,PROTECT,USB0\_DATA1,EMAC2\_PPS2,TRACE\_D6/HPS\_IOA\_5  
HPS\_IOA\_6/GPIO0\_I05,SPIM0\_MOSI,UART1\_RTS\_N,I2C0\_SCL,NAND\_ADQ2,SDMMC\_DATA2,USB0\_NXT,EMAC2\_PPSTRIG2,TRACE\_D5/HPS\_IOA\_6  
HPS\_IOA\_7/GPIO0\_I06,SPIM0\_MISO,MDIO2\_MDIO,UART1\_TX,I2C2\_EMAC2\_SDA,NAND\_ADQ3,SDMMC\_DATA3,USB0\_DATA2,TRACE\_D4/HPS\_IOA\_7  
HPS\_IOA\_8/GPIO0\_I07,SPIM0\_SS0\_N,MDIO2\_MDC,UART1\_RX,I2C2\_EMAC2\_SCL,NAND\_CLE,SDMMC\_CMD,USB0\_DATA3,TRACE\_D15/HPS\_IOA\_8  
HPS\_IOA\_9/GPIO0\_I08,SPIM1\_CLK,SPIS1\_CLK,MDIO1\_MDIO,I2C2\_EMAC1\_SDA,NAND\_ADQ4,SDMMC\_DATA4,USB0\_DATA4,I3C1\_SDA,TRACE\_D14/HPS\_IOA\_9  
HPS\_IOA\_10/GPIO0\_I09,SPIM1\_MOSI,SPIS1\_MOSI,MDIO1\_MDC,I2C2\_EMAC1\_SCL,NAND\_ADQ5,SDMMC\_DATA5,USB0\_DATA5,I3C1\_SCL,TRACE\_D13/HPS\_IOA\_10  
HPS\_IOA\_11/GPIO0\_I010,SPIM1\_MISO,SPIS1\_SS0\_N,MDIO0\_MDIO,I2C2\_EMAC0\_SDA,NAND\_ADQ6,SDMMC\_DATA6,USB0\_DATA6,I3C0\_SDA,TRACE\_D12/HPS\_IOA\_11  
HPS\_IOA\_12/GPIO0\_I011,SPIM1\_SS0\_N,SPIS1\_MISO,MDIO0\_MDC,I2C2\_EMAC0\_SCL,NAND\_ADQ7,SDMMC\_DATA7,USB0\_DATA7,I3C0\_SCL,TRACE\_D11/HPS\_IOA\_12  
HPS\_IOA\_13/GPIO0\_I012,NAND\_ALE,SDMMC\_PU\_PD\_DATA2,USB1\_CLK,EMAC0\_TX\_CLK,TRACE\_D10/HPS\_IOA\_13  
HPS\_IOA\_14/GPIO0\_I013,NAND\_RB,N,SDMMC\_PWR\_ENA,USB1\_STP,EMAC0\_TX\_CTL,TRACE\_D9/HPS\_IOA\_14  
HPS\_IOA\_15/GPIO0\_I014,NAND\_CE,N,USB1\_DIR,EMAC0\_RX\_CLK,TRACE\_D8/HPS\_IOA\_15  
HPS\_IOA\_16/GPIO0\_I015,NAND\_DQS,SDMMC\_DATA\_STROBE,USB1\_DATA0,EMAC0\_RX\_CTL,TRACE\_D7/HPS\_IOA\_16  
HPS\_IOA\_17/GPIO0\_I016,I3C1\_SDA,NAND\_ADQ8,USB1\_DATA1,EMAC0\_TXD0,TRACE\_D6/HPS\_IOA\_17  
HPS\_IOA\_18/GPIO0\_I017,I3C1\_SCL,NAND\_ADQ9,USB1\_NXT,EMAC0\_TXD1,TRACE\_D5/HPS\_IOA\_18  
HPS\_IOA\_19/GPIO0\_I018,I3C0\_SDA,NAND\_ADQ10,USB1\_DATA2,EMAC0\_RXD0,TRACE\_D4/HPS\_IOA\_19  
HPS\_IOA\_20/GPIO0\_I019,SPIM1\_SS1\_N,I3C0\_SCL,NAND\_ADQ11,USB1\_DATA3,EMAC0\_RXD1,TRACE\_CLK/HPS\_IOA\_20  
HPS\_IOA\_21/GPIO0\_I020,SPIM1\_CLK,SPIS0\_CLK,UART0\_CTS\_N,I2C1\_SDA,NAND\_ADQ12,USB1\_DATA4,EMAC0\_TXD2,TRACE\_D0/HPS\_IOA\_21  
HPS\_IOA\_22/GPIO0\_I021,SPIM1\_MOSI,SPIS0\_MOSI,UART0\_RTS\_N,I2C1\_SCL,NAND\_ADQ13,USB1\_DATA5,EMAC0\_TXD3,TRACE\_D1/HPS\_IOA\_22  
HPS\_IOA\_23/GPIO0\_I022,SPIM1\_MISO,SPIS0\_SS0\_N,UART0\_TX,I2C0\_SDA,NAND\_ADQ14,USB1\_DATA6,EMAC0\_RXD2,TRACE\_D2/HPS\_IOA\_23  
HPS\_IOA\_24/GPIO0\_I023,SPIM1\_SS0\_N,SPIS0\_MISO,UART0\_RX,I2C0\_SCL,NAND\_ADQ15,USB1\_DATA7,EMAC0\_RXD3,TRACE\_D3/HPS\_IOA\_24

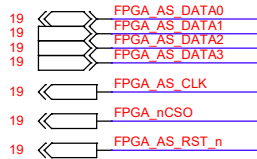
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HPS\_I0B\_2/GPIO1\_I01,SPIM1\_MOSI,UART0\_RTS\_N,EMAC0\_PPSTRIG0,NAND\_ADQ1,SDMMC\_DATA1,EMAC1\_TX\_CTL,TRACE\_D9/HPS\_I0B\_2  
HPS\_I0B\_3/GPIO1\_I02,SPIM1\_MISO,UART0\_TX,I2C0\_SDA,NAND\_WE,N,SDMMC\_CLK,EMAC1\_RX\_CLK,TRACE\_D8/HPS\_I0B\_3  
HPS\_I0B\_4/GPIO1\_I03,SPIM1\_SS0\_N,UART0\_RX,I2C0\_SCL,NAND\_RE,N,EMAC1\_RX\_CTL,TRACE\_D7/HPS\_I0B\_4  
HPS\_I0B\_5/GPIO1\_I04,SPIM1\_SS1\_N,SPIS1\_CLK,UART1\_CTS\_N,EMAC2\_PPS2,NAND\_WP,N,SDMMC\_WRITE,PROTECT,I3C1\_SDA,EMAC1\_TXD0,TRACE\_D6/HPS\_I0B\_5  
HPS\_I0B\_6/GPIO1\_I05,SPIS1\_MOSI,UART1\_RTS\_N,EMAC2\_PPSTRIG2,NAND\_ADQ2,SDMMC\_DATA2,I3C1\_SCL,EMAC1\_TXD1,TRACE\_D5/HPS\_I0B\_6  
HPS\_I0B\_7/GPIO1\_I06,SPIS1\_SS0\_N,UART1\_TX,I2C1\_SDA,NAND\_ADQ3,SDMMC\_DATA3,I3C0\_SDA,EMAC1\_RXD0,TRACE\_D4/HPS\_I0B\_7  
HPS\_I0B\_8/GPIO1\_I07,SPIS1\_MISO,UART1\_RX,I2C1\_SCL,NAND\_CLE,SDMMC\_CMD,I3C0\_SCL,EMAC1\_RXD1,TRACE\_D15/HPS\_I0B\_8  
HPS\_I0B\_9/GPIO1\_I08,JTAG\_TCK,SPIS0\_CLK,MDIO2\_MDIO,I2C2\_EMAC2\_SDA,NAND\_ADQ4,SDMMC\_DATA4,EMAC1\_TXD2,TRACE\_D14/HPS\_I0B\_9  
HPS\_I0B\_10/GPIO1\_I09,JTAG\_TMS,SPIS0\_MOSI,MDIO2\_MDC,I2C2\_EMAC2\_SCL,NAND\_ADQ5,SDMMC\_DATA5,EMAC1\_TXD3,TRACE\_D13/HPS\_I0B\_10  
HPS\_I0B\_11/GPIO1\_I010,JTAG\_TDO,SPIS0\_SS0\_N,MDIO0\_MDIO,I2C2\_EMAC0\_SDA,NAND\_ADQ6,SDMMC\_DATA6,EMAC1\_RXD2,TRACE\_D12/HPS\_I0B\_11  
HPS\_I0B\_12/GPIO1\_I011,JTAG\_TDI,SPIS0\_MISO,MDIO0\_MDC,I2C2\_EMAC0\_SCL,NAND\_ADQ7,SDMMC\_DATA7,EMAC1\_RXD3,TRACE\_D11/HPS\_I0B\_12  
HPS\_I0B\_13/GPIO1\_I012,I2C1\_SDA,NAND\_ALE,SDMMC\_PU\_PD\_DATA2,EMAC2\_TX\_CLK,TRACE\_D10/HPS\_I0B\_13  
HPS\_I0B\_14/GPIO1\_I013,I2C1\_SCL,NAND\_RB,N,SDMMC\_PWR\_ENA,EMAC2\_TX\_CTL,TRACE\_D9/HPS\_I0B\_14  
HPS\_I0B\_15/GPIO1\_I014,UART1\_TX,NAND\_CE,N,I3C1\_SDA,EMAC2\_RX\_CLK,TRACE\_D8/HPS\_I0B\_15  
HPS\_I0B\_16/GPIO1\_I015,UART1\_RX,NAND\_DQS,SDMMC\_DATA\_STROBE,I3C1\_SCL,EMAC2\_RX\_CTL,TRACE\_D7/HPS\_I0B\_16  
HPS\_I0B\_17/GPIO1\_I016,UART1\_CTS\_N,NAND\_ADQ8,I3C0\_SDA,EMAC2\_TXD0,TRACE\_D6/HPS\_I0B\_17  
HPS\_I0B\_18/GPIO1\_I017,SPIM0\_SS1\_N,UART1\_RTS\_N,NAND\_ADQ9,I3C0\_SCL,EMAC2\_TXD1,TRACE\_D5/HPS\_I0B\_18  
HPS\_I0B\_19/GPIO1\_I018,SPIM0\_MISO,MDIO1\_MDIO,I2C2\_EMAC1\_SDA,NAND\_ADQ10,EMAC2\_RXD0,TRACE\_D4/HPS\_I0B\_19  
HPS\_I0B\_20/GPIO1\_I019,SPIM0\_SS0\_N,MDIO1\_MDC,I2C2\_EMAC1\_SCL,NAND\_ADQ11,EMAC2\_RXD1,TRACE\_CLK/HPS\_I0B\_20  
HPS\_I0B\_21/GPIO1\_I020,SPIM0\_CLK,SPIS1\_CLK,I2C2\_EMAC2\_SDA,NAND\_ADQ12,EMAC2\_TXD2,TRACE\_D0/HPS\_I0B\_21  
HPS\_I0B\_22/GPIO1\_I021,SPIM0\_MOSI,SPIS1\_MOSI,I2C2\_EMAC2\_SCL,NAND\_ADQ13,EMAC2\_TXD3,TRACE\_D1/HPS\_I0B\_22  
HPS\_I0B\_23/GPIO1\_I022,SPIM0\_MISO,SPIS1\_SS0\_N,MDIO0\_MDIO,I2C2\_EMAC0\_SDA,NAND\_ADQ14,EMAC2\_RXD2,TRACE\_D2/HPS\_I0B\_23  
HPS\_I0B\_24/GPIO1\_I023,SPIM0\_SS0\_N,SPIS1\_MISO,MDIO0\_MDC,I2C2\_EMAC0\_SCL,NAND\_ADQ15,EMAC2\_RXD3,TRACE\_D3/HPS\_I0B\_24

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Title <b>DE25-Nano Board</b>	
Size B	Document Number FPGA Bank HPS
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# FPGA Configuration

## FPGA ASx4 Interface



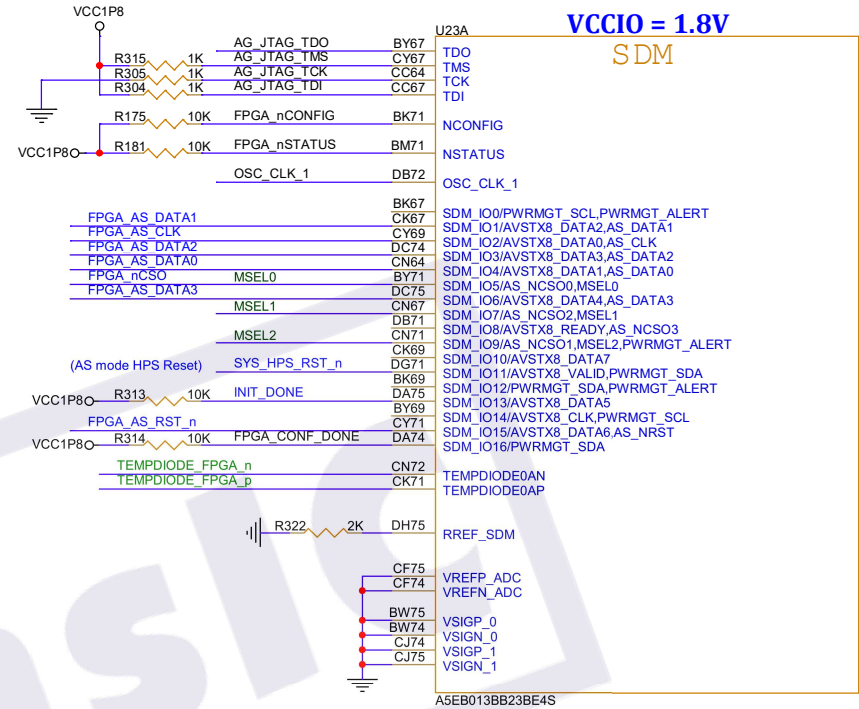
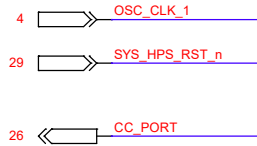
## FPGA Temperature diode



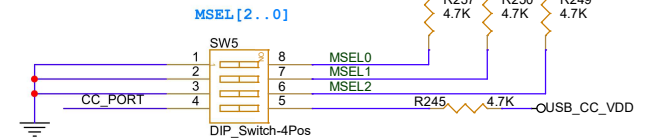
## Agilex JTAG Interface



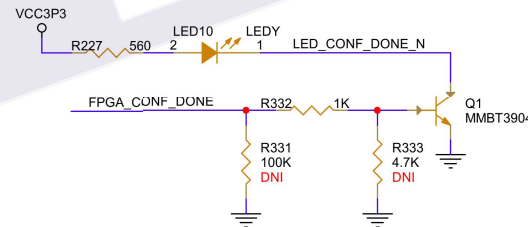
## FPGA Configuration



MSEL[2:0]	Configuration Mode
001	AS - Fast (Default Setting)
111	JTAG



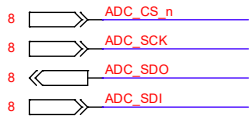
CC_PORT	USB OTG Mode Select
1 (ON)	DFP Mode
NC (OFF)	DRP Mode (Default Setting)



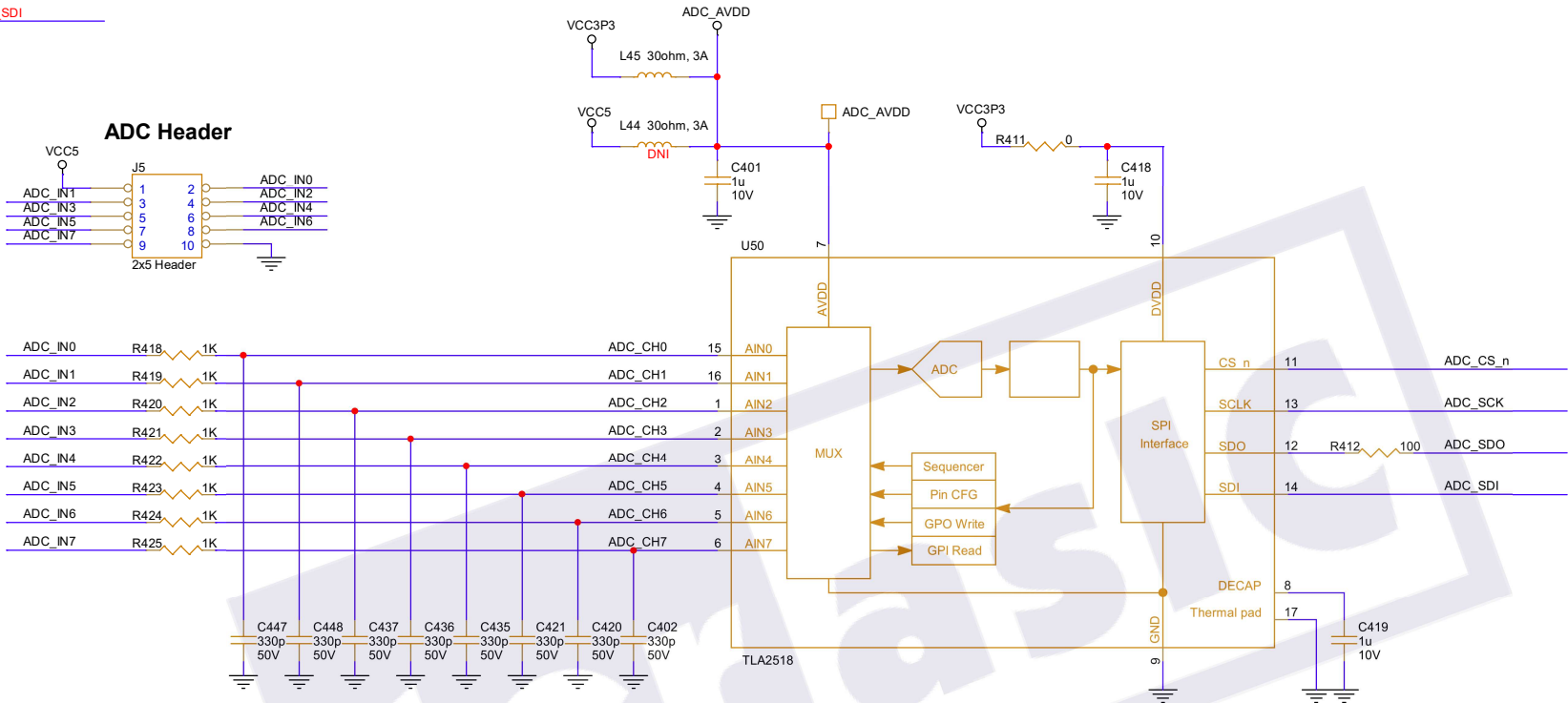
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Title <b>DE25-Nano Board</b>		
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ADC

ADC



ADC Header





# GPIO 0 / GPIO 1 and MIPI

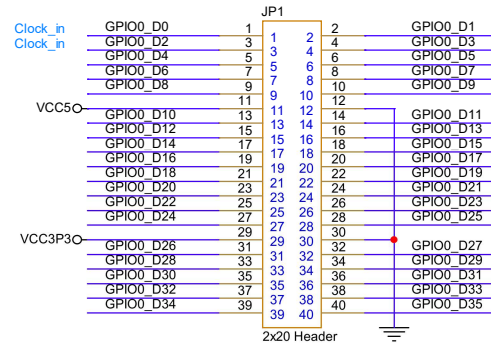
## GPIO 0

9 GPIO0\_D[35..0]

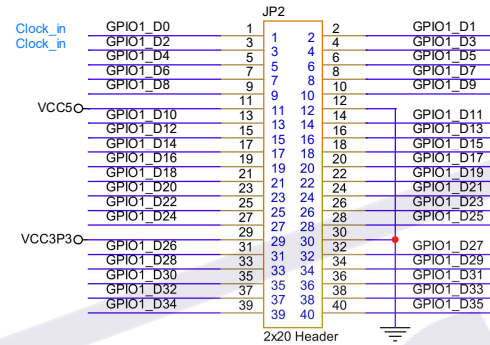
## GPIO 1

8 GPIO1\_D[35..0]

### GPIO 0 Header



### GPIO 1 Header

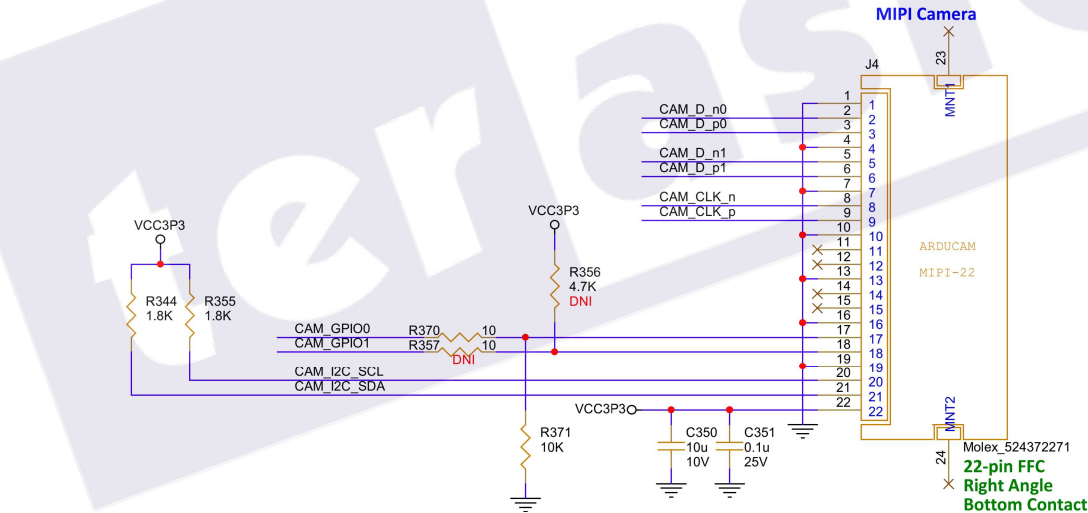


## Camera MIPI Interface

6 CAM\_D\_p[1..0]  
6 CAM\_D\_n[1..0]  
6 CAM\_CLK\_p  
6 CAM\_CLK\_n

## Camera Control Interface

6,10 CAM\_GPIO[1..0]  
10 CAM\_I2C\_SDA  
10 CAM\_I2C\_SCL



# Buttons / Switchs and LEDs

## KEY

9 << KEY1\_0I

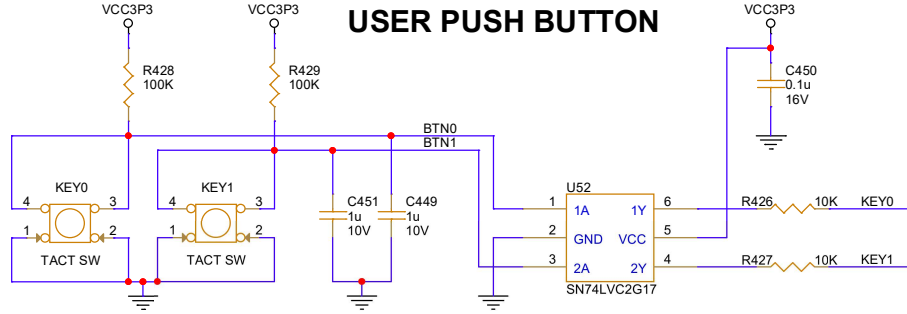
## SWITCH

6 << SW13\_0I

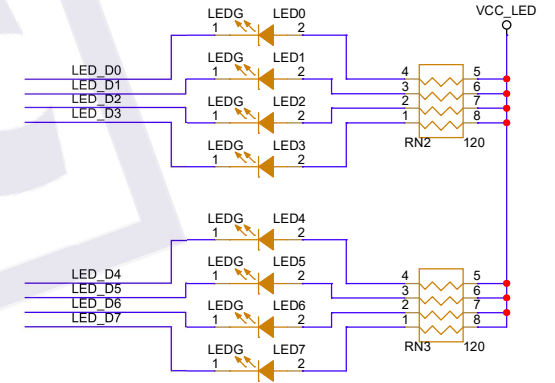
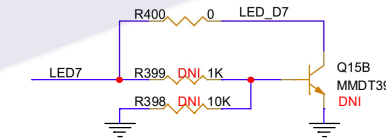
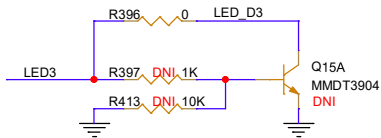
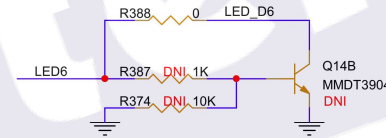
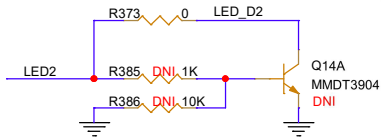
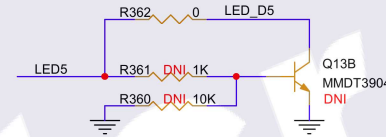
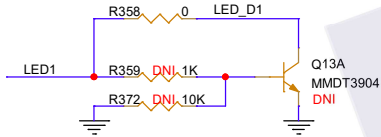
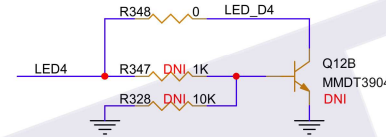
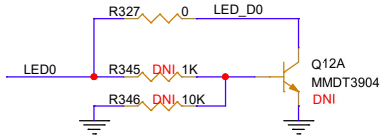
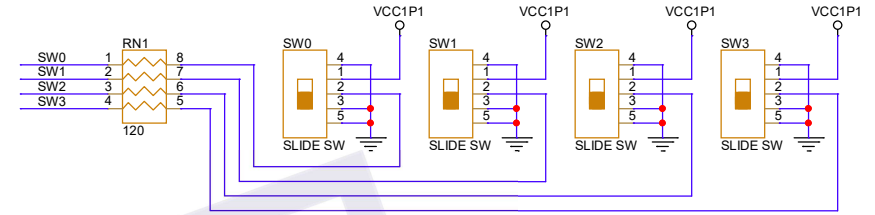
## LED

6 << LED17\_0I

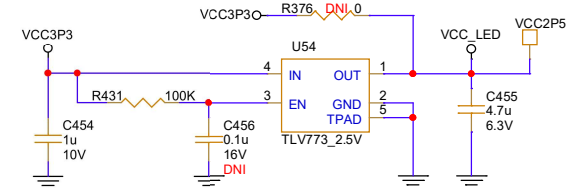
## USER PUSH BUTTON



## USER Switch



## 2.5V / 300mA



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Title			
DE25-Nano Board			
Size	Document Number	Rev	
B	FPGA Button, Switch and LED	A0	
Date:	Tuesday, July 29, 2025	Sheet	23 of 35




A circuit diagram showing a single LED connected to a 5V supply. The LED is represented by a rectangle with a right-pointing arrow. The text "HPS\_LED" is written in red above the LED. A green line connects the LED to a blue line representing the 5V supply.

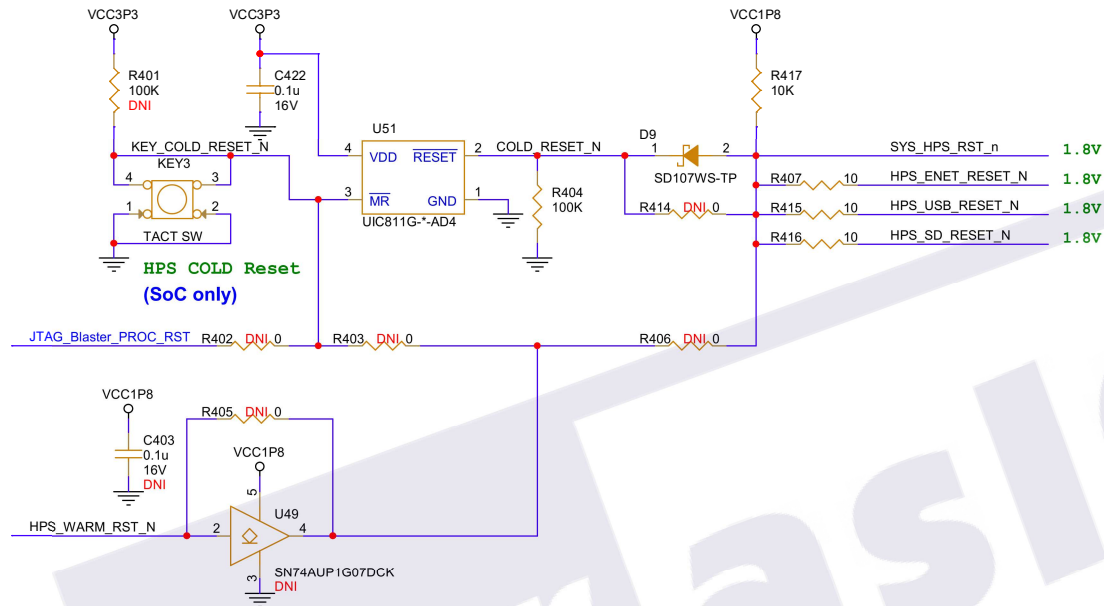
## HPS Reset



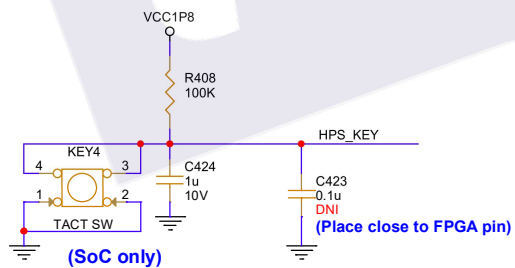
Pin 1: HPS\_SD\_RESET\_N

 **HPS\_WARM\_RST\_N**

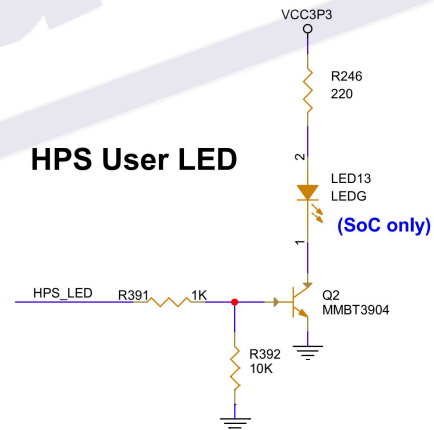
## HPS Cold Reset



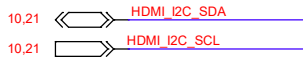
## HPS User Button



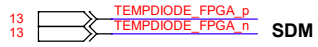
## HPS User LED



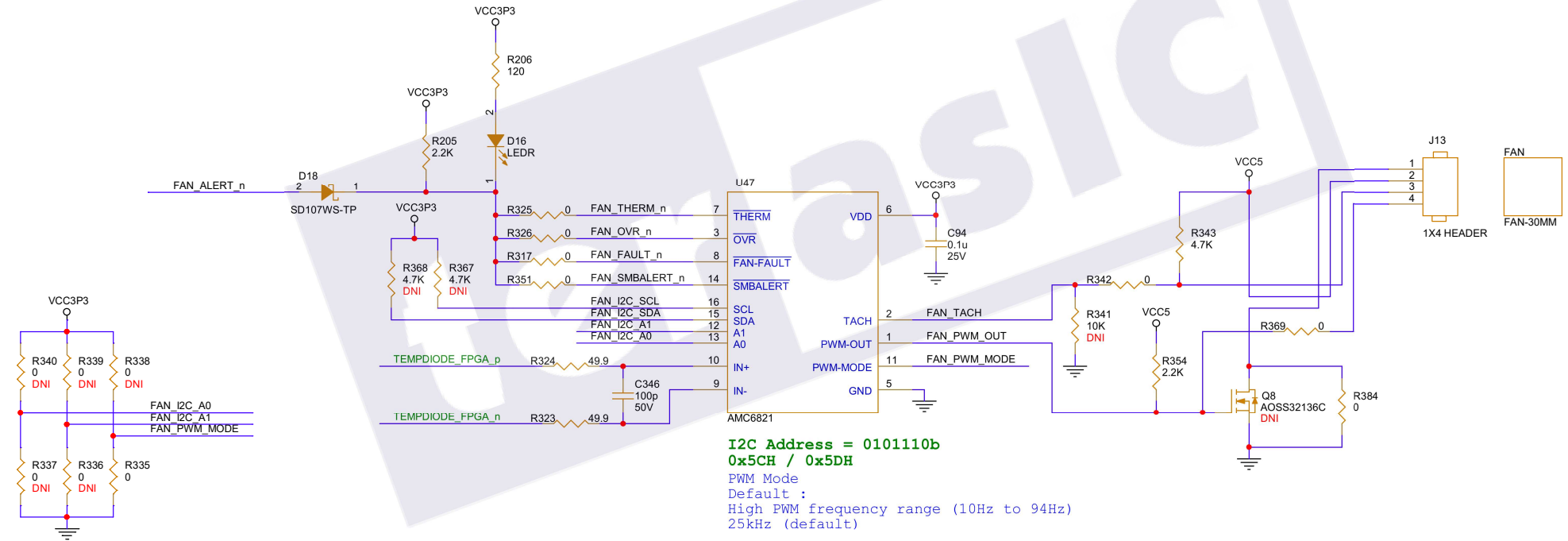
### HDMI I2C Interface




### FPGA Temperature diode



### FAN Interrupter



I2C Address = 0101110b  
0x5CH / 0x5DH  
PWM Mode  
Default :  
High PWM frequency range (10Hz to 94Hz)  
25kHz (default)

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Title			
DE25-Nano Board			
Size	Document Number		Rev
B	FAN Control and Temperature Monitor		A0
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