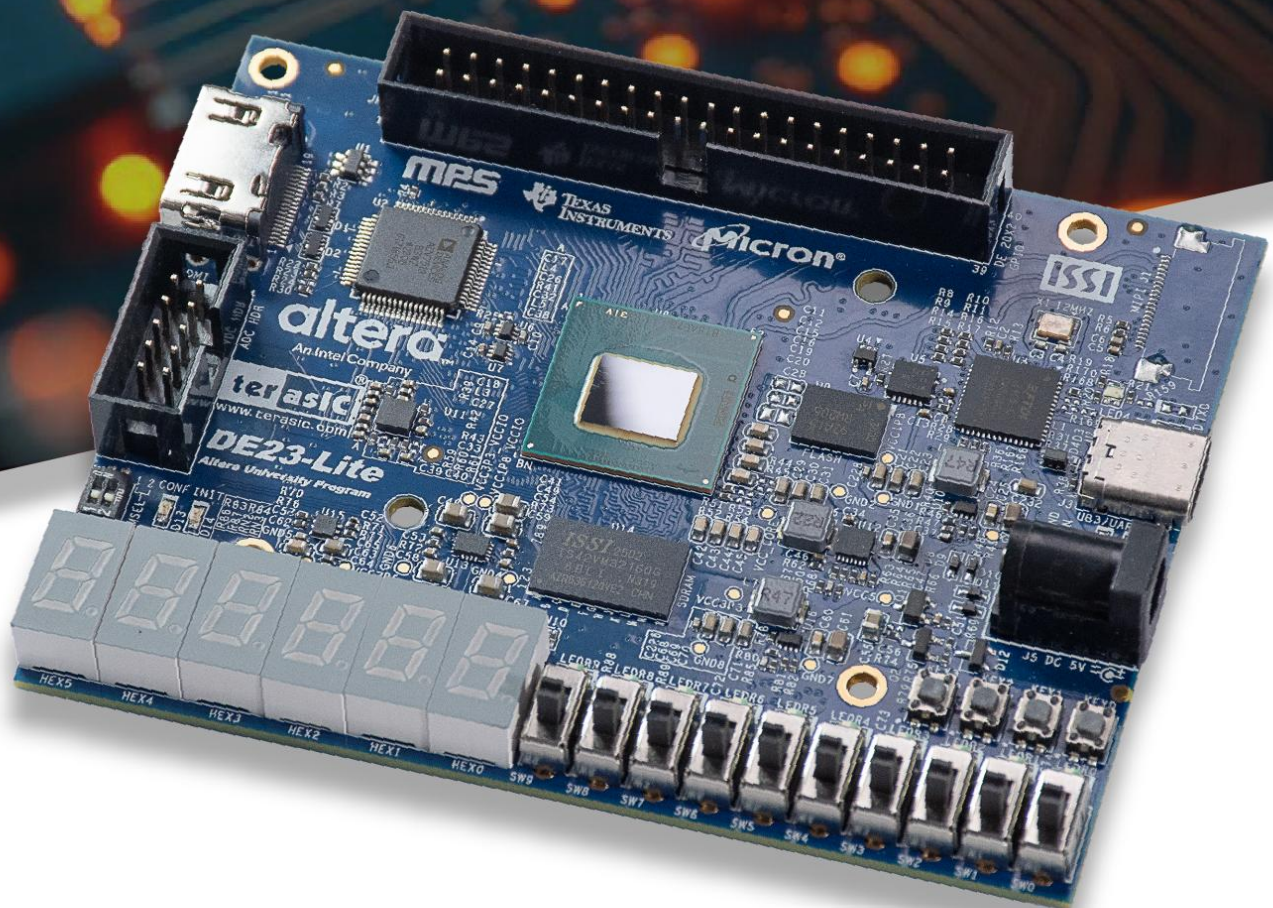


# DE23-Lite Board



## DE23-Lite Getting Started Guide

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## Chapter 1

# *About this Guide*

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The DE23-Lite Getting Started Guide contains a quick overview of the hardware and software setup including step-by-step procedures from installing the necessary software tools to use the board. The main topics that this guide covers are listed below:

- Software Installation: Installing Quartus Pro v25.1 and Ashling RiscFree IDE
- Development Board Setup: Powering on the DE23-Lite
- Perform FPGA System Test: Downloading a FPGA SRAM Object File (.sof)

# Software Installation

## 2.1 Introduction

This section explains how to install the following software:

- Intel Quartus Prime Pro v25.1 software
- Ashling\* RiscFree\* IDE for Altera

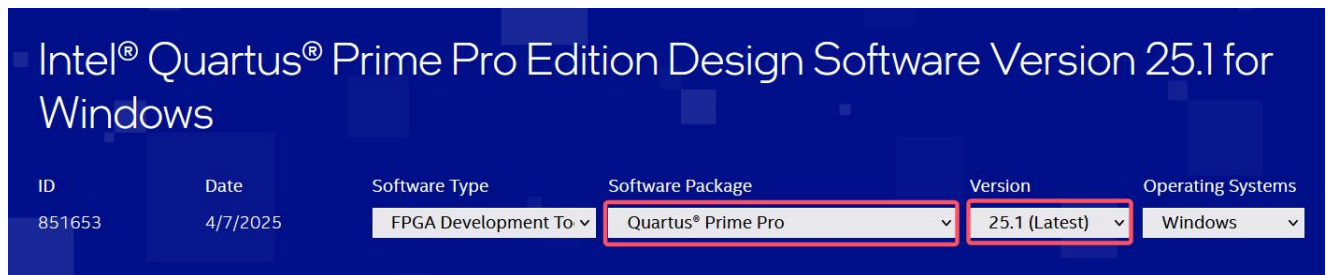
Note: 64-bit OS required

## 2.2 Installing Quartus Prime software

The Intel Complete Design Suite provides the necessary tools used for developing hardware and software solutions for Intel FPGAs. The Quartus Prime software is the primary FPGA development tool used to create reference designs along with the Nios II/V soft-core embedded processor integrated development environment.

User can download the latest Quartus Prime Pro Edition v25.1 software from:

<https://www.intel.com/content/www/us/en/software-kit/851653/intel-quartus-prime-pro-edition-design-software-version-25-1-for-windows.html>



**Figure 2- 1 Select Quartus Prime Pro Edition v25.1 software**

- From the Individual Files tab, you must download the Quartus Prime Pro Edition Part 1&Part2, Ashling RiscFree IDE Altera and Agilex 3 device support package including Agilex common files.



## Individual Files

EDA Simulation Libraries (not needed for Questa*-Intel FPGA edition or Starter edition)		
Download eda_simlib-25.1.0.129-windows.qdz	Size: 29.7 GB SHA1: ed4a8420260b19f0178d2b83108d192c39b39a1a	▼
Quartus® Prime Pro Edition Part 1		
Download QuartusProSetup-25.1.0.129-windows.exe	Size: 3.2 GB SHA1: 08c9eccc967f8d090402523b6126bf5db8da8c62	▼
Quartus® Prime Pro Edition Part 2		
Download QuartusProSetup-part2-25.1.0.129-windows.qdz	Size: 4.6 GB SHA1: 2f416e5c07fc539ac727b914ee17a584035136cf	▼
Questa*-Intel FPGA and Starter Editions		
Download QuestaSetup-25.1.0.129-windows.exe	Size: 2.3 GB SHA1: e663147bf3ec2ef001d938dccc1acd639ea0d66	▼

**Figure 2- 2 Download Quartus Prime Pro Edition installation files**

## Add-On and Stand-Alone Software

Advanced Link Analyzer Pro Edition		
Download AdvLinkAnalyzerProSetup-25.1.0.129-windows.exe	Size: 2.5 GB SHA1: 96b157f077bae0b8746331fea814316bb0dbd056	▼
Ashling* RiscFree* IDE for Altera		
Download RiscFreeSetup-25.1.0.129-windows.exe	Size: 869.5 MB SHA1: 83eb350b89598b09c7b96aba93ef198749c1453b	▼
DSP Builder for Quartus® Prime Pro Edition		
Download DSPBuilderProSetup-25.1.0.129-windows.exe	Size: 65.3 MB SHA1: 27fc2f9ff8cb581bc2acec61cd18defa0dd47f22	▼

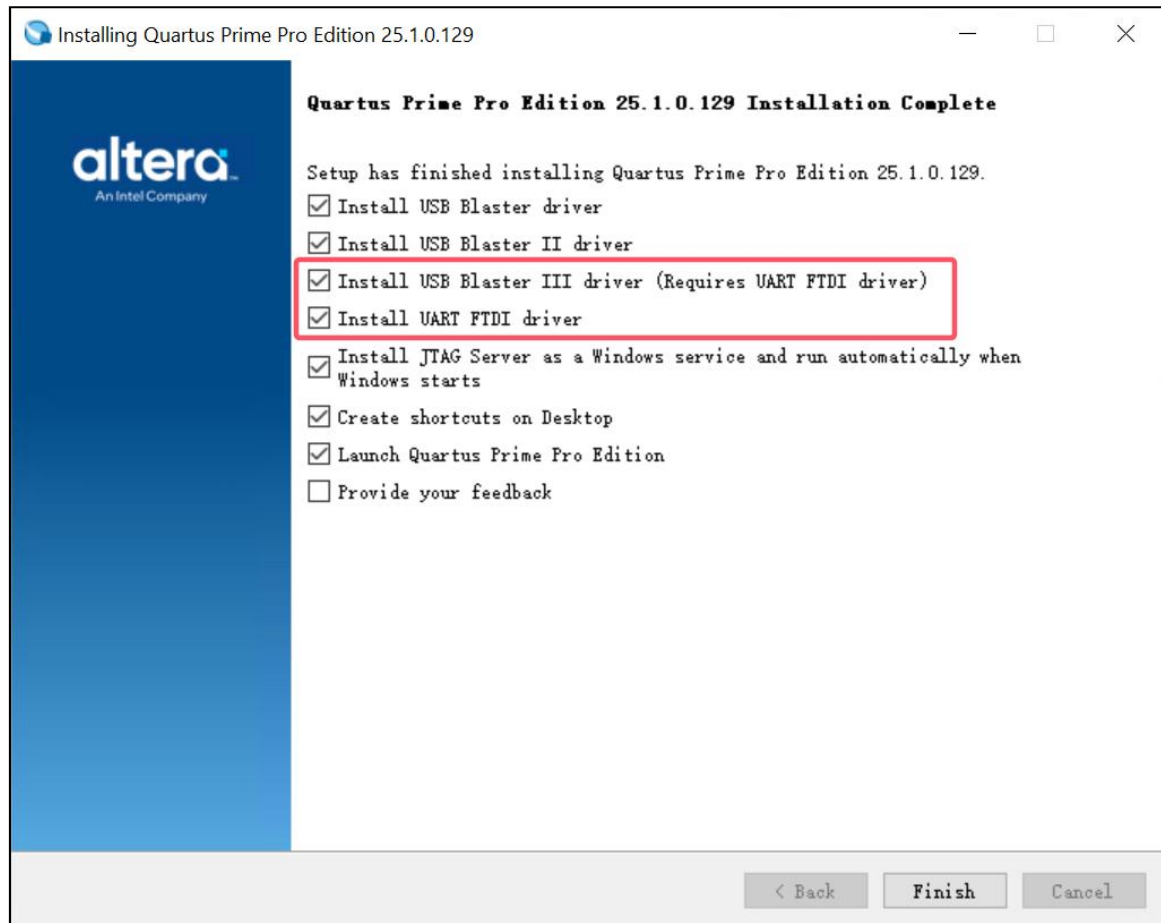
**Figure 2- 3 Download Ashling RiscFree IDE for Altera software**

## Devices

Agilex™ 3 device support (Requires Agilex™ common files)	
<a href="#">Download</a> agilex3-25.1.0.129.qdz	Size: 205.7 MB SHA1: f7264ae01f37070df500fd48b92ab052e6352232
** Installation size: 0.67 GB	
Agilex™ 5 device support (Requires Agilex™ common files)	
<a href="#">Download</a> agilex5-25.1.0.129.qdz	Size: 1.5 GB SHA1: d052e157adc0aa4ab1cfb4bc8a65b25e360dc16a
** Installation size: 4.84 GB	
Agilex™ 7 device support (Requires Agilex™ common files)	
<a href="#">Download</a> agilex7-25.1.0.129.qdz	Size: 3.2 GB SHA1: d3ac0f8f4a0bf02e8d20b0bec759d73821b2d2c5
** Installation size: 8.35 GB	
Agilex™ common files	
<a href="#">Download</a> agilex_common-25.1.0.129.qdz	Size: 4.9 GB SHA1: db3941688c103b60069677de6fa6690884eb3c30
** Installation size: 4.87 GB	

**Figure 2-4 Download Agilex 3 device package and Agilex common files**

- After the file is downloaded on the computer, run the QuartusProSetup-25.1.0.129-windows.exe file to install the software including the Ashling RiscFree IDE for Altera and Agilex 3 device. All the defaults are to be used. The USB Blaster III driver will be installed at the end of software installation, as shown in below **Figure 2-5**.



**Figure 2-5 Install USB Blaster III driver**

- **Important Note:** The DE23-Lite, powered by Altera Agilex 3 FPGA, enables developers to access Intel Quartus Pro Edition software at no cost — no additional license purchase required. Developers can leverage full design and compilation capabilities of Quartus Pro without incurring licensing fees.  
For details on how to acquire the free license, please refer to Intel’s official guide: [Acquiring Free No-Cost Licenses for Intel® Agilex™ 3 Devices](#)

## *Development Board Setup*

### 3.1 Introduction

The instructions in this section explain how to set up the DE23-Lite board. The following pictures show the board overview of the board.

### 3.2 MSEL Settings

#### ■ AS Mode(Default)

The board hardware setting (MSEL[2:1]) is set as 00 (See **Figure 3-1**), the FPGA is configured from QSPI flash.

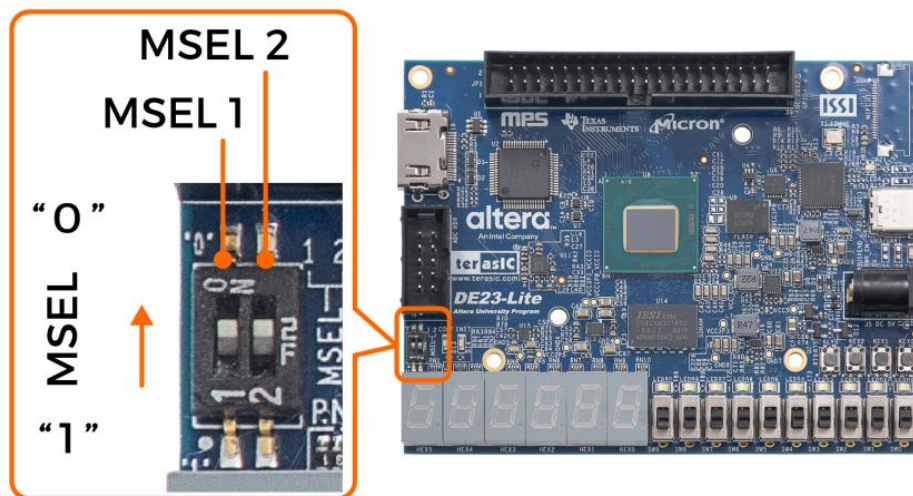


Figure 3-1 FPGA Configuration Mode Switch in AS Mode

### 3.3 DE23-Lite Board Configuration Mode

DE23-Lite board supports two kinds of configuration modes:

1. **JTAG program:** in IEEE standard, JTAG is Joint Test Action Group, with this mode, the configuration bit stream is downloaded directly into the Agilex 3 FPGA. The FPGA will retain this configuration until its power is turned off.
2. **AS program:** Active Serial programming, the configuration bit stream is downloaded into the



QSPI configuration device. The QSPI is non-volatile storage, the code is retained even when the power supply to the DE23-Lite board is turned off. When the board's power is turned on, the configuration data in the QSPI device is automatically loaded into the Agilex 3 FPGA.

## 3.4 USB Blaster III, HDMI and Power Jack

Figure 3-2 shows USB Blaster III, HDMI and Power Jack on DE23-Lite board:

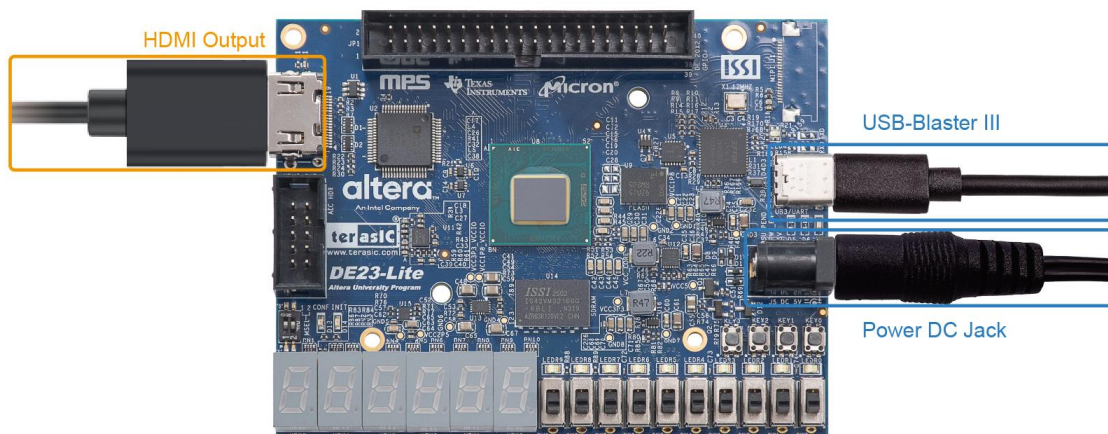


Figure 3-2 USB Blaster III, HDMI and Power Jack on DE23-Lite board

## 3.5 Powering on the Board with Default Code

To power-on the DE23-Lite board and run the default code, perform the following steps below:

1. Connect the HDMI output port of DE23-Lite to a monitor with HDMI input.
2. Make sure the SW2 MSEL[2:1] is set to 00.
3. Connect the supplied DE23-Lite power adapter to the power connector (J5) on the board. At this point, you should see the 5V indicator LED (D7) turned on blue.
4. You should now be able to see the ten user LEDRs are blinking, the HEX0~HEX5 display 0~F in a loop, and the HDMI monitor displays the board image.

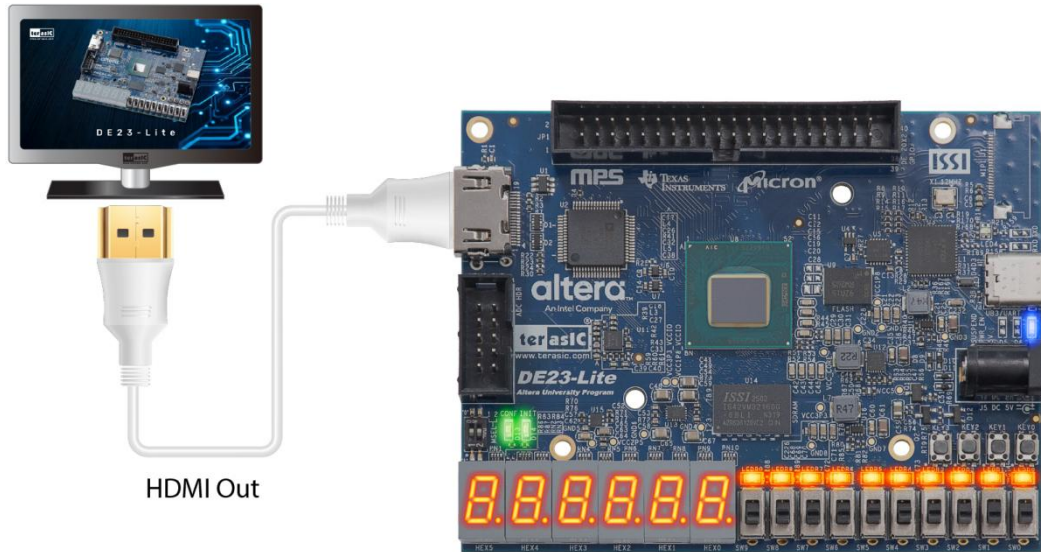


Figure 3-3 DE23-Lite board runs the default code

## Chapter 4

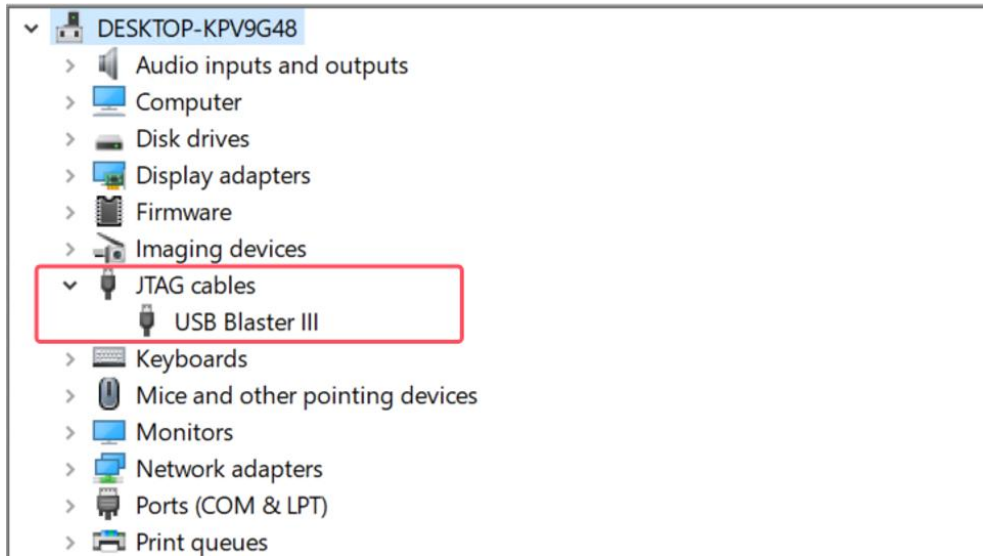
# *Performing a FPGA System Test*

## 4.1 Introduction

This chapter shows how to download a FPGA SRAM Object File(.sof) to DE23-Lite board.

## 4.2 Downloading a FPGA SRAM Object File

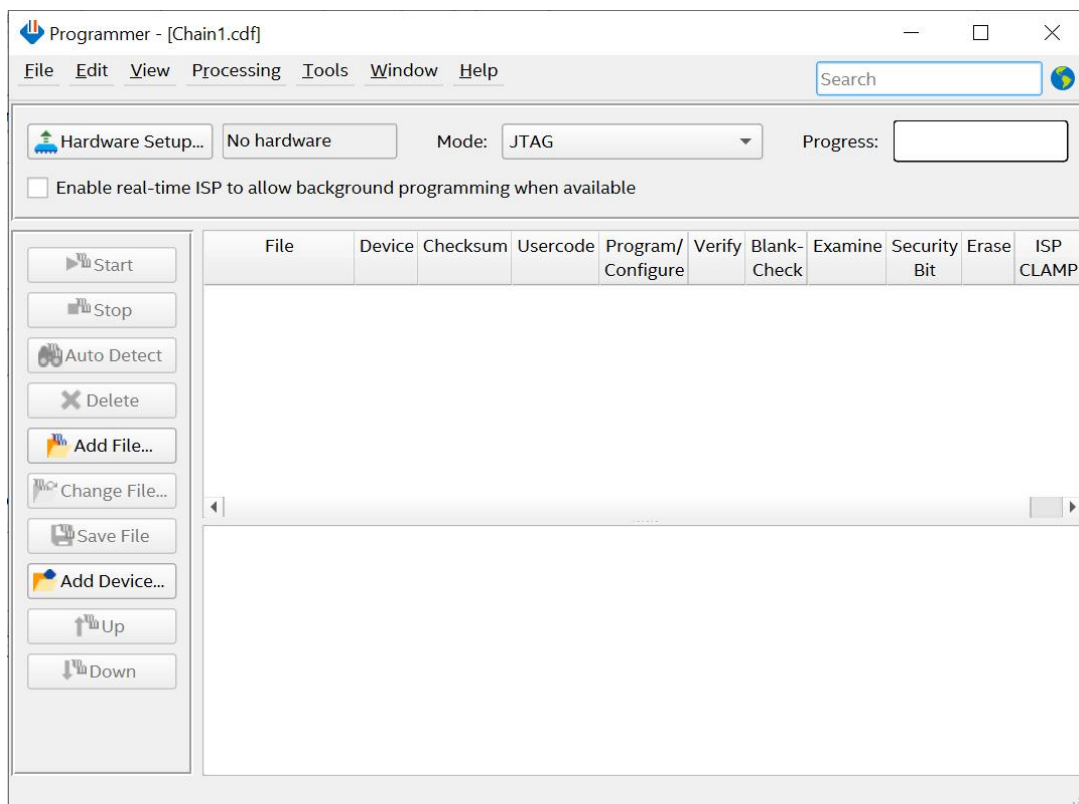
The Quartus Prime Programmer is used to configure the FPGA with a specific .sof file. Before configuring the FPGA, ensure that the Quartus Prime Pro v25.1 software and the USB-Blaster III driver are installed on the host computer. Normally you should see USB Blaster III in PC Device Manager, as shown in **Figure 4-1**.



**Figure 4-1 USB Blaster III shown in PC Device Manager**

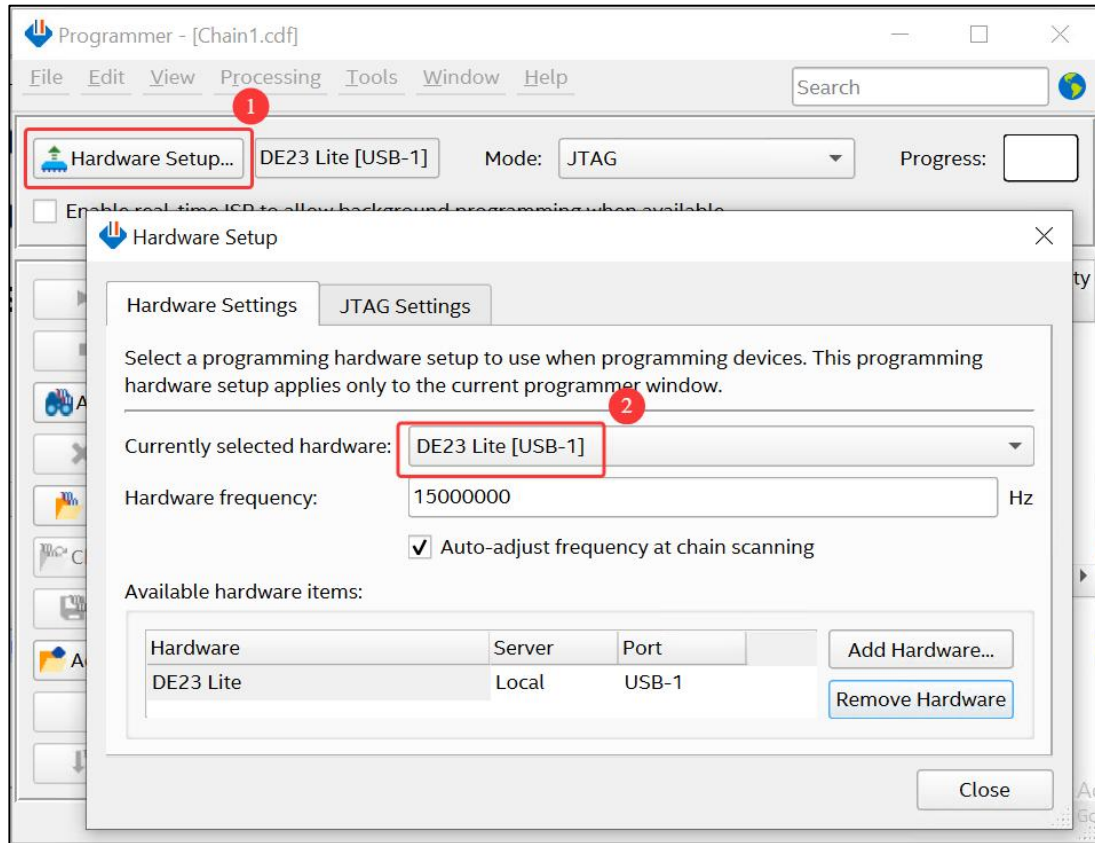
There is only one device (FPGA) on the JTAG Chain of DE23-Lite board, the following shows the programming flow with JTAG mode step by step.

1. Connect your computer to the DE23-Lite board by plugging the Type-C USB cable into the USB Blaster III connector (J3) of DE23-Lite and power up the board (details shown in [Section 3.5](#))
2. Open the Quartus Prime software and select Tools > Programmer. The Programmer window will appear as shown in [Figure 4-2](#).



**Figure 4-2 Quartus Programmer window**

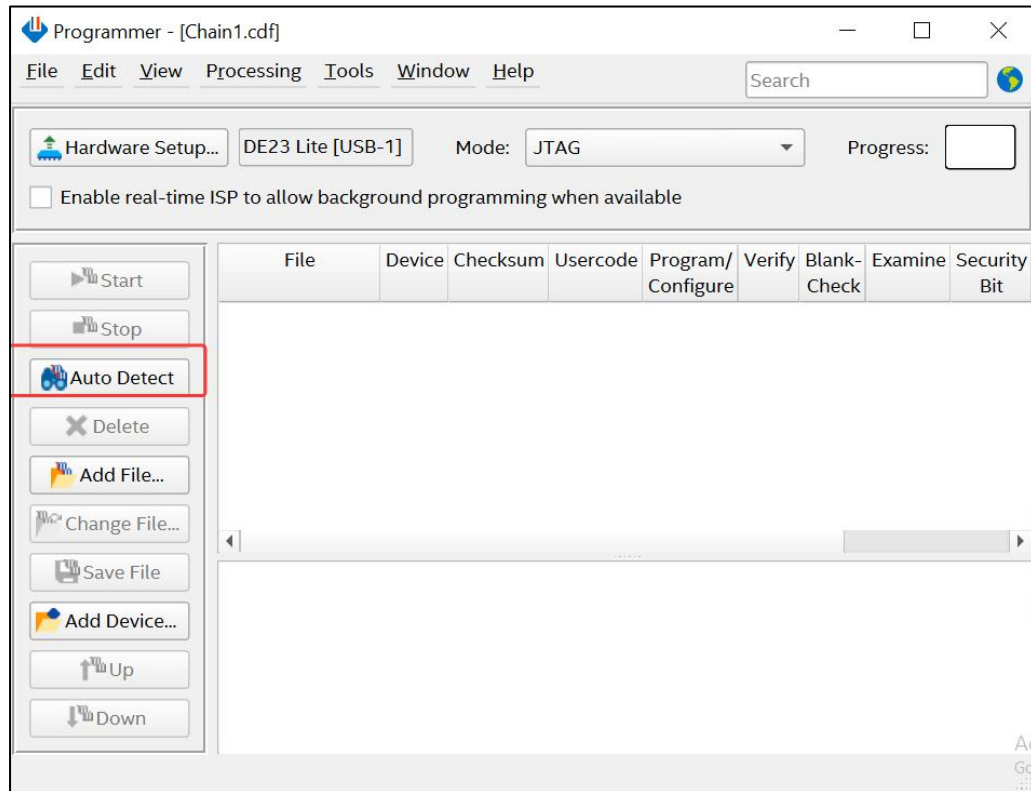
3. Click **Hardware Setup**.
4. Select **DE23-Lite[USB-1]** under **Currently selected hardware**, and click **Close** as shown in **Figure 4-3**.



**Figure 4-3 Hardware Setup**

If the USB-Blaster III does not appear under hardware options list, please confirm if the USB-Blaster III driver has been correctly installed, and the Type-C USB cable has been properly connected between the DE23-Lite board and host computer.

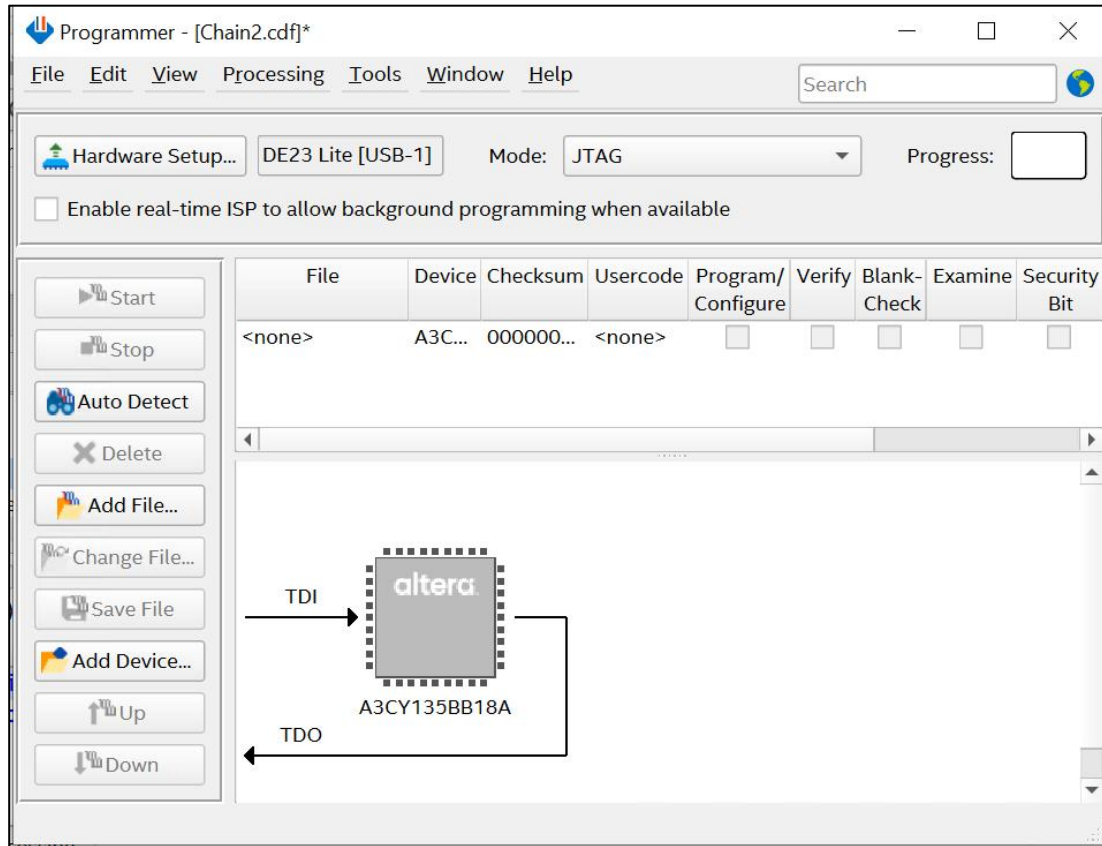
5. Click “Auto Detect”, as shown in **Figure 4-4**.



**Figure 4-4 Auto detect FPGA device**

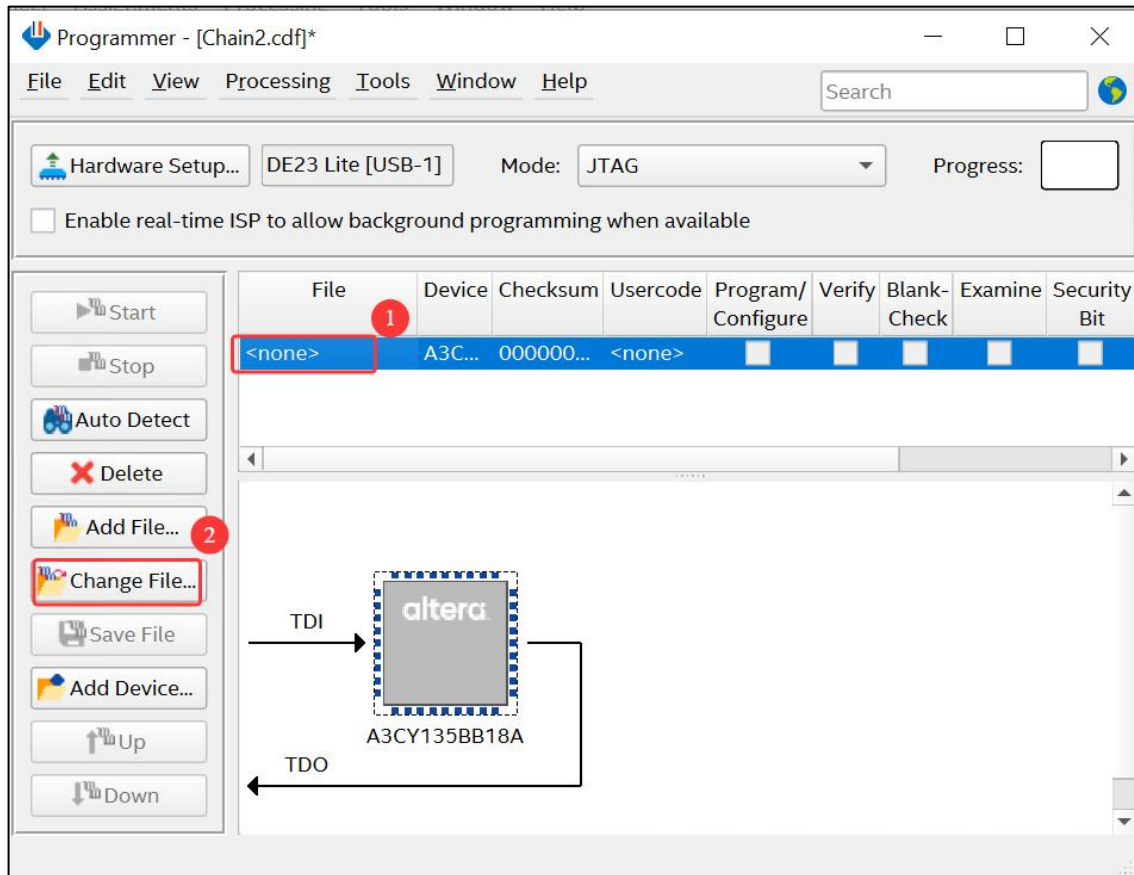
6. The FPGA device of DE23-Lite board is detected under Programmer, as shown in [Figure 4-5](#).





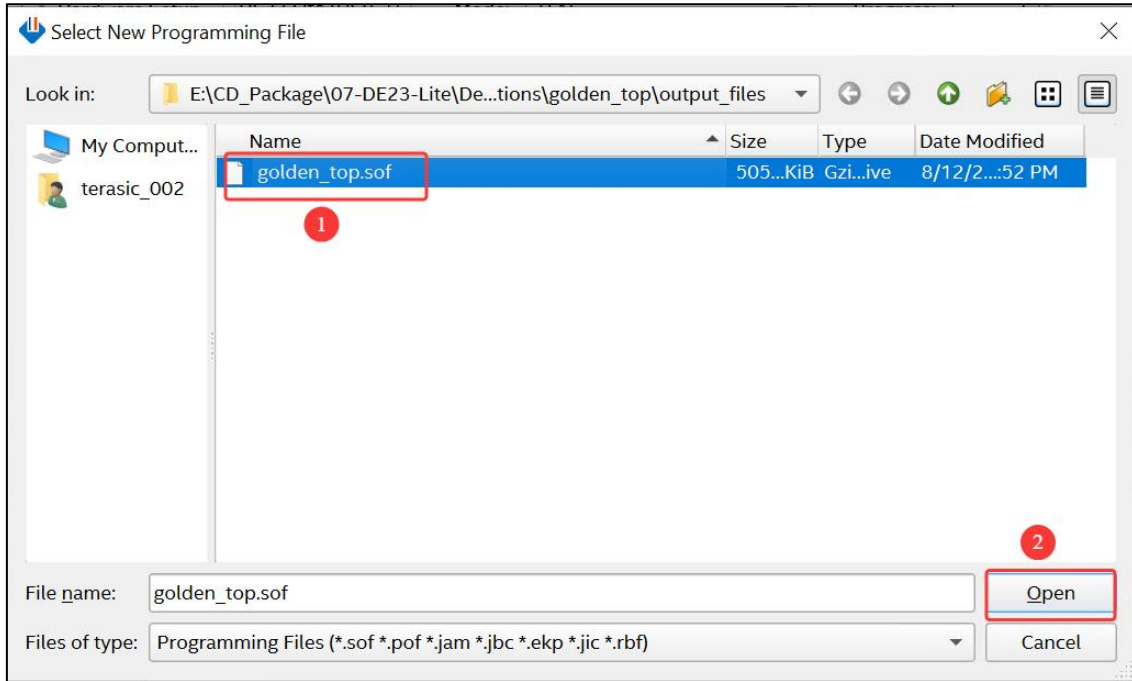
**Figure 4-5 JTAG Chain on DE23-Lite board**

- Click the FPGA device, then click **Change File** button to open the **Select New Programming File** window.



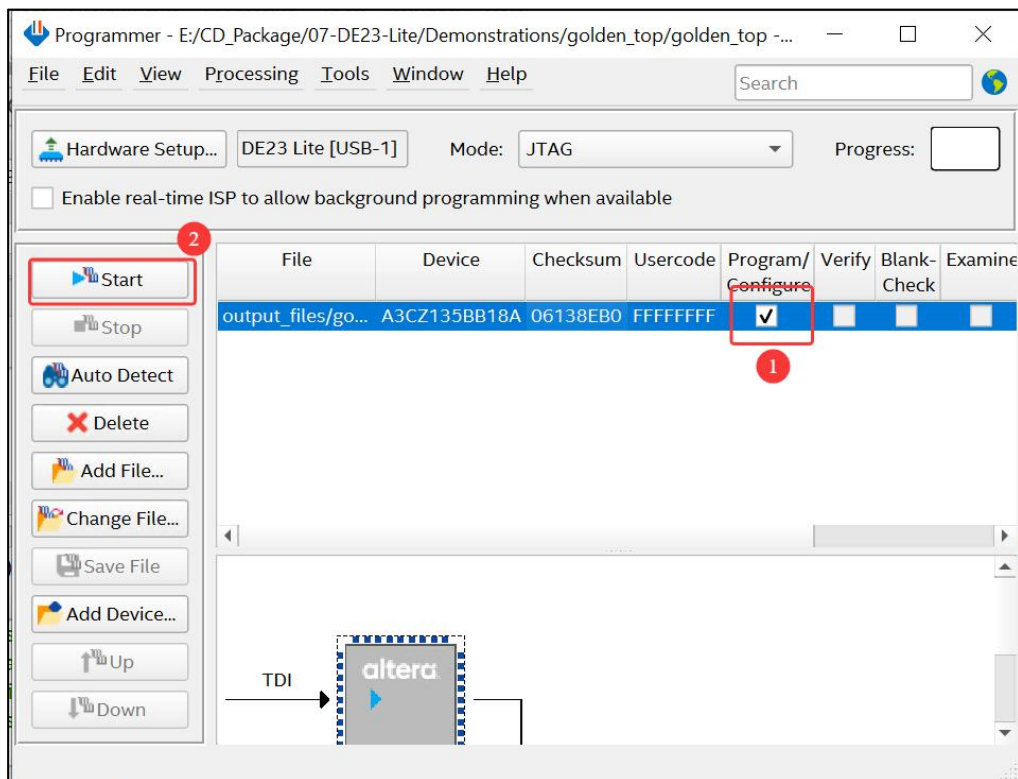
**Figure 4-6 Change file**

8. Browse to select golden\_top.sof in the **Select New Programming File** window as shown in **Figure 4-7**.

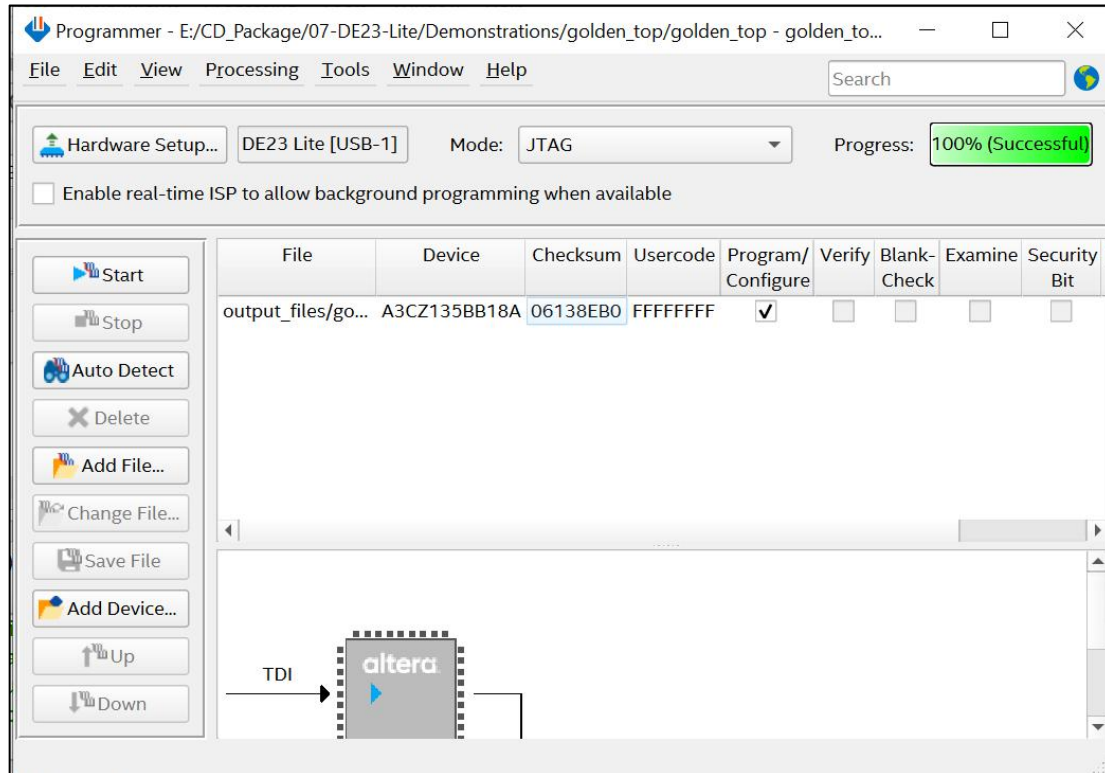


**Figure 4-7 Select golden\_top.sof file**

9. Click “Program/Configure” check box, and then click “Start” button to download .sof file into FPGA, as shown in **Figure 4-8**.



**Figure 4-8 Download .sof file**



**Figure 4-9 Download .sof successfully**

# Additional Information

## Contact Terasic

Users can refer to the following table for technical support and more information of Terasic and our product:

Contact Method	Address
Email	<a href="mailto:support@terasic.com/sales@terasic.com">support@terasic.com/sales@terasic.com</a>
Tel	+886-3-575-0880
Website	<a href="http://www.terasic.com">www.terasic.com</a>
Address	9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan, 30070

## Revision History

Date	Version	Changes
2025.08	V1.0	First Version