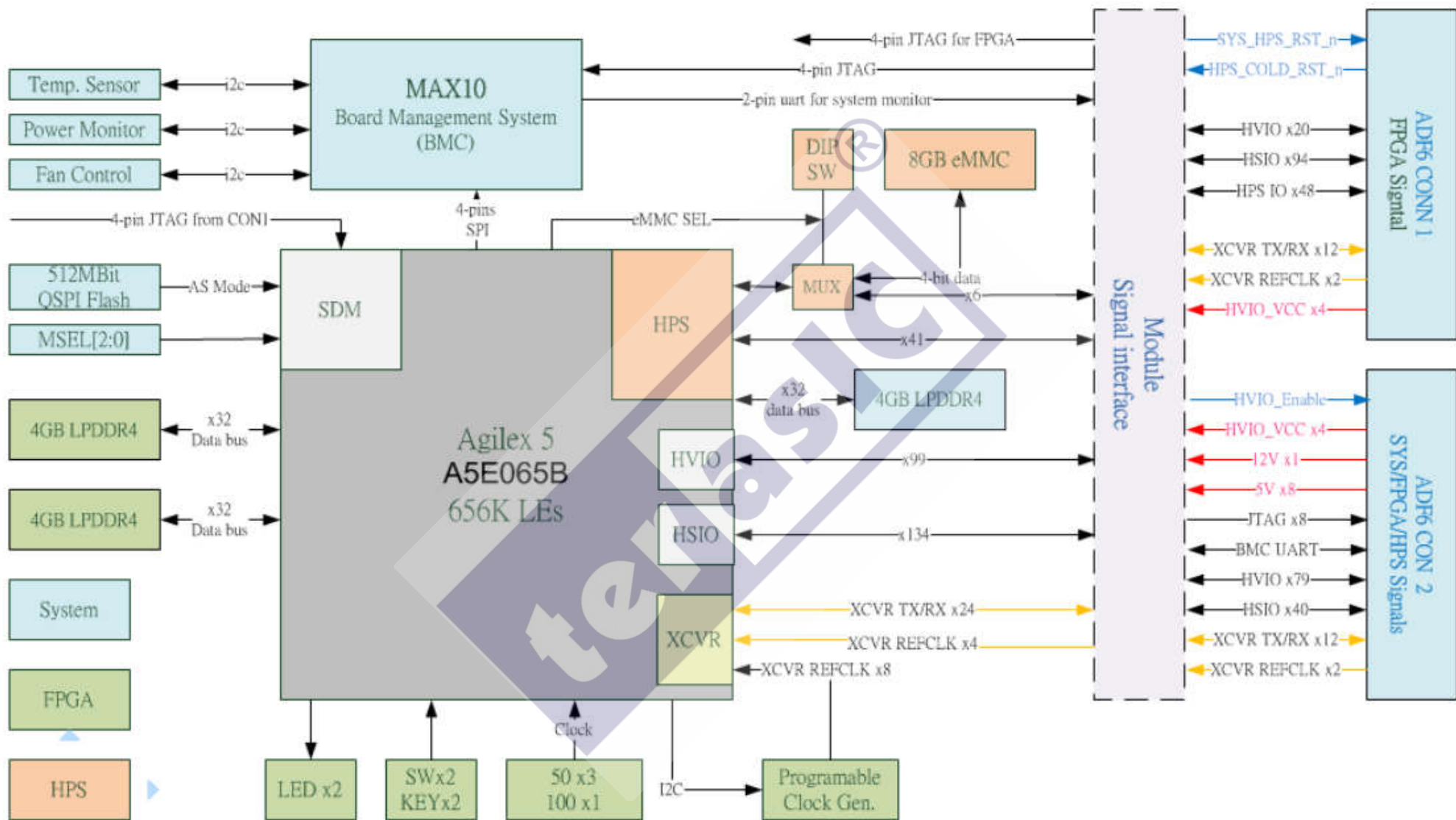
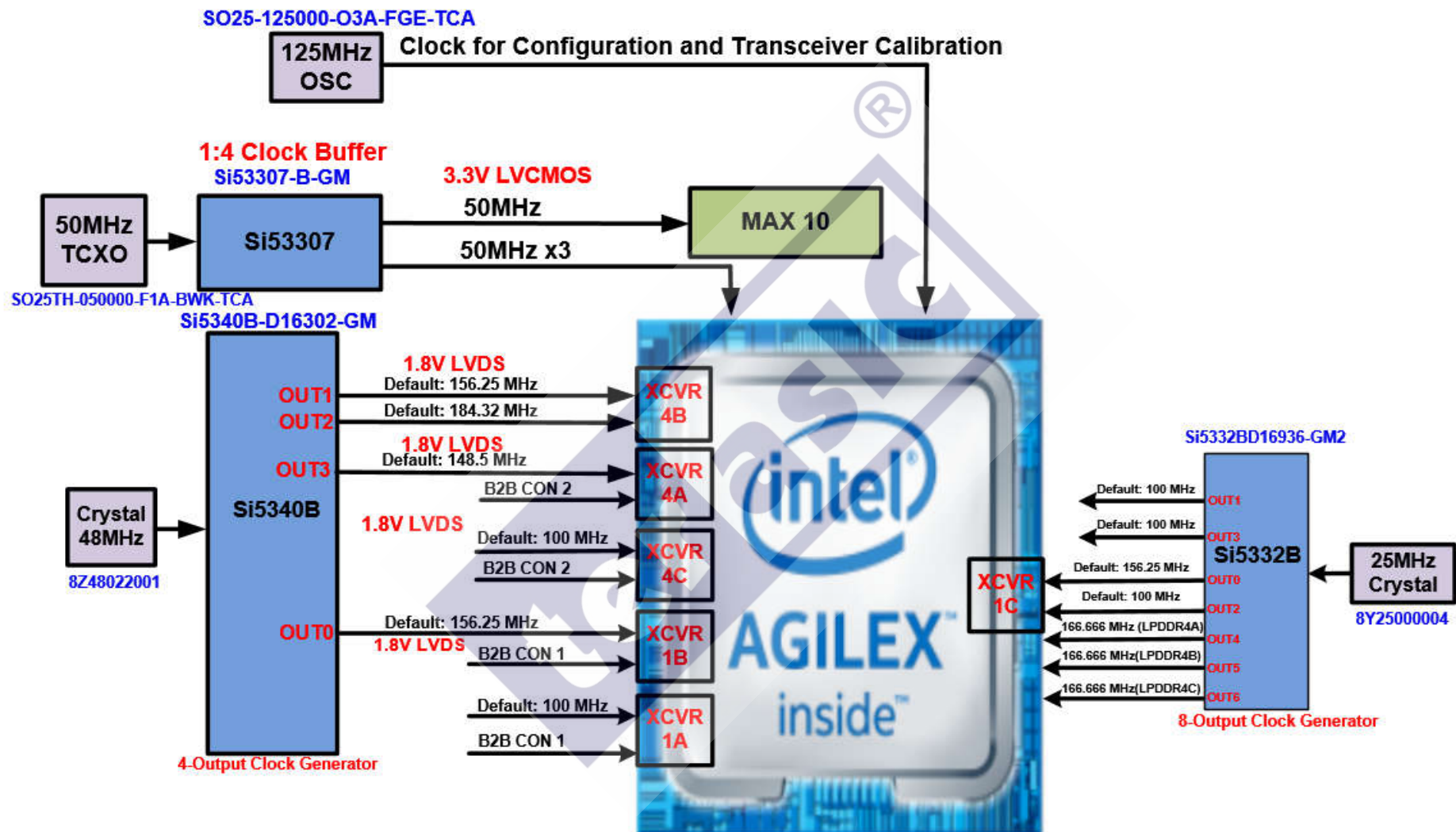


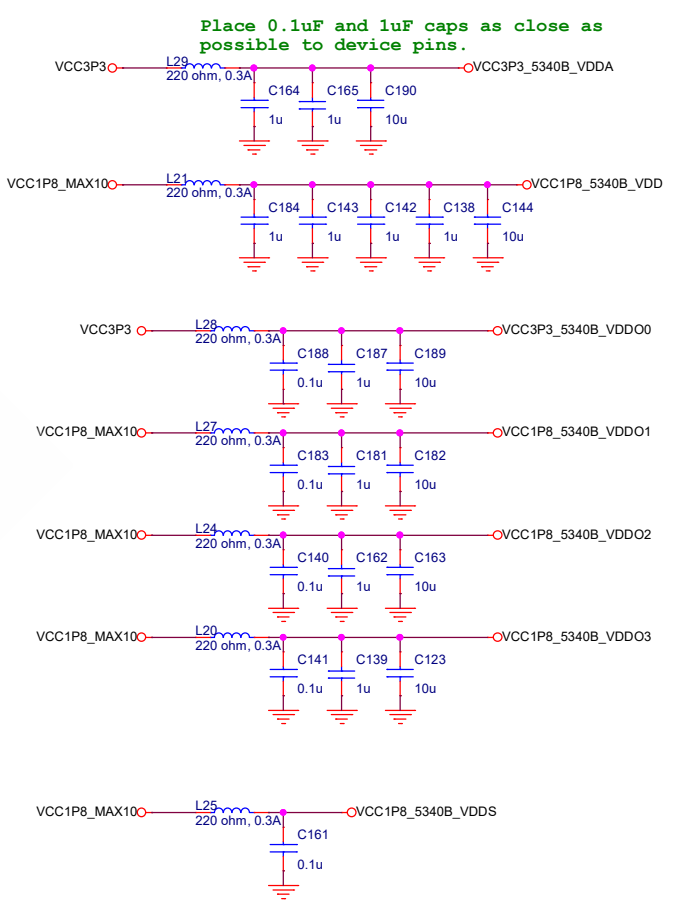
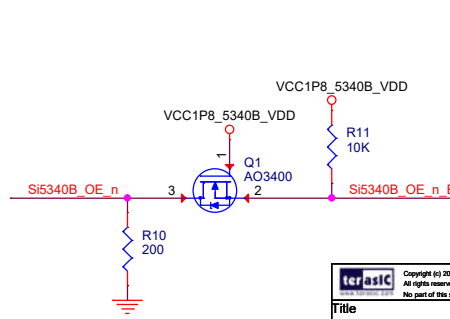
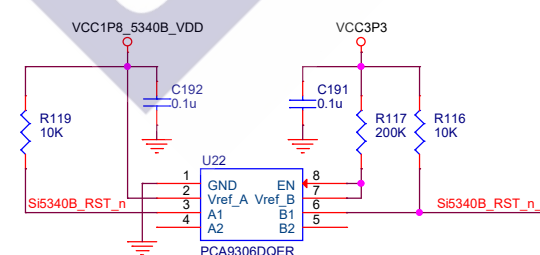
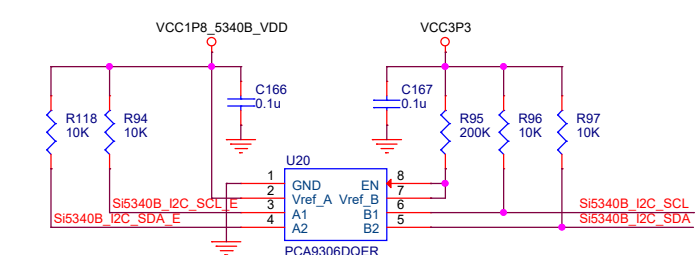
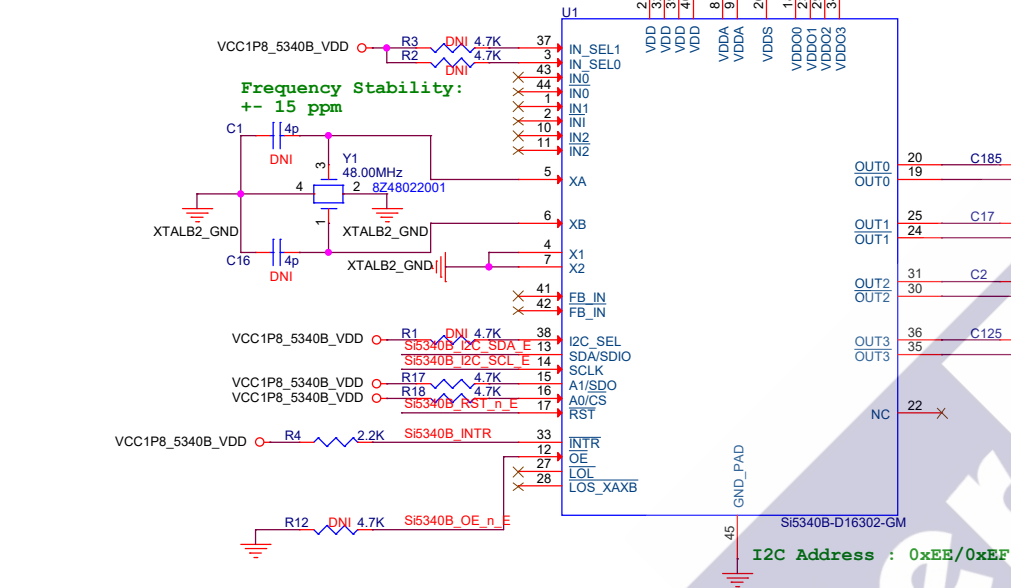
Block Diagram

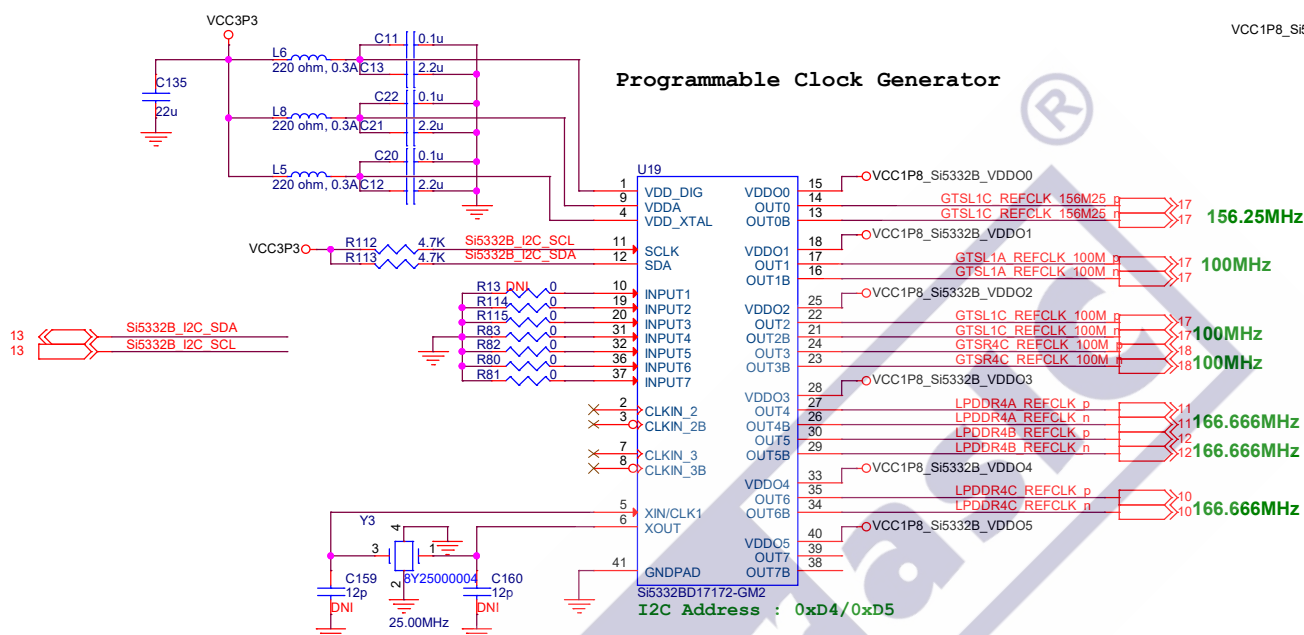


Clock Tree



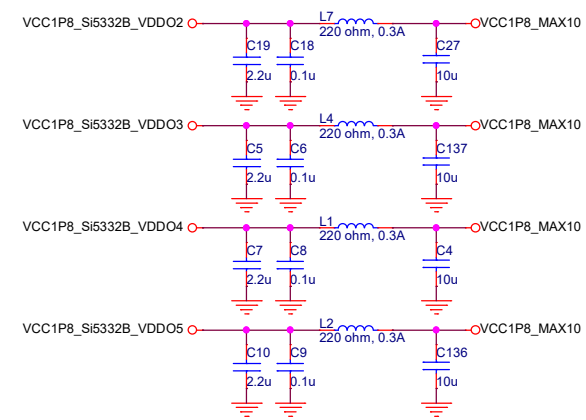
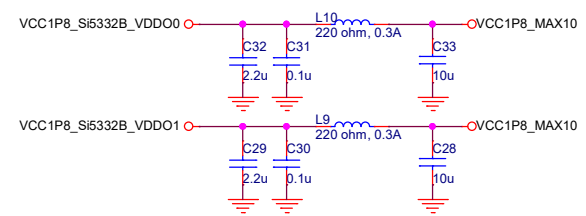
Si5340B I2C_SDA 13
Si5340B I2C_SCL 13
Si5340B RST_n 13
Si5340B OE_n 13





VDD core voltages (VDD_DIG, VDDA, VDD_XTAL) must be 3.3 V for in-circuit programming.
 Using VDD core voltage lower than 3.3V (i.e., 2.5 V or 1.8 V) will not support reliable in-circuit NVM programming.

FPGA Speed Grade	LPDDR4 REFCLK (MHz)	Data Rate (Mbps)
-4S	166.666	2666



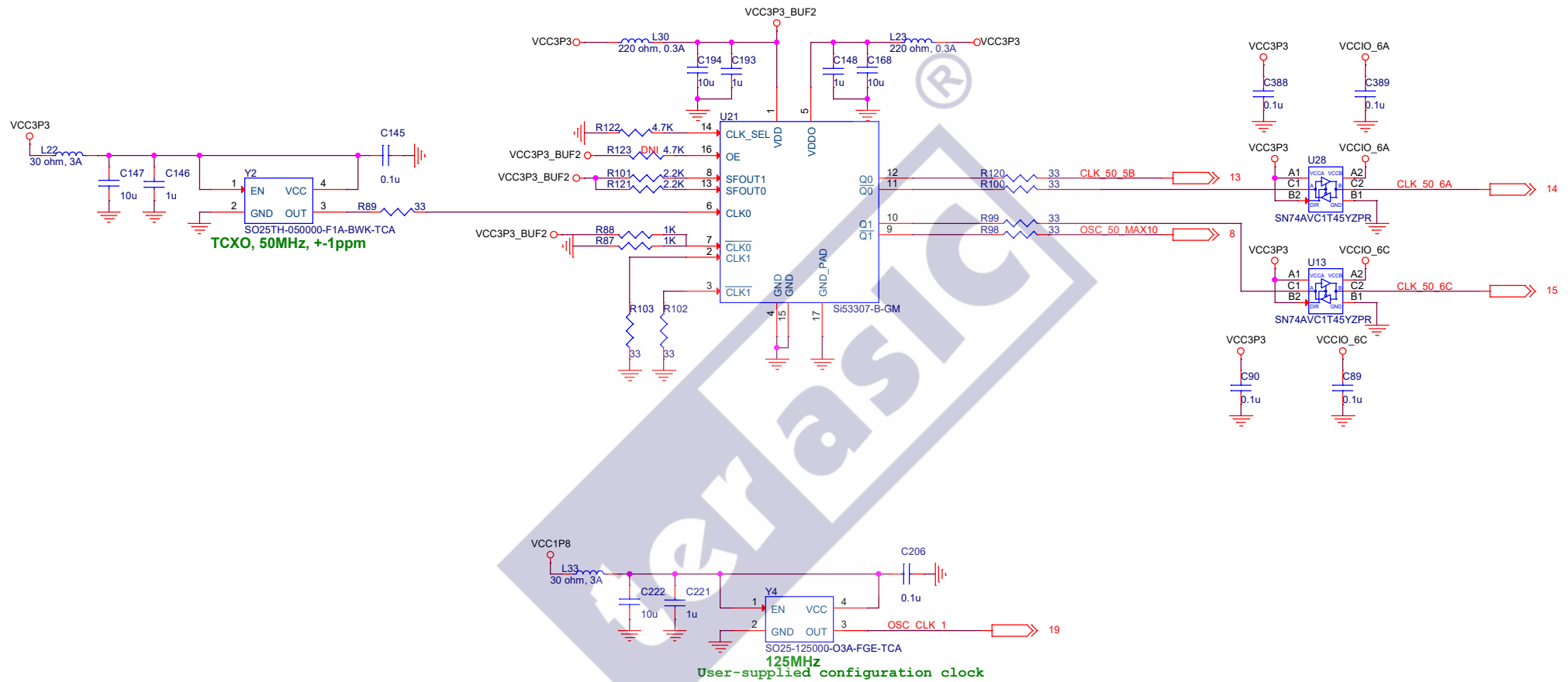
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Title

Comet A65 SOM

Size B Document Number Programmable Clock 2 Rev B

Date: Tuesday, September 30, 2025 Sheet 5 of 39



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Title		
Comet A65 SOM		
Size	Document Number	Rev
B	Clocks from Oscillators	B
Date:	Tuesday, September 30, 2025	Sheet 6 of 39

FPGA Temperature Control and Monitor (by System MAX)

TEMP I2C_SCL 32
TEMP I2C_SDA 32 3.3V

FPGA/MAX 10 SPI

INFO_SPI_SCLK 13
INFO_SPI_CS_n 13
INFO_SPI_MOSI 13
INFO_SPI_MISO 13

VCCIO_6A_PG 31
VCCIO_6B_PG 31
VCCIO_6C_PG 31
VCCIO_6D_PG 31
VCCIO_2A_PG 30
VCCIO_2A_PG 30
VCCIO_5A_PG 30

MAX 10 JTAG Interface

MAX10_JTAG_TCK 30
MAX10_JTAG_TMS 30
MAX10_JTAG_TDI 30
MAX10_JTAG_TDO 30

PM_I2C_SCL 35
PM_I2C_SDA 35
PM_ALERT_N 35

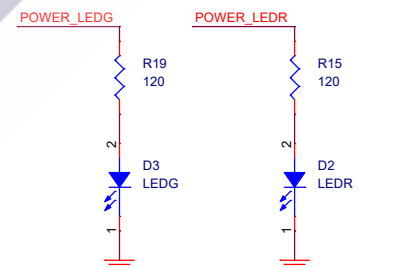
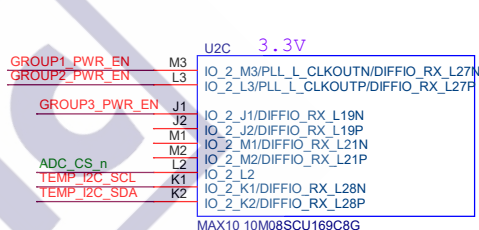
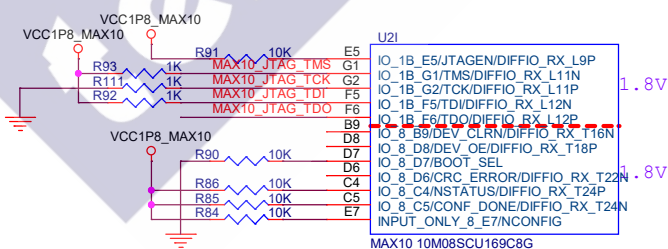
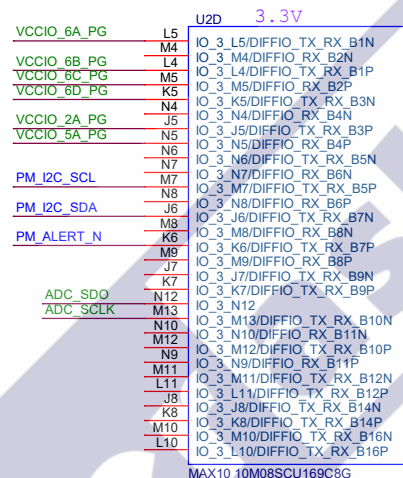
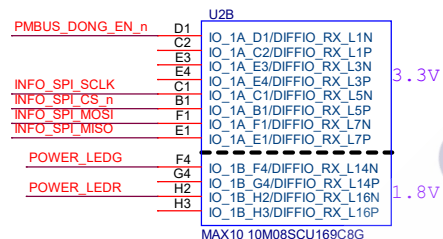
FPGA Power Enable Signal

GROUP1_PWR_EN 36,37,38
GROUP2_PWR_EN 30,38
GROUP3_PWR_EN 31,36,39

ADC

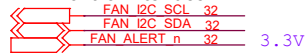
ADC_CS_n 35
ADC_SDO 35
ADC_SCLK 35

BMC MAX 10

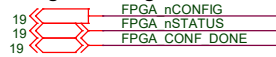


Place this LED on the top edge of the board, don't be covered by cooler

FAN Control Interface



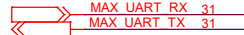
Agilex Configuration Setting



50MHz CLK



MAX 10 UART to USB



MAX10_RES0 31

AS_RST_n 19,28

MAX_MPQ8650_SCL 37
MAX_MPQ8650_SDA 37

HPS Reset

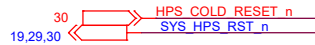
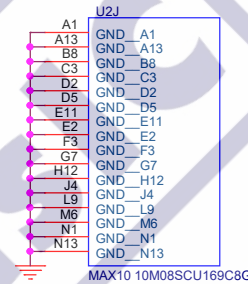
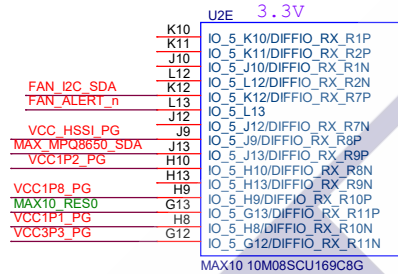
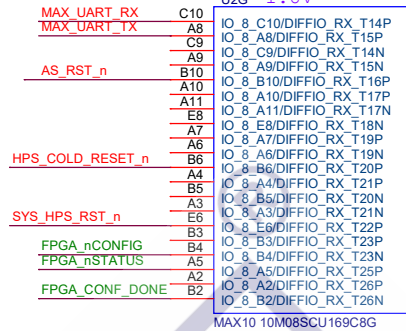
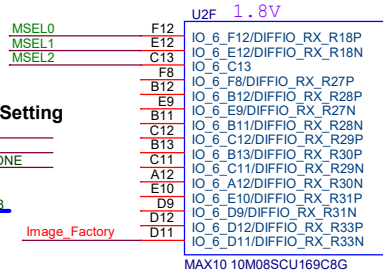
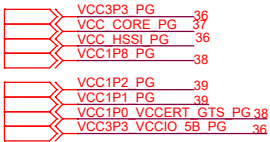


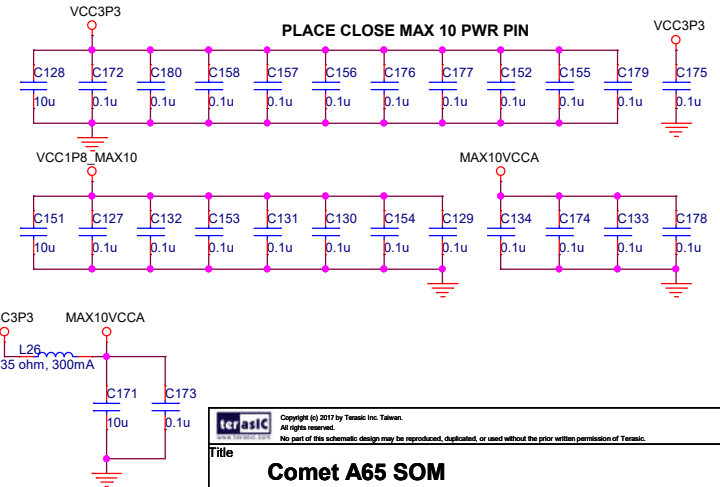
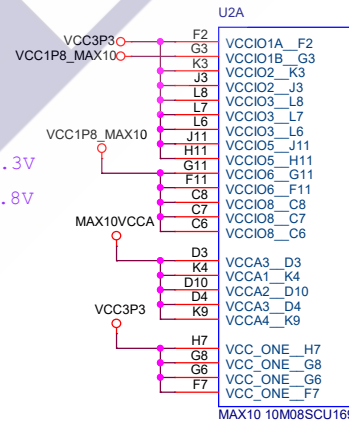
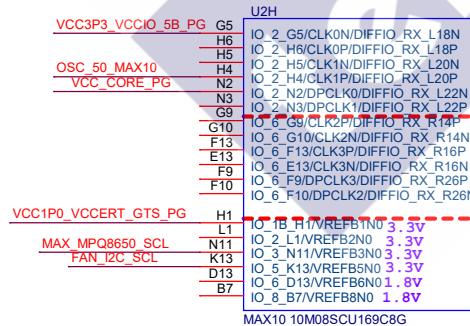
Image Factory

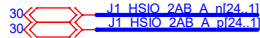
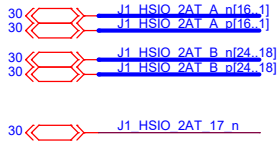


Power Good Signals



MAX 10 instant mode has power ramp up requirement





U10C

VCCIO = VCCIO_2A

BANK 2AT

BANK 2AB

J1 HSIO 2AT A n1 CH59
J1 HSIO 2AT A p1 CF59
J1 HSIO 2AT A n2 CH62
J1 HSIO 2AT A p2 CF62
J1 HSIO 2AT A n3 CC62
J1 HSIO 2AT A p3 CA62
J1 HSIO 2AT A n4 CF69
J1 HSIO 2AT A p4 CH69
J1 HSIO 2AT A n5 CA71
J1 HSIO 2AT A p5 CC71
J1 HSIO 2AT A n6 CH71
J1 HSIO 2AT A p6 CF71
J1 HSIO 2AT A n7 CA59
J1 HSIO 2AT A p7 BW59
J1 HSIO 2AT A n8 BR59
J1 HSIO 2AT A p8 BU59
J1 HSIO 2AT A n9 BR62
J1 HSIO 2AT A p9 BU62
J1 HSIO 2AT A n10 CA69
J1 HSIO 2AT A p10 BW69
J1 HSIO 2AT A n11 BU71
J1 HSIO 2AT A p11 BR71
J1 HSIO 2AT A n12 BU69
J1 HSIO 2AT A p12 BR69
J1 HSIO 2AT A n13 BK59
J1 HSIO 2AT A p13 BM59
J1 HSIO 2AT A n14 BH59
J1 HSIO 2AT A p14 BH62
J1 HSIO 2AT A n15 BP62
J1 HSIO 2AT A p15 BM62
J1 HSIO 2AT A n16 BK69
J1 HSIO 2AT A p16 BM69
J1 HSIO 2AT 17 n BH71
RZQ_B_2A_T BH69
J1 HSIO 2AT B n18 BP71
J1 HSIO 2AT B p18 BM71
J1 HSIO 2AT B n19 BF72
J1 HSIO 2AT B p19 BF75
J1 HSIO 2AT B n20 BE75
J1 HSIO 2AT B p20 BE79
J1 HSIO 2AT B n21 BF83
J1 HSIO 2AT B p21 BE83
J1 HSIO 2AT B n22 BE86
J1 HSIO 2AT B p22 BF86
J1 HSIO 2AT B n23 BF90
J1 HSIO 2AT B p23 BF93
J1 HSIO 2AT B n24 BE93
J1 HSIO 2AT B p24 BE96

IOB, DIFF_IO_2A_T1N, DQ0
IOB, DIFF_IO_2A_T1P, DQ0
IOB, DIFF_IO_2A_T2N, DQ0
IOB, DIFF_IO_2A_T2P, DQ0
IOB, DIFF_IO_2A_T3N, DQ0
IOB, DIFF_IO_2A_T3P, DQ0
IOB, DIFF_IO_2A_T4N, DQS0
IOB, DIFF_IO_2A_T4P, DQS0
IOB, CDR, DIFF_IO_2A_T5N, DQ0
IOB, CDR, DIFF_IO_2A_T5P, DQ0
IOB, DIFF_IO_2A_T6N, DQ0
IOB, DIFF_IO_2A_T6P, DQ0
IOB, DIFF_IO_2A_T7N, DQ1
IOB, DIFF_IO_2A_T7P, DQ1
IOB, DIFF_IO_2A_T8N, DQ1
IOB, DIFF_IO_2A_T8P, DQ1
IOB, DIFF_IO_2A_T9N, DQ1
IOB, DIFF_IO_2A_T9P, DQ1
IOB, DIFF_IO_2A_T10N, DQS0
IOB, DIFF_IO_2A_T10P, DQS1
IOB, CDR, DIFF_IO_2A_T11N, DQ1
IOB, CDR, DIFF_IO_2A_T11P, DQ1
IOB, DIFF_IO_2A_T12N, DQ1
IOB, DIFF_IO_2A_T12P, DQ1
IOB, DIFF_IO_2A_T13N, DQ2
IOB, DIFF_IO_2A_T13P, DQ2
IOB, DIFF_IO_2A_T14N, DQ2
IOB, DIFF_IO_2A_T14P, DQ2
IOB, DIFF_IO_2A_T15N, DQ2
IOB, DIFF_IO_2A_T15P, DQ2
IOB, PLL_2A_T_CLKOUT1N, DIFF_IO_2A_T16N, DQSN2
IOB, PLL_2A_T_CLKOUT1P, PLL_2A_T_CLKOUT1, PLL_2A_T_FB1, DIFF_IO_2A_T16P, DQS2
IOB, CDR, DIFF_IO_2A_T17N, DQ2
IOB, RZQ_T_2A, CDR, DIFF_IO_2A_T17P, DQ2
IOB, CLK_T_2A_1N, DIFF_IO_2A_T18N, DQ2
IOB, CLK_T_2A_1P, DIFF_IO_2A_T18P, DQ2
IOB, CLK_T_2A_0N, DIFF_IO_2A_T19N, DQ3
IOB, CLK_T_2A_0P, DIFF_IO_2A_T19P, DQ3
IOB, DIFF_IO_2A_T20P, DQ3
IOB, PLL_2A_T_CLKOUT0N, DIFF_IO_2A_T21N, DQ3
IOB, PLL_2A_T_CLKOUT0P, PLL_2A_T_CLKOUT0, PLL_2A_T_FB0, DIFF_IO_2A_T21P, DQ3
IOB, DIFF_IO_2A_T22N, DQSN3
IOB, DIFF_IO_2A_T22P, DQSN3
IOB, CDR, DIFF_IO_2A_T23N, DQ3
IOB, CDR, DIFF_IO_2A_T23P, DQ3
IOB, DIFF_IO_2A_T24N, DQ3
IOB, DIFF_IO_2A_T24P, DQ3

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

I/O Lane 3

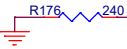
I/O Lane 2

I/O Lane 1

I/O Lane 0

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IOB, CDR, DIFF_IO_2A_B1P, DQ4
IOB, DIFF_IO_2A_B2N, DQ4
IOB, DIFF_IO_2A_B2P, DQ4
IOB, DIFF_IO_2A_B3N, DQ4
IOB, DIFF_IO_2A_B3P, DQ4
IOB, PLL_2A_B_CLKOUT1N, DIFF_IO_2A_B4N, DQSN4
IOB, PLL_2A_B_CLKOUT1P, PLL_2A_B_CLKOUT1, PLL_2A_B_FB1, DIFF_IO_2A_B4P, DQS4
IOB, CDR, DIFF_IO_2A_B5N, DQ4
IOB, RZQ_B_2A, CDR, DIFF_IO_2A_B5P, DQ4
IOB, CLK_B_2A_1N, DIFF_IO_2A_B6N, DQ4
IOB, CLK_B_2A_1P, DIFF_IO_2A_B6P, DQ4
IOB, CLK_B_2A_0N, CDR, DIFF_IO_2A_B7N, DQ5
IOB, CLK_B_2A_0P, CDR, DIFF_IO_2A_B7P, DQ5
IOB, DIFF_IO_2A_B8N, DQ5
IOB, DIFF_IO_2A_B8P, DQ5
IOB, PLL_2A_B_CLKOUT0N, DIFF_IO_2A_B9N, DQ5
IOB, PLL_2A_B_CLKOUT0P, PLL_2A_B_CLKOUT0, PLL_2A_B_FB0, DIFF_IO_2A_B9P, DQ5
IOB, DIFF_IO_2A_B10N, DQSN5
IOB, DIFF_IO_2A_B10P, DQSN5
IOB, CDR, DIFF_IO_2A_B11N, DQ5
IOB, CDR, DIFF_IO_2A_B11P, DQ5
IOB, DIFF_IO_2A_B12N, DQ5
IOB, DIFF_IO_2A_B12P, DQ5
IOB, CDR, DIFF_IO_2A_B13N, DQ6
IOB, CDR, DIFF_IO_2A_B13P, DQ6
IOB, DIFF_IO_2A_B14N, DQ6
IOB, DIFF_IO_2A_B14P, DQ6
IOB, DIFF_IO_2A_B15N, DQ6
IOB, DIFF_IO_2A_B15P, DQ6
IOB, DIFF_IO_2A_B16N, DQSN6
IOB, DIFF_IO_2A_B16P, DQSN6
IOB, CDR, DIFF_IO_2A_B17N, DQ6
IOB, CDR, DIFF_IO_2A_B17P, DQ6
IOB, DIFF_IO_2A_B18N, DQ6
IOB, DIFF_IO_2A_B18P, DQ6
IOB, CDR, DIFF_IO_2A_B19N, DQ7
IOB, CDR, DIFF_IO_2A_B19P, DQ7
IOB, DIFF_IO_2A_B20N, DQ7
IOB, DIFF_IO_2A_B20P, DQ7
IOB, DIFF_IO_2A_B21N, DQ7
IOB, DIFF_IO_2A_B21P, DQ7
IOB, DIFF_IO_2A_B22N, DQSN7
IOB, DIFF_IO_2A_B22P, DQSN7
IOB, CDR, DIFF_IO_2A_B23N, DQ7
IOB, CDR, DIFF_IO_2A_B23P, DQ7
IOB, DIFF_IO_2A_B24N, DQ7
IOB, DIFF_IO_2A_B24P, DQ7

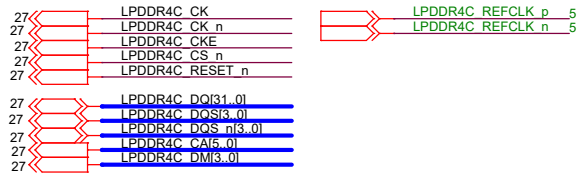
BK78 J1 HSIO 2AB A n1
BM78 J1 HSIO 2AB A p1
BH78 J1 HSIO 2AB A n2
BH81 J1 HSIO 2AB A p2
BP81 J1 HSIO 2AB A n3
BM81 J1 HSIO 2AB A p3
BK89 J1 HSIO 2AB A n4
BK89 J1 HSIO 2AB A p4
BH92 J1 HSIO 2AB A n5
BH89 J1 HSIO 2AB A p5
BM92 J1 HSIO 2AB A n6
BP92 J1 HSIO 2AB A p6
CA78 J1 HSIO 2AB A n7
BW78 J1 HSIO 2AB A p7
BU78 J1 HSIO 2AB A n8
BR78 J1 HSIO 2AB A p8
BU81 J1 HSIO 2AB A n9
BR81 J1 HSIO 2AB A p9
CA89 J1 HSIO 2AB A n10
BW89 J1 HSIO 2AB A p10
BU92 J1 HSIO 2AB A n11
BR92 J1 HSIO 2AB A p11
BU89 J1 HSIO 2AB A n12
BR89 J1 HSIO 2AB A p12
CF78 J1 HSIO 2AB A n13
CH78 J1 HSIO 2AB A p13
CC81 J1 HSIO 2AB A n14
CA81 J1 HSIO 2AB A p14
CH81 J1 HSIO 2AB A n15
CF81 J1 HSIO 2AB A p15
CF89 J1 HSIO 2AB A n16
CH89 J1 HSIO 2AB A p16
CH92 J1 HSIO 2AB A n17
CF92 J1 HSIO 2AB A p17
CA92 J1 HSIO 2AB A n18
CC92 J1 HSIO 2AB A p18
CL76 J1 HSIO 2AB A n19
CK76 J1 HSIO 2AB A p19
CL82 J1 HSIO 2AB A n20
CK80 J1 HSIO 2AB A p20
CL85 J1 HSIO 2AB A n21
CK85 J1 HSIO 2AB A p21
CK88 J1 HSIO 2AB A n22
CL88 J1 HSIO 2AB A p22
CL97 J1 HSIO 2AB A n23
CK97 J1 HSIO 2AB A p23
CK94 J1 HSIO 2AB A n24
CL91 J1 HSIO 2AB A p24



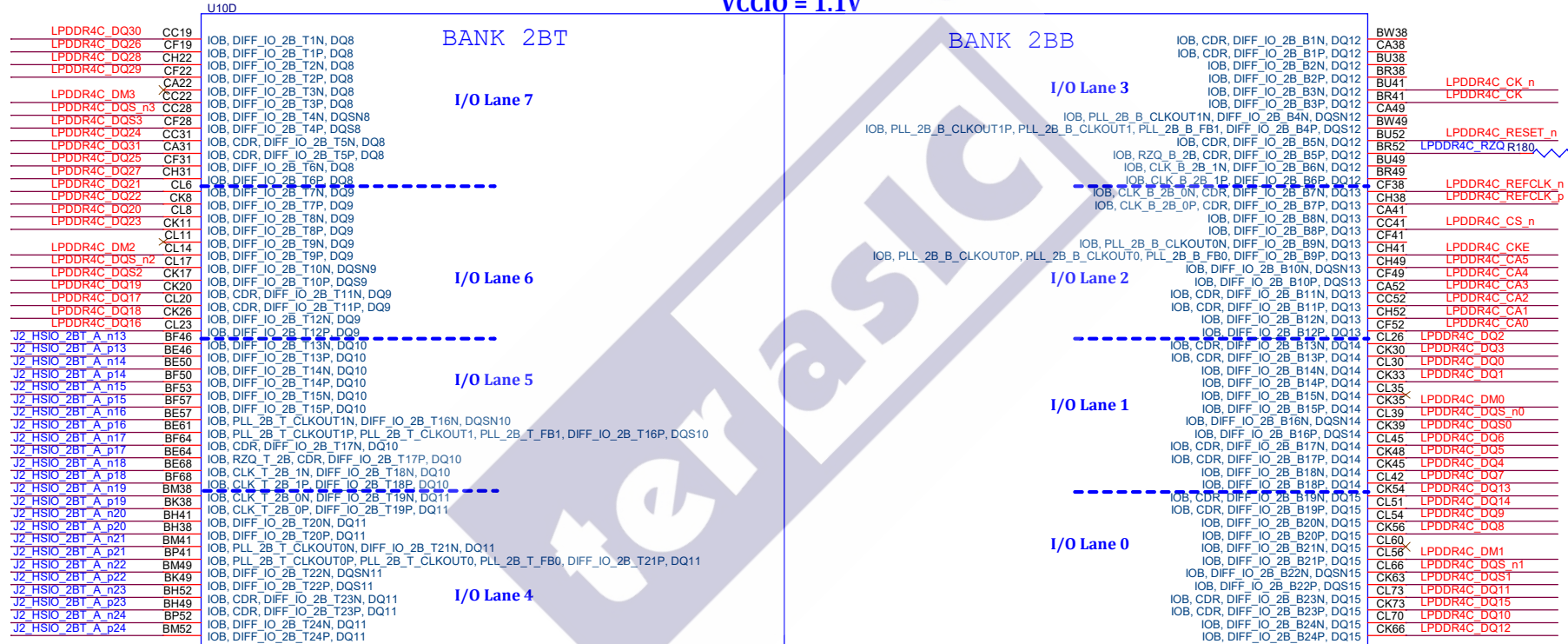
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terasic			Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title					
Comet A65 SOM					
Size	Document Number				Rev
B	FPGA Bank 2A				B
Date:	Tuesday, September 30, 2025				Sheet 9 of 39


LPDDR4C



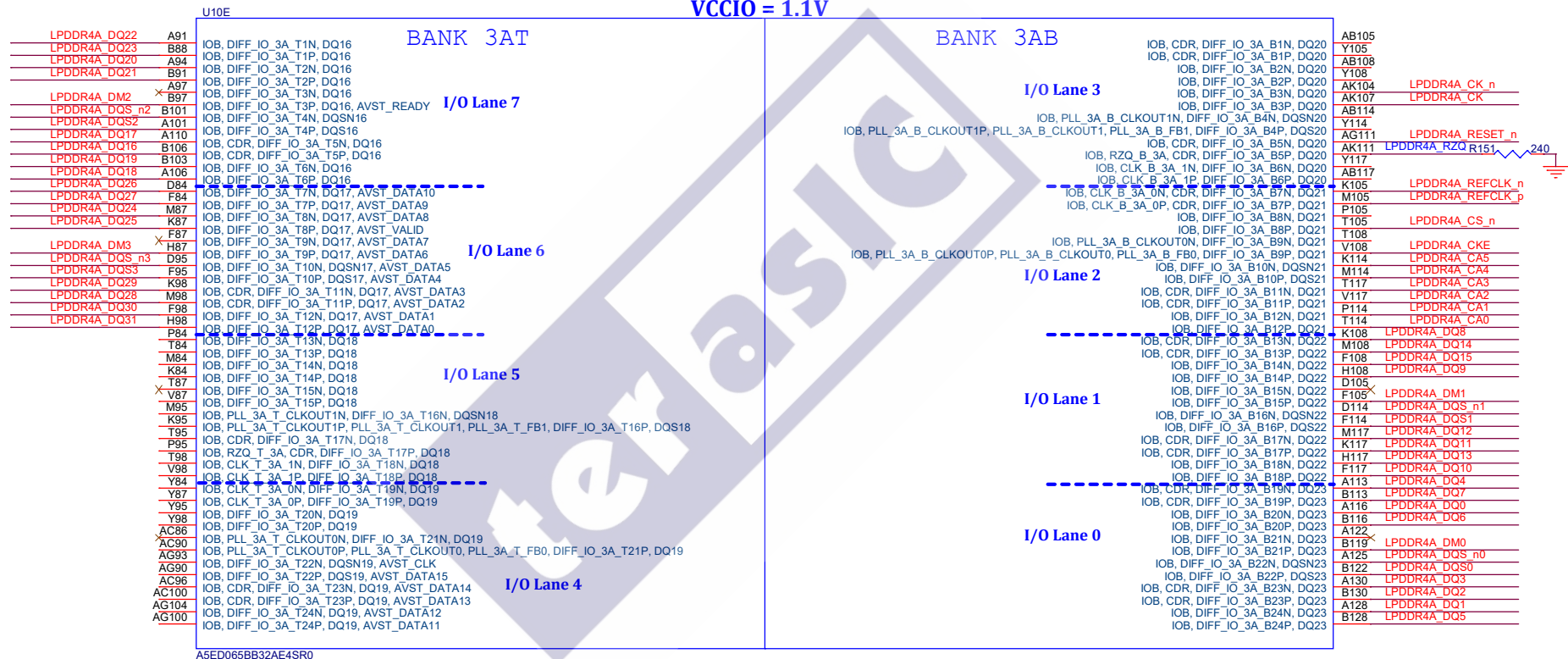
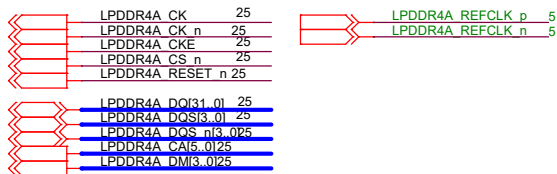
VCCIO = 1.1V



A5ED065BB32AE4SR0

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Title Comet A65 SOM		
Size B	Document Number FPGA Bank 2B	Rev B
Date:	Tuesday, September 30, 2025	Sheet 10 of 39

LPDDR4A



LPDDR4B

LPDDR4B CK 26
LPDDR4B CK_n 26
LPDDR4B CKE 26
LPDDR4B CS_n 26
LPDDR4B RESET_n 26

LPDDR4B_REFCLK_p_5
LPDDR4B_REFCLK_n_5

LPDDR4B_DQI31_01 26
LPDDR4B_DQS14_01 26
LPDDR4B_DQS_n13_026
LPDDR4B_CA16_026
LPDDR4B_DM13_026

J2_HSIO_3BT_A_n124_131
J2_HSIO_3BT_A_n124_131

VCCIO = 1.1V

LPDDR4B_DQ23 B42
LPDDR4B_DQ21 A45
LPDDR4B_DQ20 A48
LPDDR4B_DQ22 B45
LPDDR4B_DM2 B51
LPDDR4B_DQS_n2 B54
LPDDR4B_DQ2 A54
LPDDR4B_DQ18 B60
LPDDR4B_DQ17 A63
LPDDR4B_DQ16 A60
LPDDR4B_DQ19 B56
LPDDR4B_DQ25 F44
LPDDR4B_DQ26 D44
LPDDR4B_DQ24 H47
LPDDR4B_DQ27 F47
LPDDR4B_DM3 M47
LPDDR4B_DQS_n3 D55
LPDDR4B_DQS3 F55
LPDDR4B_DQ28 K58
LPDDR4B_DQ29 M58
LPDDR4B_DQ30 F58
LPDDR4B_DQ31 H58
J2_HSIO_3BT_A_n13 M44
J2_HSIO_3BT_A_p13 K44
J2_HSIO_3BT_A_n14 T44
J2_HSIO_3BT_A_p14 P44
J2_HSIO_3BT_A_n15 T47
J2_HSIO_3BT_A_p15 V47
J2_HSIO_3BT_A_n16 M55
J2_HSIO_3BT_A_p16 K55
J2_HSIO_3BT_A_n17 T58
J2_HSIO_3BT_A_p17 V58
J2_HSIO_3BT_A_n18 T55
J2_HSIO_3BT_A_p18 P55
J2_HSIO_3BT_A_n19 Y47
J2_HSIO_3BT_A_p19 Y44
J2_HSIO_3BT_A_n20 Y55
J2_HSIO_3BT_A_p20 Y58
J2_HSIO_3BT_A_n21 AC50
J2_HSIO_3BT_A_p21 AC53
J2_HSIO_3BT_A_n22 AG53
J2_HSIO_3BT_A_p22 AG57
J2_HSIO_3BT_A_n23 AC61
J2_HSIO_3BT_A_p23 AG61
J2_HSIO_3BT_A_n24 AG64
J2_HSIO_3BT_A_p24 AC64

U10F

BANK 3BT

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

BANK 3BB

I/O Lane 3

I/O Lane 2


I/O Lane 1

I/O Lane 0

IOB_CDR_DIFF_IO_3B_B1N, DQ28
IOB_CDR_DIFF_IO_3B_B1P, DQ28
IOB_DIFF_IO_3B_B2N, DQ28
IOB_DIFF_IO_3B_B2P, DQ28
IOB_DIFF_IO_3B_B3N, DQ28
IOB_DIFF_IO_3B_B3P, DQ28
IOB_PLL_3B_B_CLKOUT1N, DIFF_IO_3B_B4N, DQSN28
IOB_PLL_3B_B_CLKOUT1P, PLL_3B_B_FB1, DIFF_IO_3B_B4P, DQSN28
IOB_CDR_DIFF_IO_3B_B5N, DQ28
IOB_RZQ_B_3B, CDR_DIFF_IO_3B_B5P, DQ28
IOB_CLK_B_3B_1N, DIFF_IO_3B_B6N, DQ28
IOB_CLK_B_3B_1P, DIFF_IO_3B_B6P, DQ28
IOB_CLK_B_3B_0N, CDR_DIFF_IO_3B_B7N, DQ29
IOB_CLK_B_3B_0P, CDR_DIFF_IO_3B_B7P, DQ29
IOB_DIFF_IO_3B_B8N, DQ29
IOB_DIFF_IO_3B_B8P, DQ29
IOB_PLL_3B_B_CLKOUT0N, DIFF_IO_3B_B9N, DQ29
IOB_PLL_3B_B_CLKOUT0P, PLL_3B_B_FB0, DIFF_IO_3B_B9P, DQ29
IOB_DIFF_IO_3B_B10N, DQSN29
IOB_DIFF_IO_3B_B10P, DQSN29
IOB_CDR_DIFF_IO_3B_B11N, DQ29
IOB_CDR_DIFF_IO_3B_B11P, DQ29
IOB_DIFF_IO_3B_B12N, DQ29
IOB_DIFF_IO_3B_B12P, DQ29
IOB_CDR_DIFF_IO_3B_B13N, DQ30
IOB_CDR_DIFF_IO_3B_B13P, DQ30
IOB_DIFF_IO_3B_B14N, DQ30
IOB_DIFF_IO_3B_B14P, DQ30
IOB_DIFF_IO_3B_B15N, DQ30
IOB_DIFF_IO_3B_B15P, DQ30
IOB_DIFF_IO_3B_B16N, DQSN30
IOB_DIFF_IO_3B_B16P, DQSN30
IOB_CDR_DIFF_IO_3B_B17N, DQ30
IOB_CDR_DIFF_IO_3B_B17P, DQ30
IOB_DIFF_IO_3B_B18N, DQ30
IOB_DIFF_IO_3B_B18P, DQ30
IOB_CDR_DIFF_IO_3B_B19N, DQ31
IOB_CDR_DIFF_IO_3B_B19P, DQ31
IOB_DIFF_IO_3B_B20N, DQ31
IOB_DIFF_IO_3B_B20P, DQ31
IOB_DIFF_IO_3B_B21N, DQ31
IOB_DIFF_IO_3B_B21P, DQ31
IOB_DIFF_IO_3B_B22N, DQSN31
IOB_DIFF_IO_3B_B22P, DQSN31
IOB_CDR_DIFF_IO_3B_B23N, DQ31
IOB_CDR_DIFF_IO_3B_B23P, DQ31
IOB_DIFF_IO_3B_B24N, DQ31
IOB_DIFF_IO_3B_B24P, DQ31

Y65
Y67
Y74
Y77
AC83 LPDDR4B_CK_n
AG83 LPDDR4B_CK
AG75
AG72 LPDDR4B_RESET_n
AG79 LPDDR4B_RZQ R172 240
AC68
P65 LPDDR4B_REFCLK_n
T65 LPDDR4B_REFCLK_p
K65
M65 LPDDR4B_CS_n
V67 LPDDR4B_CKE
K74 LPDDR4B_CA5
M74 LPDDR4B_CA4
T77 LPDDR4B_CA3
V77 LPDDR4B_CA2
T74 LPDDR4B_CA1
P74 LPDDR4B_CA0
D65 LPDDR4B_DQ15
F65 LPDDR4B_DQ9
F67 LPDDR4B_DQ14
H67 LPDDR4B_DQ8
K67 LPDDR4B_DM1
M67 LPDDR4B_DQS_n1
D74 LPDDR4B_DQS1
H77 LPDDR4B_DQ10
F77 LPDDR4B_DQ13
M77 LPDDR4B_DQ11
K77 LPDDR4B_DQ12
A66 LPDDR4B_DQ5
B66 LPDDR4B_DQ7
A70 LPDDR4B_DQ0
B70 LPDDR4B_DQ6
A76
B73 LPDDR4B_DM0
B76 LPDDR4B_DQS_n0
A80 LPDDR4B_DQS0
A85 LPDDR4B_DQ3
B85 LPDDR4B_DQ4
B82 LPDDR4B_DQ1
A82 LPDDR4B_DQ2

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Title		
Comet A65 SOM		
Size	Document Number	Rev
B	FPGA Bank 3B	B
Date:	Tuesday, September 30, 2025	Sheet 12 of 39

B2B Connector J1 Interface

30 J1 HVIO 5A A120_11

6 CLK 50 5B

33 LED

33 BUTTON

19 SD MMC SEL

B2B Connector J1 Interface

30 J1 HVIO 5B A17_41

5 SI5332B I2C_SDA
5 SI5332B I2C_SCL

4 SI5340B I2C_SDA
4 SI5340B I2C_SCL
4 SI5340B RST_n
4 SI5340B OE_n

FPGA/System MAX SPI

INFO SPI SCLK 7
INFO SPI CS_n 7
INFO SPI MOSI 7
INFO SPI MISO 7

U10G

J1 HVIO 5A A1	CD134
J1 HVIO 5A A2	CD135
J1 HVIO 5A A3	CG134
J1 HVIO 5A A4	CG135
J1 HVIO 5A A5	CH132
J1 HVIO 5A A6	CF132
J1 HVIO 5A A7	CF128
J1 HVIO 5A A8	CK134
J1 HVIO 5A A9	CH128
J1 HVIO 5A A10	CL125
J1 HVIO 5A A11	CF121
J1 HVIO 5A A12	CF118
J1 HVIO 5A A13	BU118
J1 HVIO 5A A14	BR118
J1 HVIO 5A A15	CA118
J1 HVIO 5A A16	BW118
J1 HVIO 5A A17	CL128
J1 HVIO 5A A18	CL130
J1 HVIO 5A A19	CK125
J1 HVIO 5A A20	CK128

VCCIO = VCCIO_5A	
HVIO_5A_1, SYSPLLREFCLK_L1A_0, TXCLK1, DATA_CTRL1	
HVIO_5A_2, SYSPLLREFCLK_L1A_1, TXCLK2, DATA_CTRL2	
HVIO_5A_3, SYSPLLREFCLK_L1B_0, TXCLK3, DATA_CTRL3	
HVIO_5A_4, SYSPLLREFCLK_L1B_1, TXCLK4, DATA_CTRL4	
HVIO_5A_5, PIN_PERST_N_CVP_L1A_0, TXCLK5, DATA_CTRL5	
HVIO_5A_6, PIN_PERST_N_CVP_L1B_0, TXCLK6, DATA_CTRL6	
HVIO_5A_7, PIN_PERST_N_CVP_L1C_0, TXCLK7, DATA_CTRL7	
HVIO_5A_8, TXCLK8, DATA_CTRL8	
HVIO_5A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9	
HVIO_5A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10	
HVIO_5A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11	
HVIO_5A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12	
HVIO_5A_13, TXCLK13, DATA_CTRL13	
HVIO_5A_14, TXCLK14, DATA_CTRL14	
HVIO_5A_15, TXCLK15, DATA_CTRL15	
HVIO_5A_16, TXCLK16, DATA_CTRL16	
HVIO_5A_17, TXCLK17, DATA_CTRL17	
HVIO_5A_18, TXCLK18, DATA_CTRL18	
HVIO_5A_19, SYSPLLREFCLK_L1C_0, TXCLK19, DATA_CTRL19	
HVIO_5A_20, TXCLK20, DATA_CTRL20	

BANK 5A

VCCIO = 3.3V

HVIO_5B_1, SYSPLLREFCLK_L1A_2, TXCLK1, DATA_CTRL1	
HVIO_5B_2, SYSPLLREFCLK_L1A_3, TXCLK2, DATA_CTRL2	
HVIO_5B_3, SYSPLLREFCLK_L1B_2, TXCLK3, DATA_CTRL3	
HVIO_5B_4, SYSPLLREFCLK_L1B_3, TXCLK4, DATA_CTRL4	
HVIO_5B_5, PIN_PERST_N_CVP_L1A_1, TXCLK5, DATA_CTRL5	
HVIO_5B_6, PIN_PERST_N_CVP_L1B_1, TXCLK6, DATA_CTRL6	
HVIO_5B_7, PIN_PERST_N_CVP_L1C_1, TXCLK7, DATA_CTRL7	
HVIO_5B_8, TXCLK8, DATA_CTRL8	
HVIO_5B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9	
HVIO_5B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10	
HVIO_5B_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11	
HVIO_5B_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12	
HVIO_5B_13, TXCLK13, DATA_CTRL13	
HVIO_5B_14, TXCLK14, DATA_CTRL14	
HVIO_5B_15, TXCLK15, DATA_CTRL15	
HVIO_5B_16, TXCLK16, DATA_CTRL16	
HVIO_5B_17, TXCLK17, DATA_CTRL17	
HVIO_5B_18, TXCLK18, DATA_CTRL18	
HVIO_5B_19, SYSPLLREFCLK_L1C_1, TXCLK19, DATA_CTRL19	
HVIO_5B_20, TXCLK20, DATA_CTRL20	

BANK 5B

BF111	INFO SPI SCLK
BH109	INFO SPI CS_n
BE115	INFO SPI MOSI
BF115	J1 HVIO 5B A4
BF107	J1 HVIO 5B A5
BU109	J1 HVIO 5B A6
BF104	J1 HVIO 5B A7
BR109	INFO SPI MISO
BE107	CLK 50 5B
BK109	SI5340B I2C_SDA
BE111	SI5340B I2C_SCL
BM109	SI5340B RST_n
BR112	SI5340B OE_n
BK118	SD MMC SEL
BM118	SI5332B I2C_SDA
BP112	SI5332B I2C_SCL
BM112	
BK112	BUTTON
BH118	
BF120	LED

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Title

Comet A65 SOM

Size B

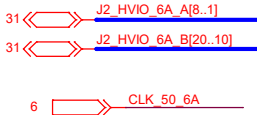
Document Number
FPGA Bank 5A - 5B

Rev B

Date: Tuesday, September 30, 2025

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B2B Connector J2 Interface




B2B Connector J2 Interface

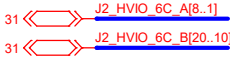


U10H		VCCIO = VCCIO_6A		VCCIO = VCCIO_6B			
J2 HVIO_6A_A1	BU28	HVIO_6A_1, SYSPLLREFCLK_R4A_0, TXCLK1, DATA_CTRL1		HVIO_6B_1, SYSPLLREFCLK_R4A_2, TXCLK1, DATA_CTRL1		BF21	J2 HVIO_6B_A1
J2 HVIO_6A_A2	BP31	HVIO_6A_2, SYSPLLREFCLK_R4A_1, TXCLK2, DATA_CTRL2		HVIO_6B_2, SYSPLLREFCLK_R4A_3, TXCLK2, DATA_CTRL2		BE21	J2 HVIO_6B_A2
J2 HVIO_6A_A3	BR28	HVIO_6A_3, SYSPLLREFCLK_R4B_0, TXCLK3, DATA_CTRL3		HVIO_6B_3, SYSPLLREFCLK_R4B_2, TXCLK3, DATA_CTRL3		BE43	J2 HVIO_6B_A3
J2 HVIO_6A_A4	BR31	HVIO_6A_4, SYSPLLREFCLK_R4B_1, TXCLK4, DATA_CTRL4		HVIO_6B_4, SYSPLLREFCLK_R4B_3, TXCLK4, DATA_CTRL4		BF40	J2 HVIO_6B_A4
J2 HVIO_6A_A5	BU31	HVIO_6A_5, PIN_PERST_N_R4A_0, TXCLK5, DATA_CTRL5		HVIO_6B_5, PIN_PERST_N_R4A_1, TXCLK5, DATA_CTRL5		BE29	J2 HVIO_6B_A5
J2 HVIO_6A_A6	BM28	HVIO_6A_6, PIN_PERST_N_R4B_0, TXCLK6, DATA_CTRL6		HVIO_6B_6, PIN_PERST_N_R4B_1, TXCLK6, DATA_CTRL6		BE25	J2 HVIO_6B_A6
J2 HVIO_6A_A7	BW28	HVIO_6A_7, PIN_PERST_N_R4C_0, TXCLK7, DATA_CTRL7		HVIO_6B_7, PIN_PERST_N_R4C_1, TXCLK7, DATA_CTRL7		BF32	J2 HVIO_6B_A7
J2 HVIO_6A_A8	BM31	HVIO_6A_8, TXCLK8, DATA_CTRL8		HVIO_6B_8, TXCLK8, DATA_CTRL8		BF36	J2 HVIO_6B_A8
CLK_50_6A	BK31	HVIO_6A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9		HVIO_6B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9		BF29	J2 HVIO_6B_A9
J2 HVIO_6A_B10	BP22	HVIO_6A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10		HVIO_6B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10		BF25	J2 HVIO_6B_A10
J2 HVIO_6A_B11	BK28	HVIO_6A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11		HVIO_6B_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11		BF16	J2 HVIO_6B_A11
J2 HVIO_6A_B12	BR22	HVIO_6A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12		HVIO_6B_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12		BH19	J2 HVIO_6B_A12
J2 HVIO_6A_B13	CH12	HVIO_6A_13, TXCLK13, DATA_CTRL13		HVIO_6B_13, TXCLK13, DATA_CTRL13		BK22	J2 HVIO_6B_A13
J2 HVIO_6A_B14	BU22	HVIO_6A_14, TXCLK14, DATA_CTRL14		HVIO_6B_14, TXCLK14, DATA_CTRL14		BM19	J2 HVIO_6B_A14
J2 HVIO_6A_B15	BW19	HVIO_6A_15, TXCLK15, DATA_CTRL15		HVIO_6B_15, TXCLK15, DATA_CTRL15		BU19	J2 HVIO_6B_A15
J2 HVIO_6A_B16	BH28	HVIO_6A_16, TXCLK16, DATA_CTRL16		HVIO_6B_16, TXCLK16, DATA_CTRL16		BR19	J2 HVIO_6B_A16
J2 HVIO_6A_B17	BM22	HVIO_6A_17, TXCLK17, DATA_CTRL17		HVIO_6B_17, TXCLK17, DATA_CTRL17		CK2	J2 HVIO_6B_A17
J2 HVIO_6A_B18	CF12	HVIO_6A_18, TXCLK18, DATA_CTRL18		HVIO_6B_18, TXCLK18, DATA_CTRL18		CJ2	J2 HVIO_6B_A18
J2 HVIO_6A_B19	BK19	HVIO_6A_19, SYSPLLREFCLK_R4C_0, TXCLK19, DATA_CTRL19		HVIO_6B_19, SYSPLLREFCLK_R4C_1, TXCLK19, DATA_CTRL19		CK4	J2 HVIO_6B_A19
J2 HVIO_6A_B20	CF9	HVIO_6A_20, TXCLK20, DATA_CTRL20		HVIO_6B_20, TXCLK20, DATA_CTRL20		CH4	J2 HVIO_6B_A20

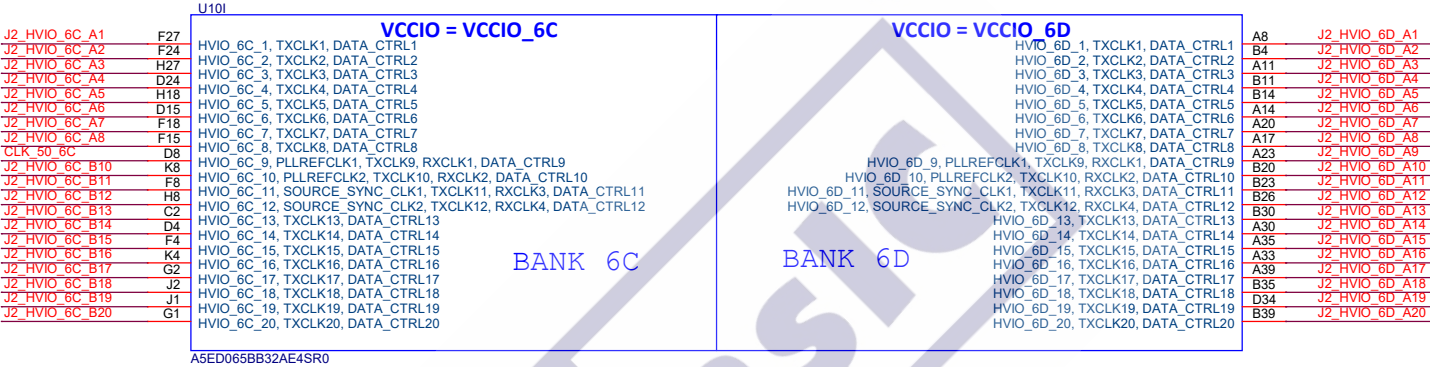
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Title	
Comet A65 SOM	
Size	Document Number
B	FPGA Bank 6A - 6B
Date:	Tuesday, September 30, 2025
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Rev	B

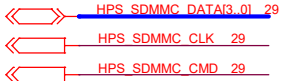
B2B Connector J2 Interface



B2B Connector J2 Interface



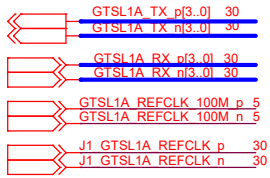
SD/eMMC Interface



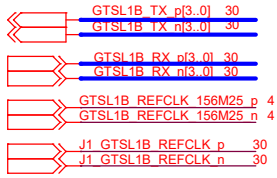
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Title			
Comet A65 SOM			
Size	Document Number		Rev
B	FPGA Bank HPS		B
Date:	Tuesday, September 30, 2025		Sheet 16 of 39

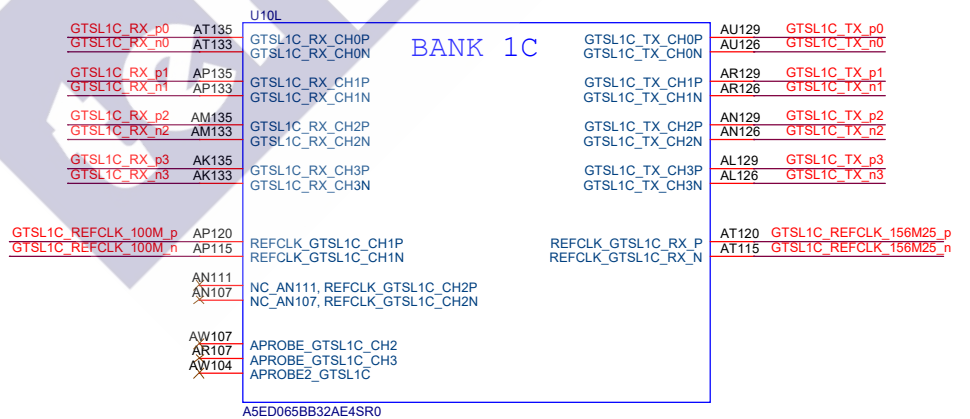
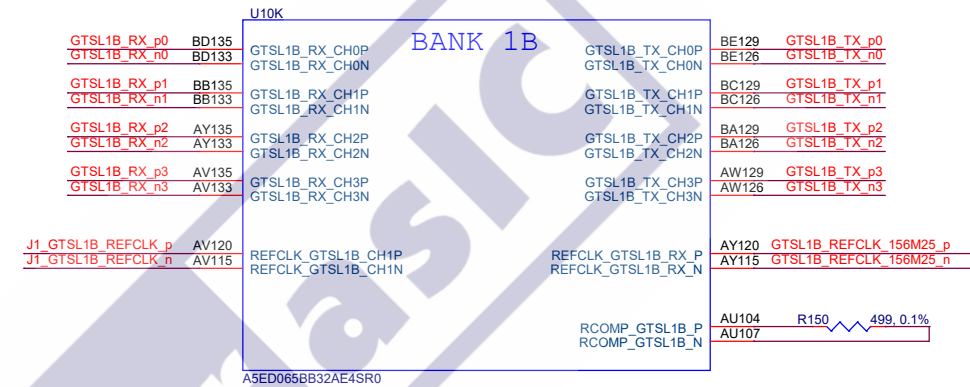
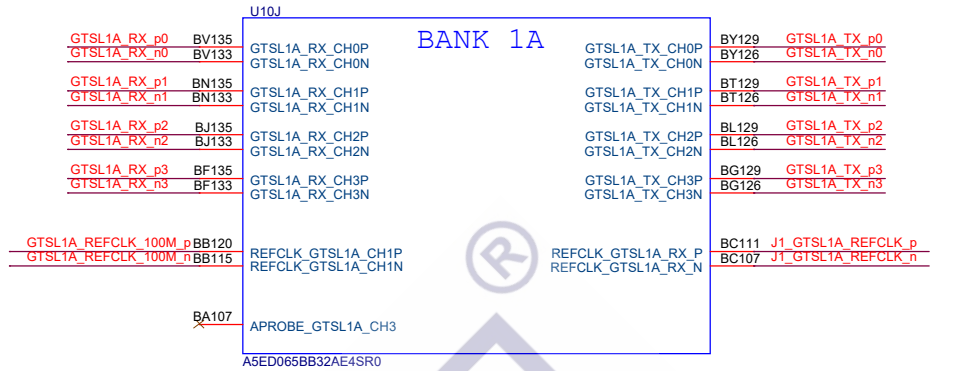
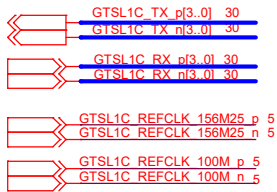
1A Transceivers



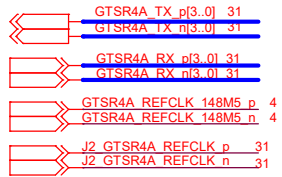
1B Transceivers



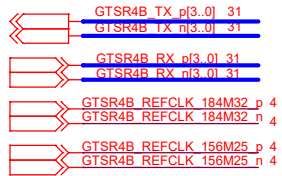
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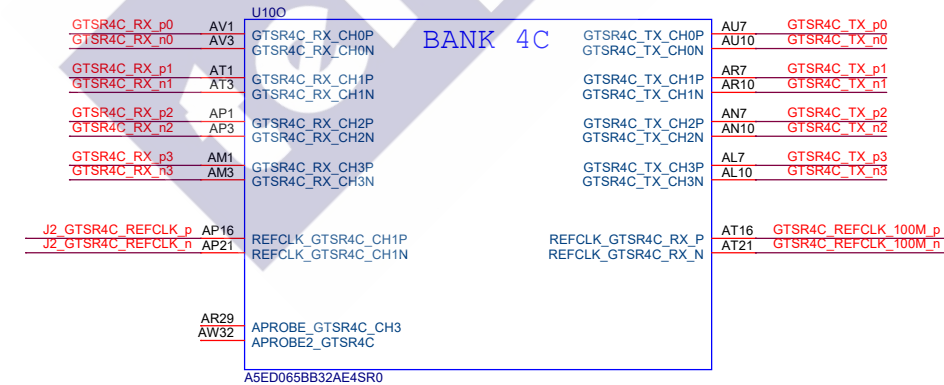
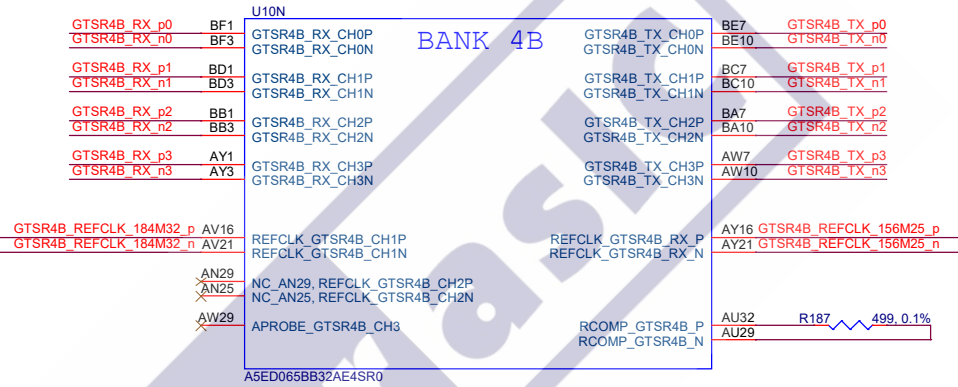
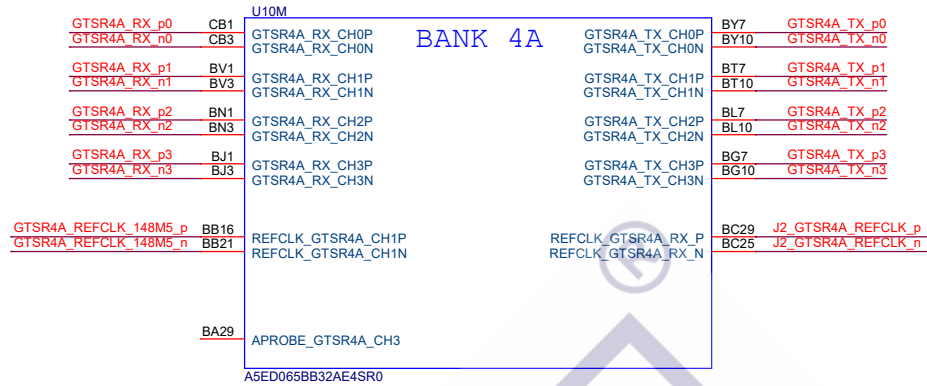
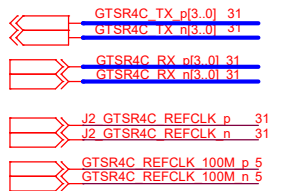
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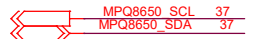
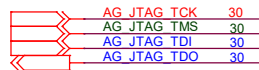
4B Transceivers



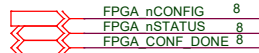
4C Transceivers



Agilex JTAG Interface



FPGA Configuration



FPGA Temperature diode



FPGA AS Configuration

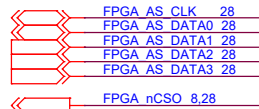
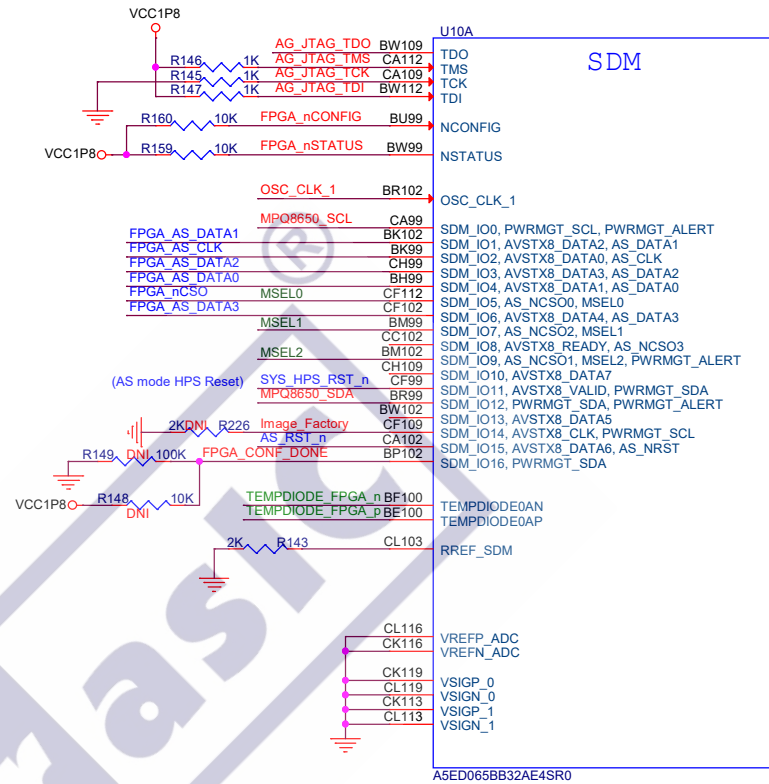
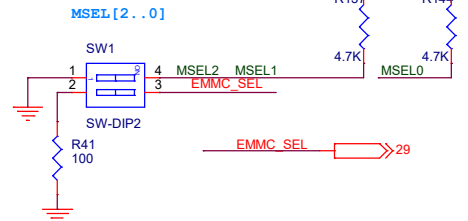


Image Factory



MSEL[2:0]	Configuration Mode
001	AS - Fast (Default Setting)
111	JTAG

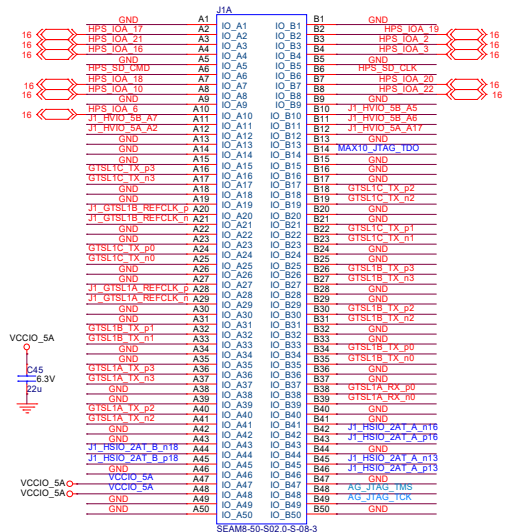
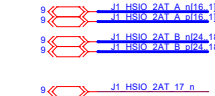
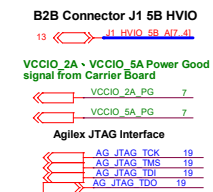
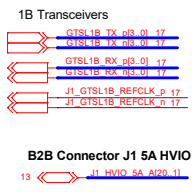
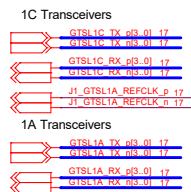
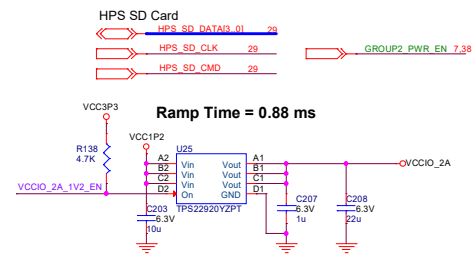


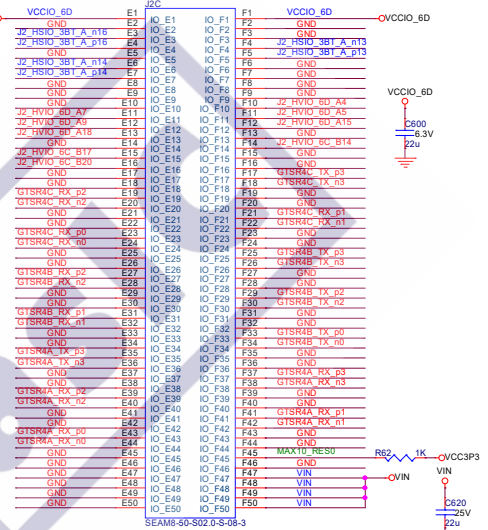
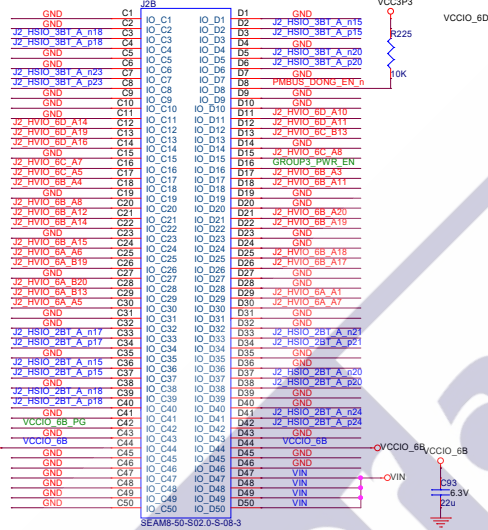
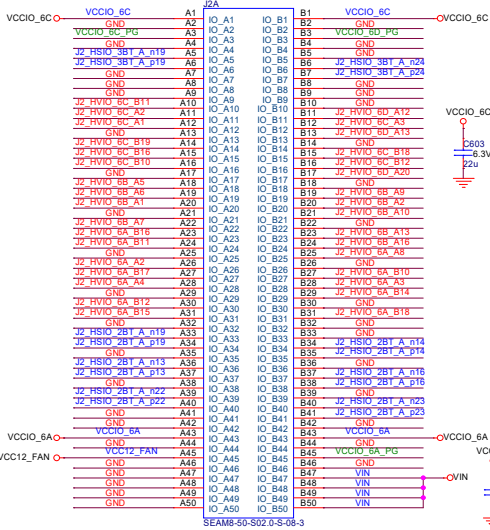
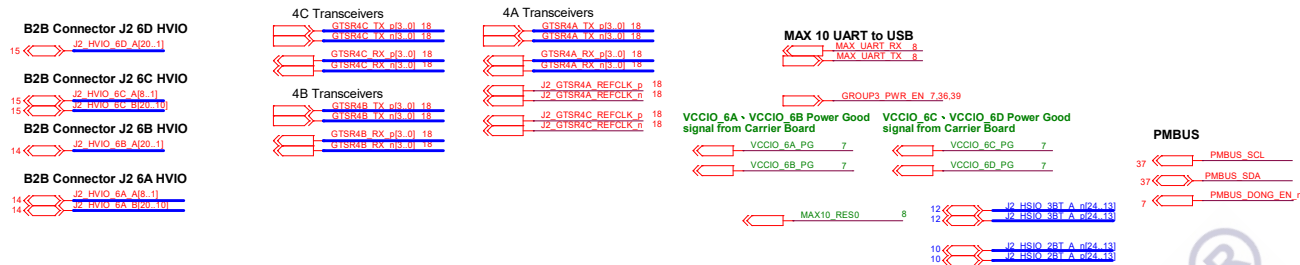
Default position : ON

SDMMC Bus Device select

SW4 2 Position	Target device
ON	SD Card
OFF	eMMC

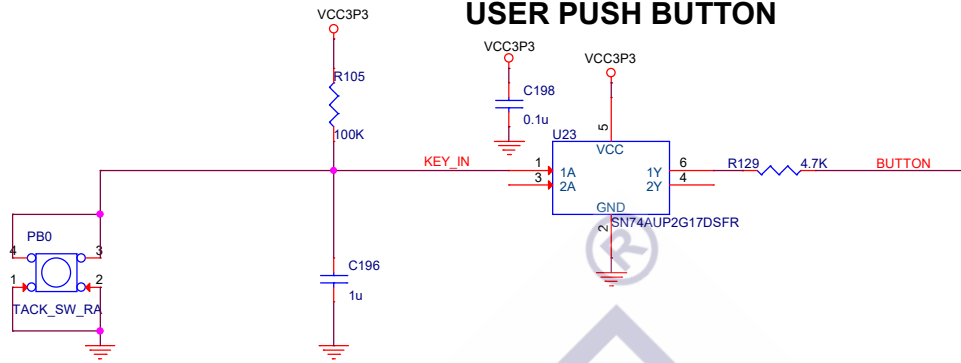
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Title Comet A65 SOM	
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13 << BUTTON

13 >> LED



USER LEDS



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Title					
Comet A65 SOM					
Size	Document Number		Rev		
B	Button, Switch, User LED		B		
Date:	Tuesday, September 30, 2025	Sheet 33 of 39			