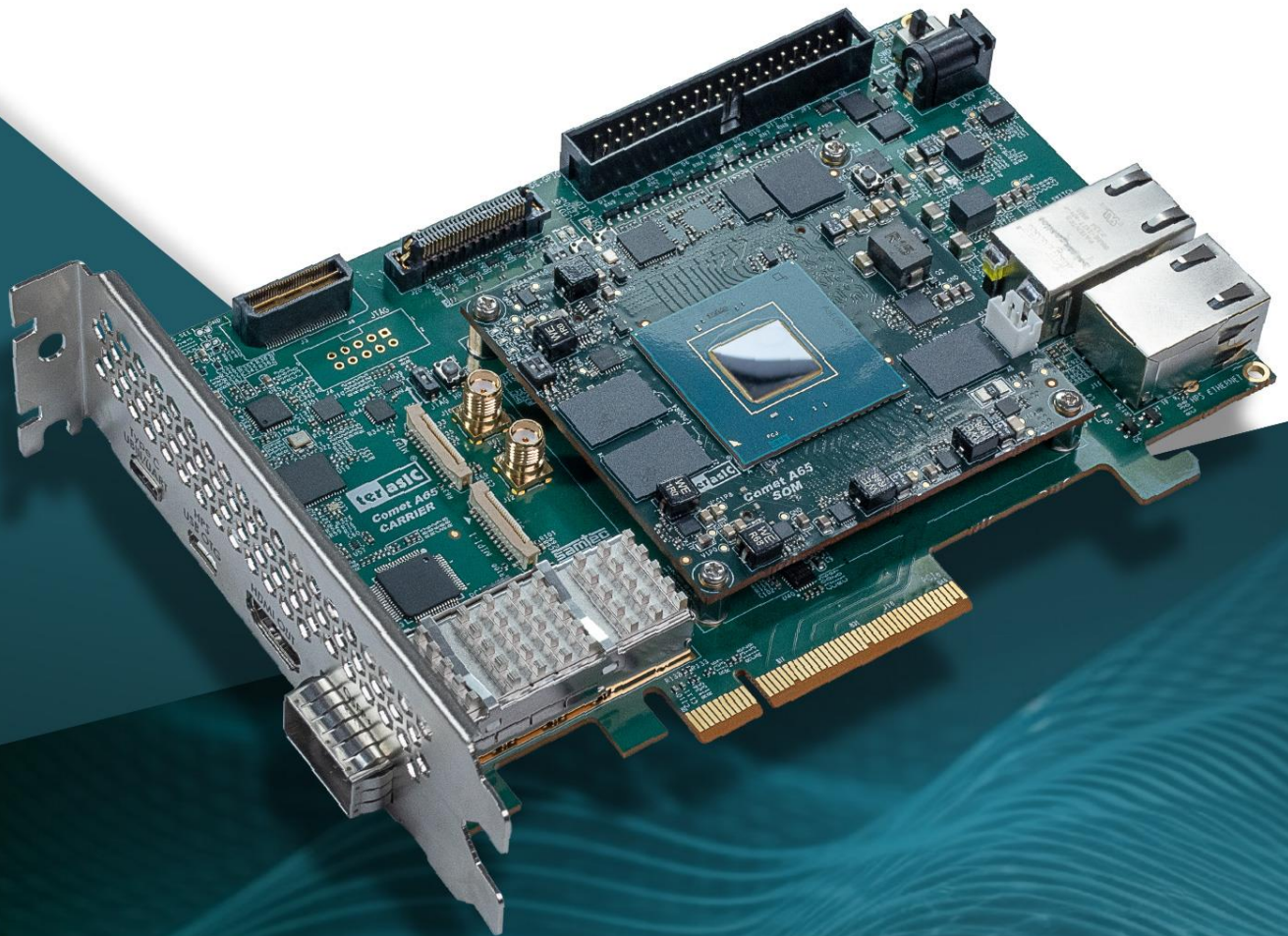


Comet-A65 Evaluation Kit



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Overview

This chapter provides an overview of the Comet A65 EVK's Carrier board and installation guide.

1.1 General Description

The Comet A65 Evaluation Kit (EVK) consists of a Comet A65 System on Module (SOM) and a Comet A65 Carrier Board (see **Figure 2-1**). The SOM is installed onto the carrier board via two SEAM8 connectors.

This manual focuses primarily on the features, interface specifications, and usage of the Comet A65 Carrier Board. For detailed information regarding the Comet A65 SOM, please refer to the dedicated [Comet A65 SOM User Manual](#).

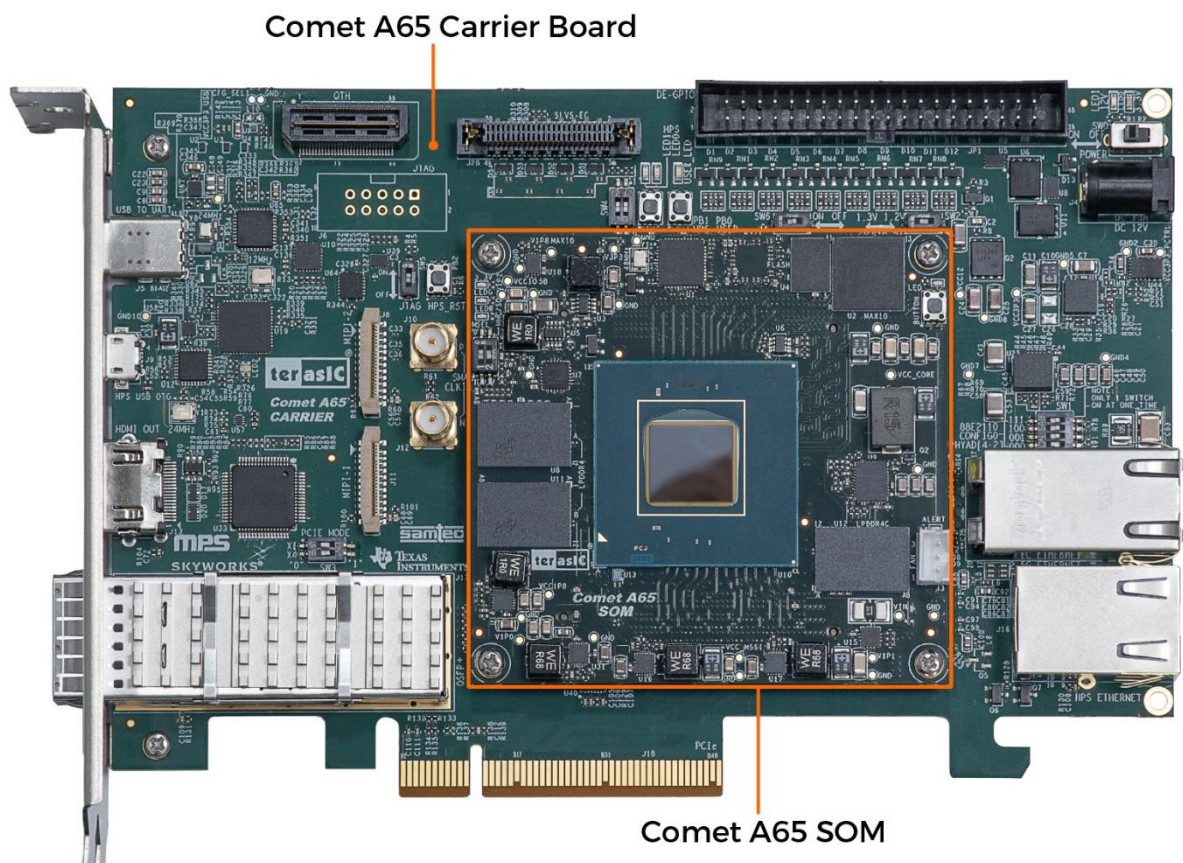


Figure 2-1 The Comet A65 Evaluation Kit

1.2 Key Features

The following hardware is implemented on the Comet A65 Carrier board:

- **Carrier Board System:**
 - PCIe Form Factor: Full Height, ½ Length
 - On-Board USB Blaster III
 - 12V DC Jack or PCIe edge power input
 - Type-C connector for HPS terminal and Board Management
 - Interface: Two SEAF8 Connectors (40x100 pin) for SOM installation
 - Active Heatsink (on SOM)

- Carrier Board FPGA Subsystem:
 - PCIe Gen4 x4 with x8 Edge
 - One QSFP+ Port for 40 GbE network interface
 - HDMI Out (1080P)
 - Two 4-lanes MIPI Connectors for Camera/Display
 - 60-pin High Speed Connector (support LVDS)
 - One 3.3V 2x20 DE-GPIO Header
 - 2.5G Ethernet PHY via RJ45, co-working with HPS
 - SMA x2 for differential clock input

- Carrier Board HPS Subsystem:
 - UART Port (Type-C Connector)
 - Gigabit Ethernet PHY via RJ45
 - MicroSD Socket
 - USB 2.0 OTG Port (Micro AB Connector)
 - COLD Reset Button

1.3 Block Diagram

Figure 2-2 shows the block diagram of the Comet A65 Carrier board.

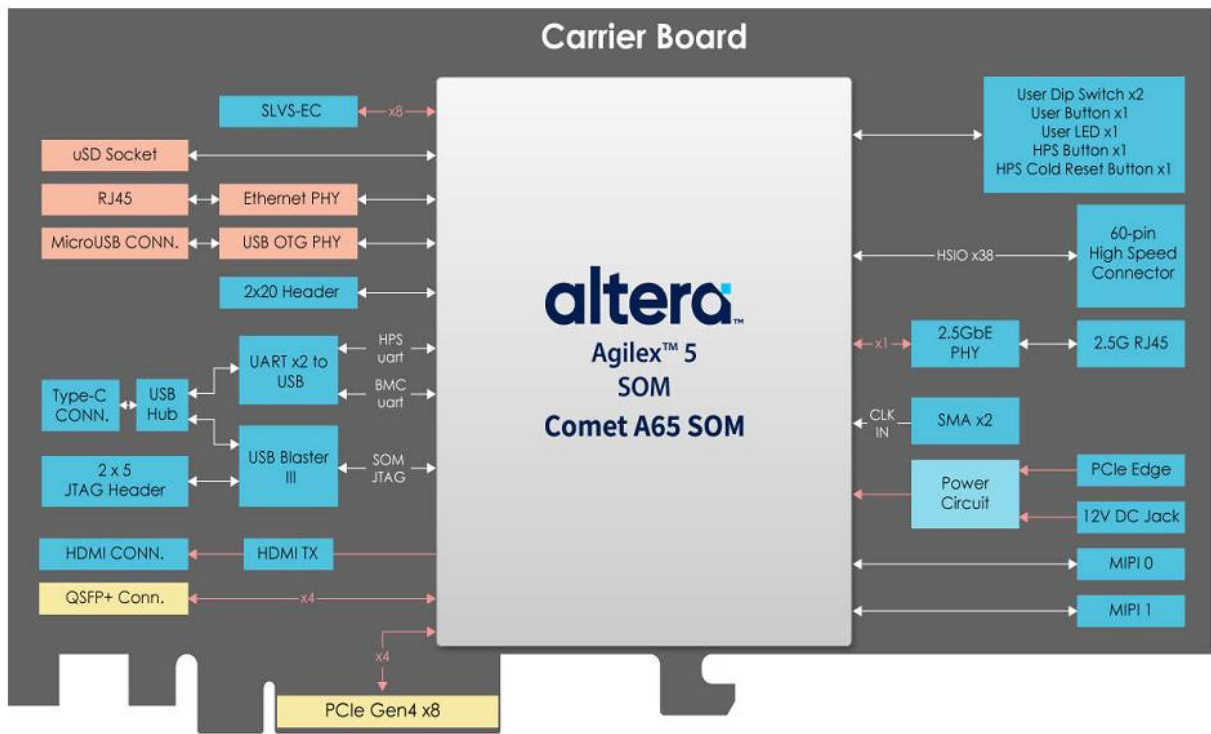


Figure 2-2 Block Diagram of the Comet A65 Carrier Board

Chapter 2

Board Components

This chapter introduces all the important components on the Comet A65 Carrier board.

2.1 Overview

Figure 2-1 is the top view of the Comet A65 Carrier board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

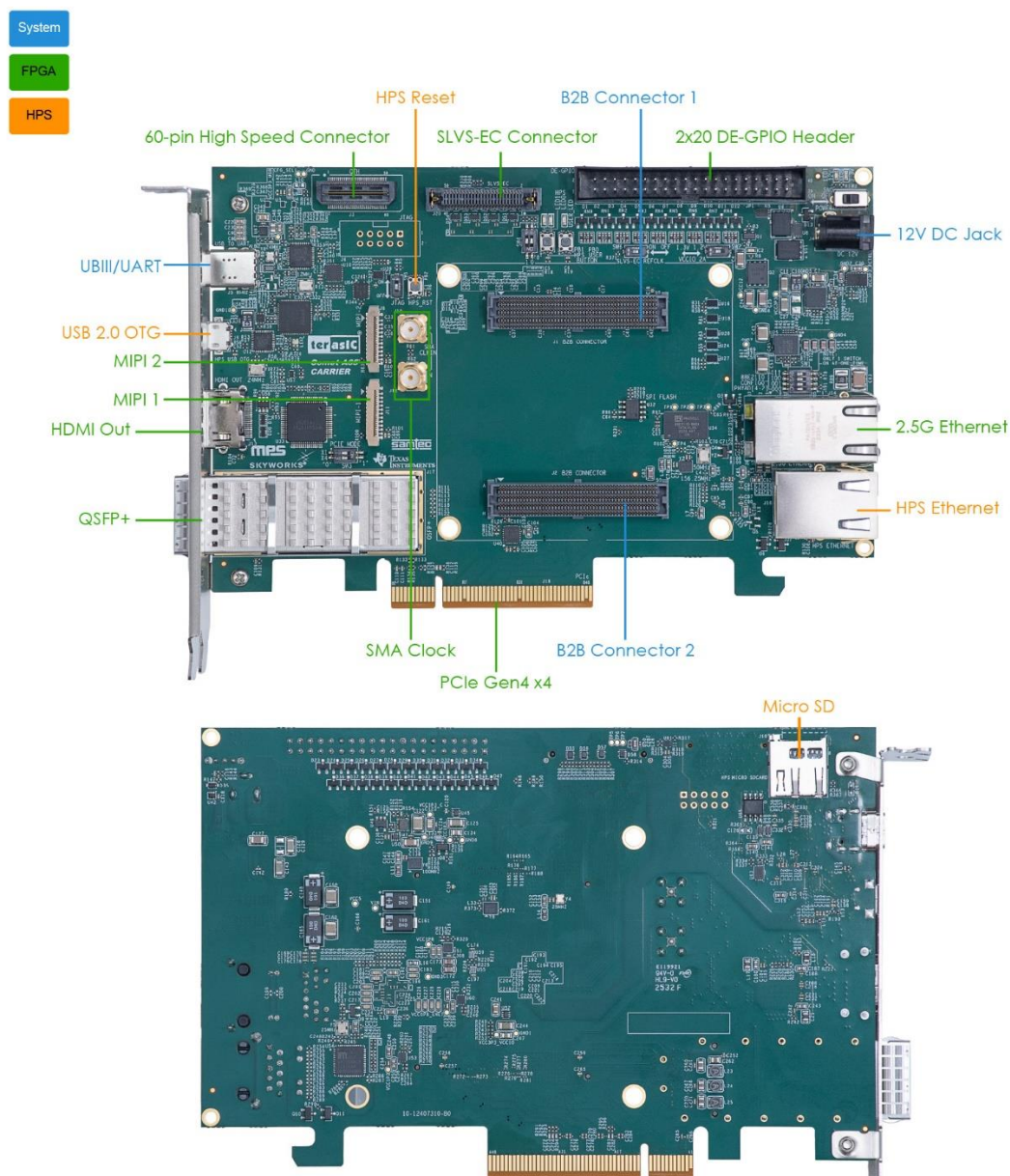


Figure 2-1 Comet A65 Carrier Board Layout

2.2 Power Input and Switch

This carrier board supports two methods for power input:

- PCIe Slot Power: Power can be supplied directly from the host motherboard's PCIe slot via its +12V rail.
- External Power Supply: Power can be provided by connecting a standalone external power supply unit (PSU) to the onboard 12V DC Jack.

Figure 2-2 illustrates the locations of the PCIe slot, 12V DC Jack and power switch.

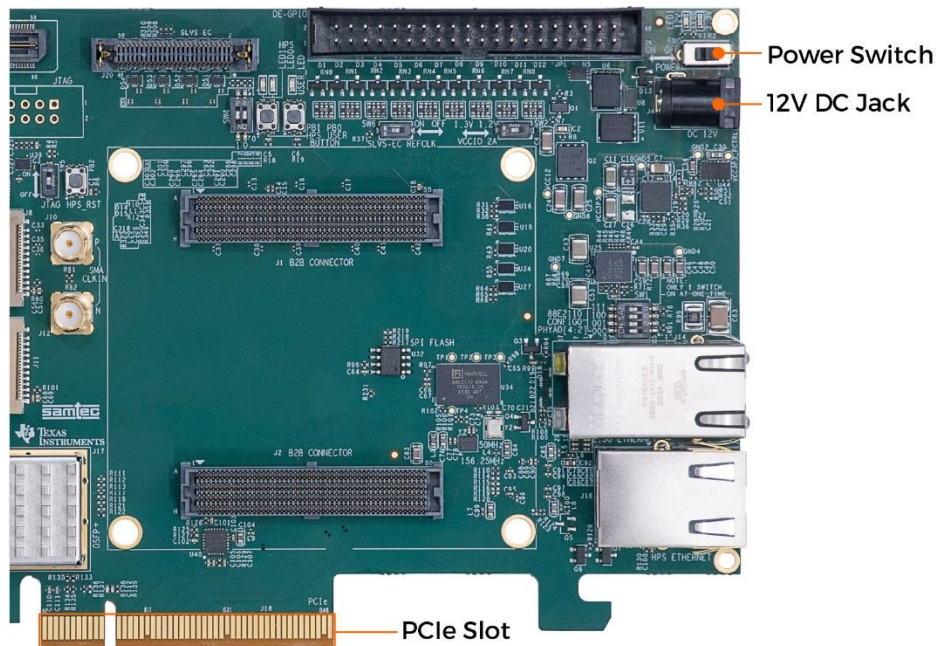


Figure 2-2 Key connectors and switches for power

2.3 Setup and Status Components

This section will introduce the use of the switch for setup on the carrier board, as well as a description of the various status LEDs.

■ Status LED

The FPGA development board includes board-specific status LEDs to indicate board status. **Figure 2-3** and **Figure 2-4** shows the location of all these status LED. Please refer to **Table 2-1** for the description of the LED indicators and **Table 2-2** for USB blaster III RGB LED.

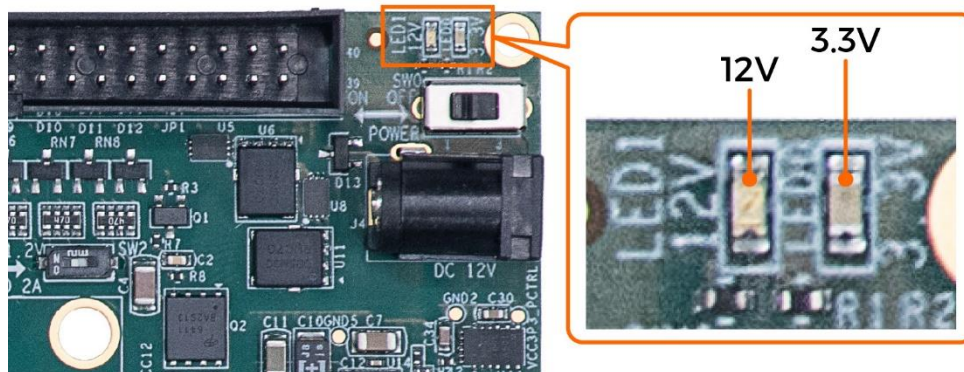


Figure 2-3 Power Status LED

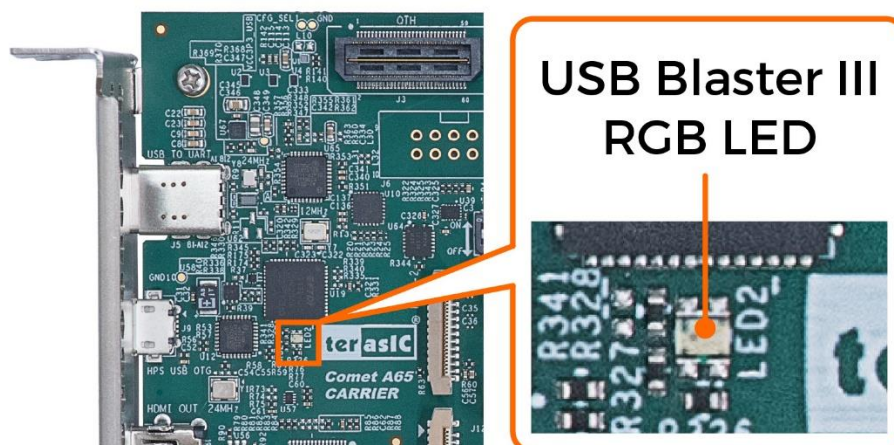


Figure 2-4 USB Blaster III Status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
LED1	12V	Illuminates when 12-V power is active.
LED0	3.3V	Illuminates when 3.3-V power is active.

Table 2-2 Status of USB blaster III RGB LED

Color	Meaning
Off	No power / not connected / suspend mode
Blue	Connected, not in use
Green	Connected, an application is using JTAG, no traffic
Green flickering	Connected, data is moving through the JTAG interface
Purple flashing	Identify function has been triggered on this cable

■ MAX 10 or Agilex 5 Select Switch

The SW5 is a switch used to select the System MAX10 or Agilex 5 FPGA to the JTAG chain of the Comet A65 EVK board. When this switch is switched to the default “**OFF**” position, there will only be Agilex 5 FPGA on the JTAG chain on the entire board. If the switch is switched to the “**ON**” position, the system MAX10 FPGA will be in the JTAG chain.

Note: To avoid erasing the MAX10 code accidentally, we advise users to keep the SW5 on the default “**OFF**” position.

ON : System MAX10 in JTAG Chain
 OFF : Agilix 5 FPGA in JTAG Chain

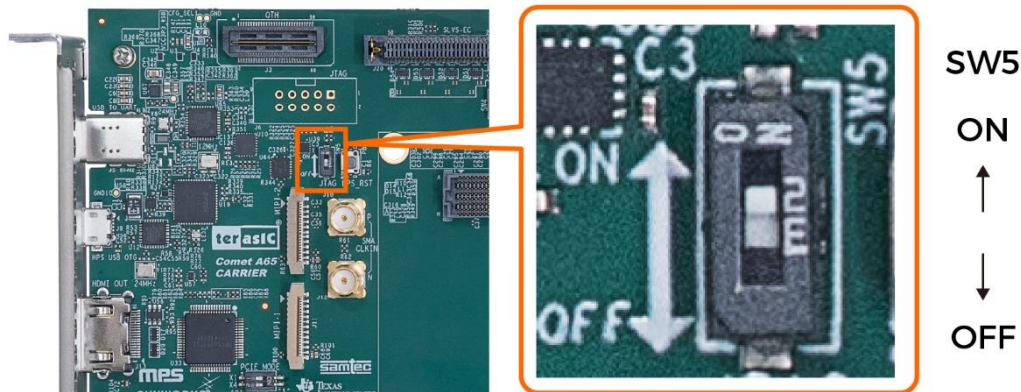


Figure 2-5 System MAX JTAG Bypass Switch

■ PCIe Mode switch

The PCIe Mode switch (SW3) is provided to enable or disable different configurations of the PCIe Connector (See **Figure 2-6**). **Table 2-3** lists the switch controls and description.

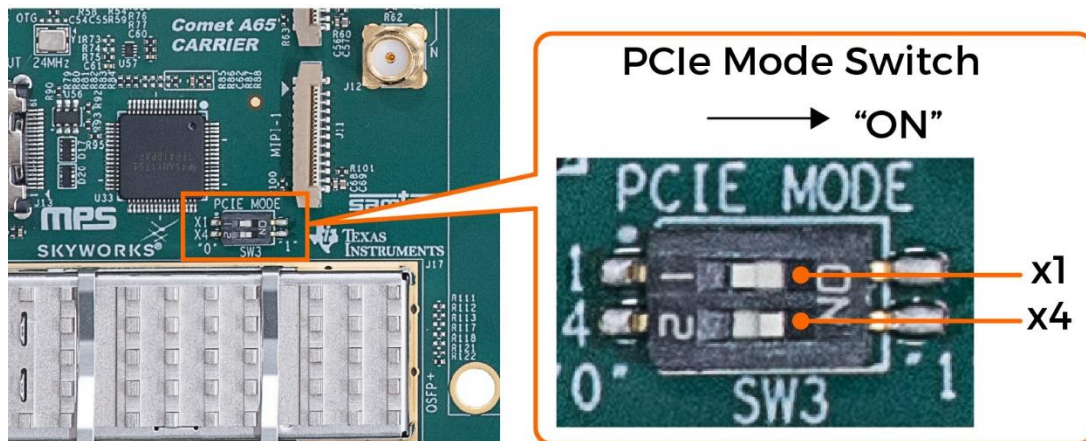


Figure 2-6 Position of the PCIe mode switch

Table 2-3 PCIe Control DIP Switch

Board Reference	Signal Name	Description	Default Setting
SW3.1	PCIE_PRSENT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW3.2	PCIE_PRSENT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	ON

■ Ethernet PHY_ADR Setting Switch

The SW1 switches are used to set bit4~2 of the PHY address (PHYAD[4:2]) for the 2.5G Ethernet PHY (Marvell 88E2110). SW1 has a total of four switches, each switch represents a group of PHYAD [4:2] setting value. Note that only one switch can be set to the on position at a time. **Figure 2-7** shows the position of this switch on the board. **Table 2-4** list the setting for each switch.

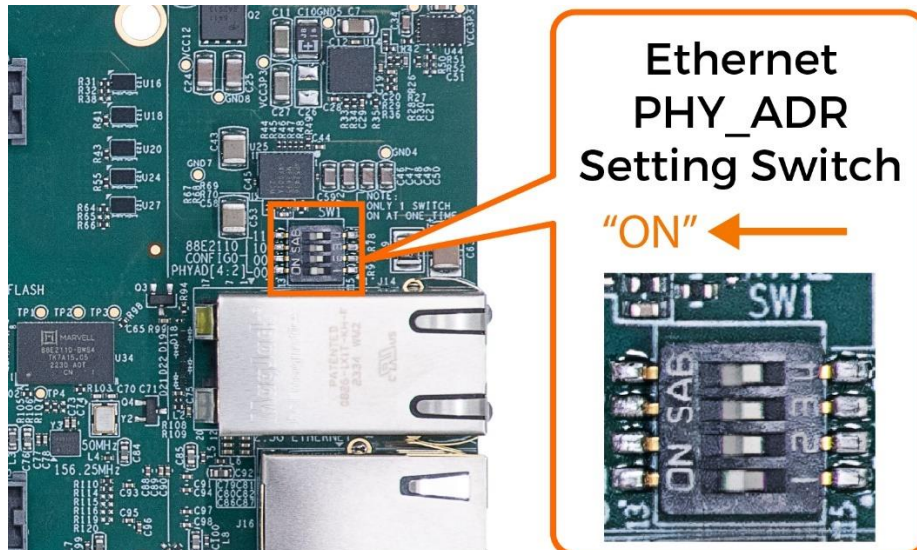


Figure 2-7 Position of slide switches SW1

Table 2-4 SW1 setting

Board Reference	Description	Default Setting
SW1.1	ON: Selects 000 for PHYAD[4:2] OFF: Deselect 000 for PHYAD[4:2]	ON
SW1.2	ON: Selects 001 for PHYAD[4:2] OFF: Deselect 001 for PHYAD[4:2]	OFF
SW1.3	ON: Selects 010 for PHYAD[4:2] OFF: Deselect 010 for PHYAD[4:2]	OFF
SW1.4	ON: Selects 111 for PHYAD[4:2] OFF: Deselect 111 for PHYAD[4:2]	OFF

■ VCCIO_2A Select Switch

The Comet A65 SoM FPGA 2A bank supports both 1.2V and 1.3V I/O standards on this EvK. The 1.2V power is supplied by the SoM itself, while the 1.3V power is provided by the carrier board. When users need to use LVDS TX function on VCCIO_2A bank, the I/O standard should be set to 1.3V. If only LVDS RX is used, set it as 1.2V. **Figure 2-8** shows the position of the SW2. When SW2 is set to ON position, the I/O standard is 1.3V, it's default set to OFF position for 1.2V I/O standard.

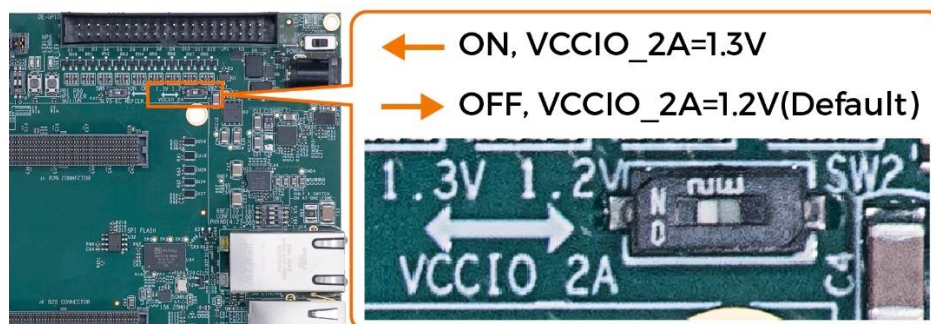


Figure 2-8 VCCIO_2A I/O standard setting switch

■ SLVS-EC REFCLK Select Switch

The SW6 is used to select SLVS-EC reference clock (SLVS_EC_REFCLK_p) for the SLVS-EC connector, there are two reference clocks 144MHz and 148.5MHz. When SW6 is set to ON position, the 144MHz clock is selected, 148.5MHz is selected when SW6 is set to OFF position. **Figure 2-9** shows the position of this switch on the board.

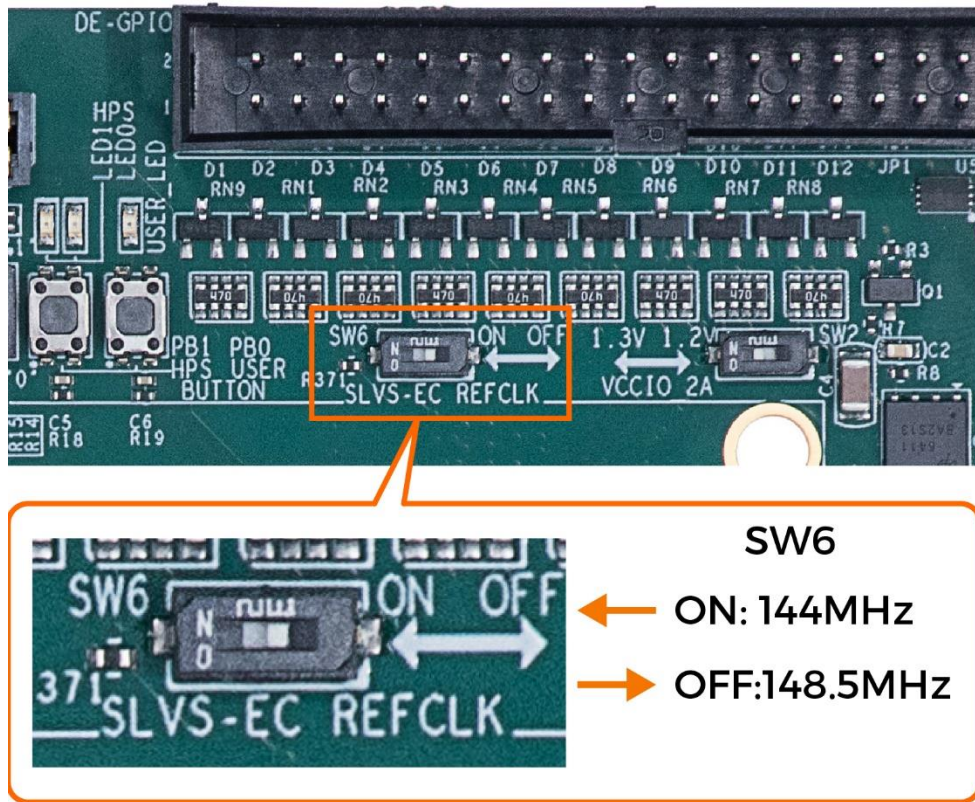


Figure 2-9 SLVS-EC REFCLK Select Switch

2.4 Reset Device

The board provides a HPS cold reset button (PB2), HPS_RST, as shown in figure below. It's used to cold reset to the HPS, Ethernet PHY and USB host device. Active low input which resets all HPS logics that can be reset. **Figure 2-11** is the HPS reset tree for Comet A65 evaluation kit.

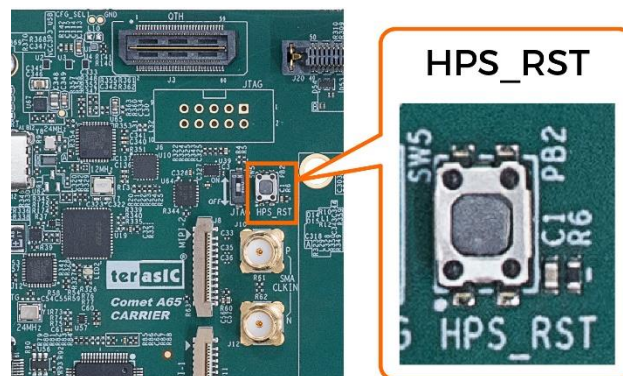


Figure 2-10 Position of the SOM_RST button

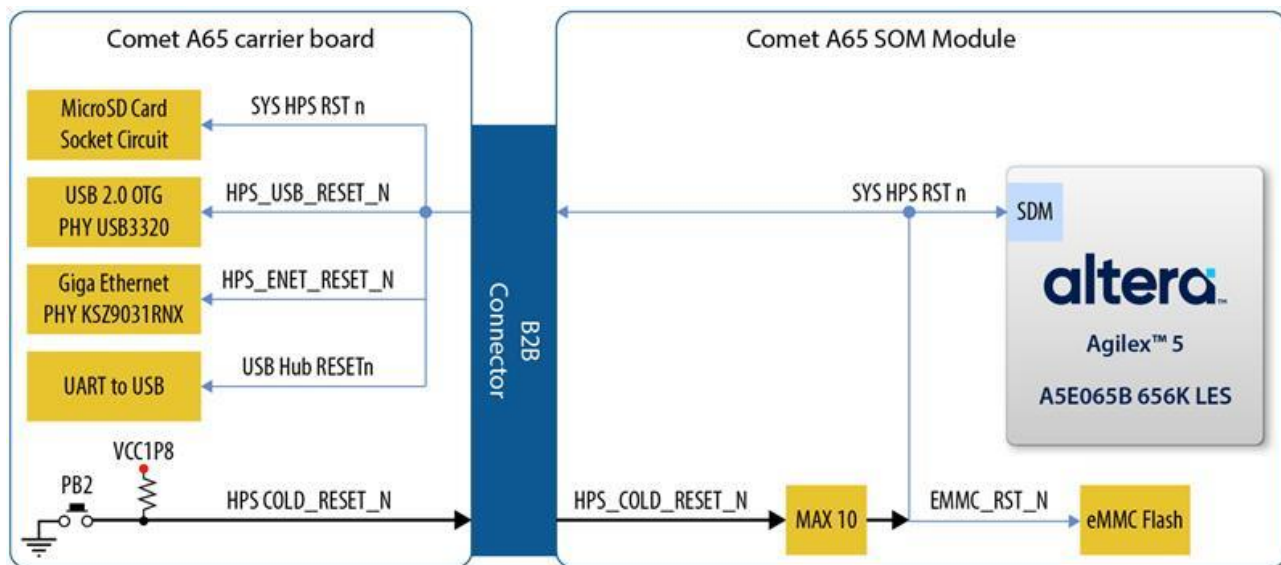


Figure 2-11 HPS reset tree on Comet A65 evaluation kit

2.5 Clock Tree

The clock tree design of the Comet Carrier Board is primarily composed of four onboard oscillators (see **Figure 2-12**). Its purpose is to provide precise reference clocks for the SOM module and high-speed transceiver interfaces. The function of each clock is as follows:

- **100 MHz Clock:** This clock signal (CLK_100_p/n) is routed through pins A45/A44 of the B2B Connector J1 to the FPGA on the Comet A65 SOM (System on Module), serving as its primary reference clock source.
- **25MHz Clock:** This clock signal (HPS_OSC_CLK) is routed through pins D8 of the B2B Connector J1 to the FPGA on the Comet A65 SOM (System on Module), serving only for SoC.
- **156.25 MHz Clock:** This clock signal (ENET_88E2110_REFCLK_156M25_p/n) is routed to the Giga Ethernet PHY 88E2110 on the Comet A65 Carrier board.
- **144/148.5 MHz Clock:** One independent oscillator provides a selectable reference clock (SLVS_EC_REFCLK_p/n), it is routed through pins A28/A29 of the B2B Connector J1 to the FPGA on the Comet A65 SOM (System on Module), serving for SLVS-EC transceivers.
- **External SMA Clock Input:** Two SMA connectors provide differential external clock input (SMA_CLKIN_p/n), it is routed through pins A5/A6 of the **B2B Connector J2** to the FPGA on the Comet A65 SOM (System on Module).

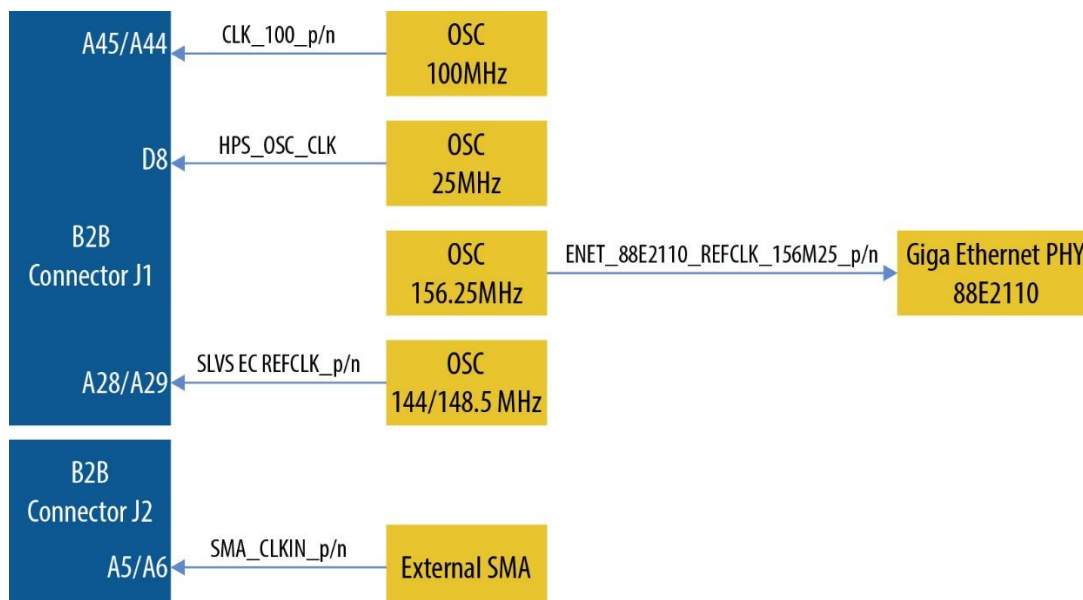


Figure 2-12 Clock tree of the Carrier Board

2.6 USB Blaster III

The board features a built-in Altera USB Blaster III debug circuit. Its USB interface is connected to the USB Type-C port via the on-board USB hub, while the JTAG signals are routed to the SOM (System on Module) through the B2B Connector J1.

Please see [Getting_Start_Guide_for_Comet_A65_SOM_EVK.pdf](#) for details on installing the USB Blaster III driver.

Figure 2-13 provides the block diagram for the on-board USB Blaster III circuitry. **Figure 2-14** shows the physical locations of the USB Type-C connector.

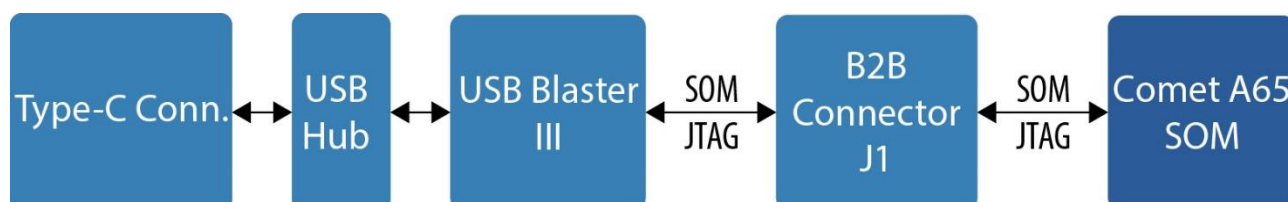


Figure 2-13 Block diagram of the USB Blaster III circuit

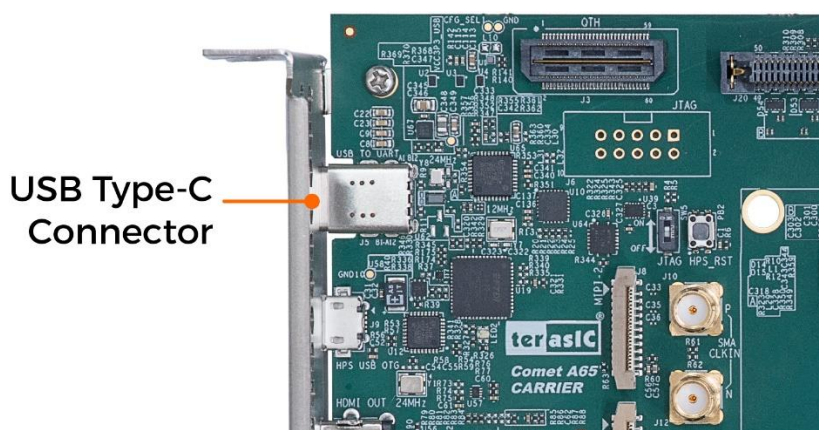


Figure 2-14 Location of the USB Type-C connector

2.7 General User I/O

This section describes the user I/O interfaces of the FPGA and HPS fabric on the carrier board. Please note that the HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. **Figure 2-15** shows the position of all these components and interface.

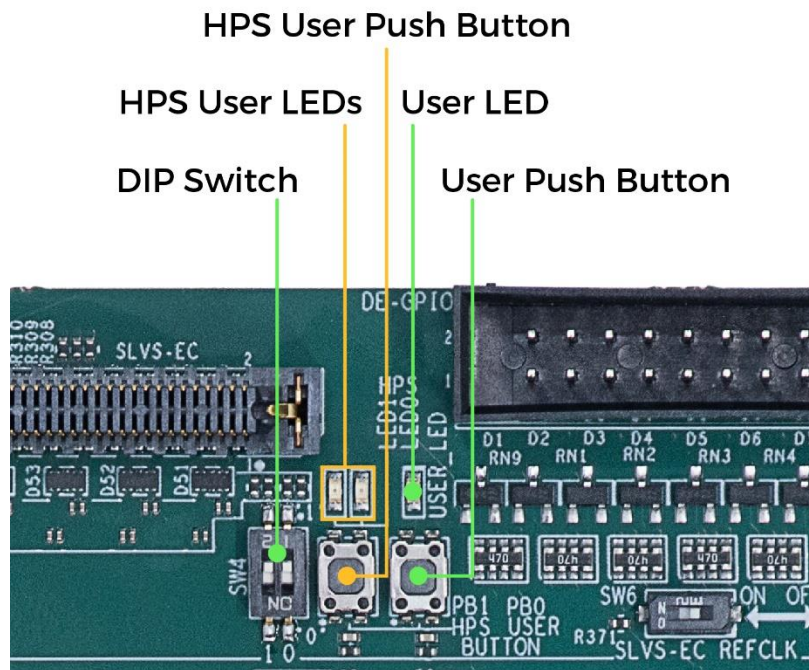


Figure 2-15 Position of all the general user components

■ User Push-buttons

The carrier board includes one FPGA and one HPS fabric user defined push-buttons that allow users to interact with the Agilex 5 SoC device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-5** lists the board references, signal names and their corresponding Agilex 5 SoC device pin numbers for the two push-buttons.

Table 2-5 Push-button (FPGA and HPS) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
PB0	USER_BUTTON	High Logic Level when the button is not pressed	3.3-V LVCMOS	J1_G10	CA118
PB1	HPS_KEY		1.8V	J1_H6	B134

■ DIP Switch

There is one two-positions slide switches on the FPGA fabric to provide additional FPGA input control. When a position of dip switch is in the ON position or the OFF position, it provides a low

logic level or a high logic level to the Agilex SoC FPGA, respectively. **Table 2-6** lists the signal names and their corresponding Agilex SoC device pin numbers.

Table 2-6 Dip Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
SW4.1	USER_SW0	High logic level when SW in the OFF position.	3.3-V LVCMOS	J1_D10	BR118
SW4.2	USER_SW1		3.3-V LVCMOS	J1_F10	BW118

■ User LEDs

The FPGA board consists of one FPGA fabric and two HPS fabric user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Agilex SoC FPGA. Each LED is driven directly by the FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA and HPS that are connected to the LEDs is given in **Table 2-7**.

Table 2-7 Pin Assignments of User LEDs

Board Reference	Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
USER_LED	USER_LED	Driving a logic 0 on the I/O port turns the LED ON.	3.3-V LVCMOS	J1_D11	CF121
HPS_LED0	HPS_LED		1.8-V	J1_F7	Y127
HPS_LED1	HPS_LED2	Driving a logic 1 on the I/O port turns the LED OFF.	1.8-V	J1_B3	U135

2.8 2x20 GPIO Expansion Header

The board has one 40-pin expansion header. It has 36 user pins connected to the Agilex 5 SoC FPGA through the B2B connector J2. It also comes with DC +5V (VCC5), DC +3.3V (VCC3P3), and two GND pins. The maximum power consumption allowed for a daughter card connected to one GPIO ports is shown in **Table 2-8**.

Table 2-8 Voltage and Max. Current Limit of Expansion Header

Supplied Voltage	Max. Current Limit
5V	1A
3.3V	1.5A

Each pin on the expansion header is connected to two diodes and a resistor for protection against high or low voltage level. **Figure 2-16** shows the protection circuitry applied to all 36 data pins. **Table 2-9** shows the pin assignment of the GPIO header.

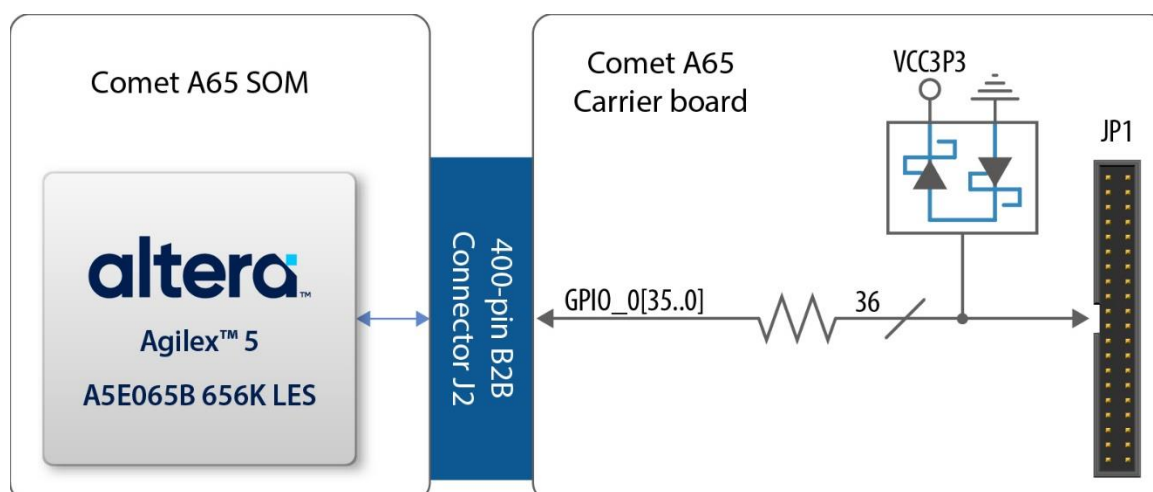


Figure 2-16 Connections between the GPIO header and Agilex 5 SoC FPGA

Table 2-9 Pin Assignment of Expansion Header

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
GPIO[0]	GPIO Connection[0]	3.3-V LVCMOS	J2_B19	PIN_BF29
GPIO[1]	GPIO Connection[1]	3.3-V LVCMOS	J2_D17	PIN_BE43
GPIO[2]	GPIO Connection[2]	3.3-V LVCMOS	J2_B27	PIN_BP22
GPIO[3]	GPIO Connection[3]	3.3-V LVCMOS	J2_C18	PIN_BF40
GPIO[4]	GPIO Connection[4]	3.3-V LVCMOS	J2_D18	PIN_BF16
GPIO[5]	GPIO Connection[5]	3.3-V LVCMOS	J2_A20	PIN_BF21
GPIO[6]	GPIO Connection[6]	3.3-V LVCMOS	J2_B20	PIN_BE21
GPIO[7]	GPIO Connection[7]	3.3-V LVCMOS	J2_B21	PIN_BF25
GPIO[8]	GPIO Connection[8]	3.3-V LVCMOS	J2_A22	PIN_BF32
GPIO[9]	GPIO Connection[9]	3.3-V LVCMOS	J2_C20	PIN_BF36
GPIO[10]	GPIO Connection[10]	3.3-V LVCMOS	J2_A23	PIN_BH28
GPIO[11]	GPIO Connection[11]	3.3-V LVCMOS	J2_C21	PIN_BH19
GPIO[12]	GPIO Connection[12]	3.3-V LVCMOS	J2_C22	PIN_BM19
GPIO[13]	GPIO Connection[13]	3.3-V LVCMOS	J2_A24	PIN_BK28
GPIO[14]	GPIO Connection[14]	3.3-V LVCMOS	J2_B23	PIN_BK22
GPIO[15]	GPIO Connection[15]	3.3-V LVCMOS	J2_D21	PIN_CH4
GPIO[16]	GPIO Connection[16]	3.3-V LVCMOS	J2_B24	PIN_BR19
GPIO[17]	GPIO Connection[17]	3.3-V LVCMOS	J2_D22	PIN_CK4
GPIO[18]	GPIO Connection[18]	3.3-V LVCMOS	J2_B25	PIN_BM31
GPIO[19]	GPIO Connection[19]	3.3-V LVCMOS	J2_C24	PIN_BU19
GPIO[20]	GPIO Connection[20]	3.3-V LVCMOS	J2_C25	PIN_BM28
GPIO[21]	GPIO Connection[21]	3.3-V LVCMOS	J2_C26	PIN_BK19
GPIO[22]	GPIO Connection[22]	3.3-V LVCMOS	J2_D25	PIN_CJ2

GPIO[23]	GPIO Connection[23]	3.3-V LVCMOS	J2_C28	PIN_CF9
GPIO[24]	GPIO Connection[24]	3.3-V LVCMOS	J2_C29	PIN_CH12
GPIO[25]	GPIO Connection[25]	3.3-V LVCMOS	J2_D26	PIN_CK2
GPIO[26]	GPIO Connection[26]	3.3-V LVCMOS	J2_D29	PIN_BU28
GPIO[27]	GPIO Connection[27]	3.3-V LVCMOS	J2_D30	PIN_BW28
GPIO[28]	GPIO Connection[28]	3.3-V LVCMOS	J2_A26	PIN_BP31
GPIO[29]	GPIO Connection[29]	3.3-V LVCMOS	J2_A27	PIN_BM22
GPIO[30]	GPIO Connection[30]	3.3-V LVCMOS	J2_A28	PIN_BR31
GPIO[31]	GPIO Connection[31]	3.3-V LVCMOS	J2_B28	PIN_BR28
GPIO[32]	GPIO Connection[32]	3.3-V LVCMOS	J2_A30	PIN_BR22
GPIO[33]	GPIO Connection[33]	3.3-V LVCMOS	J2_A31	PIN_BW19
GPIO[34]	GPIO Connection[34]	3.3-V LVCMOS	J2_B29	PIN_BU22
GPIO[35]	GPIO Connection[35]	3.3-V LVCMOS	J2_B31	PIN_CF12

2.9 QSFP+ Ports

The carrier board has one QSFP+ connector that use four transceiver channels each from the Agilex 5 SoC FPGA device. The QSFP+ module receives the serial data from the Agilex 5 SoC FPGA, and transform them to optical signals. A Low-Jitter programmable clock generator (Si5340B) on Comet A65 SoM will provide flexible clock for serial transceivers of the FPGA. **Figure 2-17** shows the connections between the QSFP+ and Agilex 5 SoC FPGA.

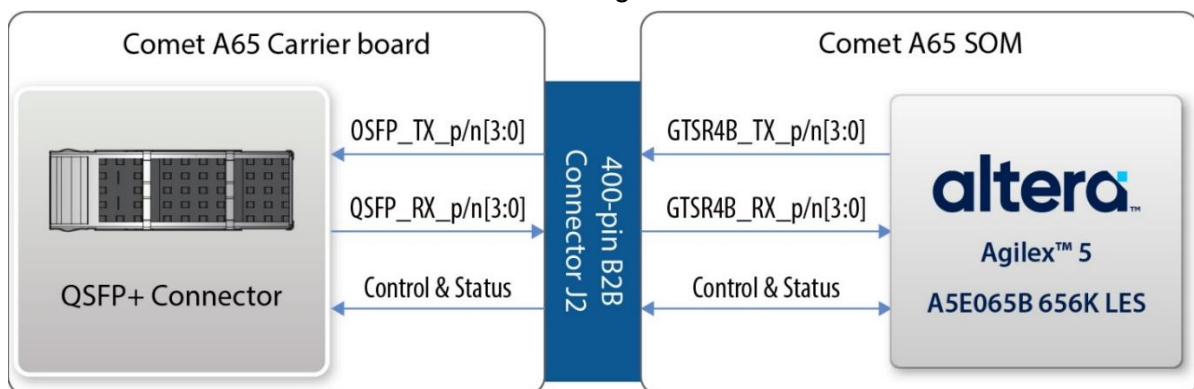


Figure 2-17 Connection between the QSFP+ and Agilex 5 SoC FPGA

Table 2-10 QSFP+ Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A5 SoM FPGA Pin Num.
QSFP_INTERRUPT_n	Interrupt	3.3-V LVCMOS	J2_B15	PIN_A39
QSFP_LP_MODE	Low Power Mode	3.3-V LVCMOS	J2_E16	PIN_A33
QSFP_MOD_PRS_n	Module Present	3.3-V LVCMOS	J2_E15	PIN_B35
QSFP_MOD_SEL_n	Module Select	3.3-V LVCMOS	J2_G16	PIN_B26
QSFP_RST_n	Module Reset	3.3-V LVCMOS	J2_B16	PIN_B30
QSFP_SCL	2-wire serial interface clock	3.3-V LVCMOS	J2_C16	PIN_A30

QSFP_SDA	2-wire serial interface data	3.3-V LVCMOS	J2_B12	PIN_A35
QSFP_REFCLK_p	QSFP transceiver reference clock p	CURRENT MODE LOGIC (CML)		PIN_AV120
CIPRI_REFCLK_p	CIPRI clock	CURRENT MODE LOGIC (CML)		PIN_AY120
QSFP_RX_p[0]	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	J2_G31	PIN_BD135
QSFP_RX_p[1]	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	J2_E31	PIN_BB135
QSFP_RX_p[2]	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	J2_E27	PIN_AY135
QSFP_RX_p[3]	Receiver data of channel 3	HSSI DIFFERENTIAL I/O	J2_G27	PIN_AV135
QSFP_RX_n[0]	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	J2_G32	PIN_BD133
QSFP_RX_n[1]	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	J2_E32	PIN_BB133
QSFP_RX_n[2]	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	J2_E28	PIN_AY133
QSFP_RX_n[3]	Receiver data of channel 3	HSSI DIFFERENTIAL I/O	J2_G28	PIN_AV133
QSFP_TX_p[0]	Transmitter data of channel 0	HSSI DIFFERENTIAL I/O	J2_F33	PIN_BE129
QSFP_TX_p[1]	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	J2_H29	PIN_BC129
QSFP_TX_p[2]	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	J2_F29	PIN_BA129
QSFP_TX_p[3]	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	J2_F25	PIN_AW129
QSFP_TX_n[0]	Transmitter data of channel 0	HSSI DIFFERENTIAL I/O	J2_F34	PIN_BE126
QSFP_TX_n[1]	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	J2_H30	PIN_BC126
QSFP_TX_n[2]	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	J2_F30	PIN_BA126
QSFP_TX_n[3]	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	J2_F26	PIN_AW126

2.10 MIPI Connector

The Agilex 5 devices offer native mobile industry processor interface (MIPI) D-PHY. This support complies to MIPI D-PHY version 2.5, and allows transmission or reception of data with MIPI D-PHY

interfaces. It provides the PHY-protocol interface (PPI) to connect with camera serial interface (CSI) and display serial interface (DSI) applications.

The carrier board also provides two 22-pin FPC connectors (1 lane clock and 4 lane data for each), allowing users to connect MIPI interface cameras and display devices through FPC cable (see **Figure 2-18**). Users can use this connector and camera cable to connect to camera devices such as Raspberry Pi camera module to form a camera input application. In addition, it can also be connected with the display device such as Raspberry Pi MIPI Displayer module to implement a display application.

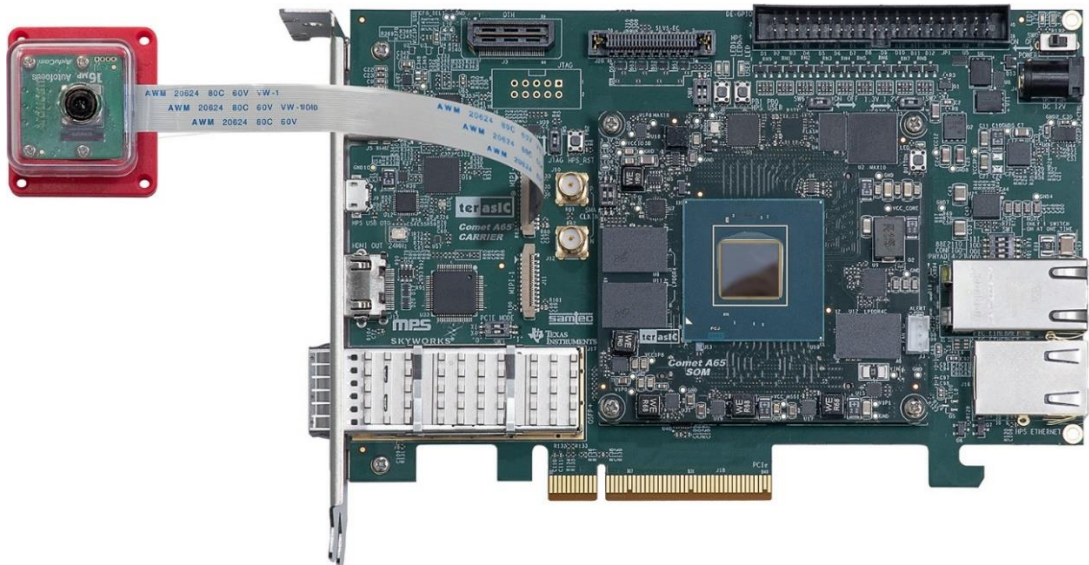


Figure 2-18 MIPI camera module connects to the carrier board via cable

See **Figure 2-19** shows the connections between the FPGA and two 22-pin MIPI connectors. **Table 2-11** shows the pin assignment of 22-pin MIPI connectors.

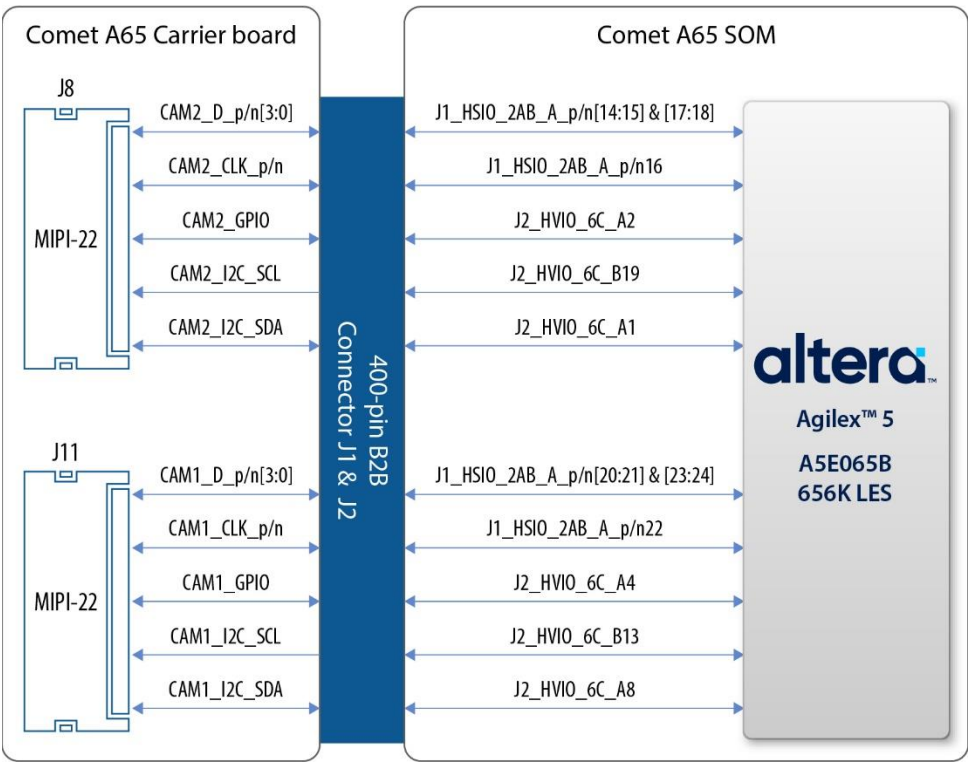


Figure 2-19 Connection between the MIPI connector and Agilex 5 FPGA

Table 2-11 MIPI connector pin assignments, schematic signal names, and functions

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A65 SoM FPGA Pin Num.
CAM1_CLK_p	MIPI Clock positive	DPHY	J1_H48	PIN_CL88
CAM1_CLK_n	MIPI Clock negative	DPHY	J1_H47	PIN_CK88
CAM1_D_p[0]	MIPI Data 0 positive	DPHY	J1_G43	PIN_CL91
CAM1_D_p[1]	MIPI Data 1 positive	DPHY	J1_G34	PIN_CK97
CAM1_D_p[2]	MIPI Data 2 positive	DPHY	J1_G46	PIN_CK85
CAM1_D_p[3]	MIPI Data 3 positive	DPHY	J1_E41	PIN_CK80
CAM1_D_n[0]	MIPI Data 0 negative	DPHY	J2_G42	PIN_CK94
CAM1_D_n[1]	MIPI Data 1 negative	DPHY	J1_G33	PIN_CL97
CAM1_D_n[2]	MIPI Data 2 negative	DPHY	J1_G45	PIN_CL85
CAM1_D_n[3]	MIPI Data 3 negative	DPHY	J1_E40	PIN_CL82
CAM1_I2C_SCL	I2C clock	3.3-V LVCMOS	J2_D13	PIN_C2
CAM1_I2C_SDA	I2C data	3.3-V LVCMOS	J2_D15	PIN_F15
CAM1_GPIO	GPIO signal	3.3-V LVCMOS	J2_G15	PIN_D24
CAM_RZQ1	External reference ball for output drive calibration	1.2V		PIN_BH69
CAM2_CLK_p	MIPI Clock positive	DPHY	J1_H30	PIN_CH89
CAM2_CLK_n	MIPI Clock negative	DPHY	J1_H29	PIN_CF89
CAM2_D_p[0]	MIPI Data 0 positive	DPHY	J1_G19	PIN_CC92
CAM2_D_p[1]	MIPI Data 1 positive	DPHY	J1_H24	PIN_CF92
CAM2_D_p[2]	MIPI Data 2 positive	DPHY	J1_G37	PIN_CF81
CAM2_D_p[3]	MIPI Data 3 positive	DPHY	J1_F45	PIN_CA81
CAM2_D_n[0]	MIPI Data 0 negative	DPHY	J1_G18	PIN_CA92
CAM2_D_n[1]	MIPI Data 1 negative	DPHY	J1_H23	PIN_CH92
CAM2_D_n[2]	MIPI Data 2 negative	DPHY	J1_G36	PIN_CH81
CAM2_D_n[3]	MIPI Data 3 negative	DPHY	J1_F44	PIN_CC81
CAM2_I2C_SCL	I2C clock	3.3-V LVCMOS	J2_A14	PIN_J1
CAM2_I2C_SDA	I2C data	3.3-V LVCMOS	J2_A12	PIN_F27
CAM2_GPIO	GPIO signal	3.3-V LVCMOS	J2_A11	PIN_F24

2.11 Gigabit Ethernet

The carrier board provides two Ethernet ports for users. The first is a Gigabit Ethernet port connected to the Micrel KSZ9031RN PHY and provided to HPS fabric. The other is a 2.5G Ethernet port connected to the FPGA through the Marvell 88E2110 PHY. Below here is the detailed information about these two ports.

■ Gigabit Ethernet Port for HPS

The board supports Gigabit Ethernet transfer by an external Micrel KSZ9031RN PHY chip and HPS Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface. **Figure 2-20** shows the connections between the Comet A65 SoM module, 400-pin B2B J1 connector and RJ-45 connectors.

For more information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, which are available on the manufacturer's website.

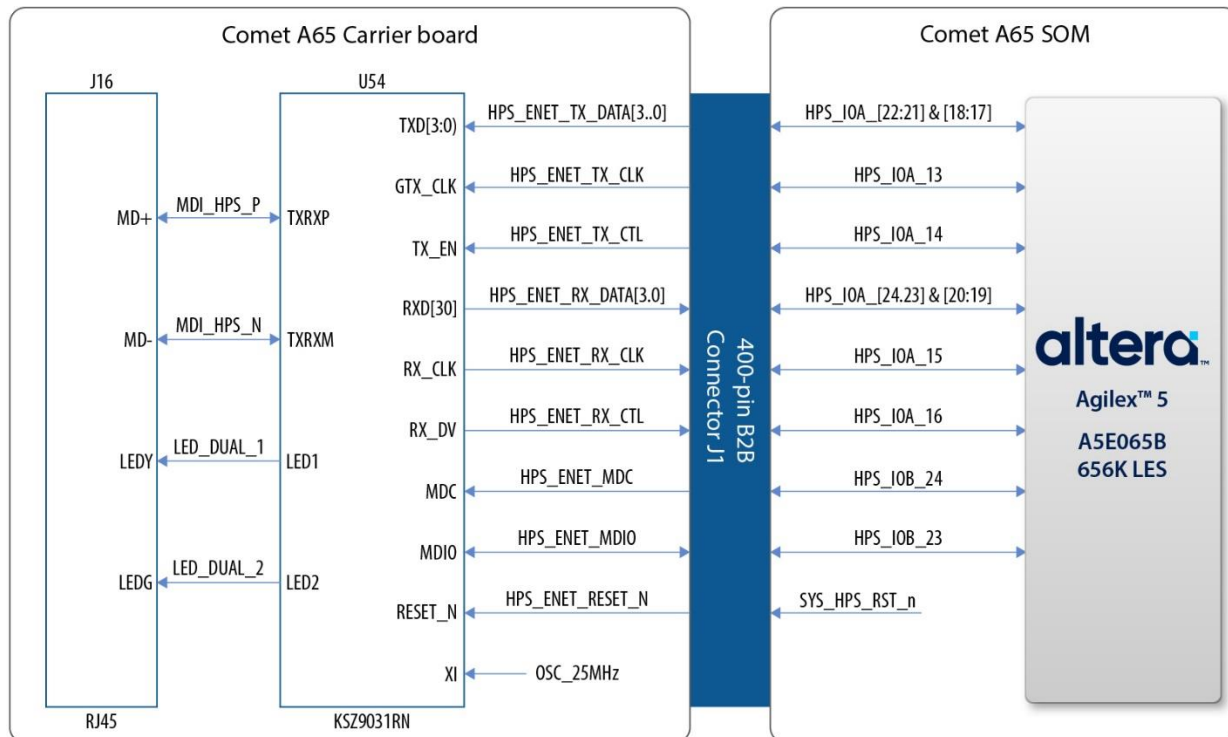


Figure 2-20 Connection between the RJ45 connector and Agilex 5 SoC FPGA

There are two LEDs, a green LED (LEDG) and a yellow LED (LEDY), which represent the status of the Ethernet PHY (KSZ9031RN). The LED control signals are connected to the LEDs on the RJ45 connector. The state and the definition of LEDG and LEDY are listed in **Table 2-12**. For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-12 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	Link / Activity (RX, TX)

Table 2-13 Pin Assignment of Gigabit Ethernet PHY and HPS on Comet A65 SoM

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A65 FPGA Pin Num.
HPS_ENET_TX_CTL	GMII and MII transmit enable	1.8 V	J1_H2	PIN_L135
HPS_ENET_TX_DATA[0]	GMII and MII transmit data[0]	1.8 V	J1_A2	PIN_M132
HPS_ENET_TX_DATA[1]	GMII and MII transmit data[1]	1.8 V	J1_A7	PIN_AD134
HPS_ENET_TX_DATA[2]	GMII and MII transmit data[2]	1.8 V	J1_A3	PIN_J134
HPS_ENET_TX_DATA[3]	GMII and MII transmit data[3]	1.8 V	J1_B8	PIN_AG120
HPS_ENET_TX_CLK	GMII and MII transmit clock	1.8 V	J1_E2	PIN_P132
HPS_ENET_RX_CTL	GMII and MII receive data valid	1.8 V	J1_A4	PIN_AD135
HPS_ENET_RX_DATA[0]	GMII and MII receive data[0]	1.8 V	J1_B2	PIN_K132
HPS_ENET_RX_DATA[1]	GMII and MII receive data[1]	1.8 V	J1_B7	PIN_AG129
HPS_ENET_RX_DATA[2]	GMII and MII receive data[2]	1.8 V	J1_C2	PIN_G134
HPS_ENET_RX_DATA[3]	GMII and MII receive data[3]	1.8 V	J1_D2	PIN_G135
HPS_ENET_RX_CLK	GMII and MII receive clock	1.8 V	J1_C3	PIN_J135
HPS_ENET_MDIO	Management Data	1.8 V	J1_F3	PIN_F124
HPS_ENET_MDC	Management Data Clock Reference	1.8 V	J1_F4	PIN_D124

There are four LEDs, two green LEDs(LEDG) and two yellow LEDs(LEDY), which represent the status of Ethernet PHY. The LED control signals are connected to the LEDs on the RJ45 connector. The state and definition of LEDG and LEDY are listed [Table 2-14](#). For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-14 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	10 Link / Activity (RX, TX)

■ 2.5 G Ethernet Port for FPGA

The board supports 10M/100M/1G/2.5G Ethernet interface by an external Marvell 88E2110 PHY. Users can implement an Ethernet MAC in the FPGA to implement network transmission. On this board, the 88E2110 PHY works in SGMII mode by default. At the same time, the user can set the

PHY address through SW1. For details, please see section 2.3. **Figure 2-21** shows the connections between the FPGA, 88E2110 PHY, and RJ-45 connector.

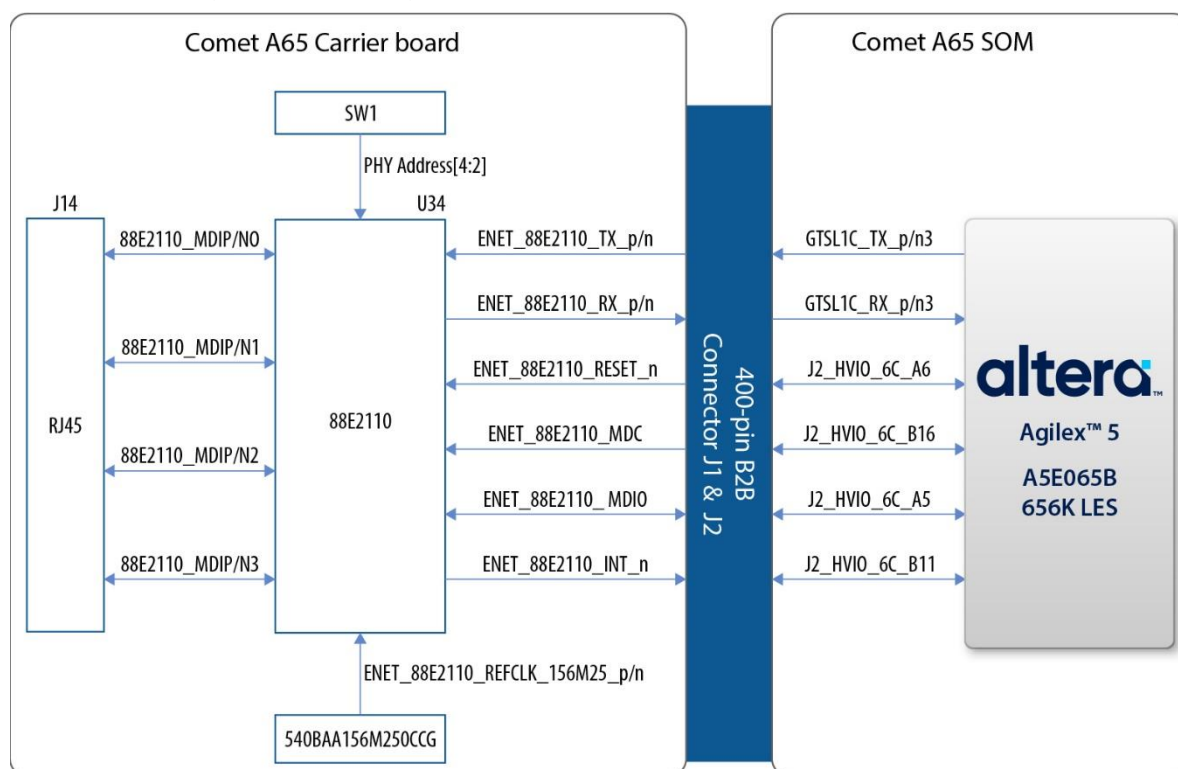


Figure 2-21 Connections between the FPGA and 88E2110 PHY

Table 2-15 Pin Assignment of 88E2110 PHY

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A65 SoM FPGA Pin No
ENET_88E2110_TX_p	SGMII transmit data	HIGH SPEED DIFFERENTIAL I/O	J1_A16	PIN_AL129
ENET_88E2110_TX_n	SGMII transmit data	HIGH SPEED DIFFERENTIAL I/O	J1_A17	PIN_AL126
ENET_88E2110_RX_p	SGMII receive data	HIGH SPEED DIFFERENTIAL I/O	J1_C16	PIN_AK135
ENET_88E2110_RX_n	SGMII receive data	HIGH SPEED DIFFERENTIAL I/O	J1_C17	PIN_AK133
ENET_88E2110_REFCLK_125M_p	88E1512 reference clock	CML		PIN_AT120
ENET_88E2110_INT_n	Interrupt output pin	3.3-V LVCMOS	J2_A10	PIN_F8
ENET_88E2110_MDC	Management data clock reference	3.3-V LVCMOS	J2_A15	PIN_K4
ENET_88E2110_MDIO	Management data	3.3-V LVCMOS	J2_C17	PIN_H18
ENET_88E2110_RESET_n	88E1512 reset pin	3.3-V LVCMOS	J2_G14	PIN_D15

2.12 USB OTG Connector

The carrier board provides an USB OTG interfaces, a SMSC USB3320 device in a 32-pin QFN package device on the carrier board is used to interface to a single Type AB Micro-USB connector. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device modes. When operating in Host mode, the interface will supply the power to the device through the Micro-USB interface. **Figure 2-22** shows the connections between the USB OTG connector, 400-pin B2B connector and Agilx 5 SoC FPGA. **Table 2-16** lists the pin assignment of USB OTG PHY to HPS.

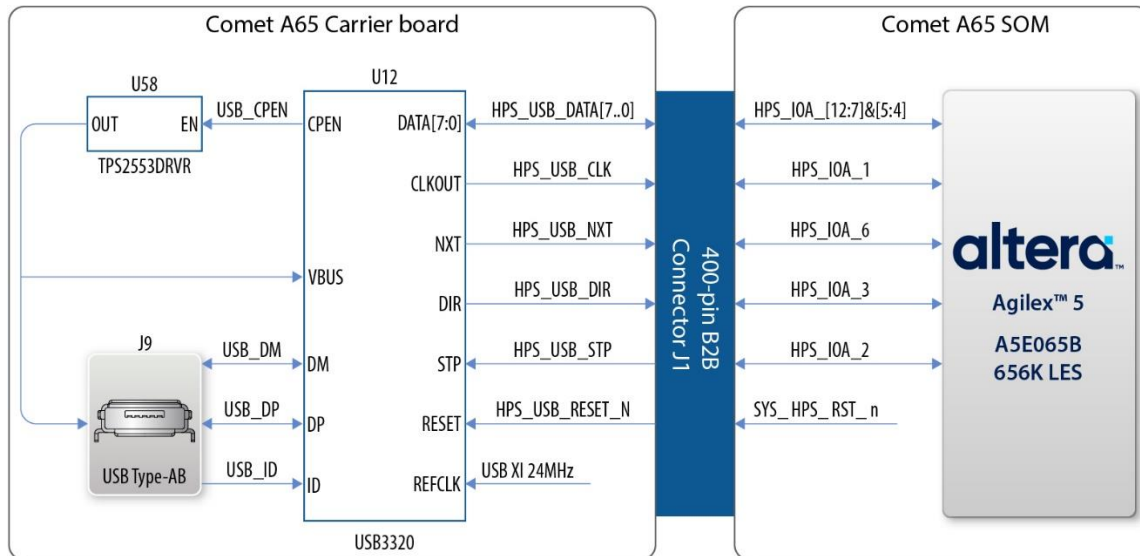


Figure 2-22 Connection between the USB OTG connector and Agilx 5 SoC FPGA

Table 2-16 The pin assignment of USB OTG PHY on the Comet A65 Carrier board

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A65 FPGA Pin Num.
HPS_USB_CLK	Reference Clock Output	1.8 V	J1_C4	PIN_W135
HPS_USB_DATA[0]	HPS USB_DATA[0]	1.8 V	J1_C10	PIN_AK115
HPS_USB_DATA[1]	HPS USB_DATA[1]	1.8 V	J1_E4	PIN_U134
HPS_USB_DATA[2]	HPS USB_DATA[2]	1.8 V	J1_D3	PIN_R134
HPS_USB_DATA[3]	HPS USB_DATA[3]	1.8 V	J1_C8	PIN_AG115
HPS_USB_DATA[4]	HPS USB_DATA[4]	1.8 V	J1_E3	PIN_N135
HPS_USB_DATA[5]	HPS USB_DATA[5]	1.8 V	J1_A8	PIN_AK120
HPS_USB_DATA[6]	HPS USB_DATA[6]	1.8 V	J1_G2	PIN_N134
HPS_USB_DATA[7]	HPS USB_DATA[7]	1.8 V	J1_F2	PIN_T132
HPS_USB_DIR	Direction of the Data Bus	1.8 V	J1_B4	PIN_W134
HPS_USB_NXT	Throttle the Data	1.8 V	J1_A10	PIN_AL120
HPS_USB_STP	Stop Data Stream on the Bus	1.8 V	J1_B3	PIN_U135

2.13 PCI Express

The carrier board features a PCI Express edge connector designed for a standard x8 PCIe slot on a PC motherboard. When populated with the SOM, the board provides a fully integrated, PCI Express 4.0 compliant solution by leveraging the device's built-in transceivers and dedicated Hard IP (HIP) block.

This HIP approach simplifies protocol implementation and conserves logic resources for your application. The interface supports multi-lane configurations (x1 and x4) and is compatible with Gen1 (2.5 Gbps/lane), Gen2 (5.0 Gbps/lane), Gen3 (8.0 Gbps/lane) and Gen 4 (16.0 Gbps/lane) data rates. Lane width is user-configurable via a DIP switch (SW3), as detailed in section 2.3.

For power, if user's PCIe slot can provide 75W power and the carrier board does not have any external daughter card (such as 2x20 GPIO daughter card), an external 12V power isn't necessary, otherwise the external 12V DC power should be provided, as this auxiliary power is essential to prevent system instability or permanent FPGA damage due to insufficient power.

Figure 2-23 shows the connections between the PCIe and Agilex 5 SoC FPGA. **Table 2-17** lists the pin assignment of PCIe and Agilex 5 SoC FPGA.

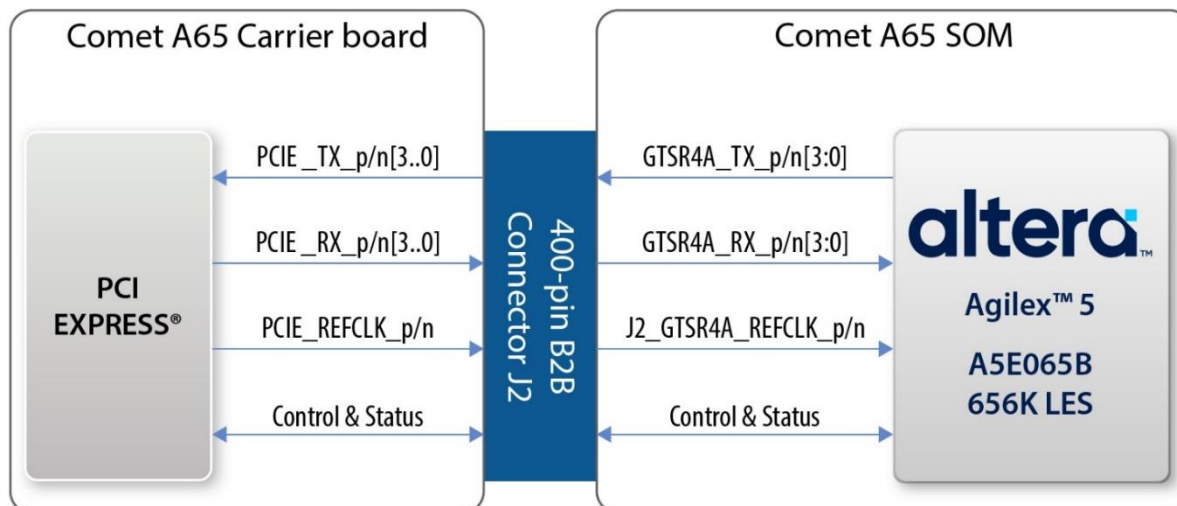


Figure 2-23 Connection between the PCIe edge connector and Agilex 5 SoC FPGA

Table 2-17 Pin Assignment of PCIe and FPGA on Comet A65 SoM

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A65 FPGA Pin Num.
PCIE_TX_p0	Add-in card transmit bus	HIGH Speed Differential I/O	J2_G39	PIN_BY7
PCIE_TX_p1	Add-in card transmit bus	HIGH Speed Differential I/O	J2_H37	PIN_BT7
PCIE_TX_p2	Add-in card transmit bus	HIGH Speed Differential I/O	J2_H33	PIN_BL7
PCIE_TX_p3	Add-in card transmit bus	HIGH Speed Differential I/O	J2_E35	PIN_BG7
PCIE_TX_n0	Add-in card transmit bus	HIGH Speed Differential I/O	J2_G40	PIN_BY10
PCIE_TX_n1	Add-in card transmit bus	HIGH Speed Differential I/O	J2_H38	PIN_BT10
PCIE_TX_n2	Add-in card transmit bus	HIGH Speed Differential I/O	J2_H34	PIN_BL10
PCIE_TX_n3	Add-in card transmit bus	HIGH Speed Differential I/O	J2_E36	PIN_BG10
PCIE_RX_p0	Add-in card receive bus	HIGH Speed Differential I/O	J2_E43	PIN_CB1
PCIE_RX_p1	Add-in card receive bus	HIGH Speed Differential I/O	J2_F41	PIN_BV1
PCIE_RX_p2	Add-in card receive bus	HIGH Speed Differential I/O	J2_E39	PIN_BN1
PCIE_RX_p3	Add-in card receive bus	HIGH Speed Differential I/O	J2_F37	PIN_BJ1
PCIE_RX_n0	Add-in card receive bus	HIGH Speed Differential I/O	J2_E44	PIN_CB3
PCIE_RX_n1	Add-in card receive bus	HIGH Speed Differential I/O	J2_F42	PIN_BV3
PCIE_RX_n2	Add-in card receive bus	HIGH Speed Differential I/O	J2_E40	PIN_BN3
PCIE_RX_n3	Add-in card receive bus	HIGH Speed Differential I/O	J2_F38	PIN_BJ3
PCIE_SMBCLK	PCIe system management bus clock	3.3-V LVCMOS	J2_A16	PIN_K8
PCIE_SMBDAT	PCIe system management Bus data	3.3-V LVCMOS	J2_F14	PIN_D4
PCIE_REFCLK_p	PCIe reference clock, positive (Differential)	CURRENT MODE LOGIC (CML)	J2_H25	PIN_BC29
PCIE_PERST_n	PCIe fundamental reset, active Low	3.3-V LVCMOS	J2_A18	PIN_BE29

2.14 USB to UART

As shown in the block diagram in **Figure 2-24**, the board provides two independent UART (Universal Asynchronous Receiver-Transmitter) communication interfaces through a single USB Type-C port, allowing users to conveniently interact with the system. These two interfaces are enabled by an on-board Silicon Labs CP2105 USB-to-Dual-UART Bridge Controller.

When the development board is connected to a computer via the USB Type-C cable, two virtual COM ports will appear in the computer's Device Manager. Their functions are as follows:

- **HPS UART:** This interface is primarily used for communication with the HPS (Hard Processor System) on the SOM. It allows users to access the HPS console, view boot messages, execute Linux commands, and perform software debugging. This serves as the primary channel for interacting with the operating system.
- **BMC UART:** This interface is used for communication with the BMC (Board Management Controller) in the system MAX10 FPGA of the SOM. The BMC is responsible for monitoring and managing the board's hardware status, such as power, temperature, and fan speed.

For instructions on how to install the drivers for these two UART interfaces, please refer to [Getting_Start_Guide_for_Comet_A65_SOM_EVK.pdf](#).

Note: The signal from the USB Type-C connector is first routed to a USB Hub. It then branches out to the CP2105 (providing the dual UART function) and the USB Blaster III circuit.

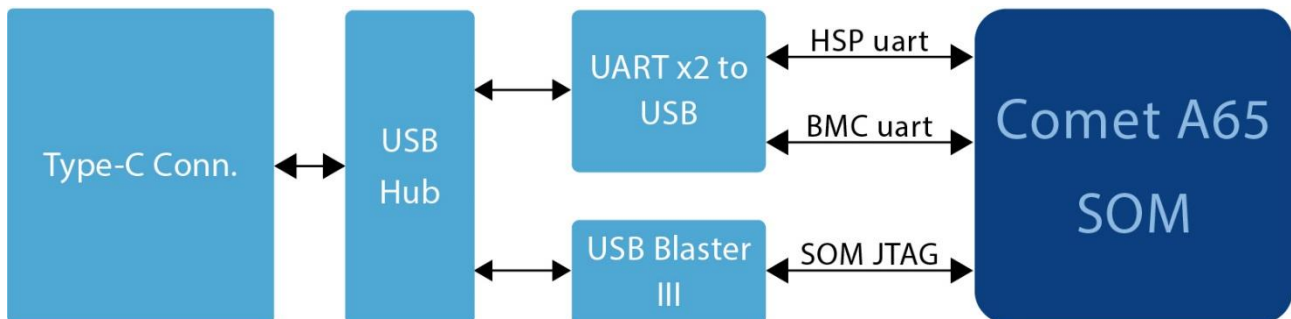


Figure 2-24 Block diagram of the USB UART interface

2.15 HPS MicroSD Card

The Comet A65 carrier board provides Micro SD Card with x4 data lines for HPS fabric in the FPGA (See **Figure 2-25**). Users can choose it for HPS boot/data/system storage. Please note that the switch SW1 on the Comet A65 SoM module can help the user select which device (Micro SD Card or eMMC) will be used for HPS fabric. **Table 2-18** lists the pin assignment of Micro SD card socket to the HPS.

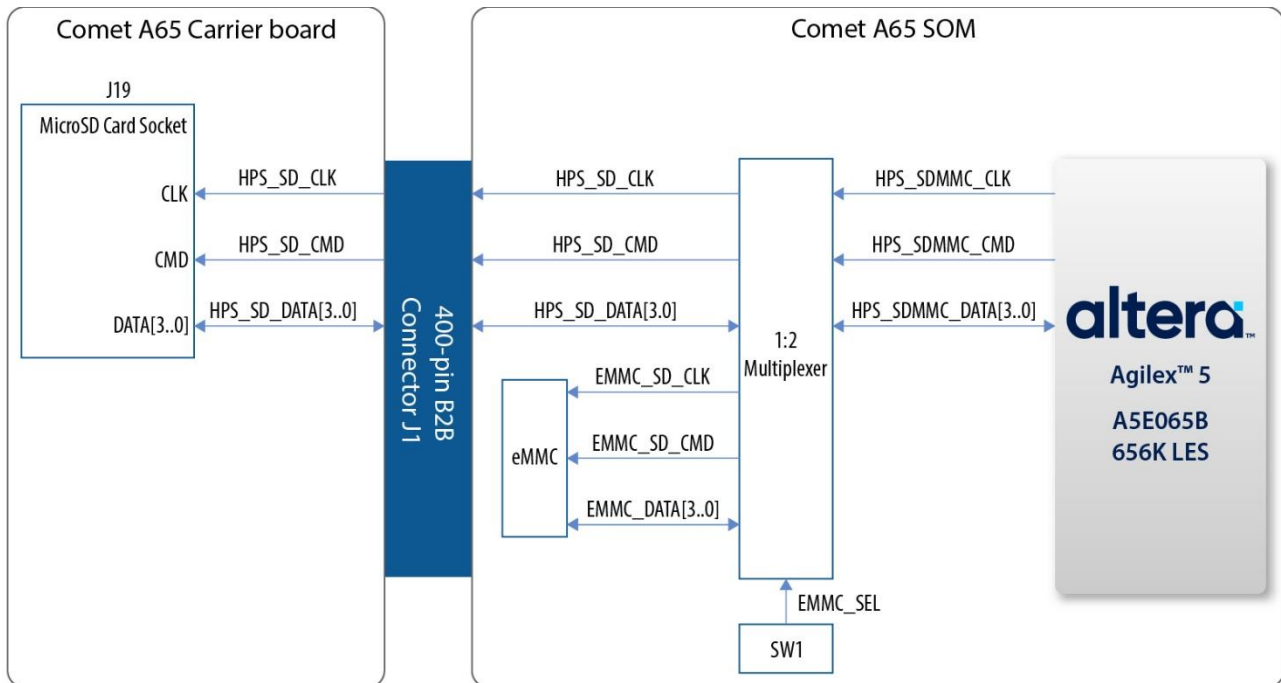


Figure 2-25 Connections between Micro SD card socket and Agilex 5 SoC FPGA

Table 2-18 The pin assignment of Micro SD card socket

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A65 FPGA Pin Num.
HPS_SD_CLK	HPS SD Clock	1.8 V	J1_B6	PIN_D132
HPS_SD_CMD	HPS SD Command Line	1.8 V	J1_A6	PIN_AB132
HPS_SD_DATA[0]	HPS SD_DATA[0]	1.8 V	J1_D6	PIN_E135
HPS_SD_DATA[1]	HPS SD_DATA[1]	1.8 V	J1_C6	PIN_F132
HPS_SD_DATA[2]	HPS SD_DATA[2]	1.8 V	J1_E6	PIN_AA135
HPS_SD_DATA[3]	HPS SD_DATA[3]	1.8 V	J1_F6	PIN_V127

2.16 HDMI TX

The development board provides a high performance DVI-compliant digital transmitter via the TI TFP410, which incorporates DVI v1.0 features and supports pixel rates up to 165MHz, including 1080p and WUXGA at 60Hz. The TFP410 is controlled via a serial I2C bus interface, which is connected to pins on the Agilex 5 SoC FPGA and output via HDMI TX interface on Comet A65 carrier board. A schematic diagram of the circuitry is shown in **Figure 2-26**. Detailed information on using the TFP410 is available on the manufacturer's website, or under the Datasheets\HDMI folder in the Comet A65 carrier board System CD.

Table 2-19 lists the HDMI Interface pin assignments and signal names relative to the FPGA.

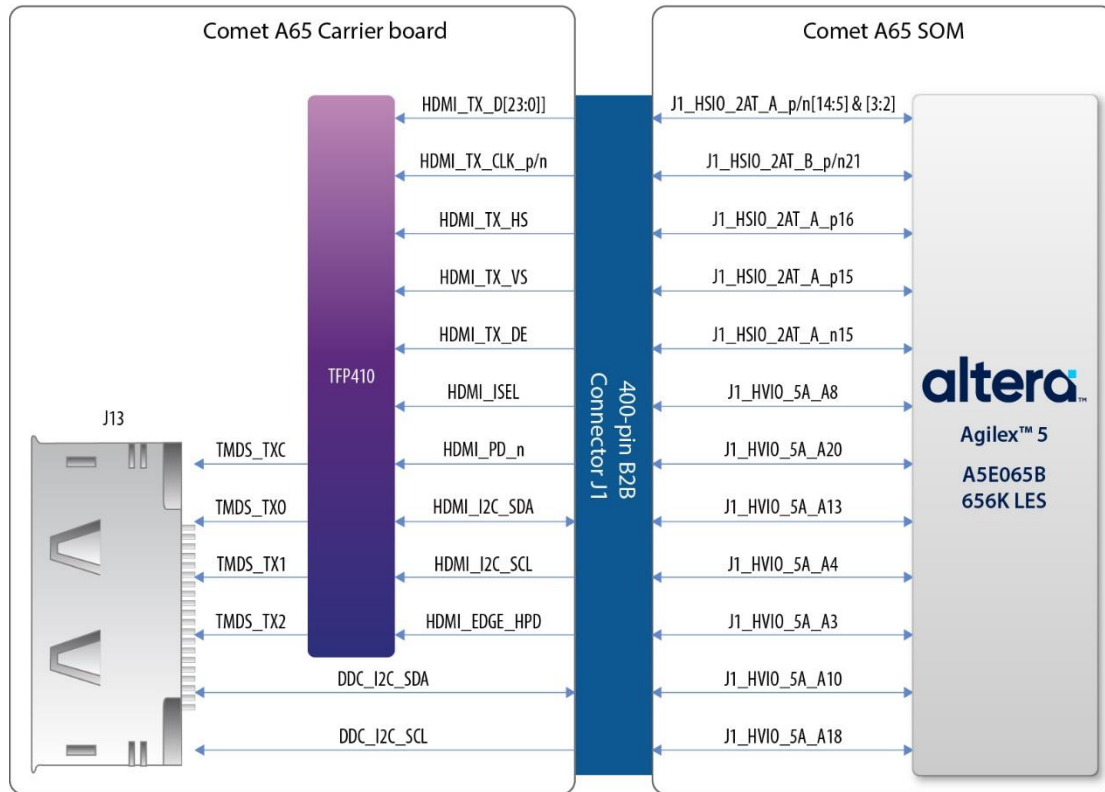


Figure 2-26 Connections between the FPGA and DVI Transmitter Chip

Table 2-19 Pin Assignment of HMDI

Schematic Signal Name	Description	I/O Standard	Comet A65 FPGA Pin Num.
HDMI_TX_D[0]	Video Data bus	1.2 V	PIN_CF62
HDMI_TX_D[1]	Video Data bus	1.2 V	PIN_CH62
HDMI_TX_D[2]	Video Data bus	1.2 V	PIN_CA62
HDMI_TX_D[3]	Video Data bus	1.2 V	PIN_CC62
HDMI_TX_D[4]	Video Data bus	1.2 V	PIN_CC71
HDMI_TX_D[5]	Video Data bus	1.2 V	PIN_CA71
HDMI_TX_D[6]	Video Data bus	1.2 V	PIN_CF71
HDMI_TX_D[7]	Video Data bus	1.2 V	PIN_CH71
HDMI_TX_D[8]	Video Data bus	1.2 V	PIN_BW59
HDMI_TX_D[9]	Video Data bus	1.2 V	PIN_CA59
HDMI_TX_D[10]	Video Data bus	1.2 V	PIN_BU59
HDMI_TX_D[11]	Video Data bus	1.2 V	PIN_BR59
HDMI_TX_D[12]	Video Data bus	1.2 V	PIN_BU62
HDMI_TX_D[13]	Video Data bus	1.2 V	PIN_BR62
HDMI_TX_D[14]	Video Data bus	1.2 V	PIN_BW69
HDMI_TX_D[15]	Video Data bus	1.2 V	PIN_CA69
HDMI_TX_D[16]	Video Data bus	1.2 V	PIN_BR71
HDMI_TX_D[17]	Video Data bus	1.2 V	PIN_BU71
HDMI_TX_D[18]	Video Data bus	1.2 V	PIN_BR69

HDMI_TX_D[19]	Video Data bus	1.2 V	PIN_BU69
HDMI_TX_D[20]	Video Data bus	1.2 V	PIN_BM59
HDMI_TX_D[21]	Video Data bus	1.2 V	PIN_BK59
HDMI_TX_D[22]	Video Data bus	1.2 V	PIN_BH62
HDMI_TX_D[23]	Video Data bus	1.2 V	PIN_BH59
DDC_I2C_SCL	Serial Port Data Clock to Sink	3.3-V LVCMOS	PIN_CL130
DDC_I2C_SDA	Serial Port Data Input/Output to Sink	3.3-V LVCMOS	PIN_CL125
HDMI_I2C_SCL	FPGA I2C Clock	3.3-V LVCMOS	PIN_CG135
HDMI_I2C_SDA	FPGA I2C Data	3.3-V LVCMOS	PIN_BU118
HDMI_TX_HS	Horizontal Synchronization	1.2 V	PIN_BM69
HDMI_TX_VS	Vertical Synchronization	1.2 V	PIN_BM62
HDMI_TX_DE	Data Enable Signal for Digital Video	1.2 V	PIN_BP62
HDMI_TX_CLK_p	HDMI transmitter clock	DIFFERENTIAL 1.2-V SSTL	PIN_BE83
HDMI_EDGE_HPD	Edge select/hot plug input	3.3-V LVCMOS	PIN_CG134
HDMI_ISEL	I ² C interface select/I ² C reset	3.3-V LVCMOS	PIN_CK134
HDMI_PD_n	Power down (active low)	3.3-V LVCMOS	PIN_CK128

2.17 QTH-030 Connector

The Comet A65 carrier board provides one 60-pin high speed QTH-030 connector (Part Number: QTH-030-02-L-D-A) that can be used as expansion header. It provides 4 single-ended signals and 16 LVDS channels which can run up to 1.6Gbps. Users can design their own daughter card for interface expansion. The part number of the connector required on the expansion daughter card is QSH-030-01-F-D-A-K-TR. Detailed information of the QTH-030 connector is available in the Datasheets\QTH-030 folder in the Comet A65 carrier board System CD.

A schematic diagram of the QTH-030 connector is shown in **Figure 2-27**. **Table 2-20** lists the connector pin assignments and signal names relative to the FPGA.

Note: If LVDS TX is required, please set the SW2 to ON position for I/O Standard 1.3V. When only LVDS RX is required, set it to OFF position for I/O Standard 1.2V.

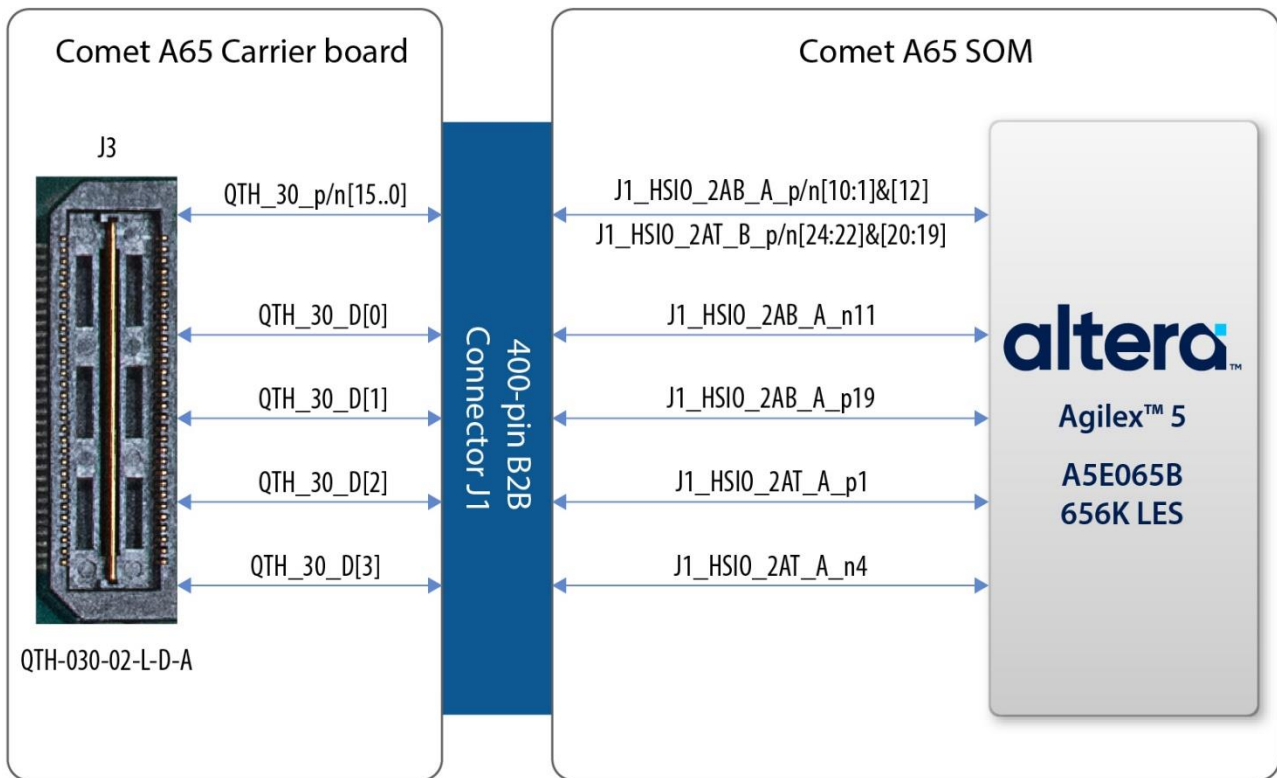


Figure 2-27 Connections between the QTH-030 connector and Agilex 5 SoC FPGA

Table 2-20 Pin Assignment of QTH-030 connector

Schematic Signal Name	Description	I/O Standard	Comet A65 FPGA Pin Num.
QTH_30_p[0]	LVDS Data Positive bit 0	1.2 V	PIN_BW89
QTH_30_p[1]	LVDS Data Positive bit 1	1.2 V	PIN_BE79
QTH_30_p[2]	LVDS Data Positive bit 2	1.2 V	PIN_BM81
QTH_30_p[3]	LVDS Data Positive bit 3	1.2 V	PIN_BH89
QTH_30_p[4]	LVDS Data Positive bit 4	1.2 V	PIN_BF93
QTH_30_p[5]	LVDS Data Positive bit 5	1.2 V	PIN_BE96
QTH_30_p[6]	LVDS Data Positive bit 6	1.2 V	PIN_BW78
QTH_30_p[7]	LVDS Data Positive bit 7	1.2 V	PIN_BK89
QTH_30_p[8]	LVDS Data Positive bit 8	1.2 V	PIN_BR78
QTH_30_p[9]	LVDS Data Positive bit 9	1.2 V	PIN_BP92
QTH_30_p[10]	LVDS Data Positive bit 10	1.2 V	PIN_BR81
QTH_30_p[11]	LVDS Data Positive bit 11	1.2 V	PIN_BF86
QTH_30_p[12]	LVDS Data Positive bit 12	1.2 V	PIN_BR89
QTH_30_p[13]	LVDS Data Positive bit 13	1.2 V	PIN_BF75
QTH_30_p[14]	LVDS Data Positive bit 14	1.2 V	PIN_BM78
QTH_30_p[15]	LVDS Data Positive bit 15	1.2 V	PIN_BH81
QTH_30_n[0]	LVDS Data Negative bit 0	1.2 V	PIN_CA89
QTH_30_n[1]	LVDS Data Negative bit 1	1.2 V	PIN_BE75
QTH_30_n[2]	LVDS Data Negative bit 2	1.2 V	PIN_BP81
QTH_30_n[3]	LVDS Data Negative bit 3	1.2 V	PIN_BH92

QTH_30_n[4]	LVDS Data Negative bit 4	1.2 V	PIN_BF90
QTH_30_n[5]	LVDS Data Negative bit 5	1.2 V	PIN_BE93
QTH_30_n[6]	LVDS Data Negative bit 6	1.2 V	PIN_CA78
QTH_30_n[7]	LVDS Data Negative bit 7	1.2 V	PIN_BM89
QTH_30_n[8]	LVDS Data Negative bit 8	1.2 V	PIN_BU78
QTH_30_n[9]	LVDS Data Negative bit 9	1.2 V	PIN_BM92
QTH_30_n[10]	LVDS Data Negative bit 10	1.2 V	PIN_BU81
QTH_30_n[11]	LVDS Data Negative bit 11	1.2 V	PIN_BE86
QTH_30_n[12]	LVDS Data Negative bit 12	1.2 V	PIN_BU89
QTH_30_n[13]	LVDS Data Negative bit 13	1.2 V	PIN_BF72
QTH_30_n[14]	LVDS Data Negative bit 14	1.2 V	PIN_BK78
QTH_30_n[15]	LVDS Data Negative bit 15	1.2 V	PIN_BH78
QTH_30_D[0]	Single-ended Signal Data	1.2 V	PIN_BU92
QTH_30_D[1]	Single-ended Signal Data	1.2 V	PIN_CK76
QTH_30_D[2]	Single-ended Signal Data	1.2 V	PIN_CF59
QTH_30_D[3]	Single-ended Signal Data	1.2 V	PIN_CF69

2.18 SLVS-EC Connector

The Comet A65 carrier board provides one 50-pin high speed SLVS-EC (Scalable Low-Voltage Signaling with Embedded Clock) connector, which is the next-generation, high-speed interface for high-resolution CMOS image sensors. The interface's simple protocol makes it easy to build camera systems. Featuring an embedded clock signal, it is ideal for applications that require higher speed, fewer lanes, or transmission over longer distances.

There are eight RX channels for the SLVS-EC connector on Comet A65 Carrier board, which can run up to 5Gbps per channel. A schematic diagram of the SLVS-EC connector is shown in **Figure 2-28**. **Table 2-21** lists the connector pin assignments and signal names relative to the FPGA.

Note: Please make sure the SW6 is correctly set for 144MHz or 148.5MHz SLVS_EC_REFCLK_p.

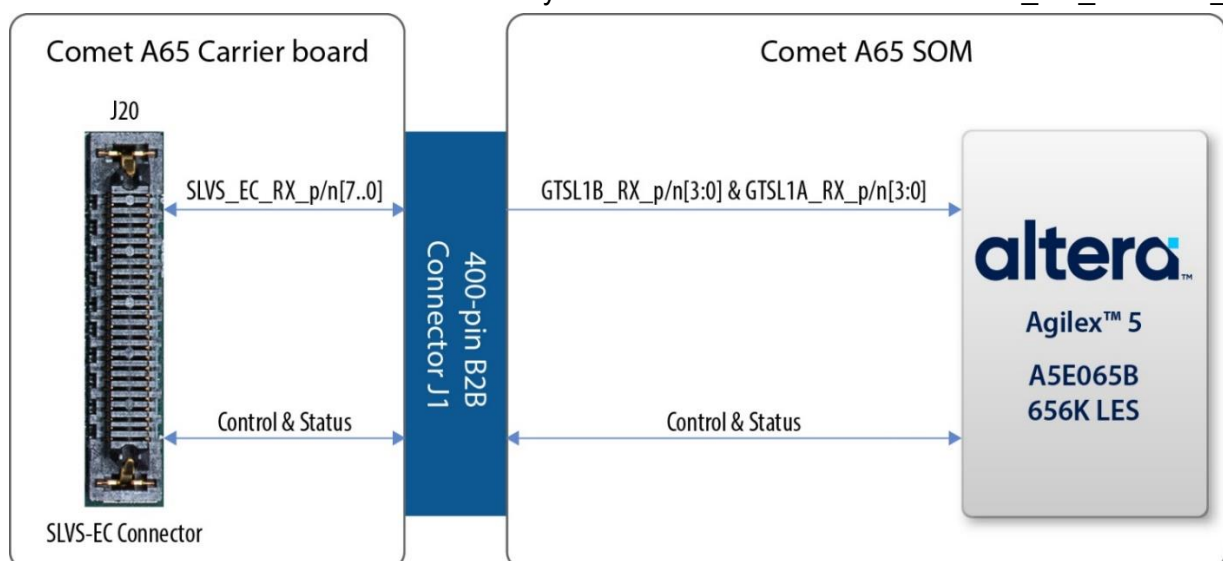


Figure 2-28 Connections between the SLVS-EC connector and Agilex 5 SoC FPGA

Table 2-21 Pin Assignment of SLVS-EC connector

Schematic Signal Name	Description	I/O Standard	Comet A65 FPGA Pin Num.
SLVS_EC_RX_p[0]	Differential RX Data 0	HIGH SPEED DIFFERENTIAL I/O	PIN_BV135
SLVS_EC_RX_p[1]	Differential RX Data 1	HIGH SPEED DIFFERENTIAL I/O	PIN_BN135
SLVS_EC_RX_p[2]	Differential RX Data 2	HIGH SPEED DIFFERENTIAL I/O	PIN_BJ135
SLVS_EC_RX_p[3]	Differential RX Data 3	HIGH SPEED DIFFERENTIAL I/O	PIN_BF135
SLVS_EC_RX_p[4]	Differential RX Data 4	HIGH SPEED DIFFERENTIAL I/O	PIN_BD135
SLVS_EC_RX_p[5]	Differential RX Data 5	HIGH SPEED DIFFERENTIAL I/O	PIN_BB135
SLVS_EC_RX_p[6]	Differential RX Data 6	HIGH SPEED DIFFERENTIAL I/O	PIN_AY135
SLVS_EC_RX_p[7]	Differential RX Data 7	HIGH SPEED DIFFERENTIAL I/O	PIN_AV135
SLVS_EC_RX_n[0]	Differential RX Data 0	HIGH SPEED DIFFERENTIAL I/O	PIN_BV133
SLVS_EC_RX_n[1]	Differential RX Data 1	HIGH SPEED DIFFERENTIAL I/O	PIN_BN133
SLVS_EC_RX_n[2]	Differential RX Data 2	HIGH SPEED DIFFERENTIAL I/O	PIN_BJ133
SLVS_EC_RX_n[3]	Differential RX Data 3	HIGH SPEED DIFFERENTIAL I/O	PIN_BF133
SLVS_EC_RX_n[4]	Differential RX Data 4	HIGH SPEED DIFFERENTIAL I/O	PIN_BD133
SLVS_EC_RX_n[5]	Differential RX Data 5	HIGH SPEED DIFFERENTIAL I/O	PIN_BB133
SLVS_EC_RX_n[6]	Differential RX Data 6	HIGH SPEED DIFFERENTIAL I/O	PIN_AY133
SLVS_EC_RX_n[7]	Differential RX Data 7	HIGH SPEED DIFFERENTIAL I/O	PIN_AV133
SLVS_EC_SDO	SPI miso signal	1.8-V LVCMOS	PIN_A20
SLVS_EC_REFCLK_p	Reference clock, positive (Differential)	CURRENT MODE LOGIC (CML)	PIN_BC111
SLVS_EC_INCK_OE	Enable Clock generator on the Sensor Card	1.8-V LVCMOS	PIN_A14
SLVS_EC_OMODE	SLVS-EC/SLVS switch (High: SLVS-EC)	1.8-V LVCMOS	PIN_B35
SLVS_EC_SCK_SCL	Serial Port Clock	1.8-V LVCMOS	PIN_B11
SLVS_EC_SDI_SDA	Serial Port Input Data	1.8-V LVCMOS	PIN_A35
SLVS_EC_SENSOR_PGOOD	Represents power status of Sensor Card	1.8-V LVCMOS	PIN_B20
SLVS_EC_SENSOR_PON	Control Power Unit on the Sensor Card	1.8-V LVCMOS	PIN_B23
SLVS_EC_XCE	SPI Chip Enable	1.8-V LVCMOS	PIN_B14
SLVS_EC_XCLR	Sensor reset (Active Low)	1.8-V LVCMOS	PIN_A39
SLVS_EC_XHS	Horizontal sync signal	1.8-V LVCMOS	PIN_A8
SLVS_EC_XMASTER	Master/Slave switch (Low Master)	1.8-V LVCMOS	PIN_A23
SLVS_EC_XTRIG[1]	Triger Input 1	1.8-V LVCMOS	PIN_A17
SLVS_EC_XTRIG[2]	Triger Input 2	1.8-V LVCMOS	PIN_B4
SLVS_EC_XVS	Vertical sync signal	1.8-V LVCMOS	PIN_A11

2.19 8x50 B2B Connector

This carrier board is equipped with two 8x50 B2B connectors J1 & J2 for interfacing with Comet A65 SOM. The functionality is partitioned between the two connectors to separate power/control from the high-speed data paths, optimizing for signal integrity.

■ J1 Connector (Primarily for System Control and HPS I/O)

This connector primarily extends system control, HPS peripherals, and auxiliary signals from the carrier board to the SOM.

- **HPS Peripherals:** Extends interfaces from the SOM's Hard Processor System (HPS), such as UART, USB OTG 2.0, SD and Gigabit Ethernet, making them physically accessible to the user via connectors on the carrier board.
- **System Control & Debug:** Carries the SOM JTAG interface and other board-to-board control signals.
- **Auxiliary Signals for High-Speed Interfaces:** Transmits the **reference clocks and data bus** for interfaces like HDMI-TX, MIPI, 2.5G Ethernet, QTH, and SLVS-EC.

■ J2 Connector (Primarily for Power, High-Speed Data)

This connector is dedicated to routing the high-speed transceiver data lanes directly to the FPGA on the SOM.

- **Power Delivery:** Serves as the primary power input for the SOM, supplying VIN, VCCIO_6A & 6B & 6C & 6D and VCC12_FAN from the carrier board.
- **High-Speed Data Lanes:** Connects the main high-speed differential pairs for the PCIe and QSFP+ interfaces.
- **Associated Control Signals:** Includes control signals directly related to the high-speed data transmission.

Figure 2-29 shows the interfaces connected to the FMC+R and FMC+L connectors.

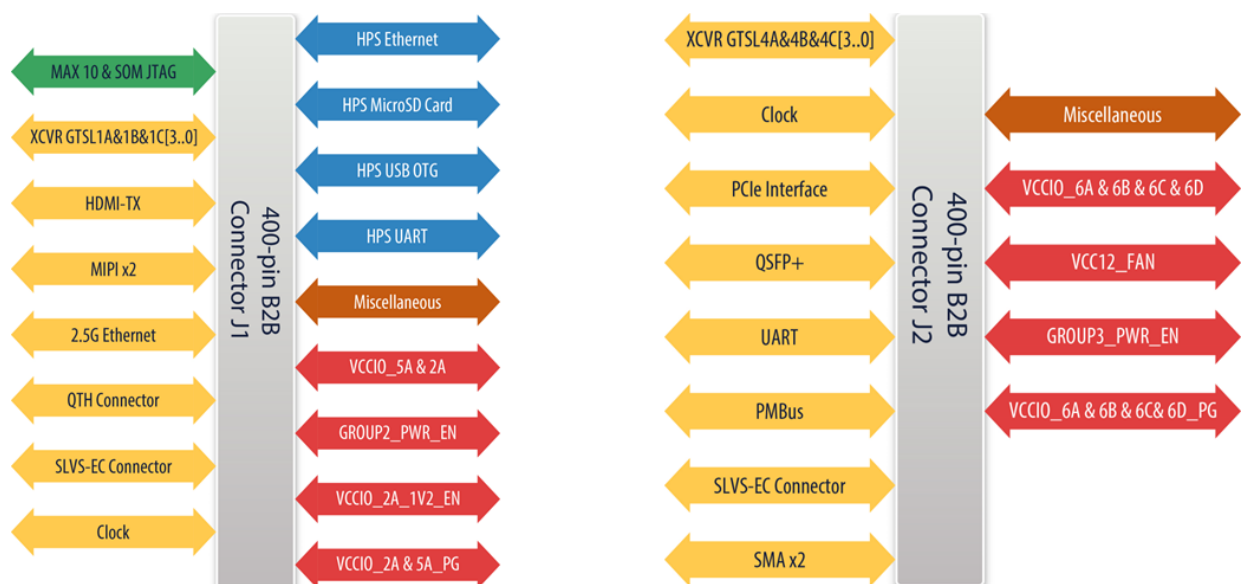


Figure 2-29 Interfaces connected to the FMC+R and FMC+L connectors.

Chapter 3

Dashboard GUI

The Comet A65 SOM Evaluation Kit Dashboard GUI is a board management system. This system is connected from the Host to the system max on the Comet A65 SOM Evaluation Kit through the UART interface, and reads various status on the board. The reported status includes FPGA/Board temperature, fan speed, FPGA core power and 12V input power. **Figure 3-1** shows the block diagram of the Comet A65 SOM Evaluation Kit Dashboard.

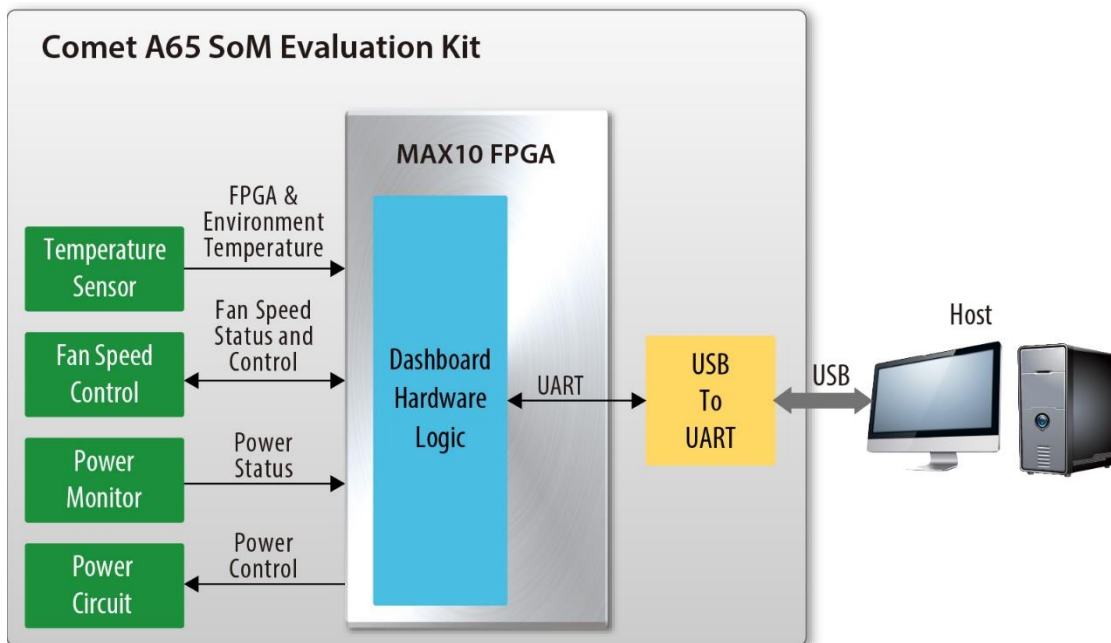


Figure 3-1 Block Diagram of the Dashboard GUI

3.1 Setup for the Dashboard GUI

To use the dashboard system, users need to install the USB to UART driver on the host first, so that user can establish a connection with the Comet A65 SOM Evaluation Kit. This section will describe how to install USB to UART driver on the windows OS host.

■ Connection Setting

Connect the USB type-C connector(J5) of the board to the host PC USB port through USB type-C cable.



Figure 3-2 Connect USB type-C cable to the board

Connect power to the Comet A65 SOM Evaluation Kit.

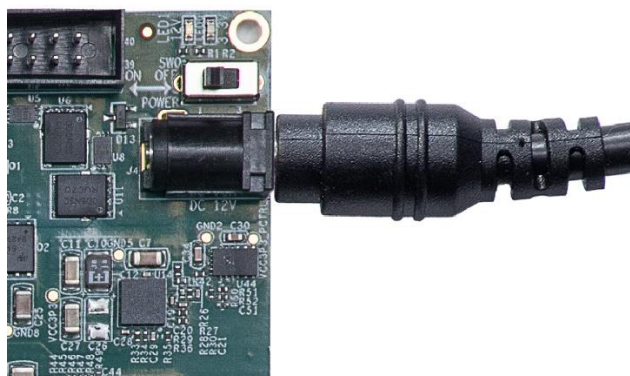


Figure 3-3 Connect power to the board

Power on the Comet A65 SOM Evaluation Kit.

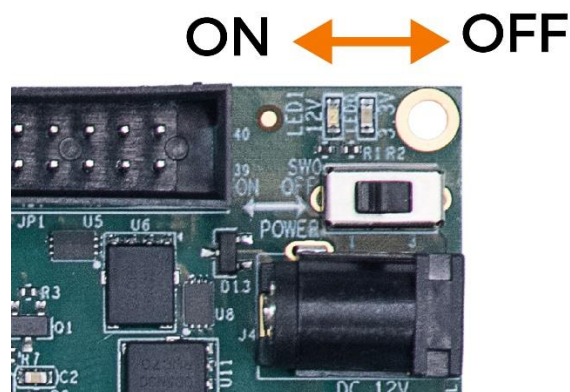


Figure 3-4 Power on the board

■ Install Driver

Please refer to the document "[The CP2105 \(USB to UART\) Driver Installation Instructions](#)" to install the driver.

After the driver installation of CP2105 is completed, two USB to UART ports can be seen in the "Device Manager" window in the Windows system of the user's computer. As shown in **Figure 3-5**, the Enhanced COM port is connected to the HPS fabric, and the Standard COM port is connected to the System MAX10. Note that the COM number (for example: COM16 and COM17) seen by each user should be different, because the hardware system of each user's computer is different.

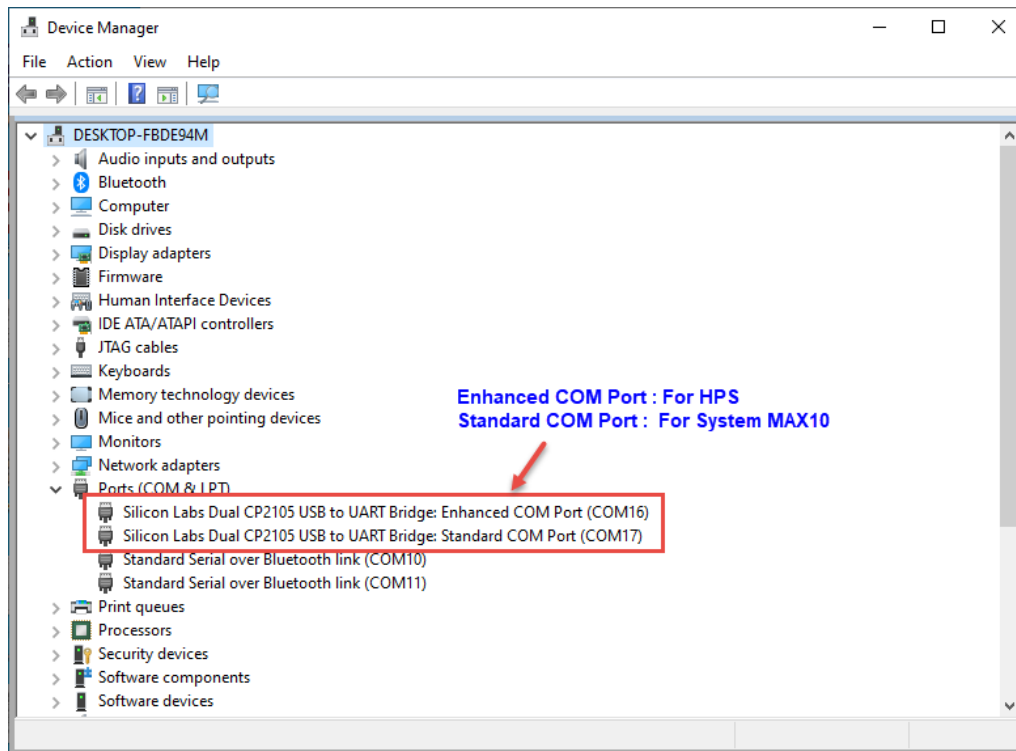


Figure 3-5 The CP2105 in the Device Manager

3.2 Run Dashboard GUI

■ Dashboard GUI software location

Users can find it from the path: Tool\dashboard_gui\Dashboard.exe in the Comet A65 SOM Evaluation Kit system CD and copy it to the host PC.

Execute the Dashboard.exe, a window will show as **Figure 3-6**. It will describe the detail functions as below.

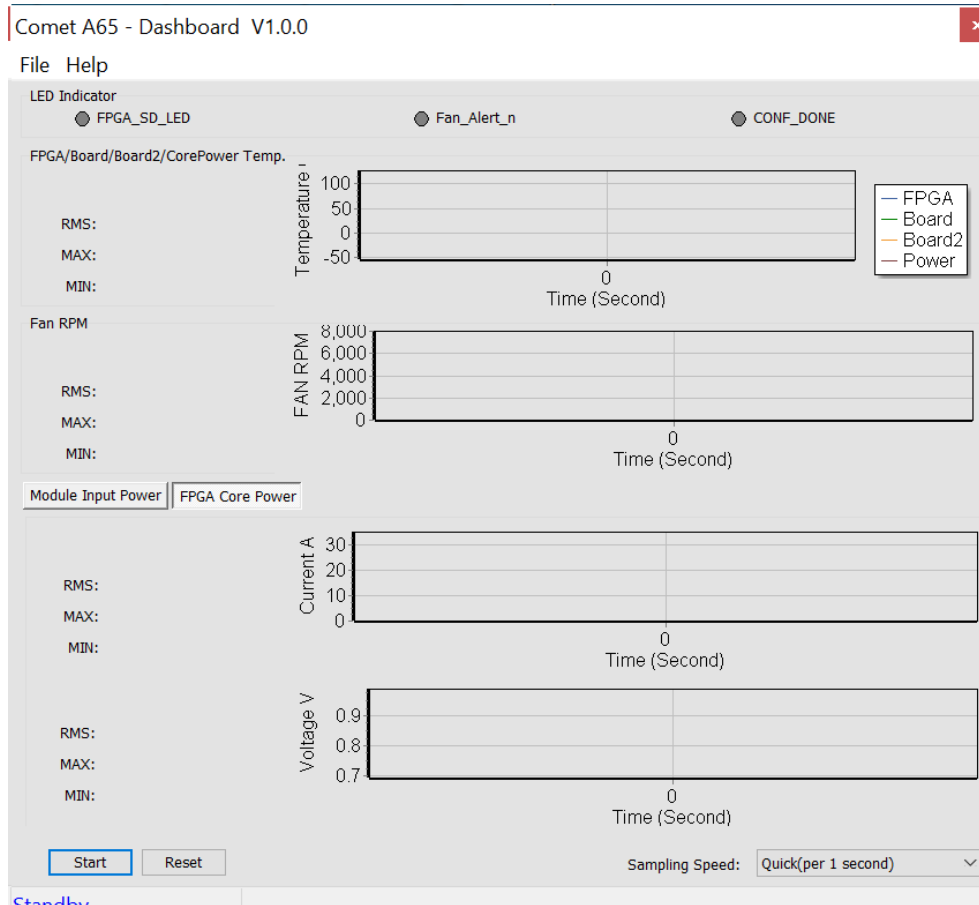


Figure 3-6 Dashboard GUI

■ Dashboard GUI function introduction

- **Start/Stop:** As shown in **Figure 3-7**, there is a **Start** button at the bottom-left of the GUI window. Click it to run the program (**Start** will change to **Stop**), it will show the Comet A65 SOM Evaluation Kit status. Users can press **Stop** button to stop the status data transmission and display.
- **Reset Button:** Press this button to clear the historical data shown in GUI, and record the data again.

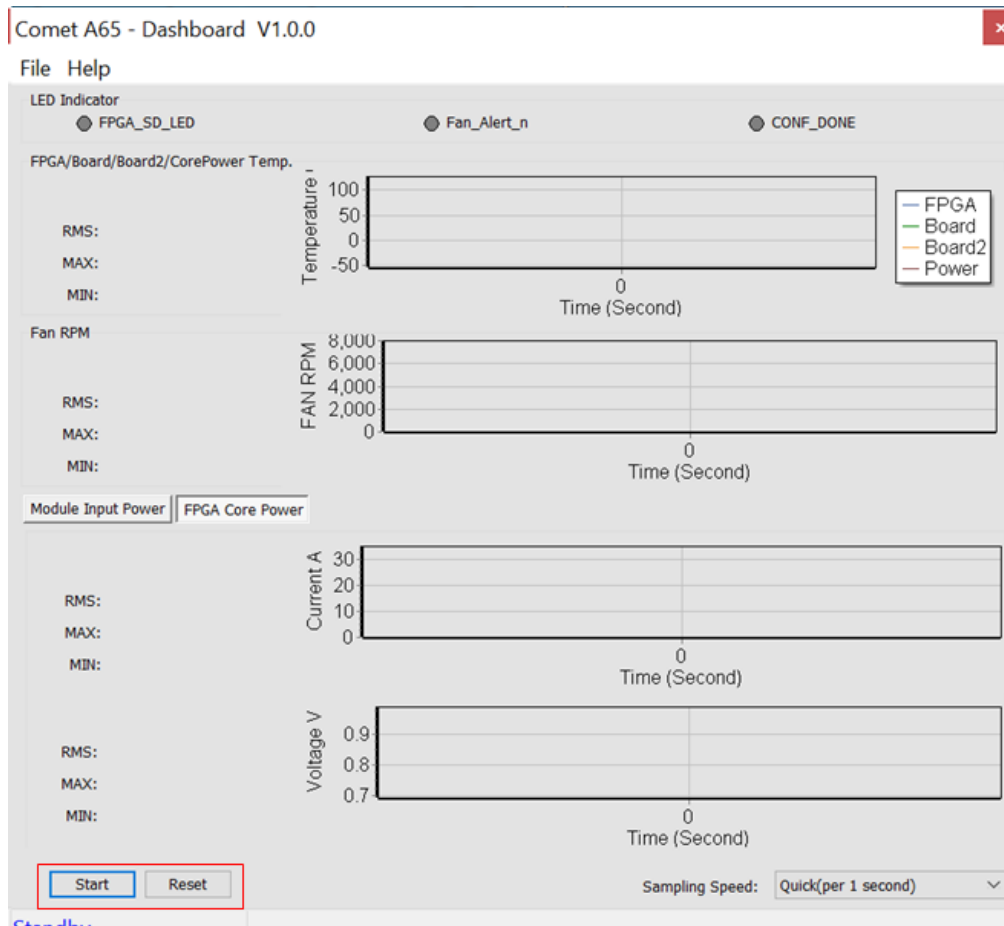


Figure 3-7 Start and Reset button

- **LED Indicator:**
 - **CONF_DONE:** As shown in [Figure 3-8](#), once you press the “Start” button, it will show the status LED number on the Comet A65 SOM Evaluation Kit. Note that “CONF_DONE” stands for FPGA configure done status. There is no LED on Comet A65 SOM Evaluation Kit to display FPGA configure status. When this status is shown in green on the GUI, it means that FPGA configuration has been completed.
 - **Fan_Alert_n:** Illuminates when the fan is abnormal, such as when the fan speed is different from expected.
 - **FPGA_SD_LED:** When this status is shown in red on the GUI, it means that the FPGA temperature or the board temperature exceeds 95 degrees. All the power of the FPGA will be cut off.

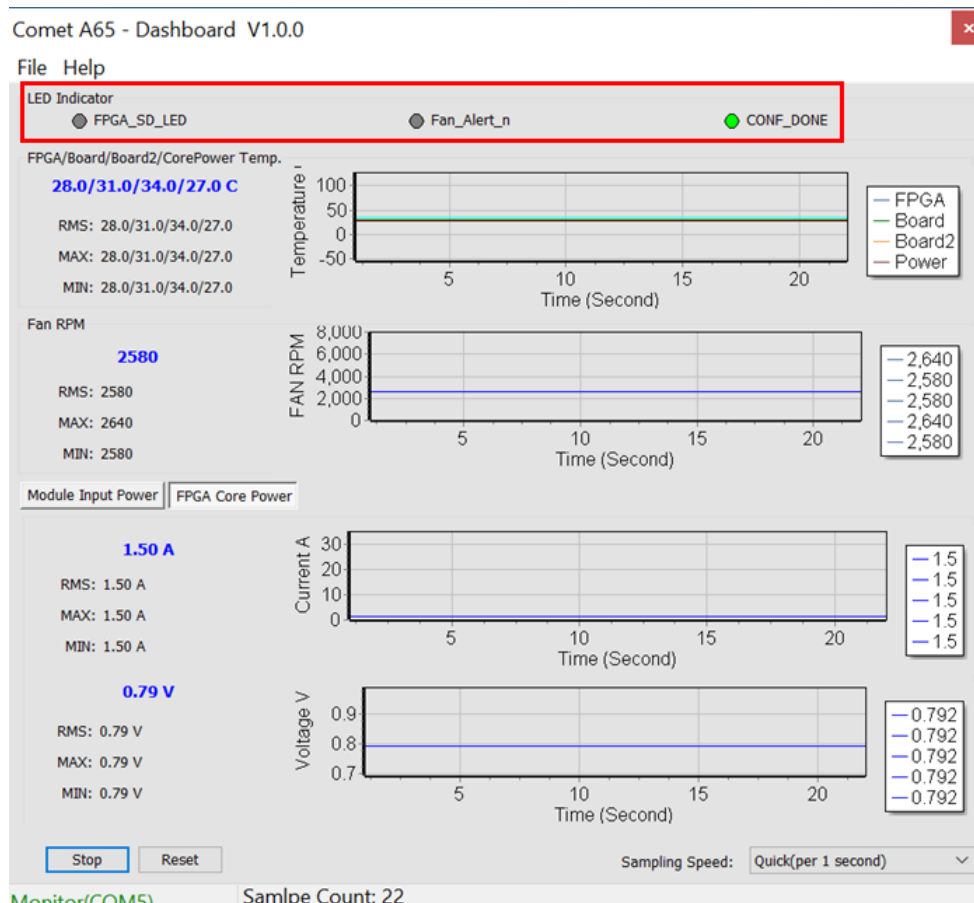


Figure 3-8 FPGA Status section

- **FPGA/Board/Board2/CorePower Temp.:** The Dashboard GUI will real-time show the fan speed, Comet A65 SOM Evaluation Kit ambient and FPGA temperature. Users can know the board temperature in time. The information will be refreshed per 1 second, and displays through diagram and number, as shown in **Figure 3-9**. **Figure 3-10** shows the location of the two temperature sensors of **Board** and **Board2** on the GUI.

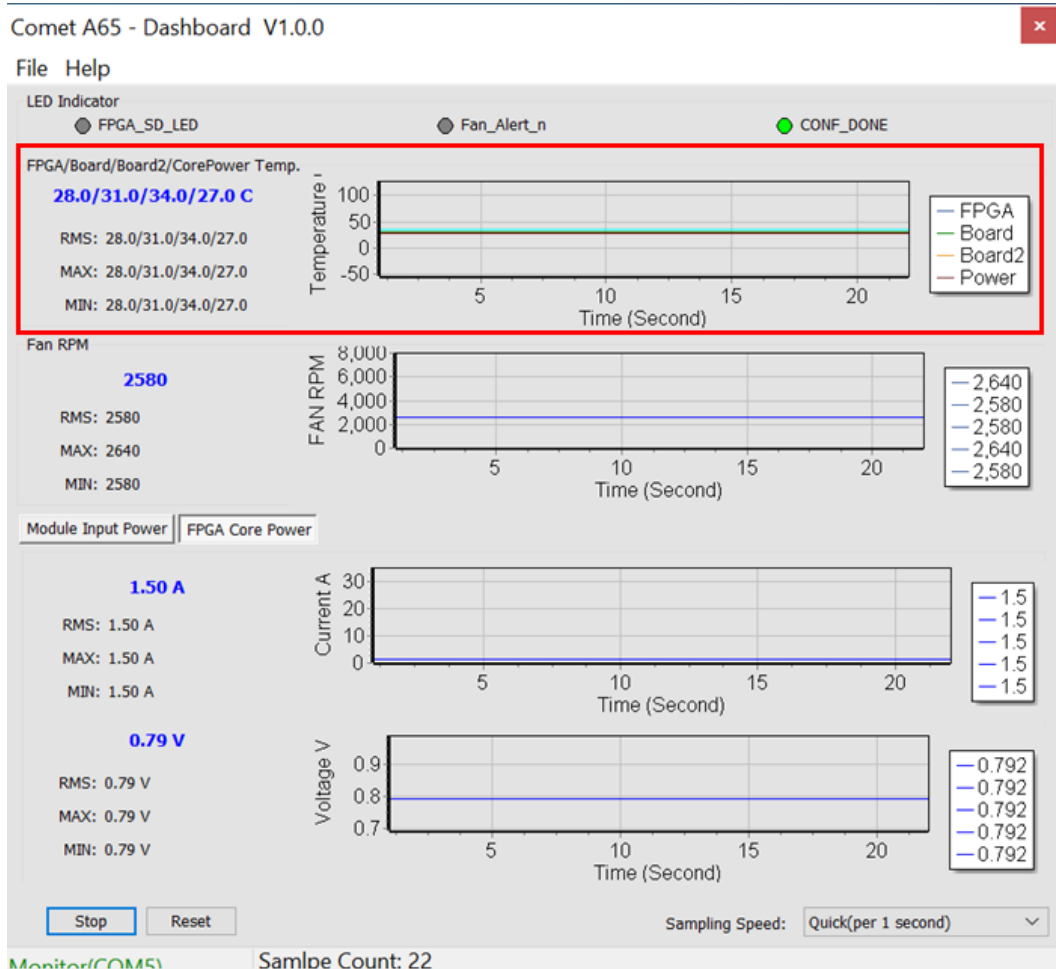


Figure 3-9 Temperature section

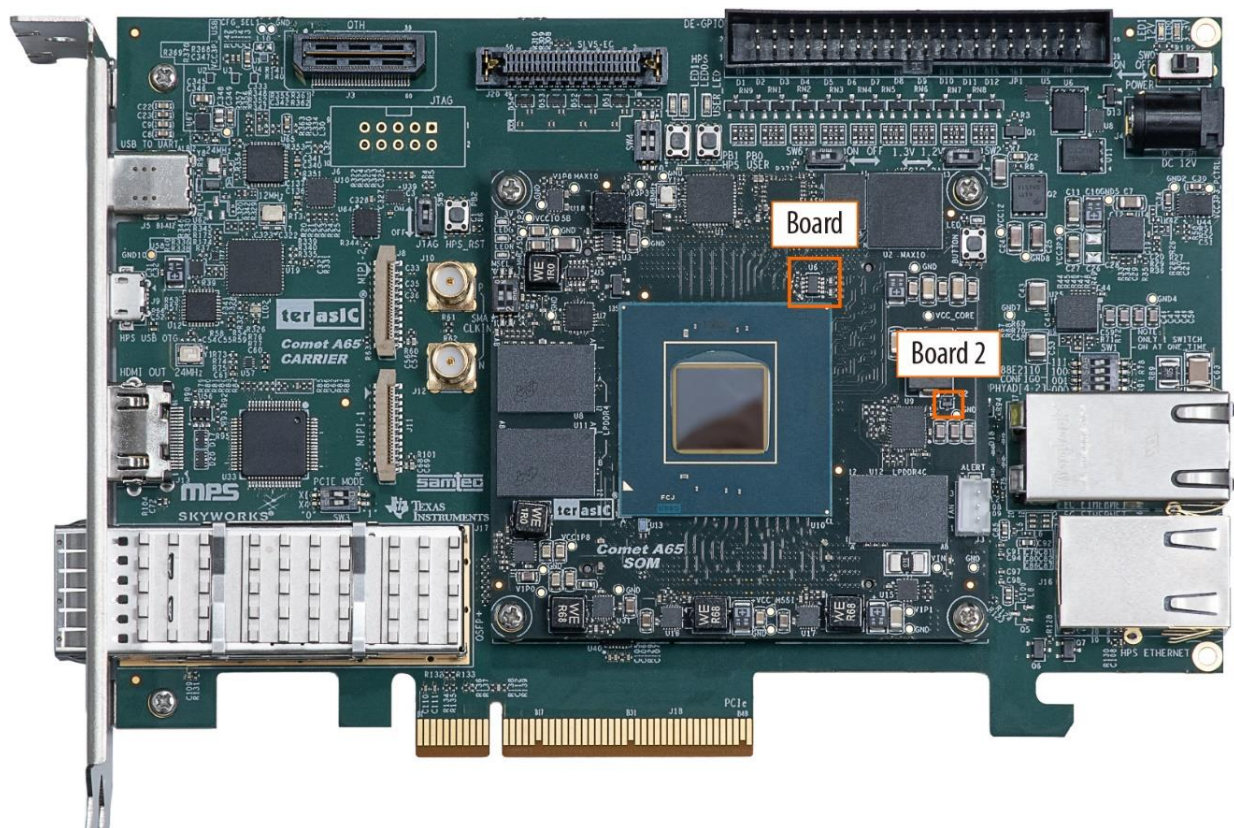


Figure 3-10 Location of the board's ambient temperature

- **Fan RPM:** It displays the real-time speed of the fan on the Comet A65 SOM Evaluation Kit, as shown in **Figure 3-11**.

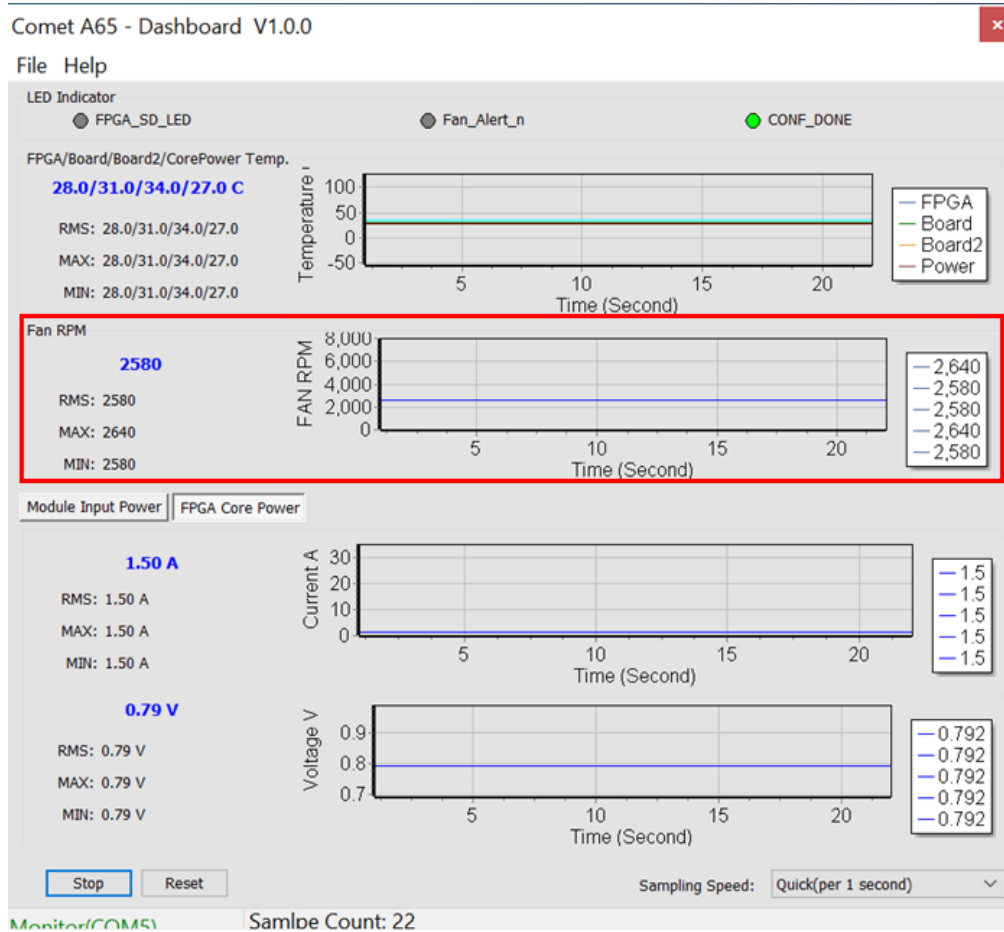


Figure 3-11 FAN RPM section

- **Module Input Power / FPGA Core Power:** It displays the real-time Comet A65 SoM module input and FPGA Core Power voltage and consumption current on the Comet A65 SOM Evaluation Kit, as shown in **Figure 3-12**.

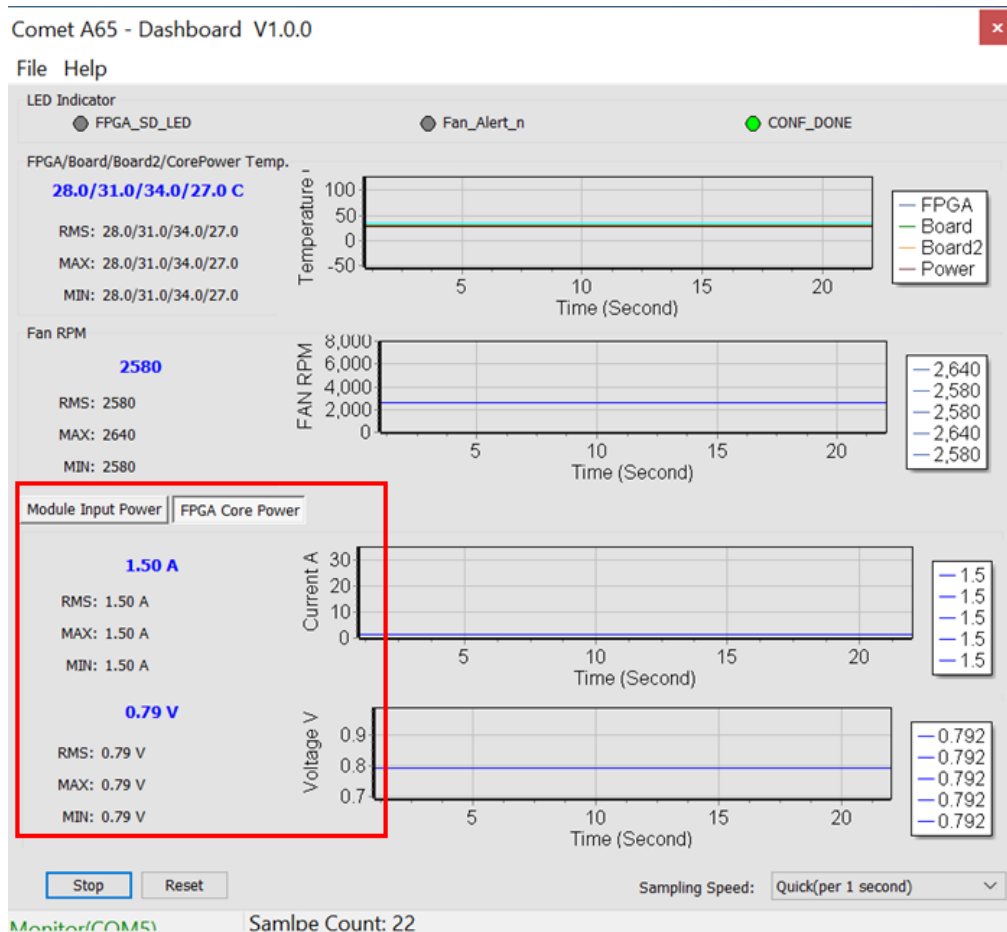


Figure 3-12 Power Monitor Section

- **Sampling Speed:** It can change interval time that the Dashboard GUI sample the board status. Users can adjust it to 1s/10s/1min/Full Speed (0.1s) to sample the board status, as shown in **Figure 3-13** and **Figure 3-14**.

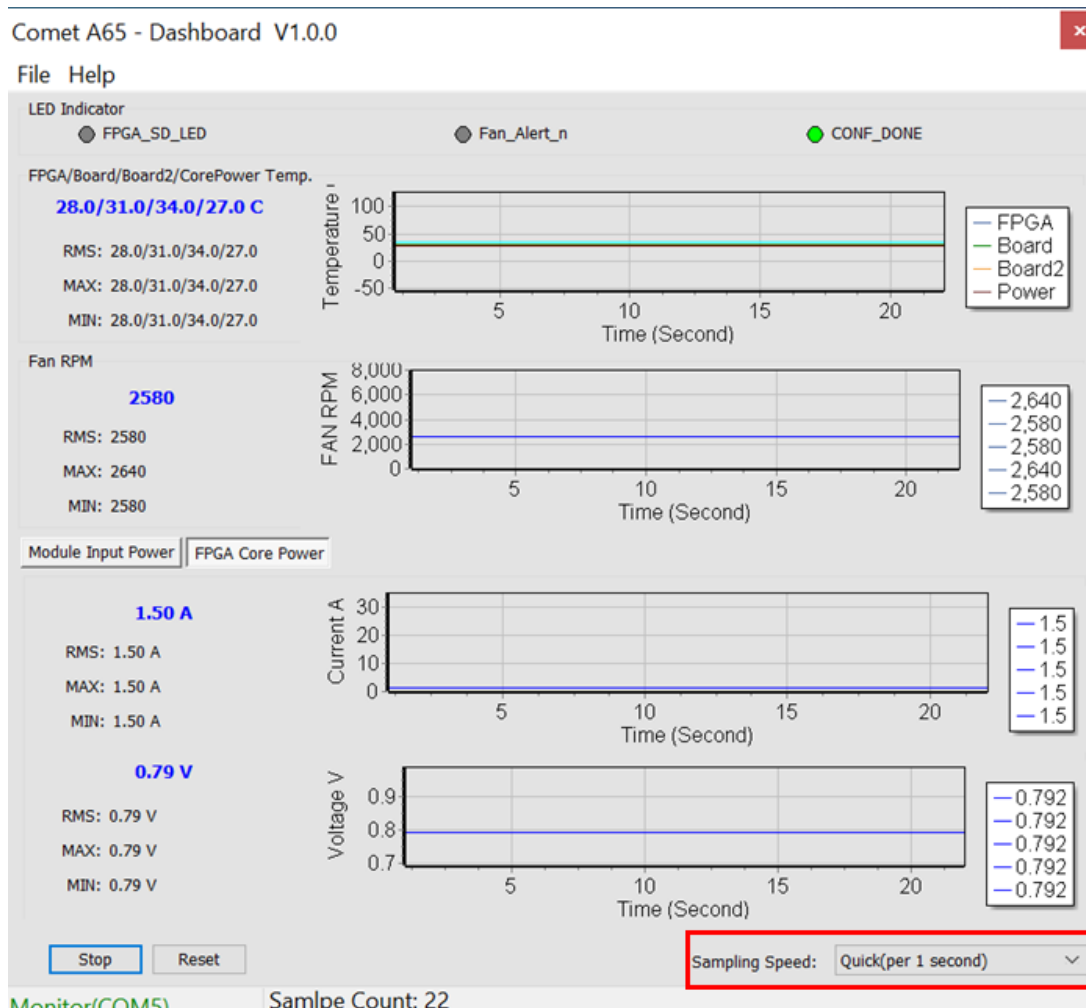


Figure 3-13 Sampling Speed section

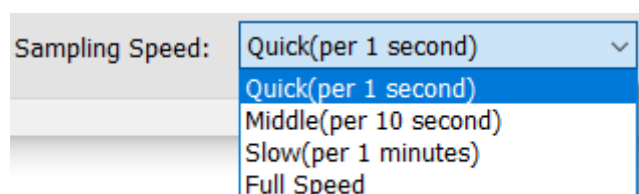


Figure 3-14 Options of Sampling Speed

- **File Menu:**

The user can click “File” menu at the top left of the GUI (See **Figure 3-15**) and some options such as board information and status export will appear. Note that to activate these functions, you will need to stop obtaining the board status (i.e. Don't Press “**Start**” button) in the GUI. Detailed introductions of these functions are described in below.

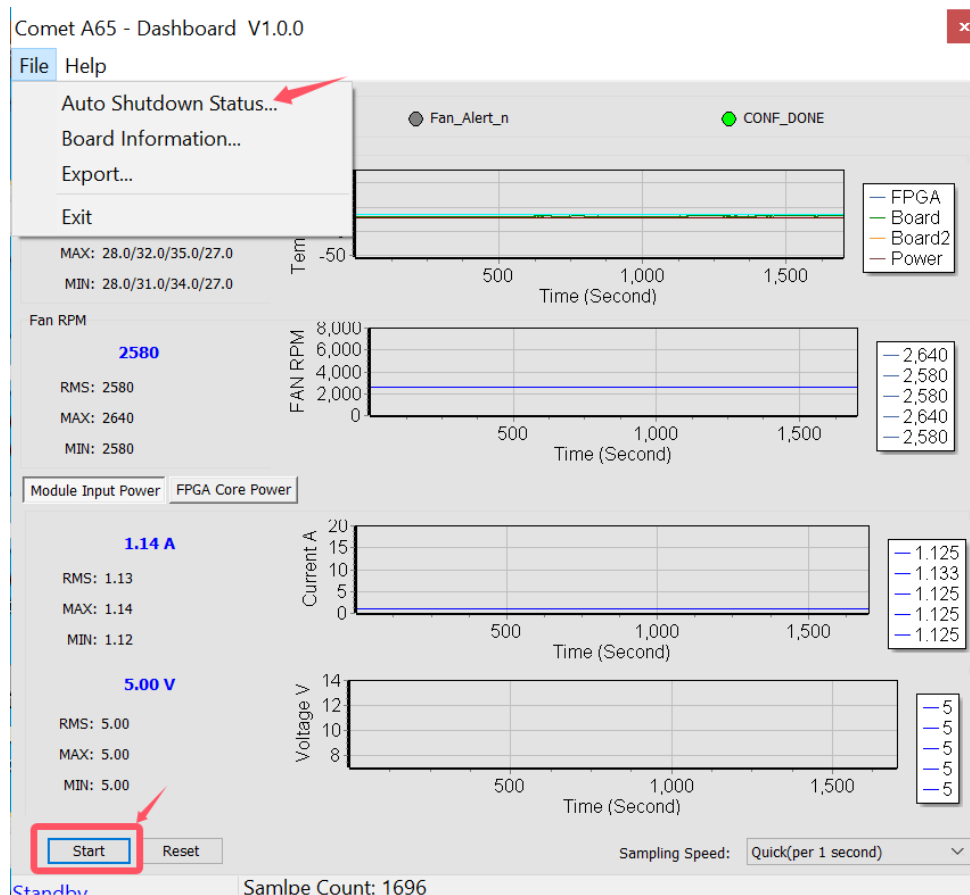


Figure 3-15 File menu

- **Auto shutdown status:** This option will report whether the board entered “**Auto shutdown status**” because the FPGA temperature is too high or the fan speed is abnormal.
- **Board Information:** There is a **File** page on the upper left of the Dashboard GUI program window, click the **Board Information** to get the current software version and the Comet A65 SOM Evaluation Kit version, as shown in **Figure 3-16**. *Note, user needs to stop the system monitor (press the “**Stop**” button on the Dashboard GUI), then you can run the Board Information.*

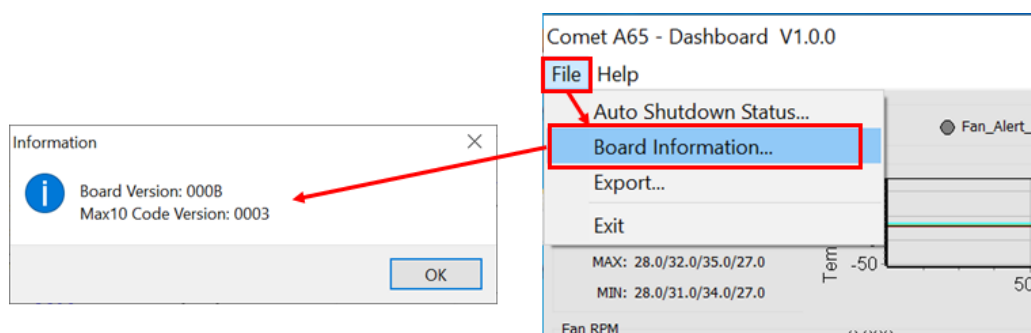


Figure 3-16 Board Information

- **Log File:** On the upper left of the Dashboard GUI program window, click the Export in the File page to save the board temperature, fan speed and voltage data in .csv format document, as shown in **Figure 3-17** and **Figure 3-18**.

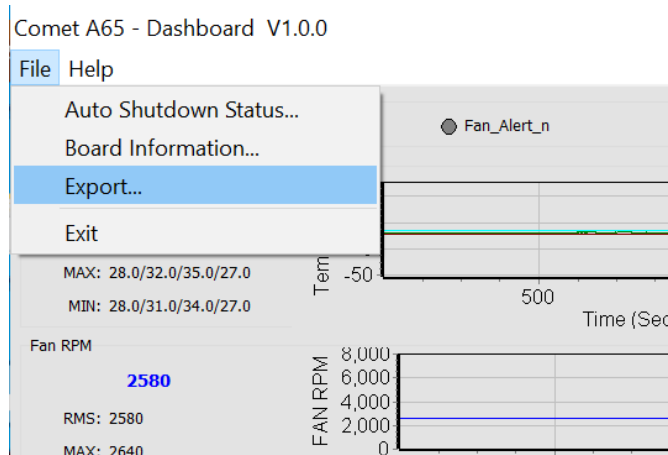


Figure 3-17 Export the log file

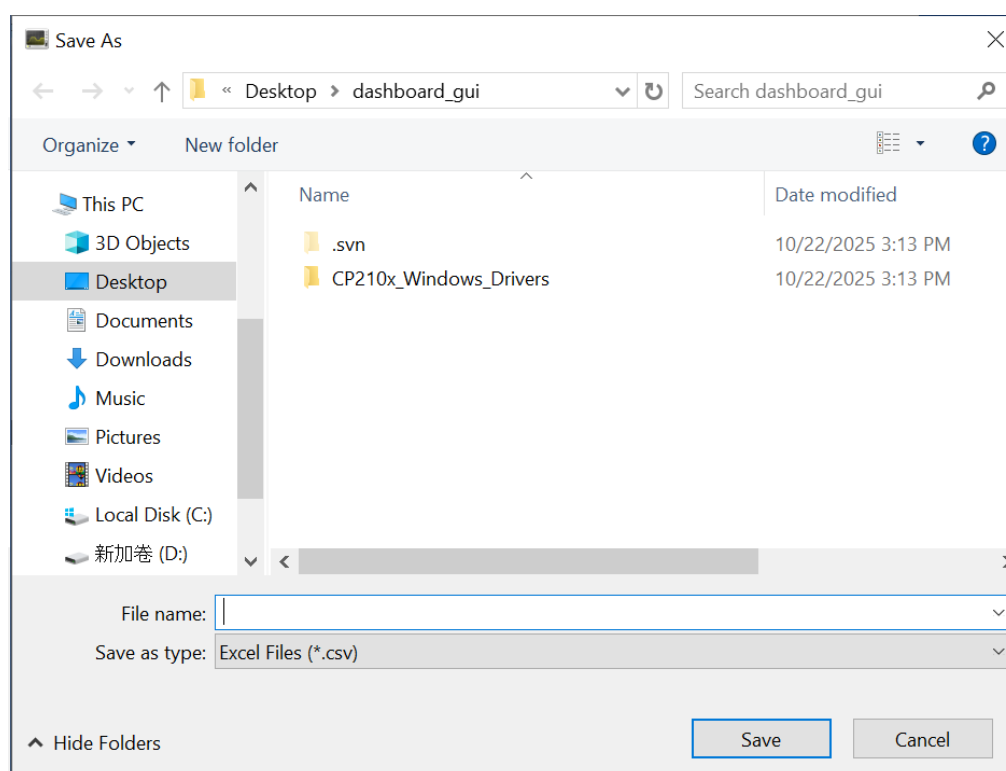


Figure 3-18 Export the log file in .csv format

Chapter 4

Board Assembly and Disassembly

This chapter explains how to assemble and disassemble the Comet A65 SOM and Terasic Comet A65 carrier board.

The video in the link below demonstrates how to install the Comet A65 SOM onto the carrier board, as well as the reverse process of removing it.

<https://youtu.be/QWGIqtni40I>

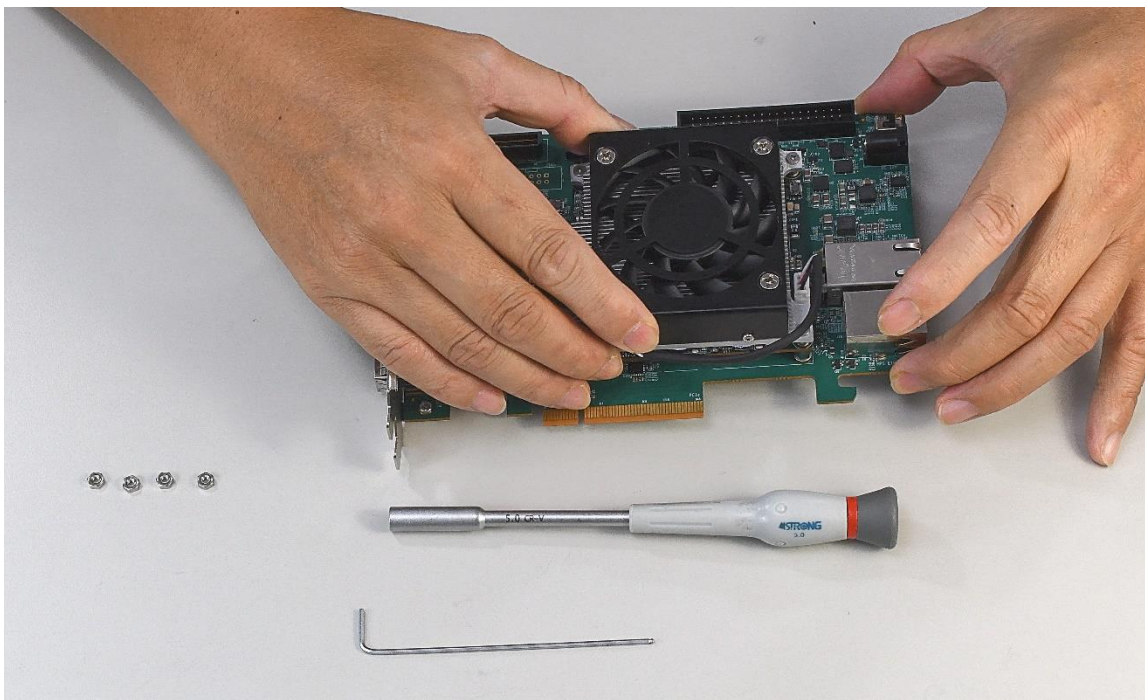


Figure 4-1 Video for installing and removing SOM and Carrier board

Chapter 5

Additional Information

5.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Revision History

Date	Version	Changes
2025.10	First publication	