



Intel® Agilex™ 5 Power Management User Guide



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1. Intel® Agilex™ 5 Power Management Overview

The Intel® Agilex™ 5 device family offers smart voltage identification (SmartVID) standard power devices and fixed-voltage devices. All SmartVID standard power devices must be driven by the Power Management BUS (PMBus*)-compliant voltage regulator, operating either in the PMBus master or PMBus slave mode.

Table 1. Device Series and Power Options

Device Series		Power Options
D-Series		SmartVID (Standard and lower power)
E-Series	Device Group A (Performance optimized)	SmartVID (Standard and lower power)
	Device Group B (Power optimized)	Fixed voltage

This user guide describes the power-optimizing features of the Intel Agilex 5 device family, and the power-up and power-down sequencing requirements for the Intel Agilex 5 devices.

1.1. Power System Design Phases

Power system design is done in the following logical phases.

1.1.1. Choosing a Power Tree

A power tree topology is chosen based on the requirements of your device.

The requirements of the power supply may not yet be known, but you can access the supply voltage and connection requirements from the *Intel Agilex 5 Device Family Pin Connection Guidelines*.

1.1.2. Power Estimation

The amount of electrical power required by the various device power supplies is estimated using the Intel FPGA Power and Thermal Calculator tool and the Power Analyzer tool.

As the design evolves to the final configuration, the quality and type of information available improve and the estimation becomes more accurate.

Related Information

[Intel FPGA Power and Thermal Calculator User Guide](#)

1.1.3. Power Optimization

The device configuration can be optimized to reduce power.

This step involves the Intel Quartus® Prime software power optimization wizard, the SmartVID feature, system cooling decisions, and dynamic workload management strategies. This phase may occur several times during the evolution of the system and device design.

1.1.4. Power Generation

Voltage regulator modules (VRMs) are selected based on the power tree and electrical power estimates. VRM selection is critical to producing high-quality power systems with the minimum number and cost of bypass elements.

1.2. Power Supplies

For more information about the supported power supplies and the nominal voltages, refer to the device data sheet.



2. Intel Agilex 5 Power Basics

2.1. Power Consumption

The total power consumption of an Intel Agilex 5 device consists of the following components:

- Static power—the power that the configured device consumes when powered up but no user clocks are operating, excluding DC bias power of analog blocks, such as I/O and transceiver analog circuitry.
- Dynamic power—the additional power consumption of the device due to signal activity or toggling. Dynamic power is dependent on the operating frequency of your design, applied voltage, and load capacitance, which depends on design connectivity.

Intel Agilex 5 devices minimize static and dynamic power using advanced process optimizations. These optimizations allow Intel Agilex 5 designs to meet specific performance requirements with the lowest possible power.

2.2. Power Estimation Basics

The Intel power analysis features, including the Intel FPGA Power and Thermal Calculator tool and the Intel Quartus Prime software Power Analyzer, give you the ability to estimate power consumption from early design concept through design implementation, as shown in the following figure.

As you provide more details about your design characteristics, estimation accuracy is improved. Intel recommends that you switch from the Intel FPGA Power and Thermal Calculator to the Power Analyzer in the Intel Quartus Prime software once your design is available. The Power Analyzer produces more accurate results because it has more detailed information about your design, including routing and configuration information about all the resources in your design.

The accuracy of the power model is determined on a per-power-rail basis for both the Power Analyzer and the Intel FPGA Power and Thermal Calculator. For most designs, the Power Analyzer and the Intel FPGA Power and Thermal Calculator have the following accuracies, with final power models:

- Power Analyzer—within 10% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates.
- Intel FPGA Power and Thermal Calculator—within 15% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates. Recommended margins are shown in the **Report** tab, only after device power model status is final.

Figure 1. Power Analysis from Design Concept Through Design Implementation

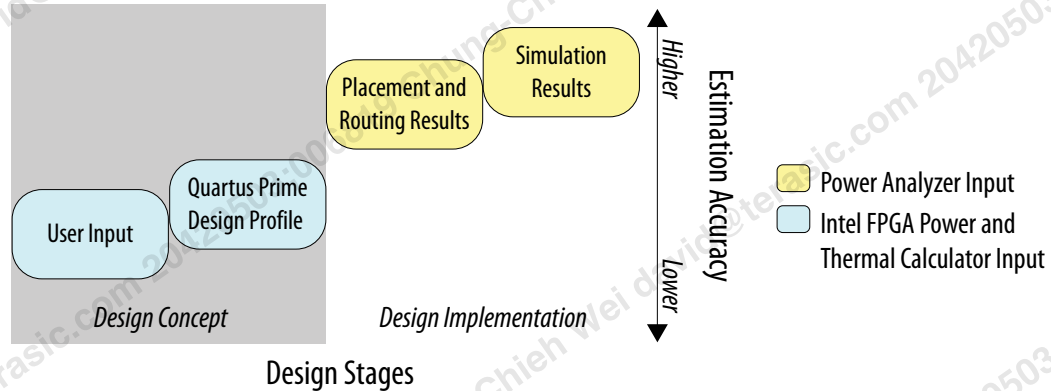


Table 2. Comparison of Intel FPGA Power and Thermal Calculator and Intel Quartus Prime Power Analyzer Capabilities

Characteristic	Intel FPGA Power and Thermal Calculator	Intel Quartus Prime Power Analyzer
When to use	Any time <i>Note:</i> For post-fit power analysis, you get better results with the Intel Quartus Prime Power Analyzer.	Post-fit
Software requirements	<ul style="list-style-type: none"> The Intel Quartus Prime software The Intel FPGA Power and Thermal Calculator <ul style="list-style-type: none"> Available in a standalone version which offers the same features as the Intel FPGA Power and Thermal Calculator version integrated within the Intel Quartus Prime software 	The Intel Quartus Prime software
Accuracy	Medium	Medium to very high
Data inputs	<ul style="list-style-type: none"> Resource usage estimates Clock requirements Environmental conditions Toggle rates 	<ul style="list-style-type: none"> Post-fit design Clock requirements Signal activity defaults Environmental conditions Register transfer level (RTL) simulation results (optional) Post-fit simulation results (optional) Signal activities per node or entity (optional)
Data outputs	<ul style="list-style-type: none"> Total thermal power dissipation Thermal static power Thermal dynamic power Off-chip power dissipation Current drawn from voltage supplies 	<ul style="list-style-type: none"> Total thermal power dissipation Thermal static power Thermal dynamic power Thermal I/O power Thermal power by design hierarchy Thermal power by block type Thermal power dissipation by clock domain Off-chip (non-thermal) power dissipation Current drawn from voltage supplies

2.3. Intel FPGA Power and Thermal Calculator

The Intel FPGA Power and Thermal Calculator results for Intel Agilex 5 devices are based on preliminary simulated data.

The Intel FPGA Power and Thermal Calculator for Intel Agilex 5 devices provides a current and power estimate based on various conditions such as room temperature and nominal voltage.

The Intel FPGA Power and Thermal Calculator calculations are estimates only and shall not be construed as a specification or a guarantee of any kind. The actual currents must be verified during device operation, as this measurement is sensitive to the design implemented in the device and the environmental operating conditions.

Related Information

- [Intel FPGA Power and Thermal Calculator User Guide](#)
- [Intel FPGA Power and Thermal Calculator Standalone](#)
Provides standalone Intel FPGA Power and Thermal Calculator tool. This standalone version is available for download from the Intel Download Center for FPGA page under the Additional Software tab.

2.4. Power Analyzer

The Intel Quartus Prime Power Analyzer allows you to estimate power consumption for a post-fit design.

To estimate power consumption before you compile the design, use the Intel FPGA Power and Thermal Calculator.

Related Information

[Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization](#)



3. Intel Agilex 5 Power and I/O State Sequencing

3.1. Overview

The Intel Agilex 5 devices require a specific power sequence.

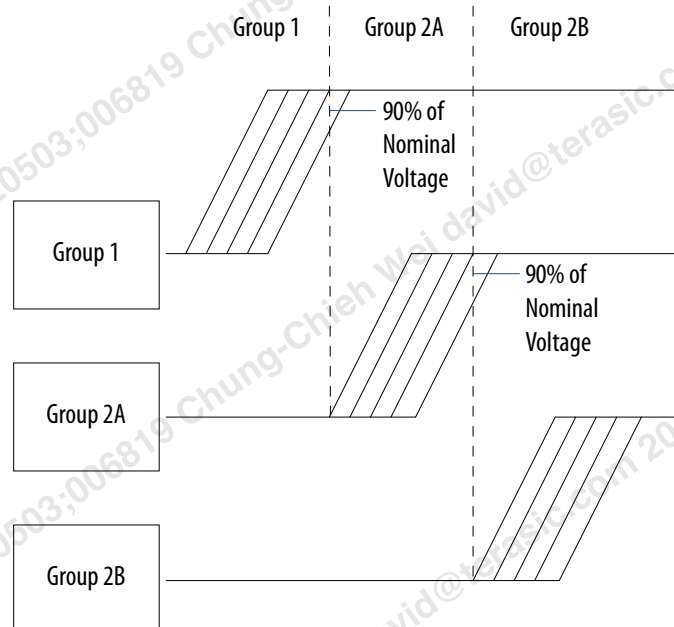
This section describes several power management options and discusses proper I/O management during device power up and power down. Design your power supply solution to properly control the complete power sequence. The requirements in this section must be followed to prevent unpredictable current draw to the FPGA device, which can potentially impact the I/O functionality.

3.2. Power-Up Sequence Requirements

The power rails in the Intel Agilex 5 devices are divided into three groups.

The following figure shows the voltage groups of the Intel Agilex 5 devices and their required power-up sequence.

Figure 2. Power-Up Sequence for the Intel Agilex 5 Devices



Note: V_{CCBAT} is not in any of the groups below. V_{CCBAT} does not have any sequence requirements. V_{CCBAT} holds the content of the security keys.

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For more information about the V_{CCBAT} connection guidelines and power supply sharing guidelines, refer to the *Intel Agilex 5 Device Family Pin Connection Guidelines*.

Table 3. Intel Agilex 5 Voltage Rails Group

Power Group	FPGA Core and Hard Processor System (HPS)
Group 1	V_{CC} V_{CCP} $V_{CCLHPS_ADC_SDM}$ $V_{CC_IO_SDM}$ V_{CCL_SDM} V_{CCH_SDM} $V_{CCPLLDIG_SDM}$ V_{CCL_HPS} $V_{CCL_HPS_CORE0_CORE1}$ $V_{CCL_HPS_CORE2}$ $V_{CCL_HPS_CORE3}$ $V_{CCPLLDIG1_HPS}$ $V_{CCPLLDIG2_HPS}$ $V_{CC_HSSI_L1,R4}$ $V_{CCERT_GXB[L1,R4][A,B,C,D]}$
Group 2A	V_{CCPT_HVIO} $V_{CCFUSEWR_SDM}$ V_{CCIO_SDM} V_{CCIO_HPS} V_{CCPLL1_HPS} V_{CCPLL2_HPS} $V_{CCEHT_GXB[L1,R4][A,B,C,D]}$ V_{CCPT} V_{CCPLL_SDM} V_{CCADC}
Group 2B	V_{CCIO_PIO} $V_{CCIO_HVIO(1.8V)}$ $V_{CCIO_PIO_SDM}$ $V_{CCRCORE}$

All power rails in Group 1 must ramp up (in any order) to a minimum of 90% of their respective nominal voltage before the power rails from Group 2A can start ramping up. The power rails within Group 2A can ramp up in any order after the last power rail in Group 1 ramps to the minimum threshold of 90% of its nominal voltage. All power rails in Group 2A must ramp to a minimum threshold of 90% of their nominal value before the Group 2B power rails can start ramping up. The power rails within Group 2B can ramp up in any order after the last power rail in Group 2A ramps up to a minimum threshold of 90% of their full value. For more information, refer to the *Intel Agilex 5 Device Family Pin Connection Guidelines*.

All power rails must ramp up monotonically. The power-up sequence must meet the POR delay time. For the POR specifications of the Intel Agilex 5 devices, refer to the *POR Specifications* section in the *Intel Agilex 5 FPGAs and SoCs Device Data Sheet*.

For configuration via protocol (CvP), the total t_{RAMP} must be less than 10 ms from the first power supply ramp-up to the last power supply ramp-up. For the t_{RAMP} specifications, refer to the *Recommended Operating Conditions* section in the *Intel Agilex 5 FPGAs and SoCs Device Data Sheet*.

For Intel Agilex 5 devices, there is no power-down sequence requirement. Intel recommends that you reverse the power-up sequence when you power down your device.

3.2.1. Guidelines for I/O Pins in HSIO, HVIO, HPS IO, and SDM IO Banks During Power Sequencing

Intel Agilex 5 devices do not support hot-socketing and require a specific power sequence. Design your power supply solution to properly control the complete power sequence.

Adhere to the following guidelines to prevent unnecessary current draw on the I/O pins located in the HSIO, HVIO, HPS IO, and SDM IO banks. These guidelines are applicable for unpowered, power up to POR, POR delay, POR delay to configuration, configuration, initialization, user mode, and power down device states.

- The I/O pins in these banks can be in one the following states:
 - HSIO banks—tri-stated, driven to ground, or driven to the V_{CCIO_PIO} level.
 - HVIO banks—tri-stated, driven to ground, or driven to the V_{CCIO_HVIO} level.
 - HPS banks—tri-stated, driven to ground, or driven to the V_{CCIO_HPS} level.
 - SDM banks—tri-stated, driven to ground, or driven to the V_{CCIO_SDM} level.
- While the Intel Agilex 5 device is powering up or down:
 - The input signals of an I/O pin at all times must not exceed the I/O buffer power supply rail of the bank where the I/O pin resides.
 - If you use a pin in a HSIO bank with 1.3 V V_{CCIO_PIO} , the pin voltage must not exceed the V_{CCIO_PIO} rail or 1.2 V, whichever is lower.
 - The input signals of an HVIO pin at all times must not exceed the V_{CCIO_HVIO} rail.
- While the Intel Agilex 5 device is powering up, powering down, or not turned on, the HSIO, HVIO, SDM IO, and HPS IO pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per I/O bank.
- While the Intel Agilex 5 device is not turned on, tri-state the I/O pin and do not drive the pin with any external voltage.
- After the Intel Agilex 5 device fully powers up, the voltage levels for the HSIO, HVIO, HPS IO, and SDM IO pins must not exceed the DC input voltage (V_I) value.

Table 4. Guideline Examples

Condition	Guideline
The V_{CCIO_SDM} pin ramps up and at period X, the V_{CCIO_SDM} voltage is 0.9 V.	At period X, keep the signals driven by the device connected to the SDM I/O pin at a voltage of 0.9 V or lower.
The V_{CCIO_PIO} pin ramps up and at period X, the V_{CCIO_PIO} voltage is 1.1 V.	At period X, keep the signals driven by the device connected to the HSIO I/O pin at a voltage of 1.1 V or lower.
The 1.3 V V_{CCIO_PIO} pin ramps up and the voltage continues to rise pass the 1.2 V level.	Keep the HSIO I/O pin voltage at 1.2 V or lower until the Intel Agilex 5 device fully powers up.

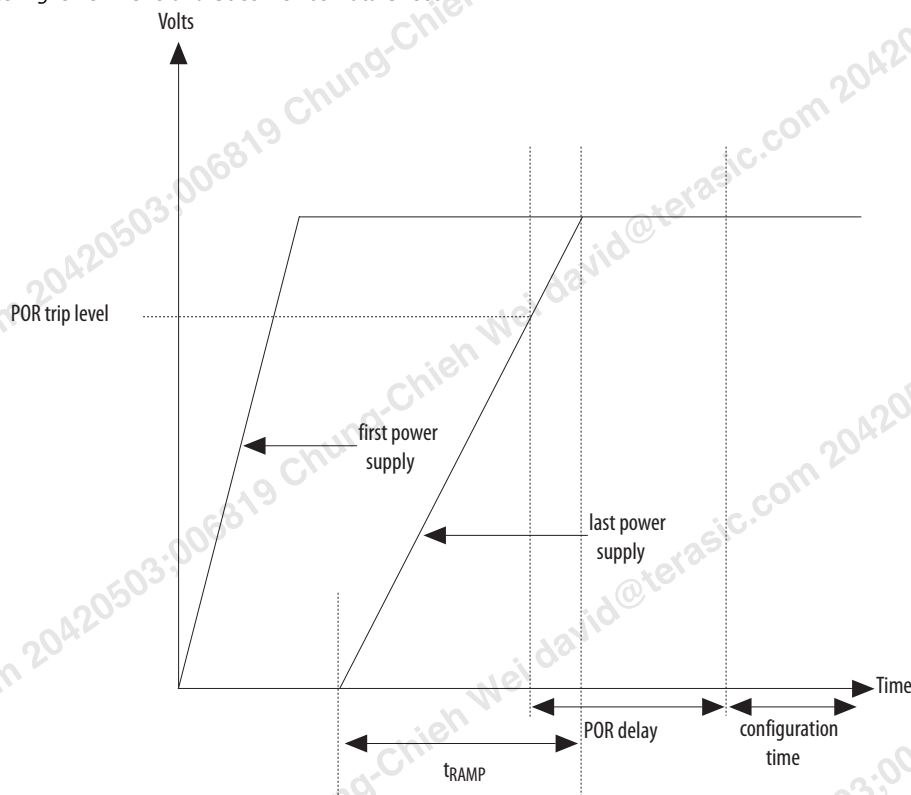
3.3. Power-On Reset

The power-on reset (POR) circuitry keeps the Intel Agilex 5 device in the reset state until the power supply outputs are within the recommended operating range.

A POR event occurs when you power up the Intel Agilex 5 device until all power supplies monitored by the POR circuitry reach the recommended operating range within the maximum power supply ramp time, t_{RAMP} . If t_{RAMP} is not met, the Intel Agilex 5 device I/O pins and programming registers remain tri-stated, which may cause device configuration to fail.

Figure 3. Relationship Between t_{RAMP} and POR Delay

The boot ROM initialization sequence is part of the POR delay. For t_{RAMP} and POR delay specifications, refer to the *Intel Agilex 5 FPGAs and SoCs Device Data Sheet*.



The Intel Agilex 5 POR circuitry uses individual detection circuitry to monitor each of the configuration-related power supplies independently. The POR circuitry is gated by the outputs of all the individual detectors. The SDM POR is gated by the outputs of the SDM associated power detectors.

POR delay is defined as the delay between the last power rail (VCCIO_SDM) monitored by the POR to reach the minimum operating condition voltage to the time your device is ready to begin configuration. For POR trip level, you can use the minimum value of the last power supply as a reference.

The Intel Agilex 5 device is held in the POR state until all power supplies have passed their trigger point. After power supplies have passed the trigger point, the Secure Device Manager (SDM) waits for a specific POR delay time and then starts device configuration.

3.3.1. Power Supplies Monitored by the POR Circuitry

The following power supplies are monitored by the Intel Agilex 5 POR circuitry:

- V_{CCL_SDM}
- V_{CCPT}
- V_{CCIO_SDM}
- V_{CCADC}
- V_{CC}
- V_{CCL_HPS}
- V_{CCIO_PIO_SDM}
- V_{CCRCORE}
- V_{CC_IO_SDM}
- V_{CCLHPS_ADC_SDM}
- V_{CCERT_GXB[L1,R4][A,B,C,D]}



4. Intel Agilex 5 Sensor Monitoring System

Intel Agilex 5 devices provide you with on-chip voltage and temperature sensors. You can use these sensors to monitor external voltages and on-chip operation conditions such as the internal power rail and on-chip junction temperature.

The Intel Agilex 5 sensor monitoring system stores sampled data in the secure device manager (SDM). You can read the voltage and temperature values in the SDM by using the Mailbox Client Intel FPGA IP or the Mailbox Client with Avalon® Streaming Interface Intel FPGA IP.

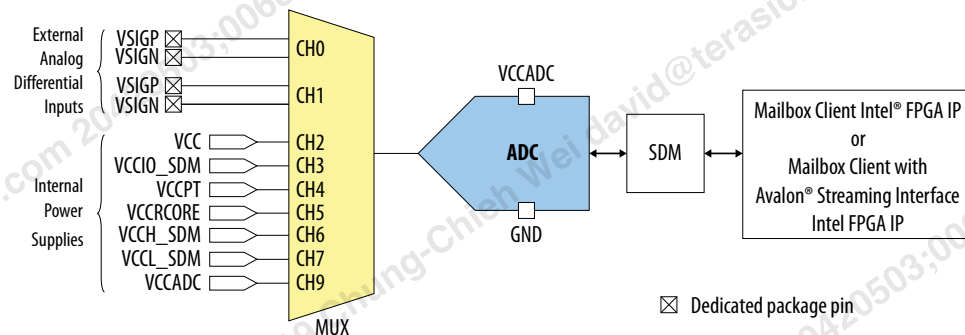
Related Information

- [Operation Commands, Mailbox Client Intel FPGA IP User Guide](#)
Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- [Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide](#)
Provides information about reading the voltage and temperature values using the Mailbox Client with Avalon Streaming Interface IP.

4.1. Voltage Monitoring System

The Intel Agilex 5 voltage monitoring system uses a built-in 7-bit analog to digital converter (ADC). The ADC can sample up to one kilo samples per second (KSPS).

Figure 4. Intel Agilex 5 Voltage Sensor



The voltage sensor has the following capabilities:

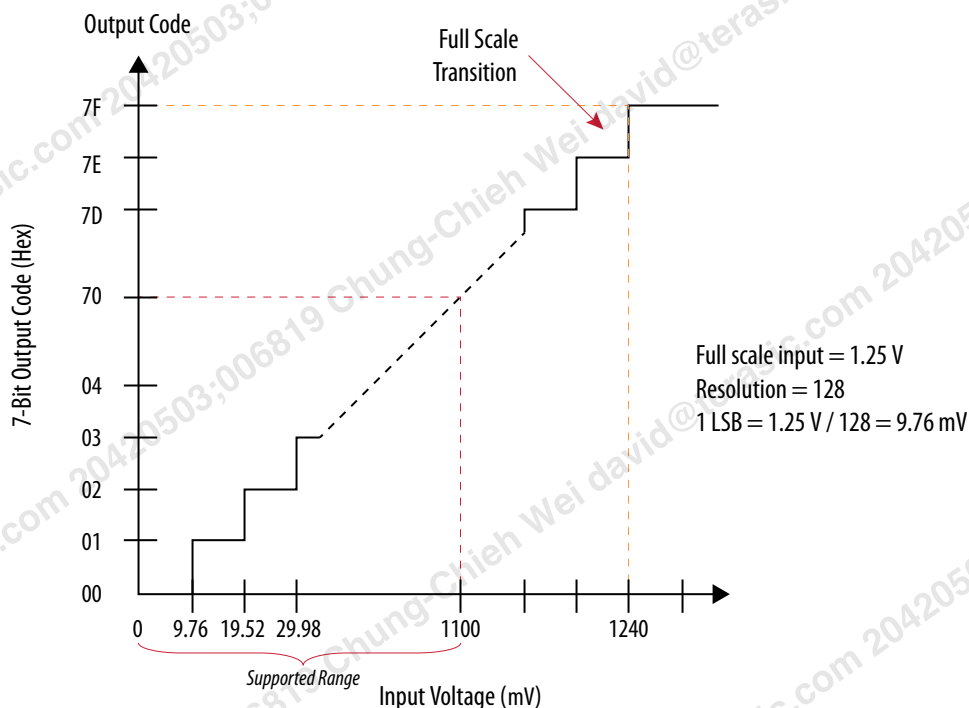
- Monitor external voltages up to 1.10 V through two pairs of differential input pins.
- Monitor internal power supplies. For internal high-voltage rails, a voltage divider function divides the input voltage by half and feeds the voltage to the ADC. The SDM then doubles the ADC reading to get the actual voltage.

4.1.1. Voltage Sensor Transfer Function

The Intel Agilex 5 voltage sensor supports the ADC's unipolar operation mode.

Figure 5. Intel Agilex 5 ADC 7-Bit Unipolar Transfer Function

The analog input scale has full scale code from 00h to 7Fh. The measurement can only display up to *full scale* – 1 LSB



4.2. Temperature Monitoring System

The Intel Agilex 5 temperature monitoring system allows you to measure the on-chip temperature (T_{JUNCTION}) using local temperature sensors or remote temperature sensing diodes (TSDs).

Table 5. Overview of the Local and Remote Temperature Sensors

Feature	Local Temperature Sensor	Remote TSD
Temperature sensing	Uses the built-in ADC to sample the on-chip temperature.	Interfaces the TSD with an external temperature sensing chip.
Readout access	From the SDM mailbox through the Mailbox Client or Mailbox Client with Avalon Streaming Interface IPs.	From the external temperature sensing chip.
Operation capability	While the Intel Agilex 5 devices are in user mode.	While the Intel Agilex 5 devices are powered on or off.
User calibration	Not required.	Required. Refer to the related information.

Related Information

Guidelines: Calibrate Temperature Sensing Chip Interfacing the Intel Agilex 5 Remote TSD on page 20

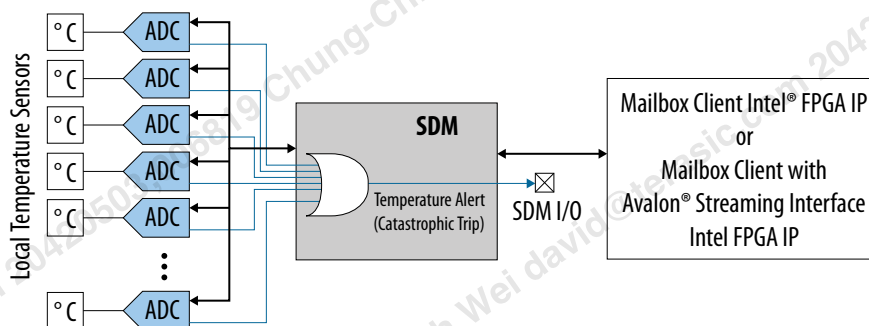
4.2.1. Local Temperature Sensor

The Intel Agilex 5 local temperature sensors use built-in 11-bit ADCs and provide temperature readouts through the SDM mailbox.

Each temperature sensor location contains up to four local TSDs in the core fabric.

Figure 6. Intel Agilex 5 FPGAs Local Temperature Sensor

This figure is a block diagram of the local temperature sensors. For the physical locations of the sensors, refer to the related information.



Intel Agilex 5 devices provide up to 11 local temperature sensor locations for monitoring on-chip temperature.

Catastrophic Trip Signal

The catastrophic trip signal, `nCATTRIP`, is an optional signal that you can assign to any unused `SDM_IO` pin. You can set the temperature threshold point for `nCATTRIP` from 95°C to 120°C, in 1°C increments, through the **Device and Pin Options** window of the Intel Quartus Prime software.

If enabled, the `nCATTRIP` signal asserts and stays high. When the core temperature reaches the threshold that you set, the `nCATTRIP` signal drives low—you must immediately power down the FPGA to avoid permanent damage to the device. The `nCATTRIP` signal is only valid after the device enters user mode.

Note:

The catastrophic signal is not supported for the local TSD in the SDM location.

Related Information

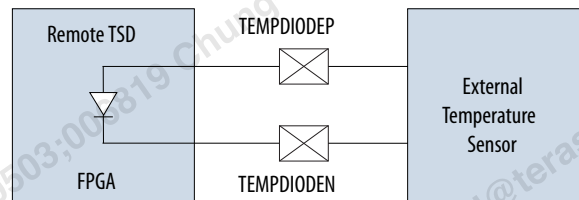
Temperature Sensor Locations on page 16

4.2.2. Remote Temperature Sensing Diode

The remote TSD interface allows you to monitor the temperature of the core fabric using an external temperature sensor.

Figure 7. External Temperature Sensor Connection to the Remote TSD

The remote TSD requires a two-pins connection.



- In the device pin-out files, the remote TSD pins are marked as TEMPDIODEP and TEMPDIODEN.
- For the remote TSD characteristics, refer to the relevant section in the device datasheet.

Related Information

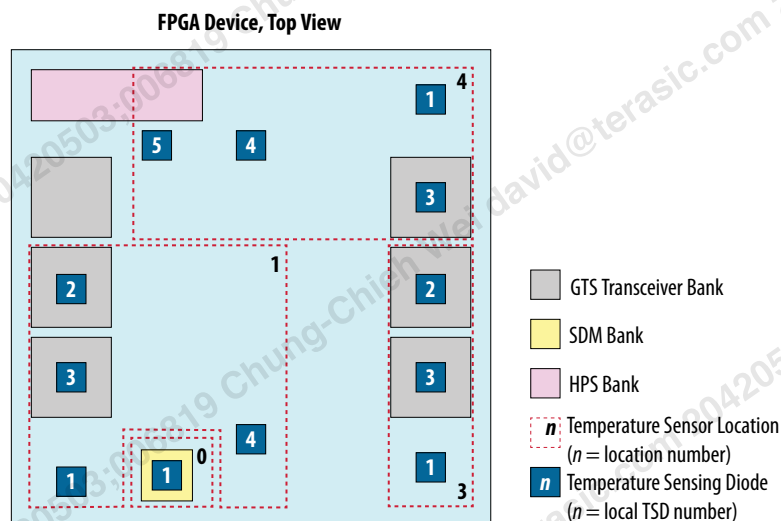
[Temperature Sensor Locations](#) on page 16

4.2.3. Temperature Sensor Locations

The Intel Agilex 5 local and remote TSDs are located in the core fabric and GTS transceiver banks. There are several local temperature sensor locations within the core fabric to support temperature readout across the core fabric and the GTS transceiver banks.

Figure 8. Temperature Sensing Diode Locations

This figure shows approximate locations of the temperature sensors and is not to scale. The figure shows the view of the die, as shown in the Intel Quartus Prime **Chip Planner**. In the **Pin Planner**, the view is flipped.



Note: The count and availability of the temperature sensors, TSDs, and GTS transceiver banks vary among Intel Agilex 5 devices. The HPS bank is available only in Intel Agilex 5 SoC FPGAs.

- To monitor the HPS temperature, use TSD 5 in location 4.
- To monitor the SDM temperature, use the TSD in location 0.

Figure 9. Bit Format to Mailbox Client with Avalon Streaming Interface IP to Specify Local TSDs to Read

To specify which local TSD to read, provide the Mailbox Client with Avalon Streaming Interface IP with the 32-bit value in fixed length hexadecimal codes.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Location Code														Sensor Mask													

Table 6. Local Temperature Sensor Locations and Corresponding Bank Names

The availability of the sensor locations and TSDs varies among Intel Agilex 5 FPGAs. This table lists the availability of temperature sensor resources for E-Series devices.

Sensor Location	TSD Location	E-Series Devices			
		A5E 005B A5E 007B A5E 008B	A5E 013A A5E 013B	A5E 028A A5E 028B	A5E 043A A5E 065A A5E 043B A5E 065B
0	1	Yes	Yes	Yes	Yes
1	1	—	Yes	Yes	Yes
	2	—	—	Yes	Yes
	3	—	Yes	Yes	Yes
	4	—	Yes	Yes	Yes
3	1	Yes	Yes	Yes	Yes
	2	—	—	—	Yes
	3	—	—	Yes	Yes
4	1	Yes	Yes	Yes	Yes
	2	—	—	—	—
	3	—	—	—	Yes
	4	—	Yes	Yes	Yes
	5	—	Yes	Yes	Yes

Table 7. Local Temperature Sensor Locations and Equivalent Remote TSD Pin Names

Not all locations have a remote TSD. In locations with a remote TSD, the remote TSD is physically located next to the local TSDs that are marked as local TSD 1. The temperature sensor locations of the core fabric and GTS transceiver banks are as shown in the preceding figure.

Location Number	Sensor Location [31..16] (Hexadecimal code)	Supported Channel ⁽¹⁾ (Specify sensor bitmask[15..0] as hexadecimal value)	Equivalent Remote TSD Pin Name (Next to local TSD 1 in sensor location)
0	0000	0 ⁽²⁾	TEMPDIODE0Ap / TEMPDIODE0An
1	0001	4, 3, 2, 1, 0	—
3	0003	3, 2, 1, 0	—
4	0004	5, 4, 3, 1, 0	—

Related Information

- [Operation Commands, Mailbox Client Intel FPGA IP User Guide](#)
Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- [Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide](#)
Provides information about reading the voltage and temperature values using the Mailbox Client with Avalon Streaming Interface IP.

4.2.4. Retrieving Local Temperature Sensor Reading

To retrieve the temperature readings, provide the location code and sensor masks to the Mailbox Client with Avalon Streaming Interface Intel FPGA IP. The Mailbox Client with Avalon Streaming Interface IP accepts a 32-bit value in fixed length hexadecimal format.

Bits [27..16] carry the local TSD location code while bits [15..0] represent the temperature channels in the location. Bits [31..28] are reserved.

Table 8. Sensor Mask Function for Each Local TSD Location

For locations that have only a single local TSD, the sensor mask defaults to 0. You can specify only the location code. The Mailbox Client with Avalon Streaming Interface IP returns an error if you try to retrieve temperature reading from an invalid temperature sensor or TSD location.

Function	Sensor Location	Max TSD Count	Applicable Sensor Masks
Specify the local TSDs to read	0	1	[0]
	1	4	[4..1]
continued...			

⁽¹⁾ For sensor locations with several local TSDs, channel 0 (mask [0]) returns the highest temperature among the local TSDs in the particular location. For sensor locations with one local TSD, channel 0 returns the same value as channel 1.

⁽²⁾ For location 0, only channel 0 (mask [0]) is supported, returning the temperature reading for the TSD in that location.

Function	Sensor Location	Max TSD Count	Applicable Sensor Masks
Read the TSD with the highest temperature in the location	3	3	[3..1]
	4	4	[5..3], [1]
	All locations except location 0	Varies	[0]

Table 9. Examples for Reading Temperature through the SDM Mailbox

This example is applicable to devices with two or more local TSDs in the location.

Location	Channels to Read in the Location	Hexadecimal Code to Send	Values Returned
1	Temperature from all local TSDs in location 1 and the highest temperature in the location.	0x0001001F	Returns five values—temperature for local TSDs 1, 2, 3, and 4 in the location, and the highest temperature among them.
	Temperature from TSD with the highest temperature in location 1.	0x00010001	Returns one value—the value of the TSD with the highest temperature in the location.

Related Information

- [Operation Commands, Mailbox Client Intel FPGA IP User Guide](#)
Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- [Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide](#)
Provides information about reading the voltage and temperature values using the Mailbox Client with Avalon Streaming Interface IP.

4.2.5. Temperature Sensor Error Codes**Table 10. Temperature Sensor Error Codes and Solutions**

Error Code	Invalid Condition	Solution
0x80000000	Selected temperature sensor channel is currently inactive.	Ensure that the tile where the TSD is located is actively in use.
0x80000001	Selected temperature sensor channel returned a value that is not the latest reading.	Retrieve the temperature reading again
0x80000002	Selected temperature sensor channel is invalid for the device.	Ignore the returned data because the temperature sensor channel location is invalid
0x80000003	System is corrupted or failed to respond	Contact Intel FPGA support
0x80000004		
0x80000005	Communication mechanism is busy	Retrieve the temperature reading again
0x800000FF	System is corrupted or failed to respond	Contact Intel FPGA support

4.3. Sensors Design Considerations

To ensure the success of your designs, follow the recommended design guidelines. These guidelines apply to all variants of the device family unless noted otherwise.

4.3.1. Voltage Monitor Design Guidelines

- Connect the power pins and VSIG pins according to the requirements in the device pin connection guidelines.
- If you use the voltage sensor in single-ended mode, tie the VSIGN pin to the GND pin.
- To prevent damage, do not drive VSIGP and VSIGN pins until the VCCADC power rail has reached 1.62 V.

4.3.2. Temperature Monitor Design Guidelines

You can measure the on-chip temperature of the core fabric through the remote TSDs while the device is powered on or powered off. However, the local temperature sensors are available only after the device is powered up and configured.

- Connect the remote TSD pins to external temperature sensing devices to monitor the on-chip temperature.
- To interface with the remote TSD, use temperature sensing chips with features that allow you to perform calibration and measurement compensation to improve accuracy, such as:
 - Configurable ideality factor
 - Offset adjustment with or without Beta compensation
- Keep the resistance of both board traces to the remote TSD p and n pins to less than 0.2 Ω .
- Route both traces in equal lengths and shield them.
- Intel recommends a 10-mils width and space for both traces.
- Route both traces through the most minimum number of vias and crossunders possible to minimize the thermocouple effects.
- Ensure that the number of vias for both traces are the same.
- To avoid coupling, insert a GND plane between the remote TSD pins traces and high-frequency toggling signals, such as clocks and I/O signals.
- To filter high-frequency noise, place an external capacitor between the traces close to the external sensors.
- If you use only the local temperature sensors, you can leave the remote TSD p and n pins unconnected.

For details about device specifications and connection guidelines, refer to the external temperature sensor manufacturer's documentation.

4.3.3. Guidelines: Calibrate Temperature Sensing Chip Interfacing the Intel Agilex 5 Remote TSD

If you interface an external temperature sensing chip to the Intel Agilex 5 remote TSD, you must calibrate the external chip to avoid temperature measurement inaccuracy.



The calibration of the external temperature sensing chip identifies optimized settings such as the temperature offset and change in ideality factor. The external chip uses these settings to accurately sample the temperature from the Intel Agilex 5 remote TSD.

Related Information

[AN 769: Intel FPGA Remote Temperature Sensing Diode Implementation Guide](#)

Provides guidelines for selecting external temperature sensing chips to use with Intel Agilex 5 FPGAs.



[Send Feedback](#)



5. Intel Agilex 5 Power Optimization Techniques and Features

Intel Agilex 5 devices leverage on advanced 10-nm process technology, an enhanced core architecture, and various optimizations to reduce total power consumption. The power optimization techniques and features are listed below:

- SmartVID Standard Power Devices
 - Temperature Compensation
- Digital signal processing (DSP) and M20K Power Gating
- Clock Gating
- Power Sense Line

5.1. SmartVID Standard Power Devices

The SmartVID feature compensates for process variation by narrowing the process distribution using voltage adaptation.

This feature is supported in all Intel Agilex 5 devices with the –V and –E power options only. For the –V and –E power option devices, you must connect the PWRMGT_SCL and PWRMGT_SDA pins in both the Power Management BUS (PMBus) master and PMBus slave modes. The PWRMGT_ALERT pin is optional for the Intel Agilex 5 device in the PMBus slave mode. The PWRMGT_ALERT pin is an active low pin and is used to perform the handshake flow between the FPGA device and an external PMBus master. If you do not connect the PWRMGT_ALERT pin, the external PMBus master has to rely on the nCONFIG, nSTATUS, and INIT_DONE signals to perform the handshake flow. All connections must be set up on the circuit board and in the Intel Quartus Prime software.

Table 11. The PMBus Master and Slave Modes Interfaces for the Intel Agilex 5 Devices

PMBus Interfaces	Operating Modes	
	PMBus Master Mode	PMBus Slave Mode
PWRMGT_SCL	Required	Required
PWRMGT_SDA	Required	Required
PWRMGT_ALERT	—	Optional

The PMBus master and PMBus slave modes only support the 1.8-V single-ended I/O standard.

Note: The PWRMGT_SDA, PWRMGT_SCL, and PWRMGT_ALERT signals are in the undetermined state during device power-up and power-down. The PWRMGT_SDA, PWRMGT_SCL, and PWRMGT_ALERT signals are only valid after the device is fully powered up.

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For more information about how to connect these pins on the circuit board, refer to the *Intel Agilex 5 Device Family Pin Connection Guidelines*.

For instructions on how to set up the connections in the Intel Quartus Prime software, refer to the [Specifying Power Management and VID Parameters and Options](#) on page 36.

Note:

Intel Agilex 5 standard power devices (–1V, –2V, –2E, and –3V power grades) are SmartVID devices. The core voltage supplies (V_{CC} and V_{CCP}) for each SmartVID device is mandatory to be driven by a PMBus-compliant voltage regulator dedicated to the Intel Agilex 5 –V and –E power option devices that is connected to that Intel Agilex 5 device via PMBus. Intel Agilex 5 devices does not configure or function correctly if the core voltage is driven by a non-PMBus compliant regulator with a fixed output voltage.

Intel programs the optimum voltage level required by each individual Intel Agilex 5 device into a fuse block during device manufacturing. The Secure Device Manager (SDM) Power Manager reads these values and can communicate them to an external power regulator or a system power controller through the PMBus interface.

The SmartVID feature allows a power regulator to provide the Intel Agilex 5 device with V_{CC} and V_{CCP} voltage levels that maintain the performance of the specific device speed grade. When the SmartVID feature is used:

1. Intel Agilex 5 devices are powered up at 0.85 V for the –V speed grade and 0.80 V for the –E speed grade for both V_{CC} and V_{CCP} .
2. After the VID-fused value in the Intel Agilex 5 device is determined and propagated to the external voltage regulator, both the V_{CC} and V_{CCP} voltages are regulated based on the boosted VID-fused value.

Related Information

- [Intel Agilex 5 Device Family Pin Connection Guidelines](#)
Provides more information about the connection guidelines of each pin.
- [AN 974: Intel Stratix® 10 and Intel Agilex SmartVID Debug Checklist and Voltage Regulator Guidelines](#)

5.1.1. SmartVID Feature Implementation in Intel Agilex 5 Devices

Devices supporting the SmartVID feature have a VID-fused value programmed into a fuse block during device manufacturing. The VID-fused value represents a voltage level in the range of 0.7 V to 0.9 V. Each device has its own specific VID-fused value.

The boosted VID-fused value is sent to the external regulator or system power controller through the PMBus interface. Upon receiving the boosted VID-fused value, an adjustable regulator tunes the V_{CC} and V_{CCP} voltage levels to the voltage specified by the VID-fused value.

Intel Agilex 5 devices perform the SmartVID setup in the early stage of the configuration process. The SmartVID process continues to monitor the V_{CC} and V_{CCP} voltage rails in user mode. The Power Manager monitors the temperature and adjusts the voltage when required. For more information, refer to the *Temperature Compensation* section.

Table 12. SmartVID Regulator Requirements

Specification ⁽³⁾	Value
Voltage range	0.7 V – 0.9 V
Voltage step	5 – 10 mV
Ramp time	<ul style="list-style-type: none"> Non-CvP—10 mV/10 ms to 10 mV/20 μs Configuration via Protocol (CvP)—10 mV/60 μs to 10 mV/20 μs ⁽⁴⁾

Table 13. Supported Voltage Output Format for Intel Agilex 5 Devices with the –V and –E Power Options

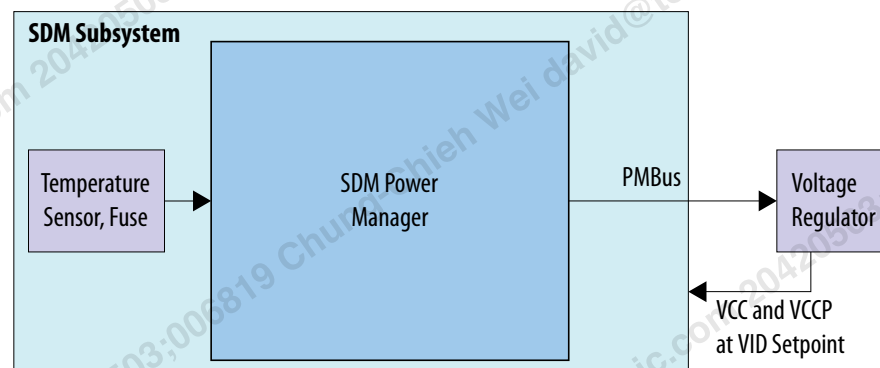
Voltage Output Format	Operating Modes	
	PMBus Master Mode	PMBus Slave Mode
Linear mode	Yes	No
VID mode	No	No
Direct mode	Yes	Yes, with coefficient m=1, b=0, and R=0. Translated output voltage is in millivolts (mV).

Related Information

Temperature Compensation on page 35

5.1.2. SDM Power Manager

In Intel Agilex 5 devices, the SmartVID feature is managed by the SDM subsystem. The SDM subsystem is powered up after V_{CC} and V_{CCP} voltage levels are powered up to 0.8V. The SDM Power Manager reads the VID-fused value and communicates this value to the external voltage regulator through the PMBus interface.

Figure 10. SDM Power Manager Block Diagram


⁽³⁾ To ensure the specifications are meeting requirements, refer to your selected voltage regulator data sheet.

⁽⁴⁾ When the system is required to support the CvP functionality and meet the PCI Express* (PCIe*) link-up timing budget during the initial power up, the minimum ramp time is 10 mV/60 μ s.

The SDM Power Manager has the following stages:

- Initial stage
 - Set the external voltage regulator to supply power to V_{CC} and V_{CCP} to the voltage level based on the boosted VID-fused value and the device temperature.
 - Configures the FPGA and switches the FPGA to user mode.
- Monitor stage
 - Monitors temperature and updates V_{CC} and V_{CCP} .

5.1.2.1. PMBus Master Mode

In the PMBus master mode, during the initial stage, the SDM Power Manager sets the external voltage regulator to supply V_{CC} and V_{CCP} voltage levels based on the VID-fused value and the device temperature before it starts to configure the FPGA.

After entering user mode (in the monitor stage), the SDM Power Manager monitors temperature changes and decides if the V_{CC} and V_{CCP} output voltage values need to be updated. If voltages require updating, the SDM Power Manager identifies the voltage value based on the fuse values and the current temperature and sends the desired voltage value to the voltage regulators through the PMBus interface.

Figure 11. PMBus Master Mode

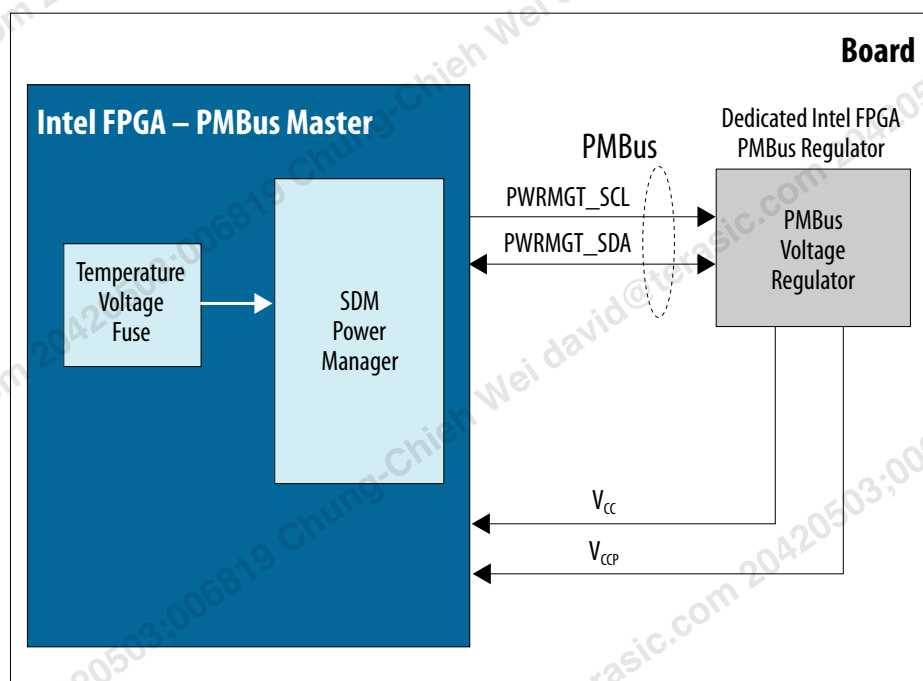
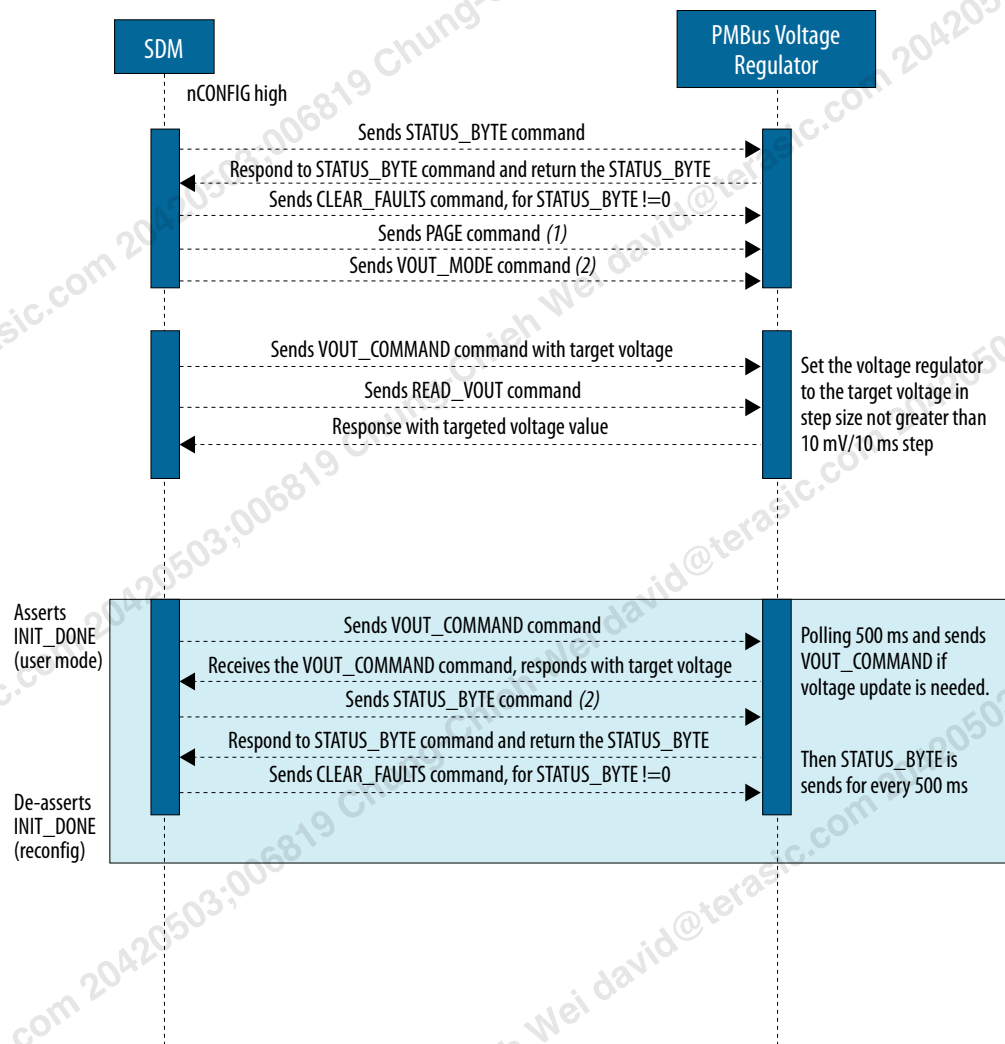


Table 14. Supported Commands for the PMBus Master Mode

Command Name	Command Code	Default	PMBus Transaction Type	Number of Bytes
PAGE ⁽⁵⁾	00h	—	Write byte	1
VOUT_MODE	20h	40h	Read byte	1
VOUT_COMMAND	21h	—	Write word	2
READ_VOUT	8Bh	—	Read word	2
MFR_ADC_CONTROL ⁽⁶⁾	D8h	—	Write byte	1
STATUS_BYTE	78h	00h	Read byte	1
CLEAR_FAULTS	03h	—	Send byte	0

⁽⁵⁾ This is an optional command. This command is only applicable if you enable the PAGE command parameter. For more information, refer to the Power Management and VID Parameters section.

⁽⁶⁾ This command is sent when you set the device type to LTM4677 only.

Figure 12. Flow between the PMBus Voltage Regulator and FPGA in the PMBus Master Mode**Notes:**

- (1) The PAGE command is only sent if PAGE is enabled in the Intel Quartus GUI setting.
- (2) This command is only sent if the slave device type selected is not "Other" in the Intel Quartus GUI setting.

Multi-Master Mode

The PMBus master mode supports the multi-master mode.

When multiple devices start to communicate at the same time, the device writing the most zeros to the bus or the slowest device wins the arbitration. The other devices immediately discontinue any operation on the bus. When there is an on-going bus communication, all devices must detect the communication and not interrupt it. The devices must wait for a stop condition to appear before starting communication to the bus. Once the stop condition is received on the bus, the next device that wins arbitration sends a start condition by pulling the PWRMGT_SDA low to re-initialize the bus communication.

In this mode, all master devices must be multi masters in a multi-master system. Single-master systems may not understand the arbitration and the busy detection mechanisms can cause unpredictable results.

5.1.2.2. PMBus Slave Mode

Intel Agilex 5 devices can also be configured in the PMBus slave mode with an external power management controller acting as the PMBus master. The external power management controller that interact with Intel Agilex 5 devices over PMBus must support clock stretching. The external power management controller is responsible for driving all PMBus transactions, querying the FPGA for its target voltage requirements and interacting with the voltage regulators to configure them to the FPGA's target voltage.

For the PMBus slave mode with `PWRMGT_ALERT`, you must follow the guidelines listed below for the external PMBus flow:

- Figure: *Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode with the `PWRMGT_ALERT` Signal*
- Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram with `PWRMGT_ALERT`*
- Table: *Stage Flow for the External PMBus Master when the `PWRMGT_ALERT` Signal is Asserted and `STATUS_BYTE` = 0*
- Table: *Stage Flow for the External PMBus Master when the `PWRMGT_ALERT` Signal is Asserted and `STATUS_BYTE` is not Equal to 0*

Figure 13. PMBus Slave Mode

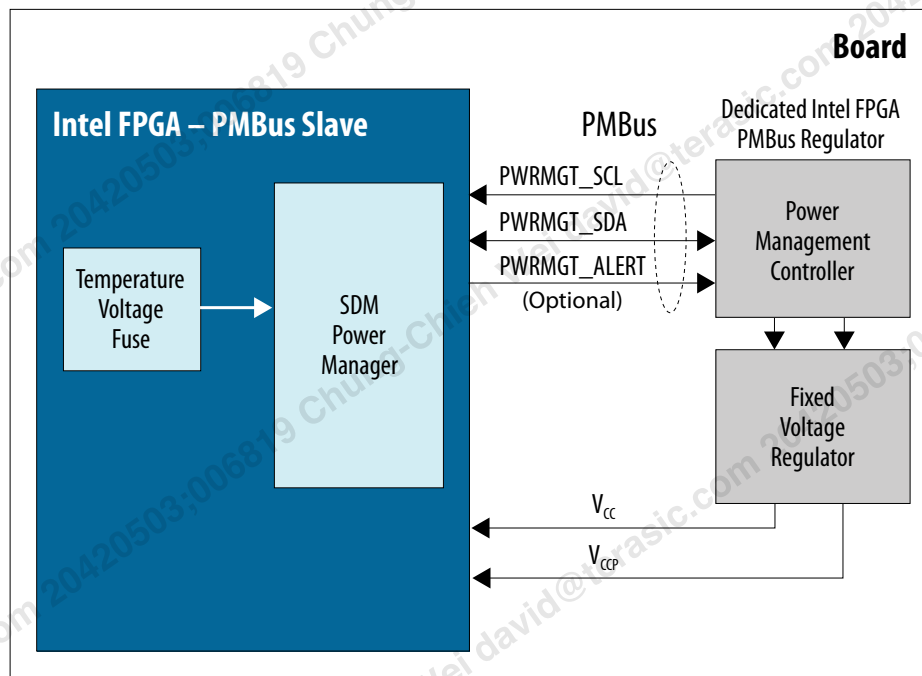
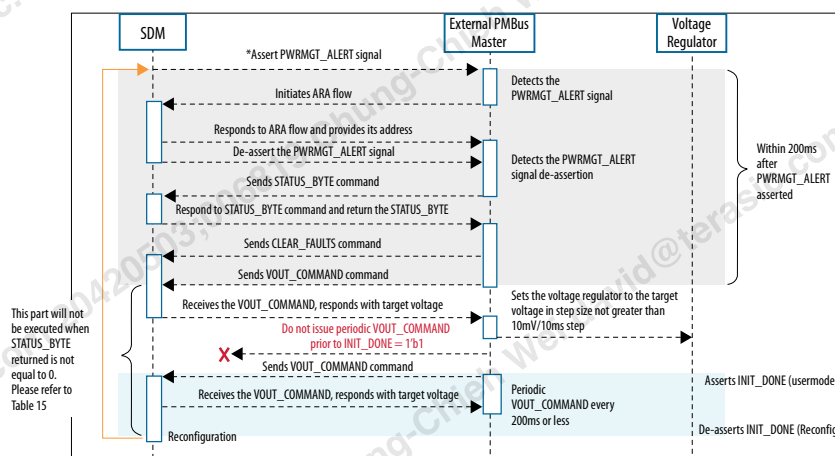


Table 15. Supported Commands for the PMBus Slave Mode

Command Name	Command Code	Default	PMBus Transaction Type	Number of Bytes
CLEAR_FAULTS	03h	—	Send byte	0
VOUT_MODE	20h	40h	Read byte	1
VOUT_COMMAND	21h	—	Read word	2
STATUS_BYTE	78h	00h	Read byte	1

Figure 14. Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode with the PWRMGT_ALERT Signal

*The external PMBus master must poll the state of the PWRMGT_ALERT pin periodically, at an interval not longer than 100 ms until the PWRMGT_ALERT signal is asserted.

Note:

(1) The following are the details of the alert response address (ARA) flow:

- (a) When operating in the slave mode with PWRMGT_ALERT PMBus connection, the slave device uses the PWRMGT_ALERT signal to indicate the master device that an update is required.
- (b) Upon reception of the PWRMGT_ALERT signal, the external master device uses the ARA flow to determine which slave device has asserted the PWRMGT_ALERT signal.
- (c) The ARA flow is one-byte, broadcast read from the master device to the reserved Alert Response Address (0x0C).
- (d) The slave device that has asserted the PWRMGT_ALERT signal responds to this ARA flow with its address.
- (e) The slave device de-asserts the PWRMGT_ALERT signal after providing its address. The external master device uses the address provided to communicate with the correct slave device.

Table 16. Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE=0

Sequence	SDM	PMBus Master	Notes
1	Asserts the PWRMGT_ALERT signal	—	—
2	—	Detects the PWRMGT_ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the PWRMGT_ALERT signal in step 1 responds to the ARA flow by providing its address.
continued...			

Sequence	SDM	PMBus Master	Notes
5	De-asserts the PWRMGT_ALERT signal	—	The PWRMGT_ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.
6	—	Reads the STATUS_BYTE	—
7	Returns STATUS_BYTE=0	—	Indicates the FPGA voltage requires an update.
8	—	Sends CLEAR_FAULTS	—
9	—	Sends VOUT_COMMAND	The VOUT_COMMAND must be received by the SDM within 200ms after the PWRMGT_ALERT signal is asserted. Failure to meet this requirement causes configuration error. ⁽⁷⁾
10	Receives the VOUT_COMMAND, responds with the target voltage	—	Calculated based on the temperature, the VID fuse and the coefficient for the direct format (you need to specify this input).
11	—	Sets the voltage regulator to the target voltage in step size not greater than 10mV/10ms step	—

⁽⁷⁾ When there is an error triggered by the SDM because it did not receive the VOUT_COMMAND within the specified time, you must power cycle the device to recover from the error. If you do not power cycle the device to recover from the error, you cannot configure the device successfully.

Table 17. Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE is not equals to 0

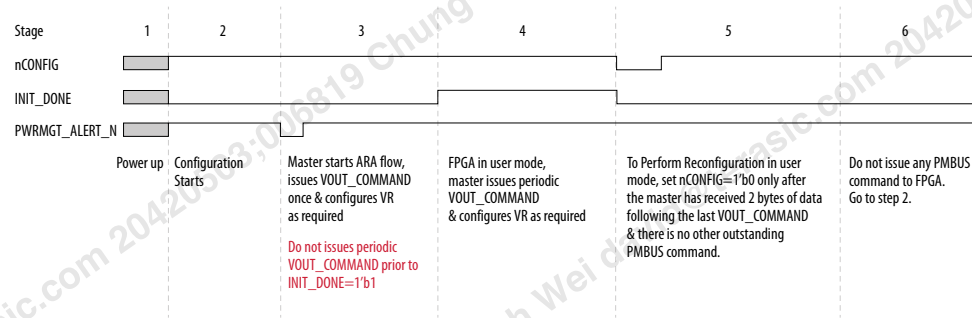
Sequence	SDM	PMBus Master	Notes
1	Asserts the PWRMGT_ALERT signal	—	The SDM detects fault and asserts the PWRMGT_ALERT signal. ⁽⁸⁾
2	—	Detects the PWRMGT_ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the PWRMGT_ALERT signal in step 1 responds to the ARA flow by providing its address.
5	De-asserts the PWRMGT_ALERT signal	—	The PWRMGT_ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.
6	—	Reads the STATUS_BYTE	—
7	Returns the STATUS_BYTE when not equal to 0	—	Indicates that other fault has occurred
8	—	Sends CLEAR_FAULTS	To reset the STATUS_BYTE.
9	—	Reads the STATUS_BYTE	To confirm that STATUS_BYTE=0.
10	—	External master to handle the faults	—

⁽⁸⁾ The following faults can raise the PWRMGT_ALERT signal:

- PMBUS_ERR_RD_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_WR_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_UNSUPPORTED_CMD (VOUT_COMMAND, VOUT_MODE, READ_STATUS, and CLEAR_FAULTS are the only supported commands in the PMBus Slave Mode)
- PMBUS_ERR_READ_FLAG (Received duplicate command before being able to respond to the first command)
- PMBUS_ERR_INVALID_DATA (Invalid or malformed PMBus/I2C message)

If any of the above errors are detected, the PWRMGT_ALERT signal is raised and bit 1 of the status register is set.

Figure 15. Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram with PWRMGT_ALERT



The Intel Agilex 5 devices in the PMBus slave mode sends the `VOUT_COMMAND` value in the direct format only. To read the actual voltage value, use the following equation to convert the `VOUT_COMMAND` value from the Intel Agilex 5 devices.

Figure 16. Direct Format Equation

$$X = \frac{1}{m} (Y \times 10^{-R} - b)$$

The equation shows how to convert the direct format value where:

- X, is the calculated, real value in mV;
- m, is the slope coefficient, a 2-byte two's complement integer;
- Y, is the 2-byte two's complement integer received from the Intel Agilex 5 devices;
- b, is the offset, a 2-byte two's complement integer;
- R, is the exponent, a 1-byte two's complement integer

The following example shows how an external power management controller retrieves values from the Intel Agilex 5 devices. Coefficients used in the `VOUT_COMMAND` are as follows:

- m = 1
- b = 0
- R = 0

If the external power management controller retrieved a value of 0384h, it is equivalent to the following:

$$X = (1/1) \times (0384h \times 10^{-0} - 0) = 900 \text{ mV} = 0.90 \text{ V}$$

5.1.2.3. Fail Safe Mechanism

If a miscommunication situation happens between the FPGA device and the external voltage regulator, the voltage regulator might be supplying unexpected voltage to the FPGA device.

To avoid voltage supply issue to the FPGA device, a safety net check processing is implemented in the Intel Quartus Prime software against your input setting (coefficient value—m, b, r for the direct mode and N for the linear mode) in the power management GUI.

The fail safe mechanism detects the early issue during the configuration phase, before the PMBus communication is established with the voltage regulator, prior to any voltage adjustment. If an error occurred, configuration is unsuccessful.

The Intel Quartus Prime software maintains a list of Intel validated voltage regulator's coefficient values. During configuration, the firmware performs the calculation and conversion based on the information of your selected voltage regulator in the Intel Quartus Prime GUI to obtain the respective voltage regulator data, using the PMBus Direct or Linear format formula. The calculated data is then compared against the Intel's maintained voltage regulator information in the Intel Quartus Prime software. If there is no matching data, configuration fails and the VOUT_COMMAND is not sent. However, this safety net check is not applicable when you select the voltage regulator type as "Other" in the Intel Quartus Prime GUI.

5.1.2.4. Fault Management and Error Reporting

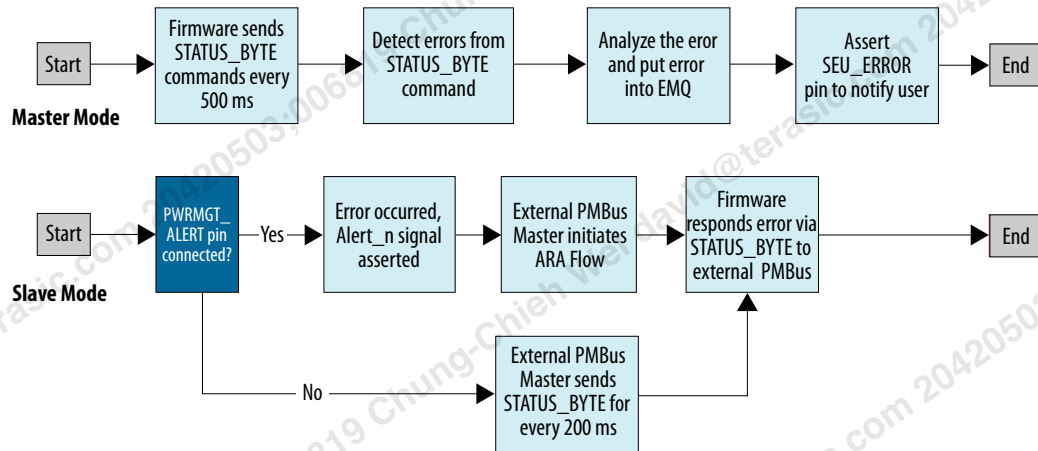
The SDM firmware has the capability to detect error, fault, or warning in the PMBus throughout the initialization and monitor states. The firmware analyzes any error and put it into the Error Message Queue (EMQ). During configuration, the CONFIG_STATUS mailbox command notifies you about the error.

In the master mode while running the monitor state, the SDM firmware queries the voltage regulator with a STATUS_BYTE command for every 500 ms. If the value returned from the STATUS_BYTE is not equal to zero, it indicates an error, fault, or warning within the voltage regulator. This firmware reports the error through the EMQ and assert the SEU_ERROR pin to notify you of this error.

In the slave mode, the PWRMGT_ALERT is an optional pin. If the PWRMGT_ALERT pin is connected, the SDM firmware asserts the ALERT_n signal whenever there is an error occurred. The external PMBus master has to initiate the ARA flow to handshake with the FPGA to read the error from the firmware. If the PWRMGT_ALERT pin is not connected, the external PMBus master sends the STATUS_BYTE command to the FPGA device periodically every 200 ms to check for errors.

The STATUS_BYTE Polling

Figure 17. Fault Management and Error Reporting



Note: The polling of the STATUS_BYTE every 500 ms in the master mode is applicable when you select the voltage regulator that has been validated by Intel. If you select "Others" in the Intel Quartus Prime GUI, the STATUS_BYTE polling is disabled.

The following table shows the error of the STATUS_BYTE based on the return bit.

Table 18. STATUS_BYTE Error Definition

Command	Error Definition
STATUS_BYTE (78h)	Bit[7]: Busy, unable to respond
	Bit[6]: Off, not enabled
	Bit[5]: Output over voltage fault occurred
	Bit[4]: Output over current fault occurred
	Bit[3]: Input under voltage fault occurred
	Bit[2]: Temperature fault or warning occurred
	Bit[1]: Communication, memory, or logic fault occurred
	Bit[0]: The fault occurred that are not listed above

Each bit returns from the STATUS_BYTE indicate a different error occurring in the voltage regulator and firmware reports each of them into the EMQ. For example, a value of 0x6 (b'0000_0110) returns from the STATUS_BYTE read reports that the voltage regulator is having communication, memory, or logic fault and temperature fault or warning asserted, the firmware inputs there 2 error entries into the EMQ for each of the error or fault occurred.

You must program non-volatile memory (NVM) in the voltage regulator correctly to ensure the error flag is not asserted incorrectly for the expected operating condition.

For Intel Agilex 5 SmartVID devices, V_{CC} and V_{CCP} operate within the 0.70 V to 0.90 V voltage range. The following is the example settings that works for this voltage range. You may revise the settings based on your system requirements.

```
VOUT_OV_WARN_LIMIT to VID_MAX 920mV
VOUT_OV_FAULT_LIMIT to VID_MAX 930mV
VOUT_MAX to VID_MAX 950mV
VOUT_UV_WARN_LIMIT to VID_MIN 690mV
VOUT_UV_FAULT_LIMIT to VID_MIN 680mV
```

Limit should be wider or larger than the expected operating conditions, but within the absolute maximum rating for the device. For more information, refer to the *Intel Agilex 5 FPGAs and SoCs Device Data Sheet*.

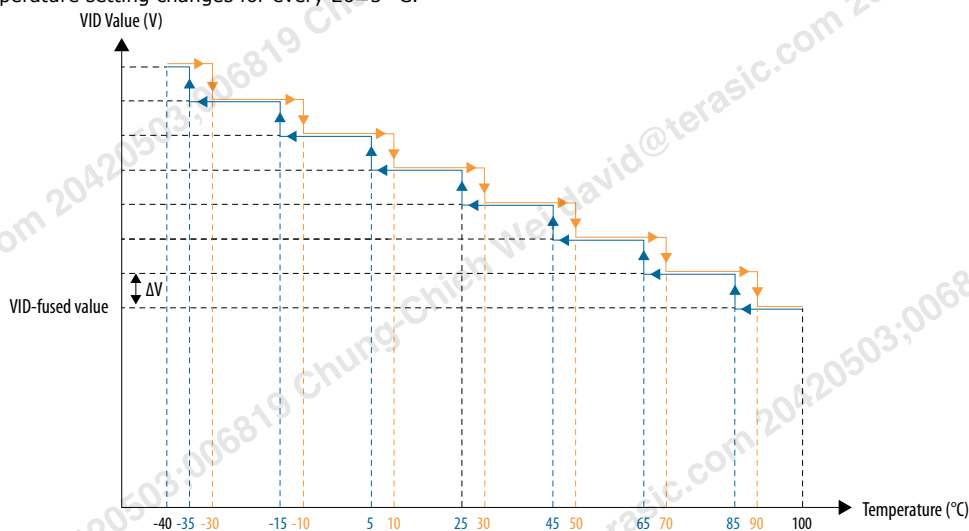
5.1.3. Temperature Compensation

Intel Agilex 5 devices are able to compensate for performance degradation at colder temperatures by raising the voltage. While raising the voltage increases the dynamic power consumption, the increase in dynamic power consumption is countered by lower leakage at cold temperatures, thus enabling total power consumption at cold temperatures to still be equal or lower than at hot temperatures.

The SmartVID feature supports this dynamic voltage adjustment. The SDM Power Manager checks for local temperature sensor changes and updates the new VID value with voltage step not more than 5 mV if the temperature crosses the threshold point.

Figure 18. Temperature Compensation for SmartVID for Intel Agilex 5 Devices—Preliminary

The SDM monitors the temperature, normally at every 100 ms, and adjusts the voltage by communicating with the power management system. Dynamic voltage adjustment is made by the SDM after the sensor detects the temperature setting changes for every 20 ± 5 °C.



5.1.4. Intel Agilex 5 Power Management and VID Implementation Guide

The Intel Agilex 5 SDM Power Management Firmware manages the SmartVID configuration and enables the FPGA to power up before you can access the FPGA.

The Intel Agilex 5 Power Management and VID interface is installed as part of the Intel Quartus Prime software.

5.1.4.1. Specifying Power Management and VID Parameters and Options

1. Create an Intel Quartus Prime project using the **New Project Wizard** available from the File menu.
2. On the **Assignments** menu, click **Device**.
3. On the **Device** dialog box, click **Device and Pin Options**.
4. On the **Device and Pin Options** dialog box, click **Configuration**.
5. On the **Configuration** page, specify the **VID Operation mode**. There are two modes available—PMBus Master and PMBus Slave.
6. The PMBus modes consist of these pins—PWMGT_SDA, PWMGT_SCL, and optional PWRMGT_ALERT. To configure these pins, on the **Configuration** page, click **Configuration Pin Options**. The PWRMGT_ALERT pin is only available and is optional to be used in the slave mode. For the configuration pin parameters, refer to Table: *Configuration Pin Parameters*.
7. On the **Configuration Pin** dialog box, assign the appropriate SDM_IO pin to the power management pins. Click **OK**.
8. On the **Device and Pin Options** dialog box, click **Power Management and VID** to specify the device settings if your device is in the PMBus Master mode. Click **OK**. For the power management and VID parameters, refer to Table: *Power Management and VID Parameters*.

This completes the SmartVID setup for the Intel Agilex 5 device.

5.1.4.1.1. Configuration Pin Parameters

Table 19. Configuration Pin Parameters

Use the parameter editor to configure these options.

Parameters	Value	Description
Use PWRMGT_SCL output	SDM_IO0	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO14 pin for this parameter.
	SDM_IO14	
Use PWRMGT_SDA output	SDM_IO11	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO11 pin for this parameter.
	SDM_IO12	
	SDM_IO16	
Use PWRMGT_ALERT output	SDM_IO0	This is an optional PMBus interface for the power management when the VID operation mode is the PMBus Slave mode.
	SDM_IO12	

continued...

Parameters	Value	Description
		Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO12 pin for this parameter.

5.1.4.1.2. Power Management and VID Parameters

You can use the following parameters to configure the Power Management and VID interface if the VID operation is in the PMBus Master mode.

Table 20. Power Management and VID Parameters

Parameters	Value	Description
Bus speed mode ⁽⁹⁾	100 KHz	Bus speed mode of PMBus interface when operating in the PMBus Master mode.
	400 KHz	
Slave device type ⁽⁹⁾	TPS53676	Supported device types. Intel recommends you to use one of the slave device type listed in the drop-down menu that has been tested with the Intel FPGA tools. If you are not using one of the slave device type listed in the drop-down menu, select Other option. When you select Other option, refer to Table: <i>SmartVID Regulator Requirements</i> , Table: <i>Supported Voltage Output Format for Intel Agilex 5 Devices with -V and -E Power Options</i> , and Table: <i>Supported Commands for the PMBus Master Mode</i> for the voltage regulator requirements details.
	LTC3882	
	ISL68223	
	Other	
Device address in PMBus Slave mode ⁽¹⁰⁾	7-bit hexadecimal value	Device address in the PMBus Slave mode.
Number of slave device	1 to 7, or All	Indicates the number of voltage regulator in the system.
Slave device_0 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address. This parameter must be non-zero when you are using the PMBus Master mode.
Slave device_1 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address.
Slave device_2 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address.
Slave device_3 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address.
Slave device_4 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address.
Slave device_5 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address.
Slave device_6 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address.
Slave device_7 address ⁽⁹⁾	7-bit hexadecimal value	External power regulator address.
Voltage output format ⁽⁹⁾	Direct format	The voltage output format when the operation mode is PMBus Master.

continued...

⁽⁹⁾ This parameter is used for the PMBus Master mode.

Parameters	Value	Description
	Linear format	<p>If the voltage output format is the Direct format, you must set the following parameters:</p> <ul style="list-style-type: none"> Direct format coefficient m Direct format coefficient b Direct format coefficient R <p>If the voltage regulator is the Linear format, you must set the Linear format N parameter. ⁽¹¹⁾</p> <p>For more information about the parameters, refer to your selected voltage regulator data sheet.</p> <p>For all voltage output format, you must also select the correct "translated voltage output unit".</p>
Direct format coefficient m ⁽⁹⁾	Signed integer: -32768 to 32767	Direct format coefficient m of the slave device type when the operation mode is PMBus Master. For more information about the coefficient value, refer to the respective voltage regulator data sheet.
Direct format coefficient b ⁽⁹⁾	Signed integer: -32768 to 32767	Direct format coefficient b of the slave device type when the operation mode is PMBus Master. For more information about the coefficient value, refer to the respective voltage regulator data sheet.
Direct format coefficient R ⁽⁹⁾	Signed integer: -128 to 127	Direct format coefficient R of the slave device type when the operation mode is PMBus Master. For more information about the coefficient value, refer to the respective voltage regulator data sheet.
Linear format N ⁽⁹⁾	Signed integer: -16 to 15	Output voltage command when the voltage output format is set to the Linear format.
Translated voltage value unit ⁽⁹⁾	millivolts	Indicates the translated output voltage is in millivolts (mV) or volts (V).
	volts	
Enable PAGE command ⁽⁹⁾	Enable	By enabling the PAGE command, the FPGA PMBus Master uses the PAGE command to set all the output channels (0xFF) on registered regulator modules to respond to VOUT_COMMAND. If only specified output channels on registered regulator modules must respond to VOUT_COMMAND, enter the corresponding page value (0x00 – 0xFF).
	Disable	

5.1.4.1.3. Power Management and VID Interface QSF Constraint Guide

You can specify the **Power Management** and **VID** parameters and options through QSF constraints command.

⁽¹⁰⁾ This parameter is used for the PMBus Slave mode.

⁽¹¹⁾ N is the exponent of a 5-bit two's complement integer.

For the configuration pin parameters, refer to Table: *Configuration Pin Parameters*. For the power management and VID parameters, refer to Table: *Power Management and VID Parameters*.

The following is the example of the VID parameter settings in the QSF. The value maybe different based on your usage and choice of voltage regulator.

Example 1. Specifying the Power Management and VID Parameters through QSF Constraints

```
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_PWRMGT_SCL SDM_IO14
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTM4677
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS41
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS42
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS43
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS44
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS45
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS46
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS47
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS48
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name PWRMGT_PAGE_COMMAND_PAYLOAD xx
```

5.2. DSP and M20K Power Gating

Intel Agilex 5 devices support power gating for both DSP blocks and M20K memory blocks. By default, the Intel Quartus Prime software automatically configures unused DSP blocks and M20K memory blocks to be power gated.

5.3. Clock Gating

Clock gating can be used to reduce dynamic power consumption. When an application is idle, its clock can be gated temporarily and ungated based on wake-up events. This is done using user logic to enable or disable the programmable clock routing.

You can perform dynamic power reduction by gating the clock signals of any circuitry not used by the design in the Intel Agilex 5 devices.

Clock networks can be gated using one of the following methods:

Root Clock Gate

You can dynamically gate each clock network at the root level using the Clock Control Intel FPGA IP Core.

Sector Clock Gate

You can dynamically gate each clock network at the clock sector level using the Clock Control Intel FPGA IP Core.

I/O PLL Clock Gate

You can dynamically gate each output counter of the Intel Agilex 5 I/O PLLs using IOPLL Reconfiguration.

Clock gating a large portion of your FPGA design could cause significant current change over a short time period when the gated circuitry is enabled or disabled. The maximum current step resulting from this clock gating should be sized such that it does not create noise exceeding the maximum allowed AC noise specification, as determined by the PDN decoupling design on your PCB. You can control the current step size by dividing a large gated area into smaller sub-regions and staging those regions to enter or exit power gating sequentially.

For more details, refer to the *Clock Gating* section in the *Intel Agilex 5 Clocking and PLL User Guide*.

5.4. Power Sense Line

Intel Agilex 5 devices support the power sense line feature. VCCLSENSE and GNDSENSE pins are differential remote sense pins used to monitor the V_{CC} power supply.

You must connect the VCCLSENSE and GNDSENSE pins to the remote sense inputs for the regulator supplying V_{CC} rail that supports the remote voltage sensing feature.

5.5. Power Optimization Techniques in the Intel Quartus Prime Software

The Intel Quartus Prime software offers power-driven compilation to fully optimize device power consumption.

Power-driven compilation focuses on reducing the design's total power consumption in synthesis and place-and-route stages. For detailed information, refer to the *Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization*.



Related Information

[Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization](#)



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6. Document Revision History for the Intel Agilex 5 Power Management User Guide

Document Version	Changes
2023.02.10	Initial release.

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