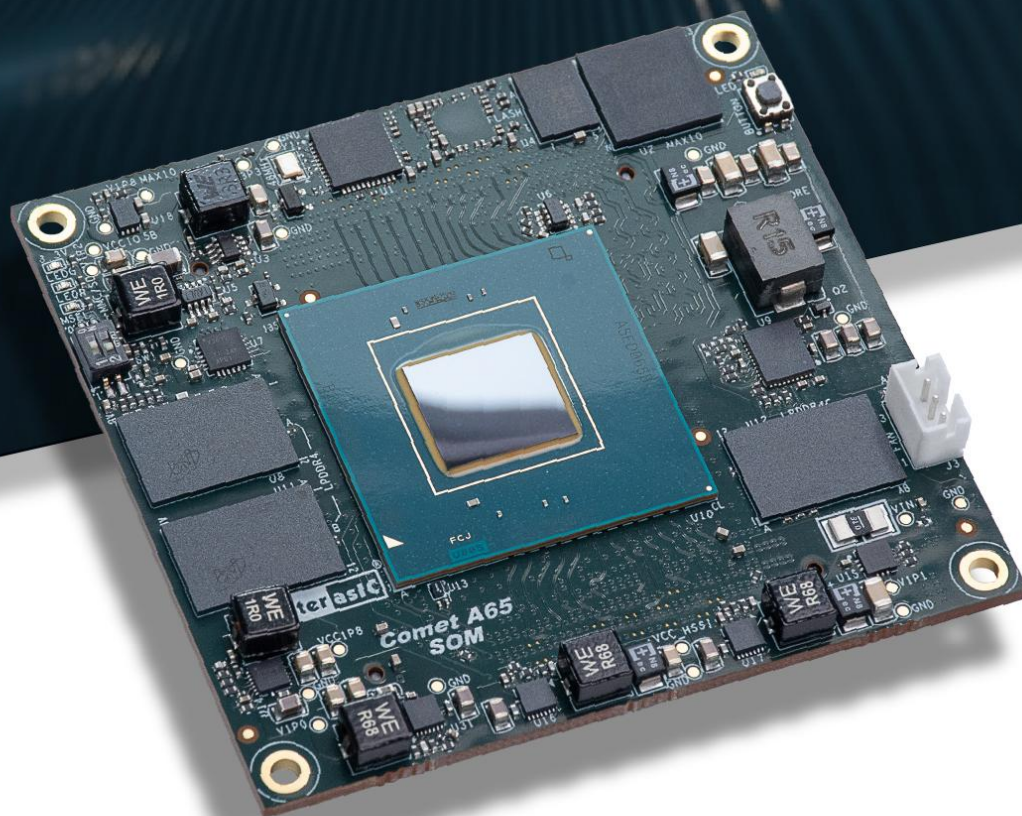


Comet-A65 SOM



User Manual

FPGA

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Chapter 1

Overview

This chapter provides an overview of the Comet A65 SoM Board and installation guide.

1.1 General Description

The Comet A65 SOM is Terasic's new System-On-Module powered by Altera's largest Agilex® 5 SoC FPGA with 656K logic elements. The SOM integrates an HPS/ARM subsystem, three 4GB high-throughput LPDDR4, two high-speed SEAM8 extension connectors, to support 71 LVDS, 245 LVCMOS and 24 transceivers. It enables embedded software/systems developers without FPGA expertise to develop various industrial applications, such as medical equipment, robotics, industrial communication and control, machine vision, smart camera and smart city.

Available in production-qualified and certified commercial grade, the Comet A65 SOM is purpose-built for your volume edge deployment and ruggedized for long life cycle operation.

Included with Comet A65 SOM is a free license for Altera® Quartus® Pro Edition software — no additional license purchase is required. Developers can leverage full design and compilation capabilities of Quartus Pro without incurring licensing fees. Learn more about acquiring your free license.

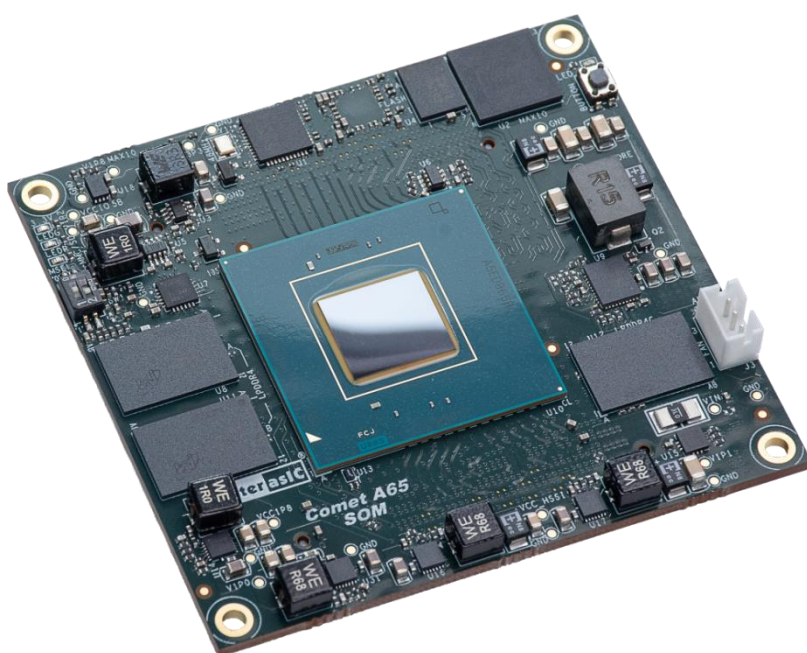


Figure 1-1 Comet A65 SoM Board

1.2 Board Layout

The figures below depict the layout of the board and indicate the location of the connectors and key components.

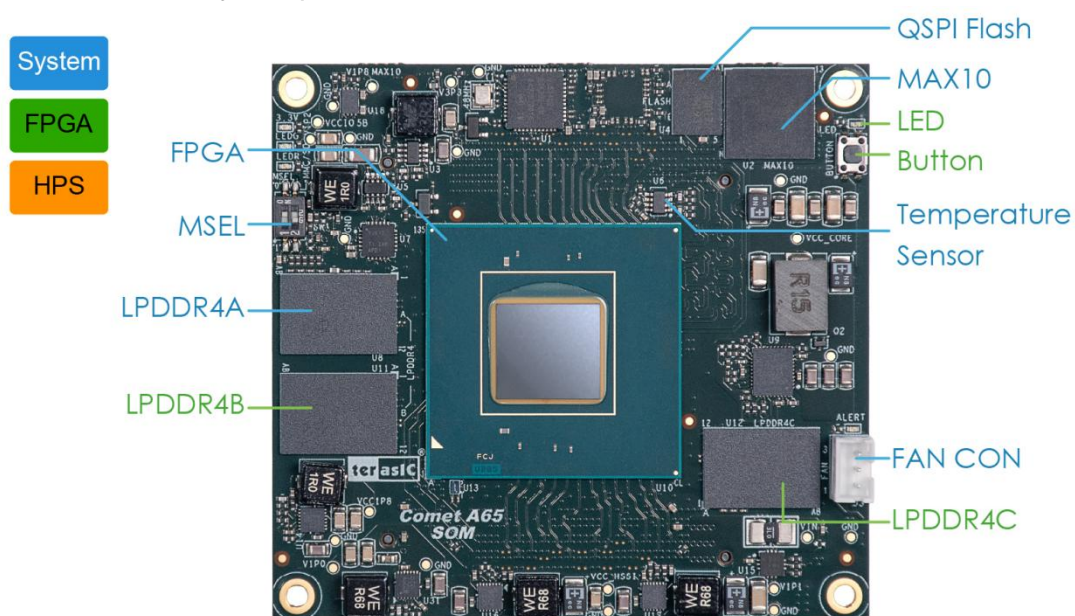


Figure 1-2 Comet A65 SoM Board top

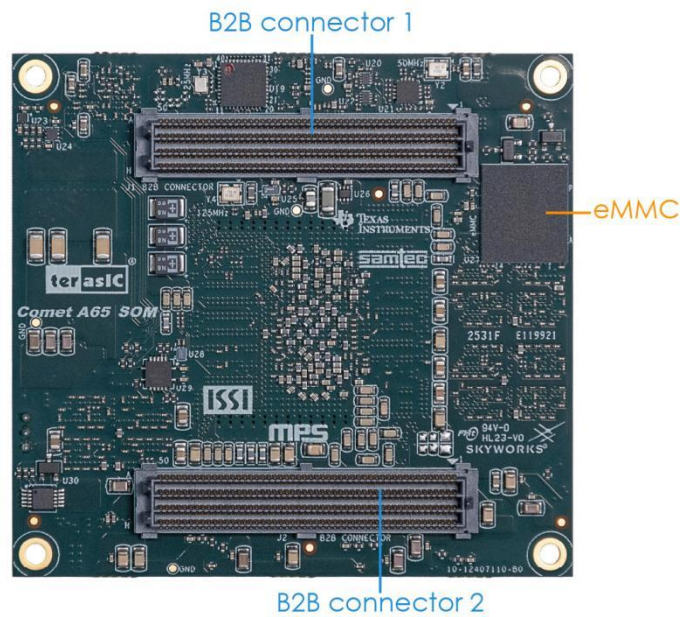


Figure 1-3 Comet A65 SoM Board bottom

1.3 Key Features

The following hardware is implemented on the Comet A65 SoM Board:

■ System

- FPGA: A5ED065BB32AE4S (Agilex 5 E-Series Device Group B*)
- Module Size : 75mm x 75mm
- 102 HVIO (3.3V x4, 1.8/2.5/3.3 x98)
- 143 HSIO (71 LVDS)
- 48 HPSIO
- 24 Transceivers
- Interface: Two SEAM8 Connectors (4x100 pin)
- Board Management System
 - Power and Temperature Monitor
 - Auto Fan Control
 - Auto shutdown when power or temperature is abnormal

■ FPGA Side

- LED x1, KEY x1
- Fixed 50 /100MHz Clock

- Programmer Clock Generator for transceiver reference clock
- LPDDR4-A: 4GB LPDDR4 with 32-bit data bus (no ECC). Shared with HPS
- LPDDR4-B: 4GB LPDDR4 with 32-bit data bus (no ECC)
- LPDDR4-C: 4GB LPDDR4 with 32-bit data bus (no ECC)
- 102-pin HVIO and 143-pin HSIO connected to SEAM8 connector
- 24 transceiver and 4 reference clock connected to SEAM8 2 connectors

■ HPS(Hard Processor System) Side

- LPDDR4-A: 4GB LPDDR4 with 32-bit data bus (no ECC). Shared with FPGA.
- 48 HPS IO connected to ADF6 connector
- 8GB eMMC (Expandable) + eMMC SEL Switch

1.3. Block Diagram

Figure 1-4 shows the block diagram of the Comet A65 SoM Board. To provide maximum flexibility for the users, all key components are connected to the Agilex 5 SoC FPGA device. Thus, users can configure the FPGA to implement any system design.

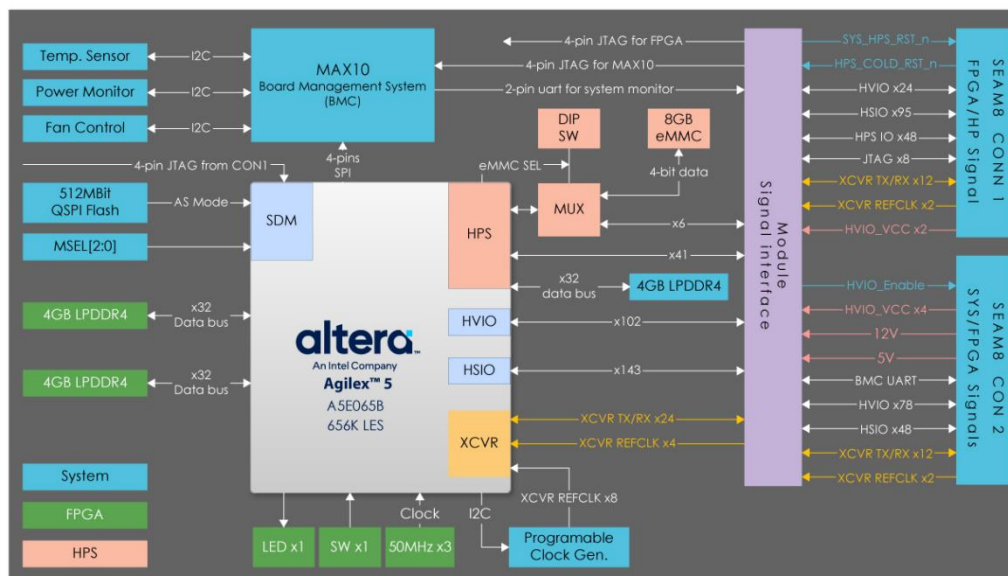


Figure 1-4 Block diagram of the Comet A65 SoM Board

1.4. Mechanical Specifications

Figure 1-5 and **Figure 1-6** shows the Mechanical Layout of Comet A65 SoM Board. The unit of the Mechanical Layout is millimeter (mm).

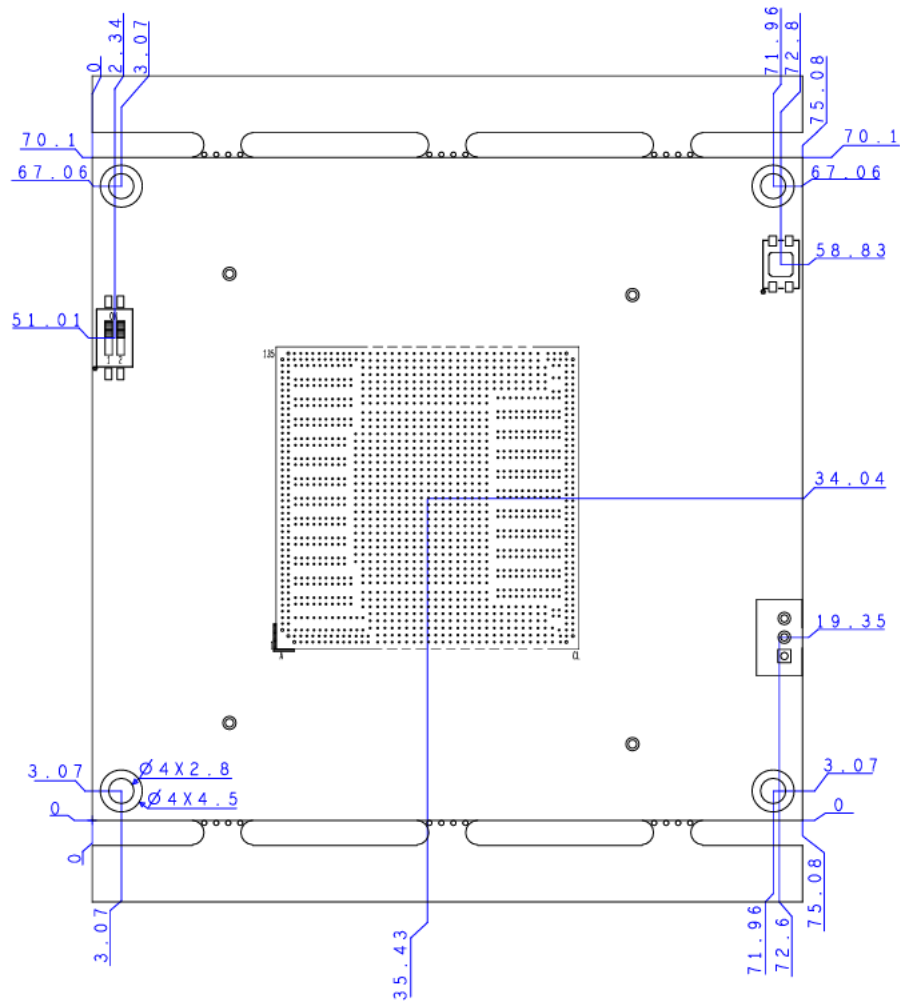


Figure 1-5 Mechanical layout (Top View)

Table 1-2 12V Power pin in B2B Connector

Number	B2B (J2) Pin Number	Comet A65 SoM Board Schematic
1	B47	VIN power pin, support 5V~12V power input
2	B48	
3	B49	
4	B50	
5	D47	
6	D48	
7	D49	
8	D50	
9	F47	
10	F48	
11	F49	
12	F50	
13	H47	
14	H48	
15	H49	
16	H50	

1.6. Connectivity

The Comet A65 SoM Board offers SEAM8 B2B connectors for expansion. Through the B2B connector, users can interface with the carrier board (see [Figure 1-7](#)) to access power delivery and multiple expansion interfaces, including USB Blaster programming, communication links, multimedia outputs, and memory peripherals.

If user wants to make their owned carrier board to connect with the Comet A65 SoM Board, The following table (Table 1-3) lists the manufacturer and manufacturer part numbers of the B2B connector that can match with the connector of the Comet A65 SoM Board.

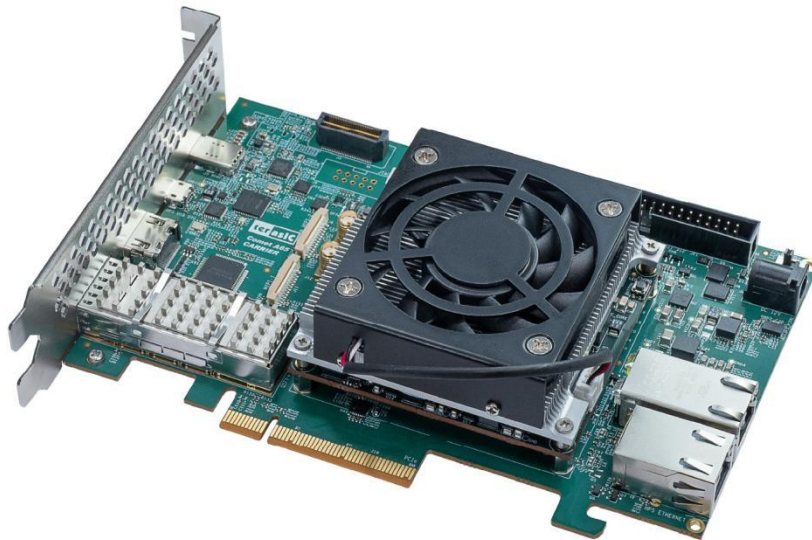


Figure 1-7 Comet A65 SoM Board connects to the carrier board

Table 1-3 Part Number of the connector on the Comet A65 SoM Board

Connector	Comet A65 SoM Board's Part Number	Carrier Board's Part Number
B2B	J1/J2 Samtec : SEAM8-50-S02.0-S-08-3	Samtec :SEAF8-50-05.0-S-08-3

Chapter 2

Board Component

This chapter introduces all the important components on the Comet A65 SoM.

2.1 Configuration Interface

The FPGA on the Comet A65 SoM Board can use two configuration modes: JTAG and Active Serial (AS). Below, we will describe these two modes in detail:

■ **JTAG Programming mode**

JTAG configuration mode is one of the most common methods for programming an FPGA during development. In this mode, a configuration file with the extension .sof (SRAM Object File) is downloaded to the FPGA via a JTAG programming circuit. However, because the .sof file is loaded into the FPGA's volatile SRAM, the configuration is lost when power is turned off. As a result, the FPGA must be reprogrammed each time it is powered on.

Note 1: The Comet A65 SoM Board does not include an on board USB Blaster circuit. Users must either provide a USB Blaster circuit or other JTAG programming interface on the carrier board.

Note 2: The Comet A65 SoM Board features two FPGA devices: Agilex 5 and MAX 10. The JTAG buses of both devices are switched through a multiplexer and share a common path routed to the carrier board via the B2B connector. Users must configure a switch to select whether the JTAG bus of the Agilex 5 or the MAX 10 is connected to the carrier board. The default setting is the JTAG bus of the Agilex 5 FPGA connected to the B2B connector.

■ **Active Serial Fast mode**

The Active Serial Fast (AS fast) mode is a non-volatile configuration scheme for altera

FPGAs, utilizing an external Quad SPI (QSPI) Flash memory to store the configuration bitstream. Upon power-up, the FPGA autonomously reads this configuration data from the QSPI Flash, enabling self-contained device initialization. Because the configuration persists across power cycles, the AS fast mode is well-suited for applications demanding reliable, standalone operation without requiring configuration by an external host after initial programming.

Figure 2-1 shows the JTAG interface and configuration device of the Comet A65 SoM Board.

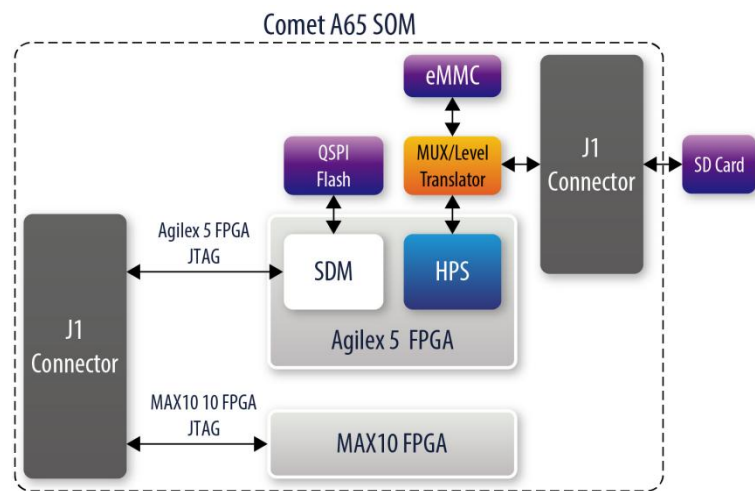


Figure 2-1 Block diagram of the JTAG interface and configuration for the board

Figure 2-2 and Table 2-1 shows the configuration switch settings.

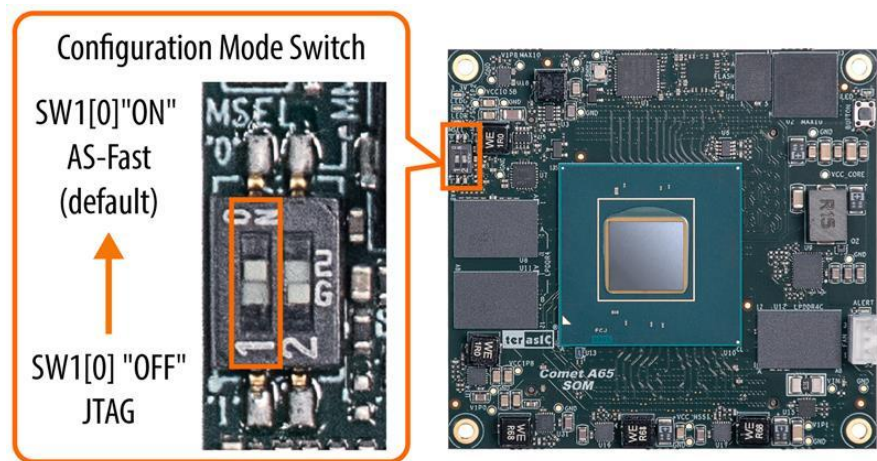


Figure 2-2 Position of slide switches SW1

Table 2-1 SW1 setting

Board Reference	Signal Name	Description	Default
SW1[0]	MSEL[2] and MSEL[1]	0: AS-Fast(Default Setting)	0
		1:Jtag	

The following content will introduce the HPS boot process within the SoC FPGA.

■ SoC FPGA boot

The boot process for Agilex 5 SoC FPGAs can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and FPGA fabric after powering on. More details can be found in the user documentation: [Hard Processor System Booting User Guide: Agilex 5 SoCs](#).

The factory setting of the SoC boot of the Comet A65 SoM Board is the **FPGA Boot First Mode**. The architecture is shown in the **Figure 2-3**. Two storage mediums are used. The system needs QSPI flash on Comet A65 SoM as SDM flash for booting.

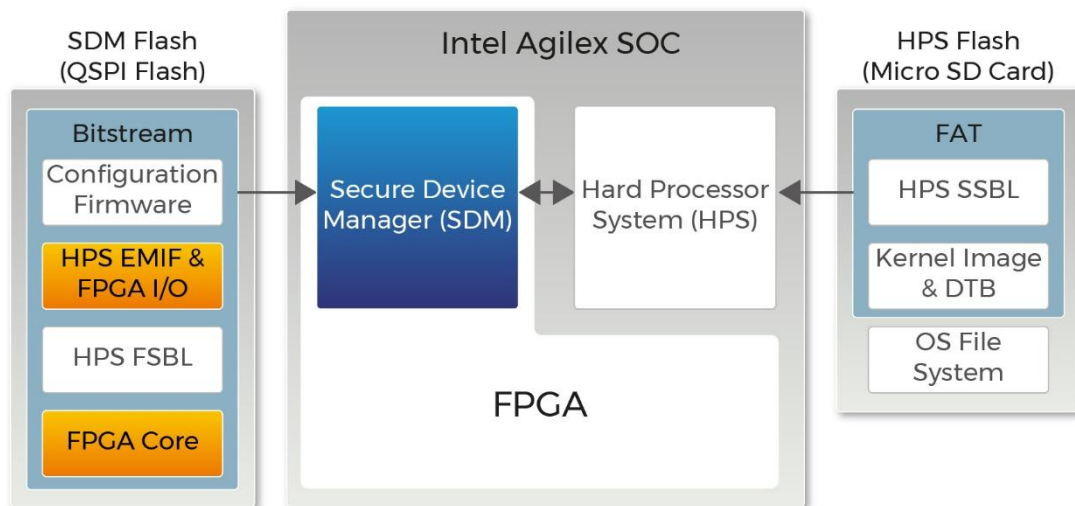


Figure 2-3 FPGA boot First Dual Flash (SDM and HPS)

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the eMMC flash with built-in image data as HPS flash, which is used for HPS boot in the later part. The eMMC flash stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Comet A65 SoM is summarized as follows:

When the Comet A65 SoM Board is powered on, the SDM will read the configuration firmware and complete SDM initial from the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the eMMC flash into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

2.2 Setup and Status Components

This section will introduce the use of the switch for setup on the Comet A65 SoM board, as well as a description of the various status LEDs.

■ Status LED

The FPGA development board includes board-specific status LEDs to indicate board status. Please refer to Table 2-2 for the description of the LED indicators. **Figure 2-4** shows the location of all these status LEDs.

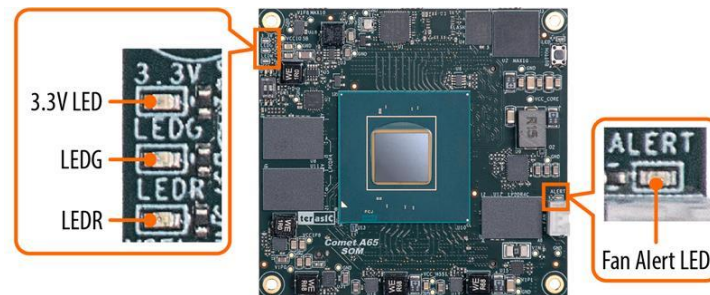


Figure 2-4 Position of the status LED

Table 2-2 Status LED

Board Reference	LED Name	Description
D1	LEDB	Illuminates when 3.3-V power is active.
D2	LEDR	<ol style="list-style-type: none"> LED will light up: <ol style="list-style-type: none"> turn on the power for 0.3 seconds The carrier board has a power-on anomaly The carrier board powers on successfully but then automatically shuts down due to some reason The power supply experiences an anomaly while the system has not been shut down LED will blink when the whole system is shutdown: <ol style="list-style-type: none"> the FPGA temperature on the board temperature exceeds 95 degrees. the power consumption exceeds 80W. when the current of VCC_CORE exceeds 45A. Also, all the power of the FPGA will be cut off when this LED is blinking.
D3	LEDG	Illuminates after power is turned on for 0.3 seconds or all carrier board power supplies are properly started (POWER_READY)
D4	FAN_ALERT	Illuminates when the fan is abnormal, such as when

		the fan speed is different from expected
--	--	------------------------------------------

2.3 Clock Circuit

Figure 2-5 shows the clock tree of the Comet A65 SoM board.

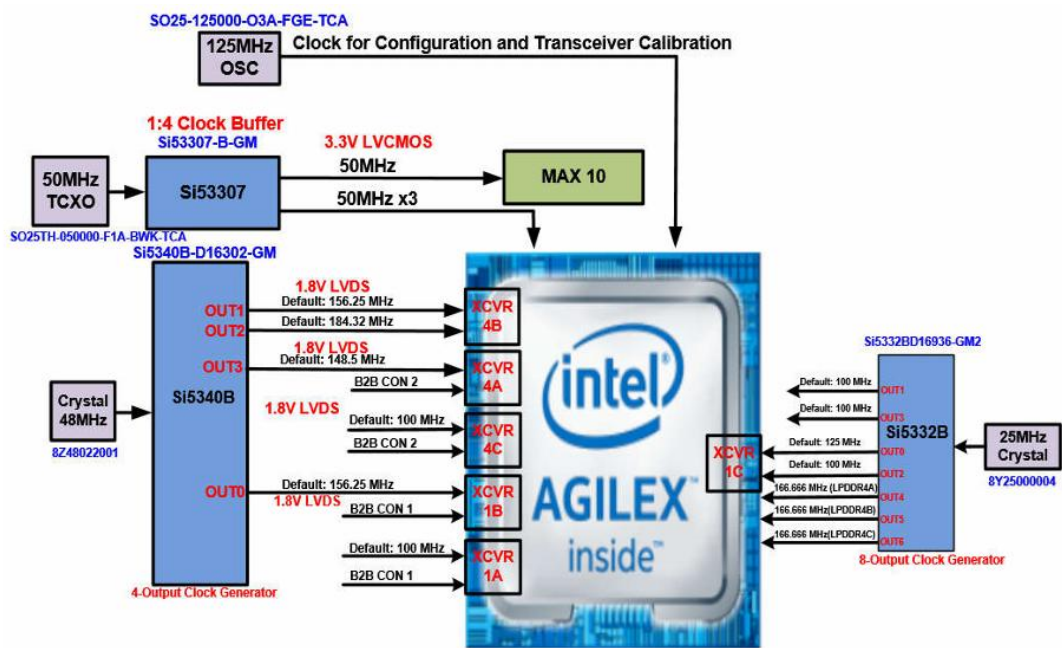


Figure 2-5 Clock tree of the FPGA Board

The primary clock sources on the SoM are generated by two programmable PLL clock generators (Si5340B and Si5332B) and a 50 MHz oscillator.

Si5340B primarily provides reference clocks for the FPGA transceivers. Si5332B supplies reference clocks to both the FPGA transceivers and the three LPDDR4 memory interfaces.

The 50 MHz oscillator, in combination with the Si53307 clock buffer, delivers reference clocks to the FPGA core and MAX 10.

The SO25-125000-O3A-FGE-TCA 125MHz oscillator functions as the reference clock for FPGA configuration and transceiver calibration.

Table 2-3, Table 2-4, Table 2-5 and Table 2-6 list the clock pin assignments and default

frequency for the **Si5340B**, **Si5332B**, **Si53307** and **SO25-125000-O3A-FGE-TCA**, respectively

Table 2-3 Clock Pin Assignments of the Si5340B

Clock Output Port	Schematic Signal Name	Default Frequency	I/O Standard	Connected to	Application
OUT0	GTSL1B_REFCLK_156M25_p	156.25 MHz	1.8V LVDS	Agilex 5 PIN_AY120	Reference clock for FPGA transceiver bank 1B
$\overline{\text{out0}}$	GTSL1B_REFCLK_156M25_n			Agilex 5 PIN_AY115	
OUT1	GTSR4B_REFCLK_156M25_p	156.25 MHz	1.8V LVDS	Agilex 5 PIN_AY16	Reference clock for FPGA transceiver bank 4B
$\overline{\text{out1}}$	GTSR4B_REFCLK_156M25_n			Agilex 5 PIN_AY21	
OUT2	GTSR4B_REFCLK_184M32_p	184.32Mhz	1.8V LVDS	Agilex 5 PIN_AV16	Reference clock for FPGA transceiver bank 4B
$\overline{\text{out2}}$	GTSR4B_REFCLK_184M32_n			Agilex 5 PIN_AV21	
OUT3	GTSR4A_REFCLK_148M5_p	148.5MHz	1.8V LVDS	Agilex 5 PIN_BB16	Reference clock for FPGA transceiver bank 4A
$\overline{\text{out3}}$	GTSR4A_REFCLK_148M5_n			Agilex 5 PIN_BB21	

Table 2-4 Clock Pin Assignments of the Si5332B

Clock Output Port	Schematic Signal Name	Default Frequency	I/O Standard	Connected to	Application
OUT0	GTSL1C_REFCLK_156M25_p	156.25MHz	LVDS	Agilex 5 PIN_AT120	Reference clock for FPGA transceiver bank 1C
OUT0B	GTSL1C_REFCLK_156M25_n			Agilex 5 PIN_AT115	
OUT1	GTSL1A_REFCLK_100M_p	100MHz	LVDS	Agilex 5 PIN_BB120	Reference clock for

OUT1B	GTSL1A_REFCLK_100M_n			Agilex 5 PIN_BB115	FPGA transceiver bank 1A
OUT2	GTSL1C_REFCLK_100M_p	100MHz	LVDS	Agilex 5 PIN_AP120	Reference clock for
OUT2B	GTSL1C_REFCLK_100M_n			Agilex 5 PIN_AP115	FPGA transceiver bank 1C
OUT3	GTSR4C_REFCLK_100M_p	100MHz	LVDS	Agilex 5 PIN_AT16	Reference clock for
OUT3B	GTSR4C_REFCLK_100M_n			Agilex 5 PIN_AT21	FPGA transceiver bank 4C
OUT4	LPDDR4A_REFCLK_p	166.666MHz	LVDS	Agilex 5 PIN_M105	LPDDR4A reference clock
OUT4B	LPDDR4A_REFCLK_n			Agilex 5 PIN_K105	
OUT5	LPDDR4B_REFCLK_p	166.666MHz	LVDS	Agilex 5 PIN_T65	LPDDR4B reference clock
OUT5B	LPDDR4B_REFCLK_n			Agilex 5 PIN_P65	
OUT6	LPDDR4C_REFCLK_p	166.666MHz	LVDS	Agilex 5 PIN_CH38	LPDDR4C reference clock
OUT6B	LPDDR4C_REFCLK_n			Agilex 5 PIN_CF38	
OUT7	-	-	-	-	-
OUT7B	-	-	-	-	-

Table 2-5 Clock Pin Assignments of the Si53307-B-GM

Clock Output Port	Schematic Signal Name	Default Frequency	I/O Standard	Connected to	Application
Q0	CLK_50_5B	50MHz	3.3V	Agilex 5 PIN_BE107	Reference clock for FPGA

$\overline{Q0}$	CLK_50_6A	50MHz	support 1.8/2.5/3.3V	Agilex 5 PIN_BK31	Reference clock for FPGA
Q1	CLK_50_6C	50Mhz	support 1.8/2.5/3.3V (Depend on VCCIO_6C)	Agilex 5 PIN_D8	Reference clock for FPGA
$\overline{Q1}$	OSC_50_MAX10	50MHz	3.3V	MAX 10 PIN_H4	Reference clock for MAX 10

Table 2-6 Clock Pin Assignments of the SO25-125000-O3A-FGE-TCA

Clcok Output Port	Schematic Signal Name	Default Frequency	I/O Standard	Connected to	Application
OUT	OSC_CLK_1	125MHz	1.8V	Agilex 5 PIN_BR102	Clock for Configuration and Transceiver Calibration

2.4 General User I/O

This section describes the user I/O interface of the FPGA as shown in **Figure 2-6**.

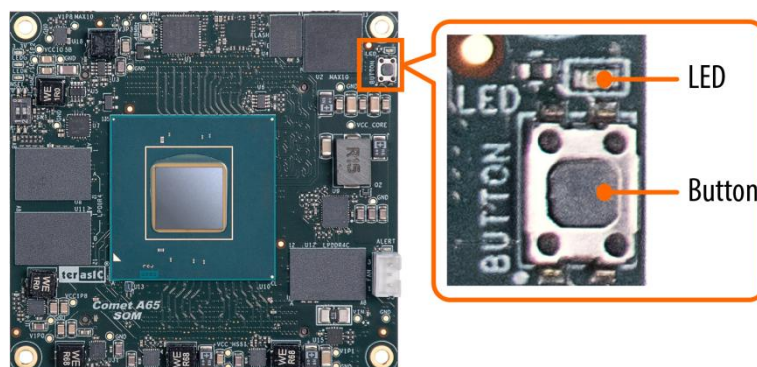


Figure 2-6 Position of all the user LEDs/Switches/Buttons

■ User Defined Push-button

The FPGA board includes one FPGA user defined push-button that allow users to interact with the Agilex 5. The push-button provides a high logic level or a low logic

level when it is not pressed or pressed, respectively. Table 2-7 lists the board references, signal name and its corresponding Agilex 5 device pin number for the push-button of the FPGA.

Table 2-7 Push-button Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
PB0	BUTTON	High Logic Level when the button is not pressed	3.0-V LVTTTL	PIN_BK112

■ User-Defined LED

The FPGA board consists of one FPGA user-controllable LED to allow status and debugging signal to be driven to the LED from the designs loaded into the Agilex 5 FPGA. The LED is driven directly by the FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin name on the FPGA that are connected to the LED is given in Table 2-8.

Table 2-8 User LEDs Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
LED	LED	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	3.3 V	PIN_BF120

2.5 Micro SD Card and eMMC

The SoM provides on-board 8GB eMMC device (IS21EF08G-JCLI) and Micro SD Card (which is on the Carrier board and using B2B connector to access) for HPS fabric in the FPGA (See Figure 2-7). Users can choose one of them for HPS boot/data/system storage. The switch SW1.2(See Figure 2-8 SW1[1]) on the board can help the user select which device (Micro SD Card on J1 or eMMC) will be used for HPS fabric. The Micro SD card socket can provide flexible capacity expansion while

eMMC device can support stable and fixed storage solutions. **Table 2-9** lists the pin assignment of Micro SD card socket and eMMC device to the HPS.

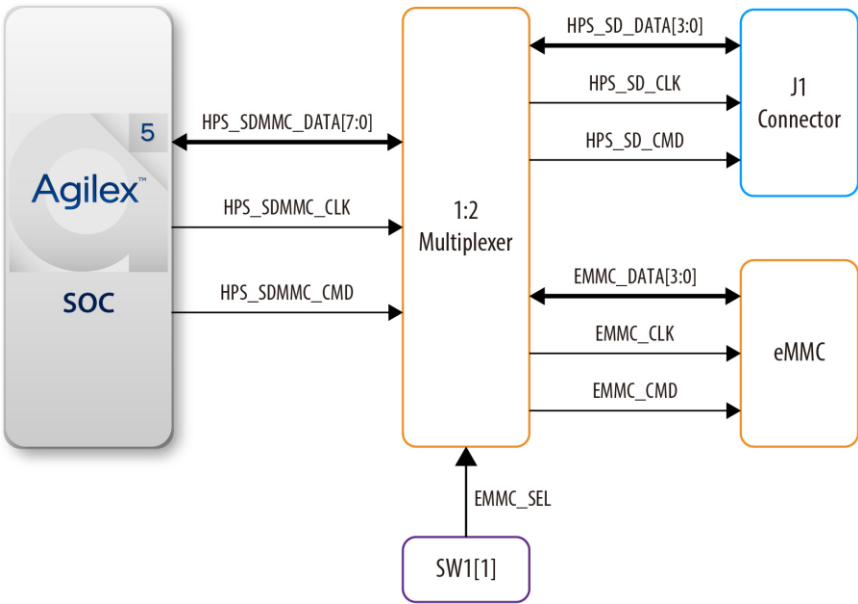


Figure 2-7 Connections between Micro SD card socket, eMMC and Agilex 5 SoC
FPGA

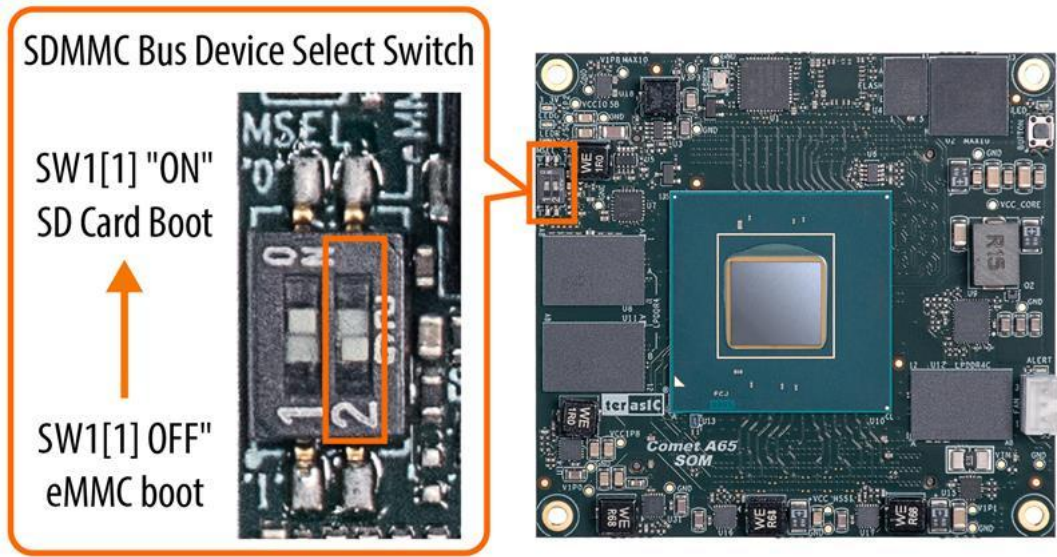


Figure 2-8 SDMMC Bus Device Select Switch

Table 2-9 Micro SD Card Socket Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_SDMMC_CLK	HPS SD/eMMC Clock	1.8-V	PIN_D132
HPS_SDMMC_CMD	HPS SD/eMMC Command Line	1.8-V	PIN_AB132
HPS_SDMMC_DATA[0]	HPS SD/eMMC Data[0]	1.8-V	PIN_E135
HPS_SDMMC_DATA[1]	HPS SD/eMMC Data[1]	1.8-V	PIN_F132
HPS_SDMMC_DATA[2]	HPS SD/eMMC Data[2]	1.8-V	PIN_AA135
HPS_SDMMC_DATA[3]	HPS SD/eMMC Data[3]	1.8-V	PIN_V127

2.6 UART for System MAX10

The UART on J1 connector is connected with the System MAX10. It allows users to monitor the status of the board from the host through the UART interface. As shown in **Figure 2-9**, the Comet A65 SoM provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX10 FPGA on the board. The board management logic (Dashboard) in the system MAX10 FPGA will monitor these status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

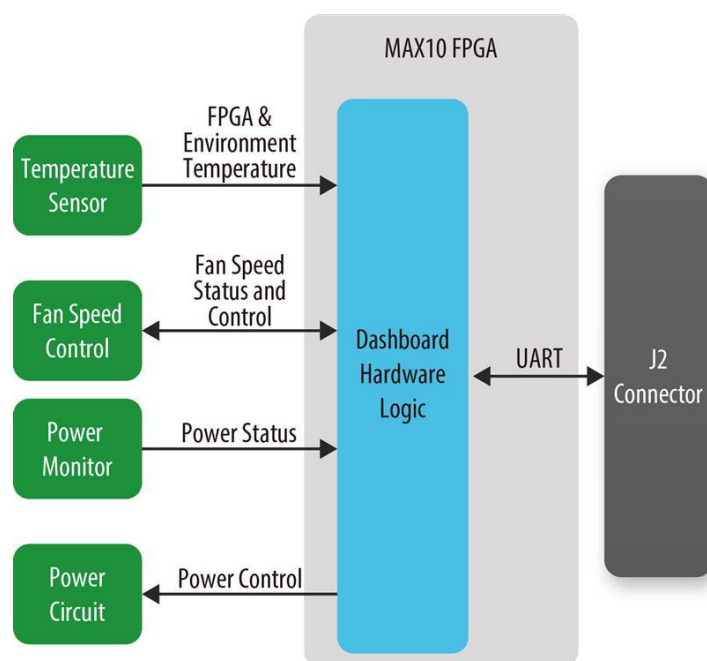


Figure 2-9 Block diagram of the system status interface

Table 2-10 Pin Assignments, Schematic Signal Names, and Functions for UART Interface of the MAX10 FPGA

Schematic Signal Name	Descriptions	I/O Standard	J2 Connector Pin Number
MAX_UART_RX	Receive data input to MAX10 FPGA	1.8-V	G2
MAX_UART_TX	Transmit data output from MAX10 MAX10 FPGA	1.8-V	H2

2.7 LPDDR4 SDRAM

The Comet A65 SOM supports three independent 4GB LPDDR4 SDRAM banks—LPDDR4A, LPDDR4B, and LPDDR4C. Each bank features a 32-bit data bus and accommodate to 4 GB of LPDDR4-2666 memory.

The LPDDR4A bank resides within the I/O bank that interfaces with the Altera Agilex 5 EMIF IP via the Hard Processor System (HPS). If the HPS EMIF is not utilized, the LPDDR4A bank may alternatively be accessed by the FPGA for EMIF implementation.

Figure 2-10 illustrates the interconnections between the LPDDR4 SDRAM banks and the Agilex 5 FPGA.

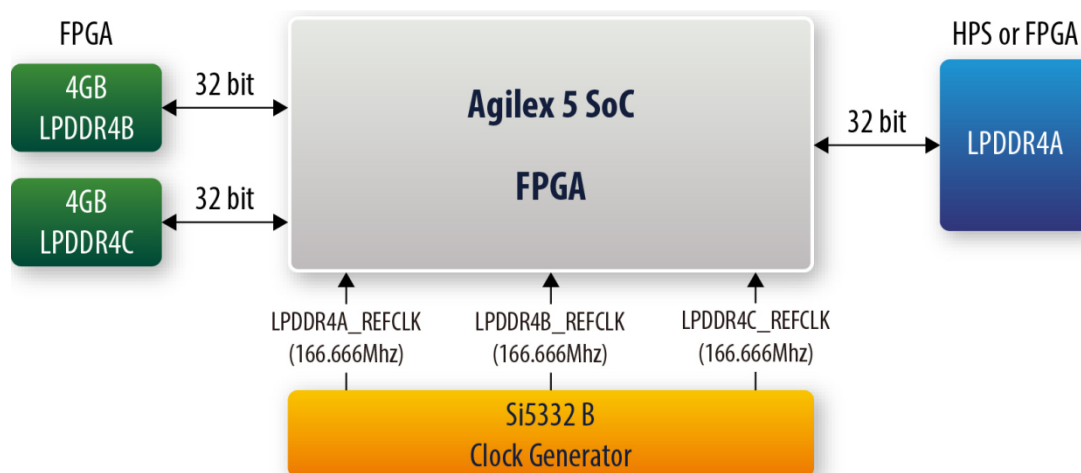


Figure 2-10 Connection between the LPDDR4 and Agilex 5 FPGA

The pin assignments for LPDDR4 SDRAM Bank A,Bank B and Bank C are listed in Table 2-11, Table 2-12 and Table 2-13 respectively.

Table 2-11 LPDDR4A Bank Pin Assignments, Schematic Signal Names, and Functions

Signal Name	FPGA Pin No.	Description	I/O Standard
LPDDR4A_CA[0]	PIN_T114	Command/Address Inputs[0]	1.1-V LVSTL
LPDDR4A_CA[1]	PIN_P114	Command/Address Inputs[1]	1.1-V LVSTL
LPDDR4A_CA[2]	PIN_V117	Command/Address Inputs[2]	1.1-V LVSTL
LPDDR4A_CA[3]	PIN_T117	Command/Address Inputs[3]	1.1-V LVSTL
LPDDR4A_CA[4]	PIN_M114	Command/Address Inputs[4]	1.1-V LVSTL
LPDDR4A_CA[5]	PIN_K114	Command/Address Inputs[5]	1.1-V LVSTL
LPDDR4A_DM[0]	PIN_B119	Data Mask[0]	1.1-V LVSTL
LPDDR4A_DM[1]	PIN_F105	Data Mask[1]	1.1-V LVSTL
LPDDR4A_DM[2]	PIN_B97	Data Mask[2]	1.1-V LVSTL
LPDDR4A_DM[3]	PIN_H87	Data Mask[3]	1.1-V LVSTL
LPDDR4A_CKE	PIN_V108	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4A_CK	PIN_AK107	LPDDR4 Clock p	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_CK_n	PIN_AK104	LPDDR4 Clock	DIFFERENTIAL 1.1-V LVSTL

LPDDR4A_CS_n	PIN_T105	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4A_DQ[0]	PIN_A116	LPDDR4 Data[0]	1.1-V LVSTL
LPDDR4A_DQ[1]	PIN_A128	LPDDR4 Data[1]	1.1-V LVSTL
LPDDR4A_DQ[2]	PIN_B130	LPDDR4 Data[2]	1.1-V LVSTL
LPDDR4A_DQ[3]	PIN_A130	LPDDR4 Data[3]	1.1-V LVSTL
LPDDR4A_DQ[4]	PIN_A113	LPDDR4 Data[4]	1.1-V LVSTL
LPDDR4A_DQ[5]	PIN_B128	LPDDR4 Data[5]	1.1-V LVSTL
LPDDR4A_DQ[6]	PIN_B116	LPDDR4 Data[6]	1.1-V LVSTL
LPDDR4A_DQ[7]	PIN_B113	LPDDR4 Data[7]	1.1-V LVSTL
LPDDR4A_DQ[8]	PIN_K108	LPDDR4 Data[8]	1.1-V LVSTL
LPDDR4A_DQ[9]	PIN_H108	LPDDR4 Data[9]	1.1-V LVSTL
LPDDR4A_DQ[10]	PIN_F117	LPDDR4 Data[10]	1.1-V LVSTL
LPDDR4A_DQ[11]	PIN_K117	LPDDR4 Data[11]	1.1-V LVSTL
LPDDR4A_DQ[12]	PIN_M117	LPDDR4 Data[12]	1.1-V LVSTL
LPDDR4A_DQ[13]	PIN_H117	LPDDR4 Data[13]	1.1-V LVSTL
LPDDR4A_DQ[14]	PIN_M108	LPDDR4 Data[14]	1.1-V LVSTL
LPDDR4A_DQ[15]	PIN_F108	LPDDR4 Data[15]	1.1-V LVSTL
LPDDR4A_DQ[16]	PIN_B106	LPDDR4 Data[16]	1.1-V LVSTL
LPDDR4A_DQ[17]	PIN_A110	LPDDR4 Data[17]	1.1-V LVSTL
LPDDR4A_DQ[18]	PIN_A106	LPDDR4 Data[18]	1.1-V LVSTL
LPDDR4A_DQ[19]	PIN_B103	LPDDR4 Data[19]	1.1-V LVSTL
LPDDR4A_DQ[20]	PIN_A94	LPDDR4 Data[20]	1.1-V LVSTL
LPDDR4A_DQ[21]	PIN_B91	LPDDR4 Data[21]	1.1-V LVSTL
LPDDR4A_DQ[22]	PIN_A91	LPDDR4 Data[22]	1.1-V LVSTL
LPDDR4A_DQ[23]	PIN_B88	LPDDR4 Data[23]	1.1-V LVSTL
LPDDR4A_DQ[24]	PIN_M87	LPDDR4 Data[24]	1.1-V LVSTL
LPDDR4A_DQ[25]	PIN_K87	LPDDR4 Data[25]	1.1-V LVSTL
LPDDR4A_DQ[26]	PIN_D84	LPDDR4 Data[26]	1.1-V LVSTL
LPDDR4A_DQ[27]	PIN_F84	LPDDR4 Data[27]	1.1-V LVSTL
LPDDR4A_DQ[28]	PIN_M98	LPDDR4 Data[28]	1.1-V LVSTL
LPDDR4A_DQ[29]	PIN_K98	LPDDR4 Data[29]	1.1-V LVSTL
LPDDR4A_DQ[30]	PIN_F98	LPDDR4 Data[30]	1.1-V LVSTL
LPDDR4A_DQ[31]	PIN_H98	LPDDR4 Data[31]	1.1-V LVSTL
LPDDR4A_DQS_n[0]	PIN_A125	LPDDR4 Data Strobe n[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS_n[1]	PIN_D114	LPDDR4 Data Strobe n[1]	DIFFERENTIAL 1.1-V LVSTL

LPDDR4A_DQS_n[2]	PIN_B101	LPDDR4 Data Strobe n[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS_n[3]	PIN_D95	LPDDR4 Data Strobe n[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[0]	PIN_B122	LPDDR4 Data Strobe p[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[1]	PIN_F114	LPDDR4 Data Strobe p[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[2]	PIN_A101	LPDDR4 Data Strobe p[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[3]	PIN_F95	LPDDR4 Data Strobe p[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_RESET_N	PIN_AG111	LPDDR4 Reset	1.1-V LVSTL
LPDDR4A_RZQ	PIN_AK111	External reference ball for output drive calibration	1.1V
LPDDR4A_REFCLK_p	PIN_M105	LPDDR4 Reference Clock p	1.1V TRUE DIFFERENTIAL SIGNALING

Table 2-12 LPDDR4B Pin Assignments, Schematic Signal Names, and Functions

Signal Name	FPGA Pin No.	Description	I/O Standard
LPDDR4B_CA[0]	PIN_P74	Command/Address Inputs[0]	1.1-V LVSTL
LPDDR4B_CA[1]	PIN_T74	Command/Address Inputs[1]	1.1-V LVSTL
LPDDR4B_CA[2]	PIN_V77	Command/Address Inputs[2]	1.1-V LVSTL
LPDDR4B_CA[3]	PIN_T77	Command/Address Inputs[3]	1.1-V LVSTL
LPDDR4B_CA[4]	PIN_M74	Command/Address Inputs[4]	1.1-V LVSTL
LPDDR4B_CA[5]	PIN_K74	Command/Address Inputs[5]	1.1-V LVSTL
LPDDR4B_DM[0]	PIN_B73	Data Mask[0]	1.1-V LVSTL
LPDDR4B_DM[1]	PIN_M67	Data Mask[1]	1.1-V LVSTL
LPDDR4B_DM[2]	PIN_B51	Data Mask[2]	1.1-V LVSTL
LPDDR4B_DM[3]	PIN_M47	Data Mask[3]	1.1-V LVSTL
LPDDR4B_CKE	PIN_V67	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4B_CK	PIN_AG83	LPDDR4 Clock p	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_CK_n	PIN_AC83	LPDDR4 Clock	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_CS_n	PIN_M65	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4B_DQ[0]	PIN_A70	LPDDR4 Data[0]	1.1-V LVSTL
LPDDR4B_DQ[1]	PIN_B82	LPDDR4 Data[1]	1.1-V LVSTL
LPDDR4B_DQ[2]	PIN_A82	LPDDR4 Data[2]	1.1-V LVSTL
LPDDR4B_DQ[3]	PIN_A85	LPDDR4 Data[3]	1.1-V LVSTL
LPDDR4B_DQ[4]	PIN_B85	LPDDR4 Data[4]	1.1-V LVSTL
LPDDR4B_DQ[5]	PIN_A66	LPDDR4 Data[5]	1.1-V LVSTL

LPDDR4B_DQ[6]	PIN_B70	LPDDR4 Data[6]	1.1-V LVSTL
LPDDR4B_DQ[7]	PIN_B66	LPDDR4 Data[7]	1.1-V LVSTL
LPDDR4B_DQ[8]	PIN_H67	LPDDR4 Data[8]	1.1-V LVSTL
LPDDR4B_DQ[9]	PIN_F65	LPDDR4 Data[9]	1.1-V LVSTL
LPDDR4B_DQ[10]	PIN_H77	LPDDR4 Data[10]	1.1-V LVSTL
LPDDR4B_DQ[11]	PIN_M77	LPDDR4 Data[11]	1.1-V LVSTL
LPDDR4B_DQ[12]	PIN_K77	LPDDR4 Data[12]	1.1-V LVSTL
LPDDR4B_DQ[13]	PIN_F77	LPDDR4 Data[13]	1.1-V LVSTL
LPDDR4B_DQ[14]	PIN_F67	LPDDR4 Data[14]	1.1-V LVSTL
LPDDR4B_DQ[15]	PIN_D65	LPDDR4 Data[15]	1.1-V LVSTL
LPDDR4B_DQ[16]	PIN_A60	LPDDR4 Data[16]	1.1-V LVSTL
LPDDR4B_DQ[17]	PIN_A63	LPDDR4 Data[17]	1.1-V LVSTL
LPDDR4B_DQ[18]	PIN_B60	LPDDR4 Data[18]	1.1-V LVSTL
LPDDR4B_DQ[19]	PIN_B56	LPDDR4 Data[19]	1.1-V LVSTL
LPDDR4B_DQ[20]	PIN_A48	LPDDR4 Data[20]	1.1-V LVSTL
LPDDR4B_DQ[21]	PIN_A45	LPDDR4 Data[21]	1.1-V LVSTL
LPDDR4B_DQ[22]	PIN_B45	LPDDR4 Data[22]	1.1-V LVSTL
LPDDR4B_DQ[23]	PIN_B42	LPDDR4 Data[23]	1.1-V LVSTL
LPDDR4B_DQ[24]	PIN_H47	LPDDR4 Data[24]	1.1-V LVSTL
LPDDR4B_DQ[25]	PIN_F44	LPDDR4 Data[25]	1.1-V LVSTL
LPDDR4B_DQ[26]	PIN_D44	LPDDR4 Data[26]	1.1-V LVSTL
LPDDR4B_DQ[27]	PIN_F47	LPDDR4 Data[27]	1.1-V LVSTL
LPDDR4B_DQ[28]	PIN_K58	LPDDR4 Data[28]	1.1-V LVSTL
LPDDR4B_DQ[29]	PIN_M58	LPDDR4 Data[29]	1.1-V LVSTL
LPDDR4B_DQ[30]	PIN_F58	LPDDR4 Data[30]	1.1-V LVSTL
LPDDR4B_DQ[31]	PIN_H58	LPDDR4 Data[31]	1.1-V LVSTL
LPDDR4B_DQS_n[0]	PIN_B76	LPDDR4 Data Strobe n[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS_n[1]	PIN_F74	LPDDR4 Data Strobe n[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS_n[2]	PIN_B54	LPDDR4 Data Strobe n[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS_n[3]	PIN_D55	LPDDR4 Data Strobe n[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[0]	PIN_A80	LPDDR4 Data Strobe p[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[1]	PIN_D74	LPDDR4 Data Strobe p[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[2]	PIN_A54	LPDDR4 Data Strobe p[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[3]	PIN_F55	LPDDR4 Data Strobe p[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_RESET_N	PIN_AG79	LPDDR4 Reset	1.1-V LVSTL

LPDDR4B_RZQ	PIN_AC79	External reference ball for output drive calibration	1.1V
LPDDR4B_REFCLK_p	PIN_T65	LPDDR4 Reference Clock p	1.1V TRUE DIFFERENTIAL SIGNALING

Table 2-13 LPDDR4B Pin Assignments, Schematic Signal Names, and Functions

Signal Name	FPGA Pin No.	Description	I/O Standard
LPDDR4C_CA[0]	PIN_CF52	Command/Address Inputs[0]	1.1-V LVSTL
LPDDR4C_CA[1]	PIN_CH52	Command/Address Inputs[1]	1.1-V LVSTL
LPDDR4C_CA[2]	PIN_CC52	Command/Address Inputs[2]	1.1-V LVSTL
LPDDR4C_CA[3]	PIN_CA52	Command/Address Inputs[3]	1.1-V LVSTL
LPDDR4C_CA[4]	PIN_CF49	Command/Address Inputs[4]	1.1-V LVSTL
LPDDR4C_CA[5]	PIN_CH49	Command/Address Inputs[5]	1.1-V LVSTL
LPDDR4C_DM[0]	PIN_CK35	Data Mask[0]	1.1-V LVSTL
LPDDR4C_DM[1]	PIN_CL56	Data Mask[1]	1.1-V LVSTL
LPDDR4C_DM[2]	PIN_CL14	Data Mask[2]	1.1-V LVSTL
LPDDR4C_DM[3]	PIN_CC22	Data Mask[3]	1.1-V LVSTL
LPDDR4C_CKE	PIN_CH41	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4C_CK	PIN_BR41	LPDDR4 Clock p	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_CK_n	PIN_BU41	LPDDR4 Clock	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_CS_n	PIN_CC41	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4C_DQ[0]	PIN_CL30	LPDDR4 Data[0]	1.1-V LVSTL
LPDDR4C_DQ[1]	PIN_CK33	LPDDR4 Data[1]	1.1-V LVSTL
LPDDR4C_DQ[2]	PIN_CL26	LPDDR4 Data[2]	1.1-V LVSTL
LPDDR4C_DQ[3]	PIN_CK30	LPDDR4 Data[3]	1.1-V LVSTL
LPDDR4C_DQ[4]	PIN_CK45	LPDDR4 Data[4]	1.1-V LVSTL
LPDDR4C_DQ[5]	PIN_CK48	LPDDR4 Data[5]	1.1-V LVSTL
LPDDR4C_DQ[6]	PIN_CL45	LPDDR4 Data[6]	1.1-V LVSTL
LPDDR4C_DQ[7]	PIN_CL42	LPDDR4 Data[7]	1.1-V LVSTL
LPDDR4C_DQ[8]	PIN_CK56	LPDDR4 Data[8]	1.1-V LVSTL
LPDDR4C_DQ[9]	PIN_CL54	LPDDR4 Data[9]	1.1-V LVSTL
LPDDR4C_DQ[10]	PIN_CL70	LPDDR4 Data[10]	1.1-V LVSTL
LPDDR4C_DQ[11]	PIN_CL73	LPDDR4 Data[11]	1.1-V LVSTL

LPDDR4C_DQ[12]	PIN_CK66	LPDDR4 Data[12]	1.1-V LVSTL
LPDDR4C_DQ[13]	PIN_CK54	LPDDR4 Data[13]	1.1-V LVSTL
LPDDR4C_DQ[14]	PIN_CL51	LPDDR4 Data[14]	1.1-V LVSTL
LPDDR4C_DQ[15]	PIN_CK73	LPDDR4 Data[15]	1.1-V LVSTL
LPDDR4C_DQ[16]	PIN_CL23	LPDDR4 Data[16]	1.1-V LVSTL
LPDDR4C_DQ[17]	PIN_CL20	LPDDR4 Data[17]	1.1-V LVSTL
LPDDR4C_DQ[18]	PIN_CK26	LPDDR4 Data[18]	1.1-V LVSTL
LPDDR4C_DQ[19]	PIN_CK20	LPDDR4 Data[19]	1.1-V LVSTL
LPDDR4C_DQ[20]	PIN_CL8	LPDDR4 Data[20]	1.1-V LVSTL
LPDDR4C_DQ[21]	PIN_CL6	LPDDR4 Data[21]	1.1-V LVSTL
LPDDR4C_DQ[22]	PIN_CK8	LPDDR4 Data[22]	1.1-V LVSTL
LPDDR4C_DQ[23]	PIN_CK11	LPDDR4 Data[23]	1.1-V LVSTL
LPDDR4C_DQ[24]	PIN_CC31	LPDDR4 Data[24]	1.1-V LVSTL
LPDDR4C_DQ[25]	PIN_CF31	LPDDR4 Data[25]	1.1-V LVSTL
LPDDR4C_DQ[26]	PIN_CF19	LPDDR4 Data[26]	1.1-V LVSTL
LPDDR4C_DQ[27]	PIN_CH31	LPDDR4 Data[27]	1.1-V LVSTL
LPDDR4C_DQ[28]	PIN_CH22	LPDDR4 Data[28]	1.1-V LVSTL
LPDDR4C_DQ[29]	PIN_CF22	LPDDR4 Data[29]	1.1-V LVSTL
LPDDR4C_DQ[30]	PIN_CC19	LPDDR4 Data[30]	1.1-V LVSTL
LPDDR4C_DQ[31]	PIN_CA31	LPDDR4 Data[31]	1.1-V LVSTL
LPDDR4C_DQS_n[0]	PIN_CL39	LPDDR4 Data Strobe n[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_DQS_n[1]	PIN_CL66	LPDDR4 Data Strobe n[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_DQS_n[2]	PIN_CL17	LPDDR4 Data Strobe n[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_DQS_n[3]	PIN_CC28	LPDDR4 Data Strobe n[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_DQS[0]	PIN_CK39	LPDDR4 Data Strobe p[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_DQS[1]	PIN_CK63	LPDDR4 Data Strobe p[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_DQS[2]	PIN_CK17	LPDDR4 Data Strobe p[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_DQS[3]	PIN_CF28	LPDDR4 Data Strobe p[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4C_RESET_N	PIN_BU52	LPDDR4 Reset	1.1-V LVSTL
LPDDR4C_RZQ	PIN_BR52	External reference ball for output drive calibration	1.1V
LPDDR4C_REFCLK_p	PIN_CH38	LPDDR4 Reference Clock p	1.1V TRUE DIFFERENTIAL SIGNALING

2.8 B2B Connector

This section provides an overview of the interfaces connected through these two B2B connectors. As shown in **Figure 2-11**, the Comet A65 SoM includes two B2B connectors (J1 and J2). These connectors serve as the primary interface for connecting the SOM to various peripherals and FPGA I/Os, and also deliver power to the SOM.

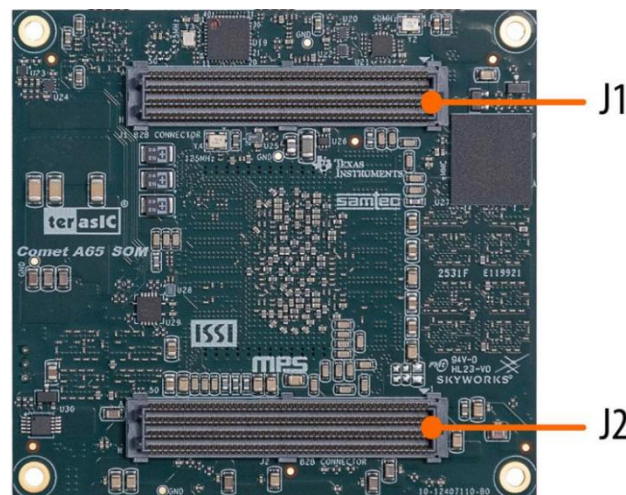


Figure 2-11 B2B connectors on Comet A65 SoM board

Below we will introduce according to the individual functions of B2B J1 connector.

■ B2B J1 connector

Figure 2-12 illustrates the interfaces connected through the J1 connector. For detailed information on net names, pin assignments, and signal descriptions, please refer to the Excel file: [Comet_A65_Pinout_v1.0.xlsx](#) included in the System CD.

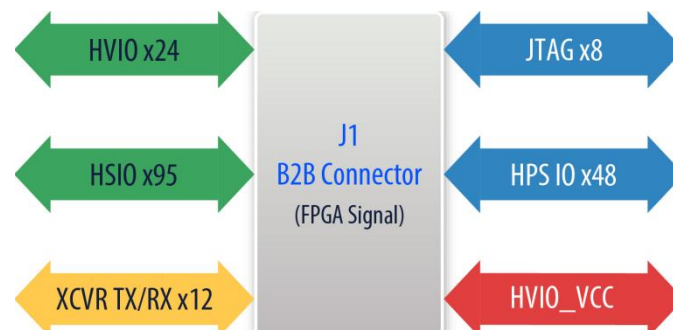


Figure 2-12 Interfaces connected through the J1 connector

The main interfaces connected to J1 are as follows:

- **Power**

- Supplies HVIO_VCC power to the SOM.

- **HPS Interface**

- There are 48 HPS GPIOs connected to the HPS (Hard Processor System) of the Agilex 5 FPGA are routed to the J1 connector and used for connections to carrier board peripherals.

- **User I/O**

- 12 pairs of 12.5 Gbps transceivers
- 2 pairs of transceiver clocks to FPGA
- 95 HSIO
- 24 HVIO

- **RESET**

- SYS_HPS_RST_n
- HPS_COLD_RST_n

- **JTAG**

- SOM JTAG: Connects to the JTAG interface of the Agilex 5 or MAX10 FPGA on the SOM.

- **B2B J2 connector**

The J2 connector primarily provides high-speed transceivers and FPGA I/O directly connected to the Agilex 5 device. **Figure 2-13** illustrates the interfaces connected through the J2 connector.

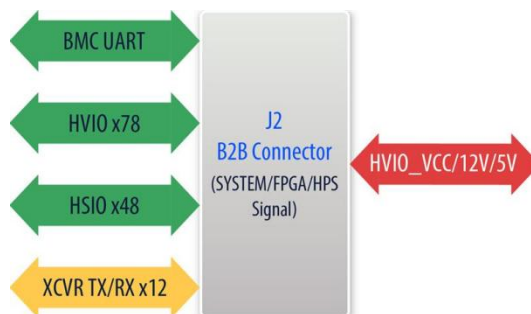


Figure 2-13 Interfaces connected through the J2 connector

For detailed information on net names, pin assignments, and signal descriptions, please refer to the Excel file: [Comet_A65_Pinout_v1.0.xlsx](#) included in the System CD.

The main interfaces connected to J2 are as follows:

- **User I/O**

- 12 pairs of 12.5 Gbps transceivers
- 2 pairs of transceiver clocks to FPGA
- 48 HSIO
- 78 HVIO

- **MAX10 UART**

- UART interface for fan, temperature, and power monitor communication from the MAX10 FPGA

- **Power**

- Supplies HVIO_VCC/12V/5V power to the SOM.

Chapter 3

Additional Information

3.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Comet A65 SoM Web: <https://comet-a65.terasic.com>

■ Revision History

Date	Version	Changes
2025.10	First publication	
2025.11.14	V1.1	Changed the A65 Web link
2025.12.11	V1.2	Major revision based on comprehensive review and proofreading corrections.
2026.05	V2.0	Modify FPGA device number to production version (revC)