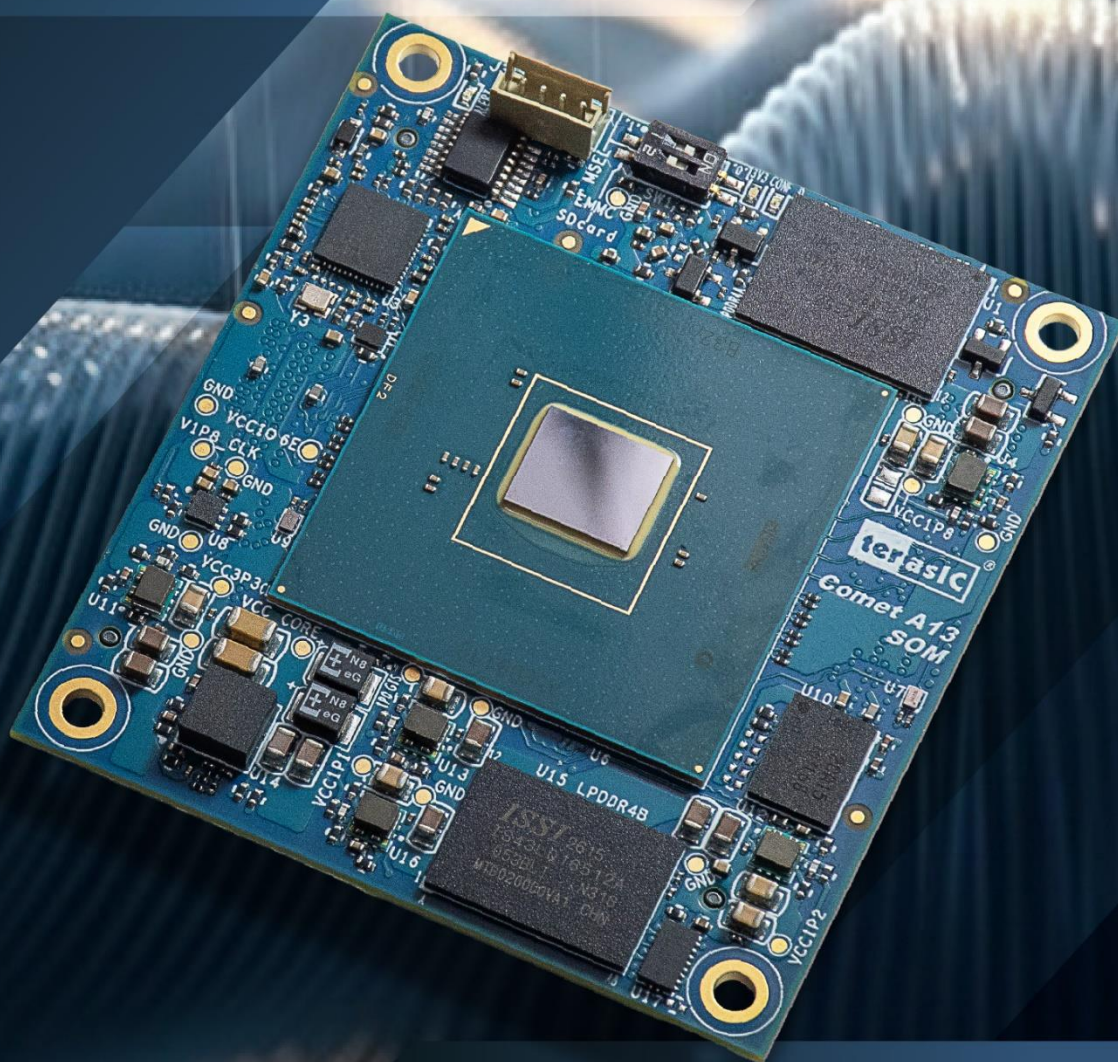


Comet-A13 SOM



User Manual

FPGA

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Chapter 1

Overview

This chapter provides an overview of the Comet A13 SoM Board and installation.

1.1 General Description

The Comet A13 SoM is Terasic's new System-On-Module powered by Altera's Agilex® 5 SoC FPGA with 138K logic elements. The SoM integrates an HPS/ARM subsystem, one 4GB high-throughput LPDDR4 and one 1GB LPDDR4, two high-speed SEAM8 extension connectors, to support 36 LVDS and 4 transceivers. It enables embedded software/systems developers without FPGA expertise to develop various industrial applications, such as medical equipment, robotics, industrial communication and control, machine vision, smart camera and smart city.

Available in production-qualified and certified commercial grade, the Comet A13 SoM is purpose-built for your volume edge deployment and ruggedized for long life cycle operation.

Included with Comet A13 SoM is a free license for Quartus Pro Edition software — no additional license purchase is required. Developers can leverage full design and compilation capabilities of Quartus Pro without incurring licensing fees. Learn more about acquiring your free license.

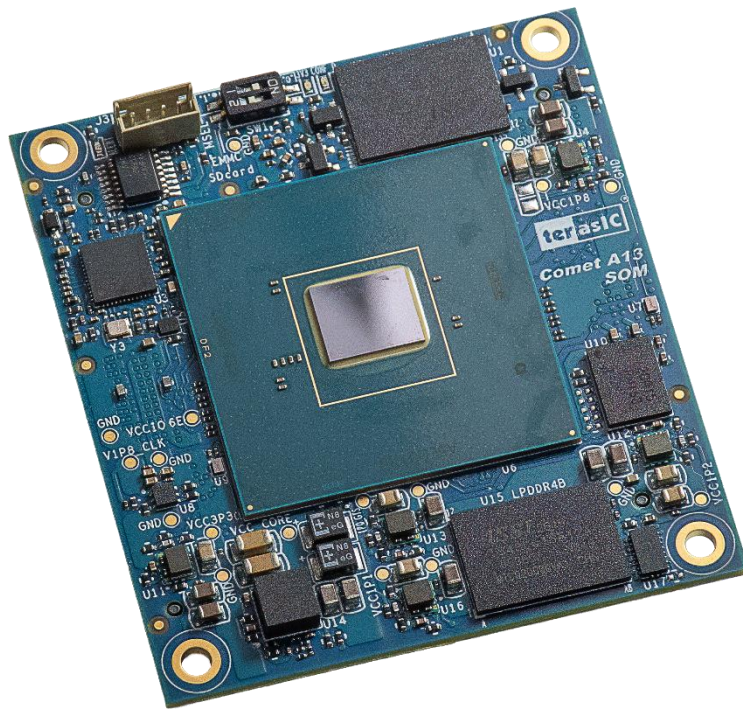


Figure 1-1 Comet A13 SoM Board

1.2 Board Layout

The figures below depict the layout of the board and indicate the location of the connectors and key components.

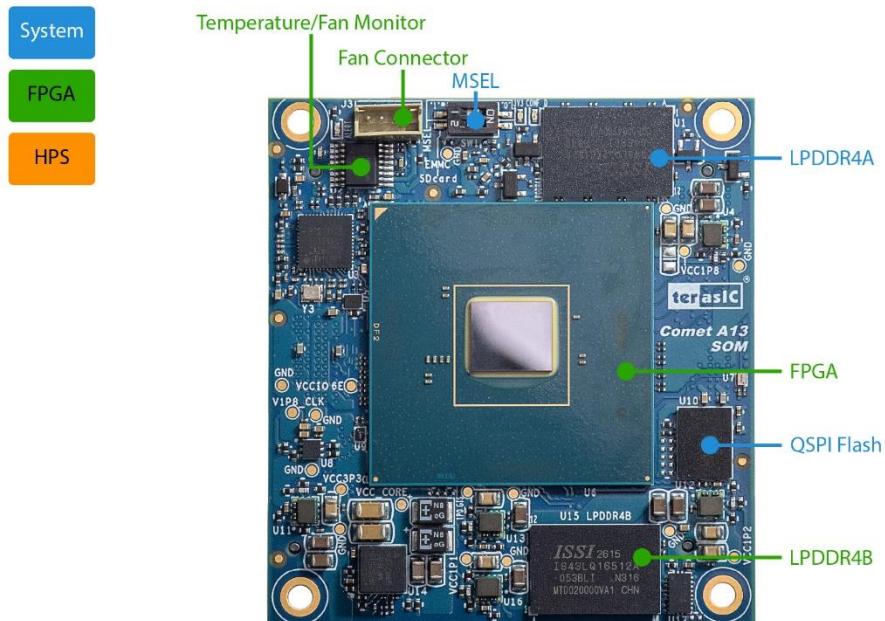


Figure 1-2 Comet A13 SoM module top view

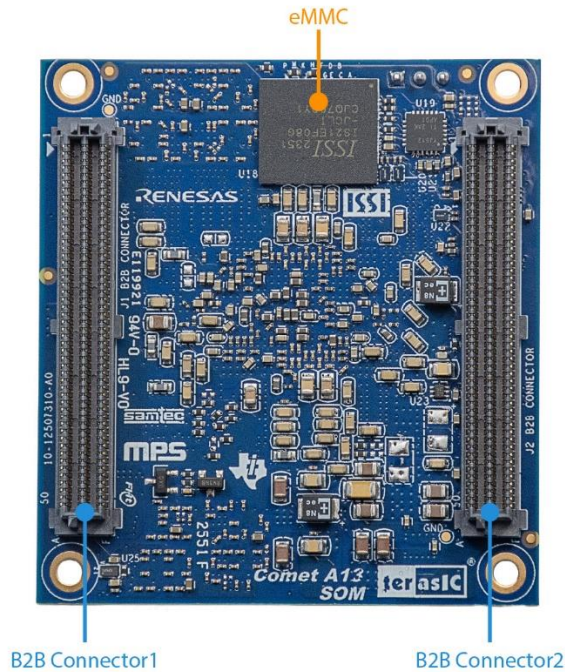


Figure 1-3 Comet A13 SoM module bottom view

1.3 Key Features

The following hardware is implemented on the Comet A13 SoM Board:

■ System

- FPGA: A5ED013BB32AE4SCS (Agilex 5 E-Series Device Group B)
- Module Size: 60mm x 55mm
- 191 HVIO (3.3V x4, 1.2/2.5/3.3V x 98)
- 72 HSIO (up to 12 LVDS RX and 24 LVDS TX/RX)
- 48 HPSIO
- 4 Transceivers
- Interface: Two SEAM8 connectors (6x50 pin)

■ FPGA Side

- Fixed 50/100MHz Clock
- LPDDR4-B: 1GB DDR4 with 16-bit data bus (no ECC)
- 191-pin HVIO and 72-pin HSIO connected to SEAM8 connector
- 4 transceiver and 1 reference clock connected to SEAM8 connectors

■ HPS(Hard Processor System) Side

- LPDDR4-A: 4GB LPDDR4 with 32-bit data bus (no ECC). Shared with FPGA.
- 48 HPS IO connected to SEAM8 connector
- 8GB eMMC (Expandable) + eMMC SEL Switch

1.3. Block Diagram

Figure 1-4 shows the block diagram of the Comet A13 SoM Board. To provide maximum flexibility for the users, all key components are connected to the Agilex 5 SoC FPGA device. Thus, users can configure the FPGA to implement any system design.

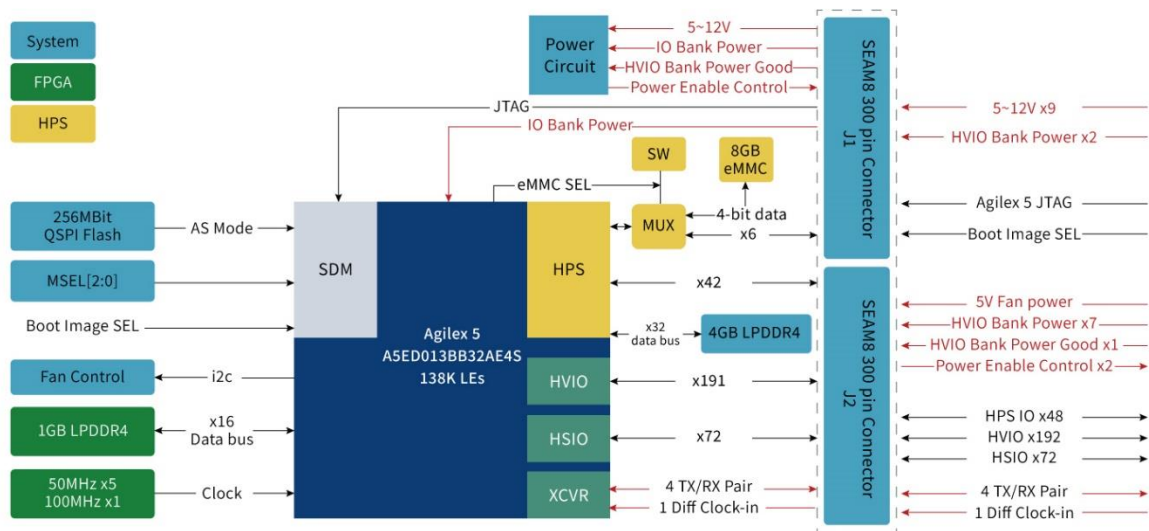


Figure 1-4 Block diagram of the Comet A13 SoM Board

1.4. Mechanical Specifications

Figure 1-5 and **Figure 1-6** shows the mechanical layout of Comet A13 SoM Board. The unit of the mechanical layout is millimeter (mm).

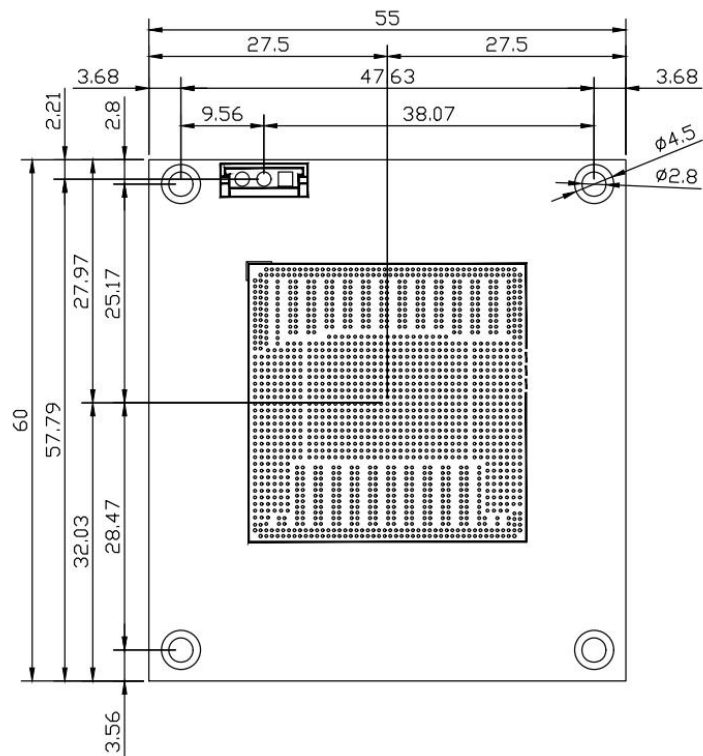


Figure 1-5 Mechanical layout (Top View)

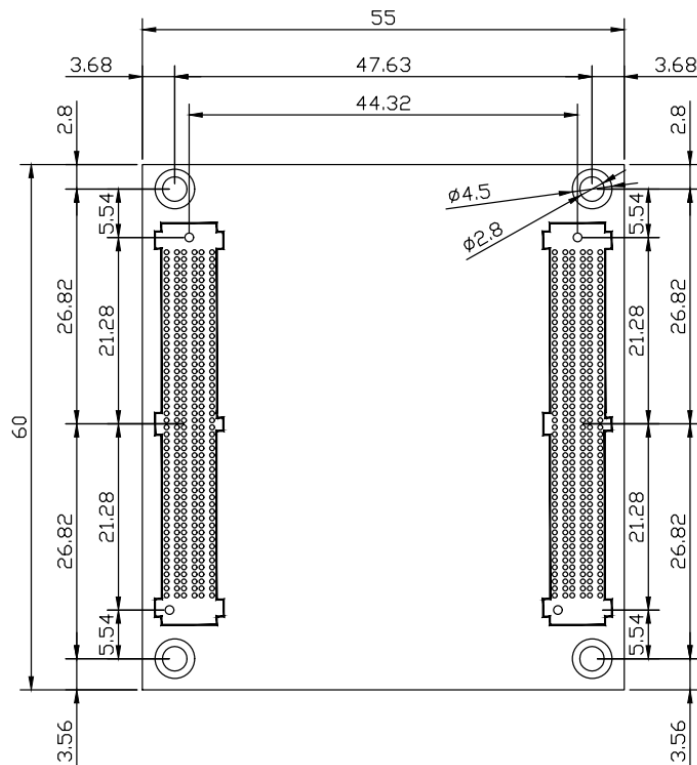


Figure 1-6 Mechanical layout (Bottom view)

1.5. Power Requirement

■ Power Consumption

Table 1-1 presents Comet A13 SoM board power consumption.

Table 1-1 Power Consumption the Comet A13 SoM Board

Status	Power Consumption
Typical	6W
Maximum	8W

■ Power Input for the SOM

The Comet A13 SoM board receives 5V~12V power from the carrier board via the B2B (J1) connector. **Table 1-2** lists the power pins used.

Table 1-2 12V Power pin in B2B Connector

Number	B2B (J1) Pin Number	Comet A13 SoM Board Schematic
1	B48	VIN power pin, support 5V~12V power input
2	B49	
3	B50	
4	D48	
5	D49	
6	D50	
7	F48	
8	F49	
9	F50	

1.6. Connectivity

The Comet A13 SoM Board offers two SEAM8 B2B connectors for expansion. Through the B2B connector, users can interface with the carrier board (see **Figure 1-7**) to access power delivery and multiple expansion interfaces, including USB Blaster programming, communication links, multimedia outputs, and memory peripherals.

If user wants to make their own carrier board to connect with the Comet A13 SoM

board, The following table (**Table 1-3**) lists the manufacturer and part number of the B2B connector that can match with the connector of the Comet A13 SoM Board.

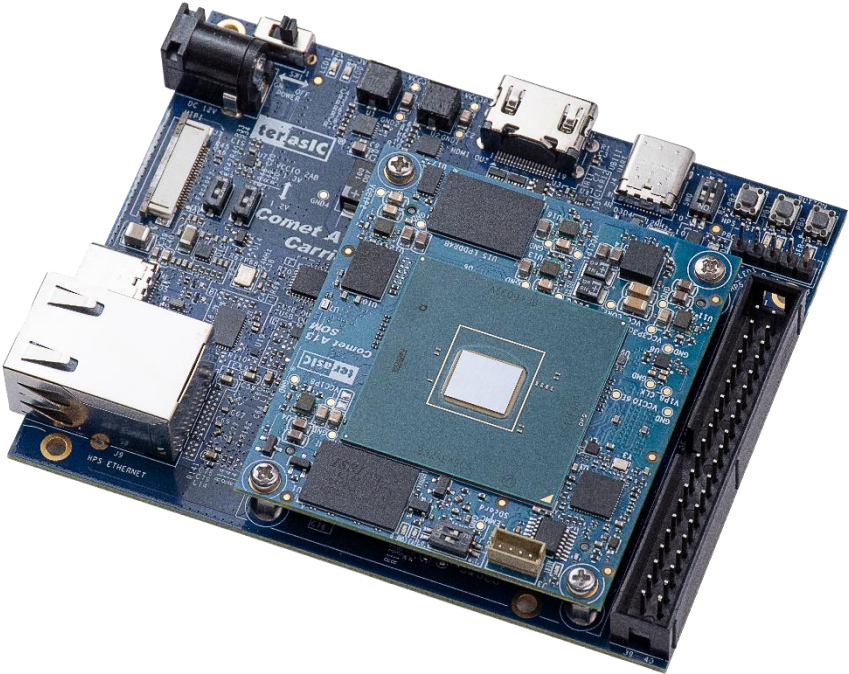


Figure 1-7 Comet A13 SoM module connects to the carrier board

Table 1-3 Part Number of the connector on the Comet A13 SoM module

Connector	Comet A13 SoM Board's Part Number	Carrier Board's Part Number
B2B	Samtec: SEAM8-50-S02.0-S-06-3	Samtec: SEAF8-50-05.0-S-06-3

Chapter 2

Board Component

This chapter introduces all the important components on the Comet A13 SoM.

2.1 Configuration Interface

The FPGA on the Comet A13 SoM board can use two configuration modes: JTAG and Active Serial (AS). Below, we will describe these two modes in detail:

■ **JTAG Programming mode**

JTAG configuration mode is one of the most common methods for programming an FPGA during development. In this mode, a configuration file with the extension .sof (SRAM Object File) is downloaded to the FPGA via a JTAG programming circuit. However, because the .sof file is loaded into the FPGA's volatile SRAM, the configuration is lost when power is turned off. As a result, the FPGA must be reprogrammed each time it is powered on.

Note 1: The Comet A13 SoM board does not include on-board USB Blaster circuit. Users must either provide a USB Blaster circuit or other JTAG programming interface on the carrier board.

■ **Active Serial Fast mode**

The Active Serial Fast (AS fast) mode is a non-volatile configuration scheme for altera FPGAs, utilizing an external Quad SPI (QSPI) Flash memory to store the configuration bitstream. Upon power-up, the FPGA autonomously reads this configuration data from the QSPI Flash, enabling self-contained device initialization. Because the configuration persists across power cycles, the AS fast mode is well-suited for applications demanding reliable, standalone operation without requiring configuration by an external host after initial programming.

Figure 2-1 and **Table 2-1** shows the configuration switch settings.

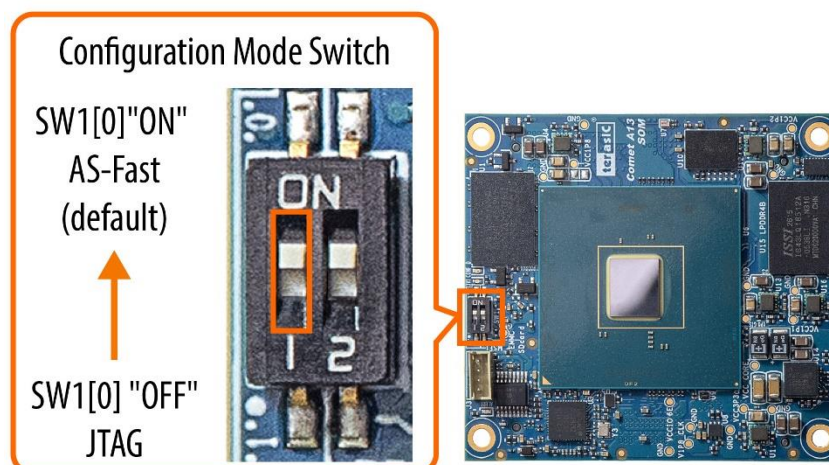


Figure 2-1 Position of slide switches SW1

Table 2-1 SW1 setting

Board Reference	Signal Name	Description	Default
SW1[0]	MSEL[2] and MSEL[1]	0: AS-Fast(Default Setting)	0
		1: Jtag	

Note: The A13 SoM module supports dual image (Factory and Application image) booting, users should set Image_Factory signal on the B2B connector J1 as High or floating to use the factory image booting, and set Image_Factory as low to use the application image booting. If users do not want to support dual-boot, then Image_Factory should be tied High or left floating.

The following content will introduce the HPS boot process within the SoC FPGA.

■ SoC FPGA boot

The boot process for Agilex 5 SoC FPGAs can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and FPGA fabric after powering on. More details can be found in the user documentation: www.terasic.com [Hard Processor System Booting User Guide: Agilex 5 SoCs](#).

Figure 2-2 shows the JTAG interface and configuration device of the Comet A13 SoM Board.

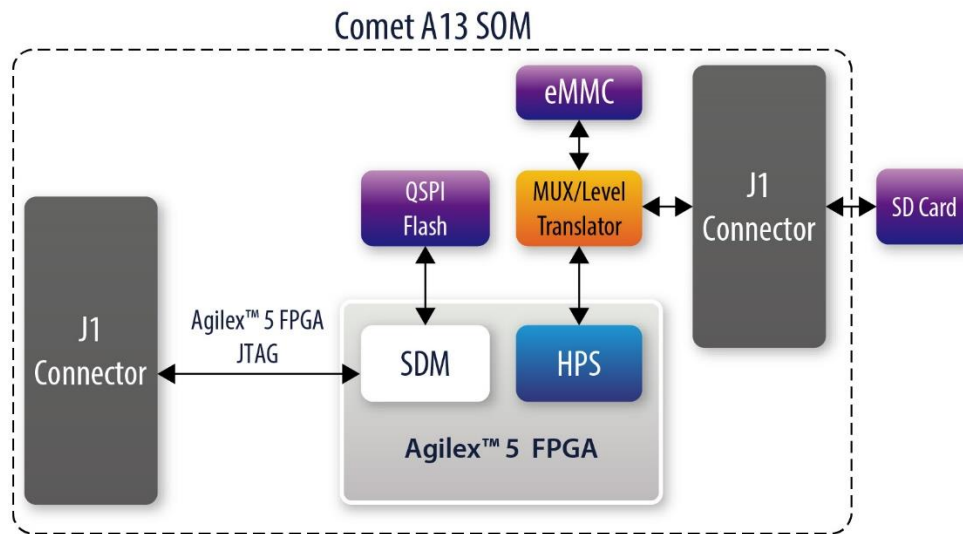


Figure 2-2 Block diagram of the JTAG interface and configuration for the board

The factory setting of the SoC boot of the Comet A13 SoM Board is the **FPGA Boot First Mode**. The architecture is shown in the **Figure 2-3**. Two storage mediums are used. The system needs QSPI flash on Comet A13 SoM as SDM flash for booting.

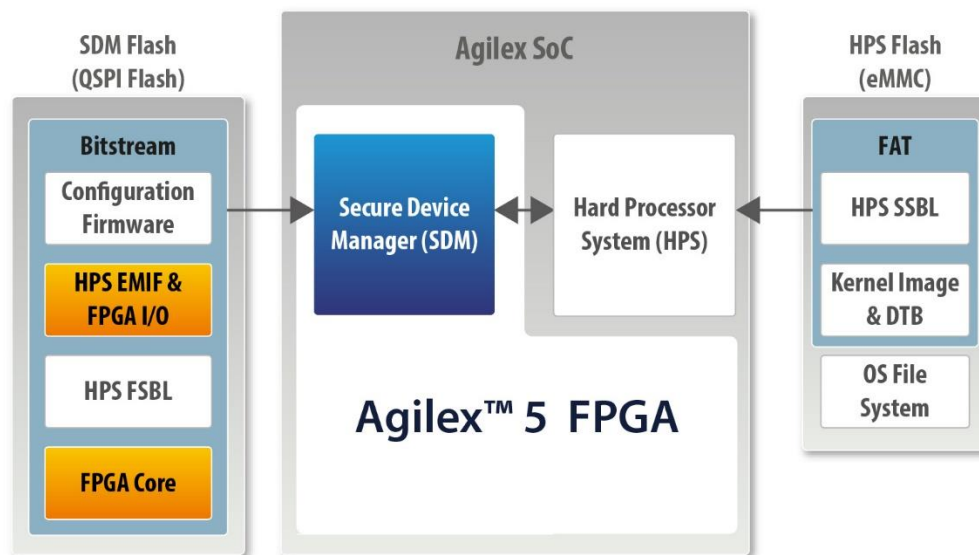


Figure 2-3 FPGA boot First Dual Flash (SDM and HPS)

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the eMMC flash with built-in image data as HPS flash, which is used for HPS boot in the later part. The eMMC flash stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Comet A13 SoM is summarized as follows:

When the Comet A13 SoM Board is powered on, the SDM will read the configuration firmware and complete SDM initial from the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the eMMC flash into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

2.2 Setup and Status Components

This section will introduce the use of the switch for setup on the Comet A13 SoM board, as well as a description of the various status LEDs.

■ Status LED

The FPGA development board includes board-specific status LEDs to indicate board

status. Please refer to **Table 2-2** for the description of the LED indicators. **Figure 2-4** shows the location of all these status LEDs.

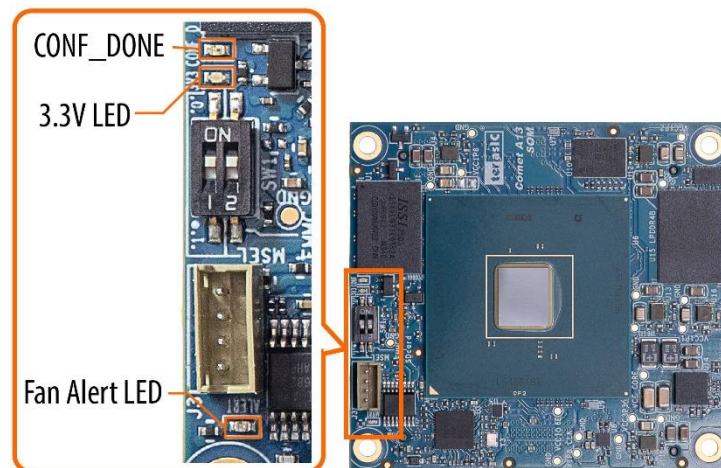


Figure 2-4 Position of the status LED

Table 2-2 Status LED

Board Reference	LED Name	Description
D1	FPGA Power Good	Illuminates when all FPGA power are active
D2	ALERT	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
LED1	CONF_DONE	Illuminates when FPGA configuration is complete and successful

2.3 Clock Circuit

Figure 2-5 shows the clock tree of the Comet A13 SoM board.

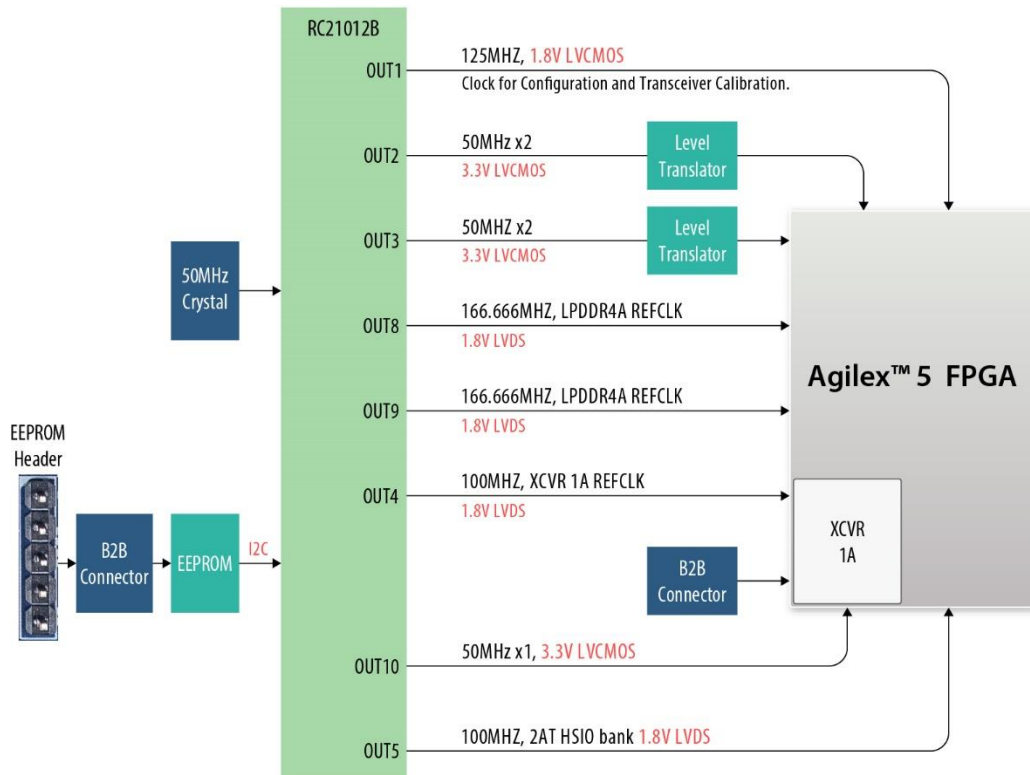


Figure 2-5 Clock tree of the Comet A13 SoM

The clock source on the Comet A13 SoM is generated by a programmable PLL clock generator RC21012B. It primarily provides 100MHz reference clock for the FPGA transceivers and 166.666MHz clock for the two LPDDR4 memory interfaces. It also delivers 50MHz reference clocks to the FPGA core. It outputs 125MHz as the reference clock for FPGA configuration and transceiver calibration.

User can provide an additional transceiver reference clock from the carrier board to the Comet A13 SoM via B2B connector J1. User should route the desired clock to J1_GTSL1A_REFCLK. If the on-board 100MHz GTSL1A_REFCLK_100M reference clock on the SoM meets the user's transceiver application requirements and the carrier board does not need to provide an additional reference clock to J1_GTSL1A_REFCLK, then J1_GTSL1A_REFCLK must be tied to ground. In addition, for any unused transceiver channels, the corresponding GTSL1A_RX_px/ GTSL1A_RX_nx pins must also be tied to ground.

Note: The EEPROM on A13 SoM is used for configuring the clock generator. The EEPROM_I2C_SDA, EEPROM_I2C_SCL and EEPROM_WC_N signals should be routed to a 1×5 programming header on the carrier board for EEPROM programming:

Table 2-3 list the clock pin assignments and default frequency for the RC21012B.

Table 2-3 Clock Pin Assignments of the RC21012B

Clock Output Port	Schematic Signal Name	Default Frequency	I/O Standard	FPGA Pin	Application
OUT1	OSC_CLK_1	125MHz	1.8V LVCMOS	PIN_BR102	Clock for Configuration and Transceiver Calibration
OUT2	CLK_50_5A	50MHz	3.3V LVCMOS	PIN_CH128	Reference clock for FPGA
OUT2b	CLK_50_6A	50MHz	3.3V LVCMOS	PIN_BK31	Reference clock for FPGA
OUT3	CLK_50_6H	50MHz	3.3V LVCMOS	PIN_V27	Reference clock for FPGA
OUT3b	CLK_50_6C	50MHz	3.3V LVCMOS	PIN_D8	Reference clock for FPGA
OUT8	LPDDR4A_REFCLK_p	166.666MHz	1.8V LVDS	PIN_M105	LPDDR4A reference clock
OUT8b	LPDDR4A_REFCLK_n	166.666MHz	1.8V LVDS	PIN_K105	LPDDR4A reference clock
OUT9	LPDDR4B_REFCLK_p	166.666MHz	1.8V LVDS	PIN_BF75	LPDDR4B reference clock
OUT9b	LPDDR4B_REFCLK_n	166.666MHz	1.8V LVDS	PIN_BF72	LPDDR4B reference clock
OUT4	GTSL1A_REFCLK_100M_p	100MHz	1.8V LVDS	PIN_AP120	Reference clock for FPGA transceiver bank 1A
OUT4b	GTSL1A_REFCLK_100M_n	100MHz	1.8V LVDS	PIN_AP115	Reference clock for FPGA transceiver bank 1A
OUT10	CLK_50_6F	50MHz	3.3V LVCMOS	PIN_Y4	Reference clock for FPGA
OUT5	CLK_2AT_100M_p	100MHz	1.8V LVDS	PIN_BM71	Reference clock for FPGA HSIO

					bank 2AT
OUT5b	CLK_2AT_100M_n	100MHz	1.8V LVDS	PIN_BP71	Reference clock for FPGA HSIO bank 2AT

2.4 Micro SD Card and eMMC

The SoM provides on-board 8GB eMMC device (IS21EF08G-JCLI) and Micro SD Card (which is on the Carrier board and using B2B connector to access) for HPS fabric in the FPGA (See Figure 2-6). Users can choose one of them for HPS boot/data/system storage. The switch SW1.2(See Figure 2-7 SW1[1]) on the board can help the user select which device (Micro SD Card on J1 or eMMC) will be used for HPS fabric. The Micro SD card socket can provide flexible capacity expansion while eMMC device can support stable and fixed storage solutions. Table 2-4 lists the pin assignment of Micro SD card socket and eMMC device to the HPS.

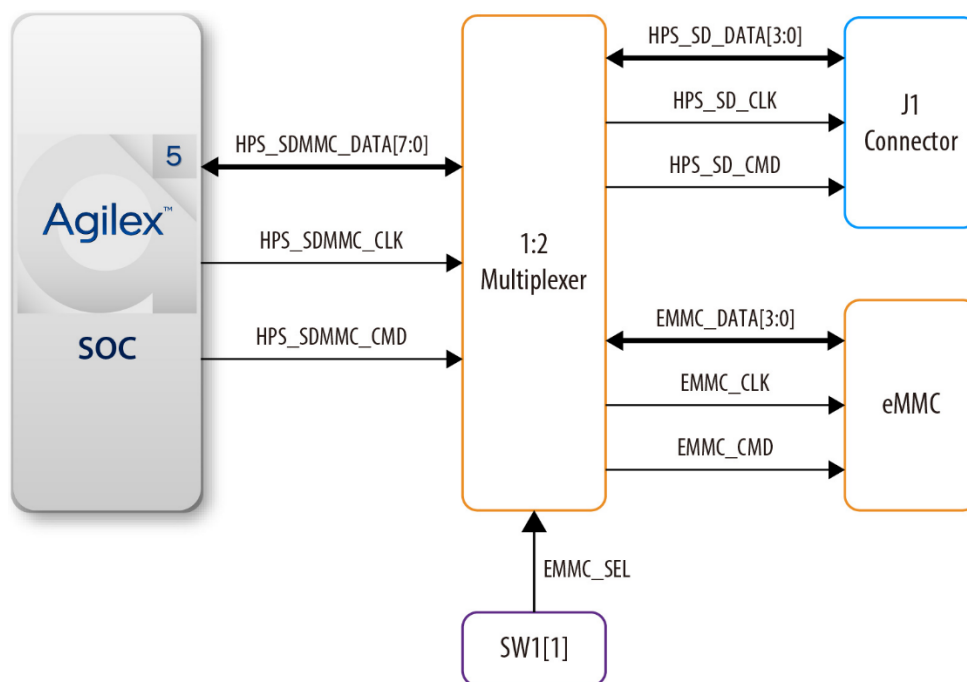


Figure 2-6 Connections between J1, eMMC and Agilinx 5 SoC FPGA

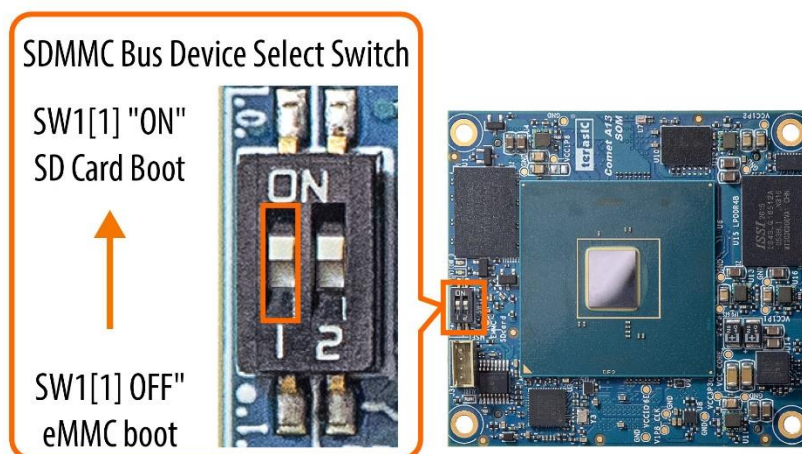


Figure 2-7 SDMMC Bus Device Select Switch

Table 2-4 Micro SD Card Socket Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_SDMMC_CLK	HPS SD/eMMC Clock	1.8-V	PIN_D132
HPS_SDMMC_CMD	HPS SD/eMMC Command Line	1.8-V	PIN_AB132
HPS_SDMMC_DATA[0]	HPS SD/eMMC Data[0]	1.8-V	PIN_E135
HPS_SDMMC_DATA[1]	HPS SD/eMMC Data[1]	1.8-V	PIN_F132
HPS_SDMMC_DATA[2]	HPS SD/eMMC Data[2]	1.8-V	PIN_AA135
HPS_SDMMC_DATA[3]	HPS SD/eMMC Data[3]	1.8-V	PIN_V127

2.5 LPDDR4 SDRAM

The Comet A13 SOM supports two independent LPDDR4 SDRAM banks—LPDDR4A and LPDDR4B. LPDDR4B is a 16-bit data bus and accommodate to 1GB. The LPDDR4A is a 32-bit data bus and accommodate to 4GB, it resides within the I/O bank that interfaces with the Agilex 5 EMIF IP via the Hard Processor System (HPS). If the HPS EMIF is not utilized, the LPDDR4A bank may alternatively be accessed by the FPGA for EMIF implementation.

Note: Clock CLK_2AT_100M_p (CLK_100_B2A_p) is located in the same I/O bank (Bank 2AT) used by LPDDR4B. When LPDDR4B is enabled, this bank is reserved by the EMIF, so this clock must not be declared as a top-level input, even if it is not used. Otherwise, it will cause fitter placement errors.

Solution: When LPDDR4B is enabled, do not declare CLK_100_B2A_p. When LPDDR4B is disabled, this clock can be declared for user designs.

Figure 2-8 illustrates the interconnections between the LPDDR4 SDRAM banks and the Agilex 5 FPGA.

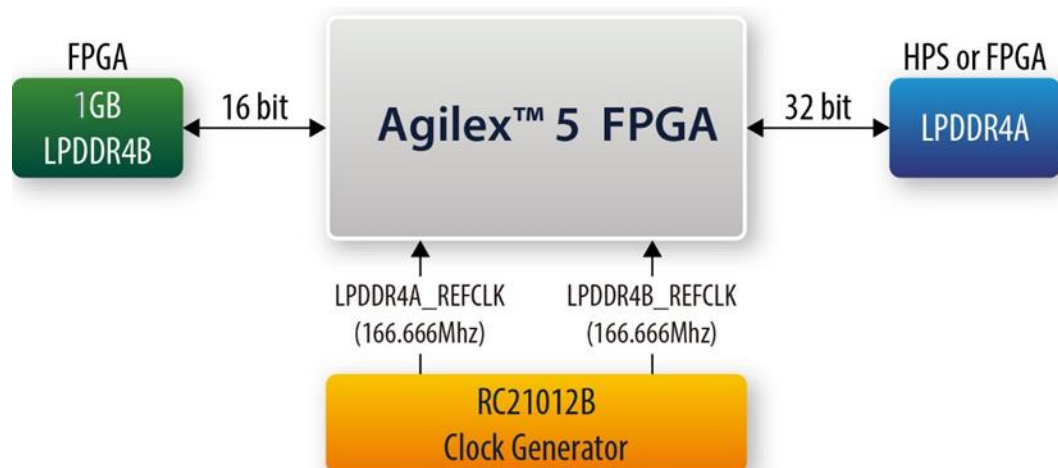


Figure 2-8 Connection between the LPDDR4 and Agilex 5 FPGA

The pin assignments for LPDDR4 SDRAM Bank A and B are listed in **Table 2-5** and **Table 2-6** respectively.

Table 2-5 LPDDR4A Bank Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin No.	Description	I/O Standard
LPDDR4A_CA[0]	PIN_T114	Command/Address Inputs[0]	1.1-V LVSTL
LPDDR4A_CA[1]	PIN_P114	Command/Address Inputs[1]	1.1-V LVSTL
LPDDR4A_CA[2]	PIN_V117	Command/Address Inputs[2]	1.1-V LVSTL
LPDDR4A_CA[3]	PIN_T117	Command/Address Inputs[3]	1.1-V LVSTL
LPDDR4A_CA[4]	PIN_M114	Command/Address Inputs[4]	1.1-V LVSTL
LPDDR4A_CA[5]	PIN_K114	Command/Address Inputs[5]	1.1-V LVSTL
LPDDR4A_DM[0]	PIN_B119	Data Mask[0]	1.1-V LVSTL
LPDDR4A_DM[1]	PIN_F105	Data Mask[1]	1.1-V LVSTL
LPDDR4A_DM[2]	PIN_B97	Data Mask[2]	1.1-V LVSTL
LPDDR4A_DM[3]	PIN_H87	Data Mask[3]	1.1-V LVSTL
LPDDR4A_CKE[0]	PIN_V108	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4A_CKE[1]	PIN_T108	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4A_CK	PIN_AK107	LPDDR4 Clock p	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_CK_n	PIN_AK104	LPDDR4 Clock	DIFFERENTIAL 1.1-V LVSTL

LPDDR4A_CS_n[0]	PIN_T105	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4A_CS_n[1]	PIN_P105	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4A_DQ[0]	PIN_A128	LPDDR4 Data[0]	1.1-V LVSTL
LPDDR4A_DQ[1]	PIN_A130	LPDDR4 Data[1]	1.1-V LVSTL
LPDDR4A_DQ[2]	PIN_A116	LPDDR4 Data[2]	1.1-V LVSTL
LPDDR4A_DQ[3]	PIN_A113	LPDDR4 Data[3]	1.1-V LVSTL
LPDDR4A_DQ[4]	PIN_B113	LPDDR4 Data[4]	1.1-V LVSTL
LPDDR4A_DQ[5]	PIN_B116	LPDDR4 Data[5]	1.1-V LVSTL
LPDDR4A_DQ[6]	PIN_B130	LPDDR4 Data[6]	1.1-V LVSTL
LPDDR4A_DQ[7]	PIN_B128	LPDDR4 Data[7]	1.1-V LVSTL
LPDDR4A_DQ[8]	PIN_K117	LPDDR4 Data[8]	1.1-V LVSTL
LPDDR4A_DQ[9]	PIN_H117	LPDDR4 Data[9]	1.1-V LVSTL
LPDDR4A_DQ[10]	PIN_M108	LPDDR4 Data[10]	1.1-V LVSTL
LPDDR4A_DQ[11]	PIN_F117	LPDDR4 Data[11]	1.1-V LVSTL
LPDDR4A_DQ[12]	PIN_F108	LPDDR4 Data[12]	1.1-V LVSTL
LPDDR4A_DQ[13]	PIN_H108	LPDDR4 Data[13]	1.1-V LVSTL
LPDDR4A_DQ[14]	PIN_K108	LPDDR4 Data[14]	1.1-V LVSTL
LPDDR4A_DQ[15]	PIN_M117	LPDDR4 Data[15]	1.1-V LVSTL
LPDDR4A_DQ[16]	PIN_B88	LPDDR4 Data[16]	1.1-V LVSTL
LPDDR4A_DQ[17]	PIN_A91	LPDDR4 Data[17]	1.1-V LVSTL
LPDDR4A_DQ[18]	PIN_B106	LPDDR4 Data[18]	1.1-V LVSTL
LPDDR4A_DQ[19]	PIN_A110	LPDDR4 Data[19]	1.1-V LVSTL
LPDDR4A_DQ[20]	PIN_A106	LPDDR4 Data[20]	1.1-V LVSTL
LPDDR4A_DQ[21]	PIN_B103	LPDDR4 Data[21]	1.1-V LVSTL
LPDDR4A_DQ[22]	PIN_A94	LPDDR4 Data[22]	1.1-V LVSTL
LPDDR4A_DQ[23]	PIN_B91	LPDDR4 Data[23]	1.1-V LVSTL
LPDDR4A_DQ[24]	PIN_M87	LPDDR4 Data[24]	1.1-V LVSTL
LPDDR4A_DQ[25]	PIN_K87	LPDDR4 Data[25]	1.1-V LVSTL
LPDDR4A_DQ[26]	PIN_K98	LPDDR4 Data[26]	1.1-V LVSTL
LPDDR4A_DQ[27]	PIN_H98	LPDDR4 Data[27]	1.1-V LVSTL
LPDDR4A_DQ[28]	PIN_F98	LPDDR4 Data[28]	1.1-V LVSTL
LPDDR4A_DQ[29]	PIN_M98	LPDDR4 Data[29]	1.1-V LVSTL
LPDDR4A_DQ[30]	PIN_D84	LPDDR4 Data[30]	1.1-V LVSTL
LPDDR4A_DQ[31]	PIN_F84	LPDDR4 Data[31]	1.1-V LVSTL
LPDDR4A_DQS_n[0]	PIN_A125	LPDDR4 Data Strobe n[0]	DIFFERENTIAL 1.1-V LVSTL

LPDDR4A_DQS_n[1]	PIN_D114	LPDDR4 Data Strobe n[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS_n[2]	PIN_B101	LPDDR4 Data Strobe n[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS_n[3]	PIN_D95	LPDDR4 Data Strobe n[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[0]	PIN_B122	LPDDR4 Data Strobe p[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[1]	PIN_F114	LPDDR4 Data Strobe p[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[2]	PIN_A101	LPDDR4 Data Strobe p[2]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_DQS[3]	PIN_F95	LPDDR4 Data Strobe p[3]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4A_RESET_N	PIN_AG111	LPDDR4 Reset	1.1-V LVSTL
LPDDR4A_RZQ	PIN_AK111	External reference ball for output drive calibration	1.1V
LPDDR4A_REFCLK_p	PIN_M105	LPDDR4 Reference Clock p	1.1-V TRUE DIFFERENTIAL SIGNALING

Table 2-6 LPDDR4B Pin Assignments, Schematic Signal Names, and Functions

Signal Name	FPGA Pin No.	Description	I/O Standard
LPDDR4B_CA[0]	PIN_BE96	Command/Address Inputs[0]	1.1-V LVSTL
LPDDR4B_CA[1]	PIN_BE93	Command/Address Inputs[1]	1.1-V LVSTL
LPDDR4B_CA[2]	PIN_BF93	Command/Address Inputs[2]	1.1-V LVSTL
LPDDR4B_CA[3]	PIN_BF90	Command/Address Inputs[3]	1.1-V LVSTL
LPDDR4B_CA[4]	PIN_BF86	Command/Address Inputs[4]	1.1-V LVSTL
LPDDR4B_CA[5]	PIN_BE86	Command/Address Inputs[5]	1.1-V LVSTL
LPDDR4B_DM[0]	PIN_BU62	Data Mask[0]	1.1-V LVSTL
LPDDR4B_DM[1]	PIN_CA62	Data Mask[1]	1.1-V LVSTL
LPDDR4B_CKE	PIN_BE83	LPDDR4 Clock Enable	1.1-V LVSTL
LPDDR4B_CK	PIN_BM62	LPDDR4 Clock p	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_CK_n	PIN_BP62	LPDDR4 Clock	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_CS_n	PIN_BE79	LPDDR4 Chip Select	1.1-V LVSTL
LPDDR4B_DQ[0]	PIN_BW59	LPDDR4 Data[0]	1.1-V LVSTL
LPDDR4B_DQ[1]	PIN_BU59	LPDDR4 Data[1]	1.1-V LVSTL
LPDDR4B_DQ[2]	PIN_CA59	LPDDR4 Data[2]	1.1-V LVSTL
LPDDR4B_DQ[3]	PIN_BR69	LPDDR4 Data[3]	1.1-V LVSTL
LPDDR4B_DQ[4]	PIN_BR71	LPDDR4 Data[4]	1.1-V LVSTL
LPDDR4B_DQ[5]	PIN_BU71	LPDDR4 Data[5]	1.1-V LVSTL
LPDDR4B_DQ[6]	PIN_BU69	LPDDR4 Data[6]	1.1-V LVSTL
LPDDR4B_DQ[7]	PIN_BR59	LPDDR4 Data[7]	1.1-V LVSTL

LPDDR4B_DQ[8]	PIN_CH62	LPDDR4 Data[8]	1.1-V LVSTL
LPDDR4B_DQ[9]	PIN_CF62	LPDDR4 Data[9]	1.1-V LVSTL
LPDDR4B_DQ[10]	PIN_CH71	LPDDR4 Data[10]	1.1-V LVSTL
LPDDR4B_DQ[11]	PIN_CF71	LPDDR4 Data[11]	1.1-V LVSTL
LPDDR4B_DQ[12]	PIN_CA71	LPDDR4 Data[12]	1.1-V LVSTL
LPDDR4B_DQ[13]	PIN_CC71	LPDDR4 Data[13]	1.1-V LVSTL
LPDDR4B_DQ[14]	PIN_CF59	LPDDR4 Data[14]	1.1-V LVSTL
LPDDR4B_DQ[15]	PIN_CH59	LPDDR4 Data[15]	1.1-V LVSTL
LPDDR4B_DQS_n[0]	PIN_CA69	LPDDR4 Data Strobe n[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS_n[1]	PIN_CF69	LPDDR4 Data Strobe n[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[0]	PIN_BW69	LPDDR4 Data Strobe p[0]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_DQS[1]	PIN_CH69	LPDDR4 Data Strobe p[1]	DIFFERENTIAL 1.1-V LVSTL
LPDDR4B_RESET_N	PIN_BH71	LPDDR4 Reset	1.1-V LVSTL
LPDDR4B_RZQ	PIN_BH69	External reference ball for output drive calibration	1.1V
LPDDR4B_REFCLK_p	PIN_BF75	LPDDR4 Reference Clock p	1.1V TRUE DIFFERENTIAL SIGNALING

2.6 B2B Connector

This section provides an overview of the interfaces connected through these two B2B connectors. As shown in **Figure 2-9**, the Comet A13 SoM includes two B2B connectors (J1 and J2). These connectors serve as the primary interface for connecting the SOM to various peripherals and FPGA I/Os, and deliver power to the SOM.

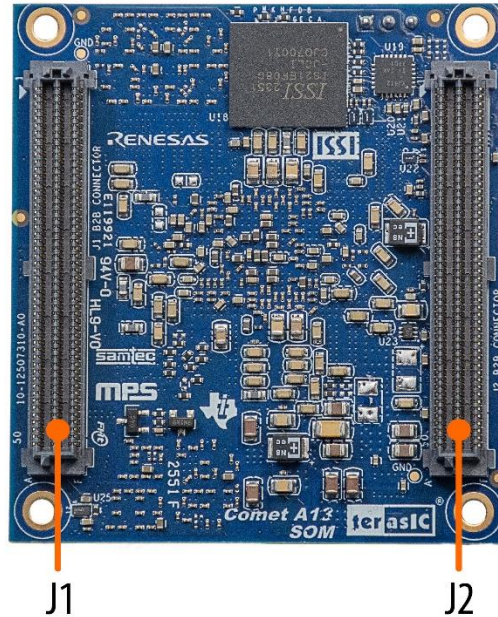


Figure 2-9 B2B connectors on Comet A13 SoM board

Below we will introduce according to the individual functions of B2B J1 connector.

■ B2B J1 connector

Figure 2-10 illustrates the interfaces connected through the J1 connector. primarily provides high-speed transceivers, FPGA and HPS I/O directly connected to the Agilex 5 device. For detailed information on net names, pin assignments, and signal descriptions, please refer to the Excel file: *Comet_A13_Pinout_v1.0.xlsx* included in the System CD.

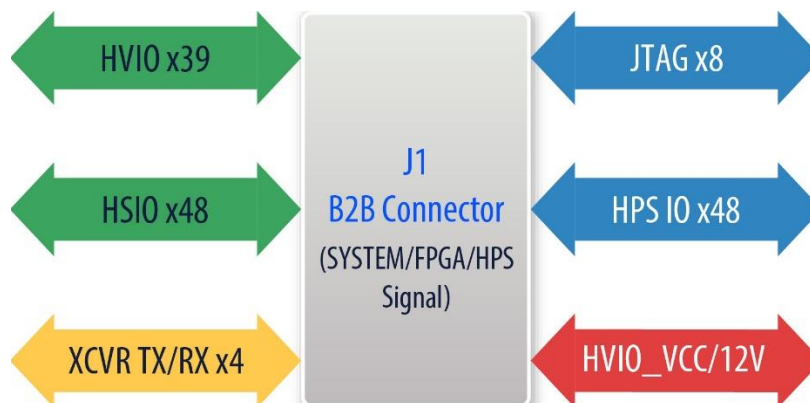


Figure 2-10 Interfaces connected through the J1 connector

The main interfaces connected to J1 are as follows:

- **Power**

- Supplies VIN 5~12V power to the SOM.

- **HPS Interface**

- There are 48 HPS GPIOs connected to the HPS (Hard Processor System) of the Agilex 5 FPGA are routed to the J1 connector and used for connections to carrier board peripherals.

- **User I/O**

- 4 pairs of 17.16Gbps transceivers
- 1 pair of transceiver clocks to FPGA
- 39 HSIO
- 48 HVIO

- **RESET**

- SYS_HPS_RST_n

- **JTAG**

- SOM JTAG: Connects to the JTAG interface of the Agilex 5 FPGA on the SOM.

■ **B2B J2 connector**

The J2 connector primarily provides FPGA I/O directly connected to the Agilex 5 device.

Figure 2-11 illustrates the interfaces connected through the J2 connector.



Figure 2-11 Interfaces connected through the J2 connector

For detailed information on net names, pin assignments, and signal descriptions, please refer to the Excel file: [Comet_A13_Pinout_v1.0.xlsx](#) included in the System CD.

The main interfaces connected to J2 are as follows:

- **User I/O**

- 24 HSIO
- 152 HVIO
- **Power**
 - Supplies HVIO_VCC/5V power to the SOM.

Chapter 3

Additional Information

3.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Comet A13 SoM Web: <https://comet-a13.terasic.com/>

■ Revision History

Date	Version	Changes
2026.01	First publication	
2626.05	V1.1	Add note for LPDDR4 SDRAM
2026.07	V1.2	Change fan connector on SoM module from 3-pin to 4-pin
2026.07	V1.3	Modify Table 1-1
2026.07	V1.4	Change LPDDR4 B to 1GB