

# General-Purpose I/O User Guide

---

## Agilex™ 5 FPGAs and SoCs

Updated for Quartus® Prime Design Suite: **25.1.1**



**Online Version**

**Send Feedback**

**813934**

**2025.08.04**

## Contents

<b>1. Agilex™ 5 General-Purpose I/O Overview.....</b>	<b>5</b>
1.1. Package Selection and I/O Vertical Migration Support.....	6
1.2. Types of I/O Banks.....	8
<b>2. Agilex 5 HSIO Banks.....</b>	<b>9</b>
2.1. HSIO Bank Overview.....	9
2.1.1. HSIO Bank Structure.....	10
2.1.2. HSIO Buffers and Registers.....	10
2.2. HSIO Features.....	12
2.2.1. Supported I/O Standards for HSIO Banks.....	12
2.2.2. HSIO Buffer Behavior.....	14
2.2.3. Programmable I/O Element Features for the HSIO Bank.....	15
2.3. HSIO Implementation Guide.....	17
2.3.1. I/O Assignments with the Quartus Prime Assignment Editor.....	18
2.3.2. Assigning Pin I/O Standards in the Quartus Prime Pin Planner.....	20
2.4. HSIO Termination.....	20
2.4.1. Single-Ended I/O Termination in Agilex 5 Devices.....	21
2.4.2. True Differential Signaling I/O Termination in Agilex 5 Devices.....	32
2.5. HSIO Design Guidelines.....	36
2.5.1. I/O Standard Placement Restrictions for True Differential I/Os.....	36
2.5.2. Placement Restrictions for True Differential and Single-Ended I/O Standards in the Same or Adjacent HSIO Bank.....	36
2.5.3. V <sub>REF</sub> Sources and Input Standards Grouping.....	38
2.5.4. HSIO Pin Restrictions for External Memory Interfaces.....	39
2.5.5. RZQ Pin Requirement.....	39
2.5.6. I/O Standards Implementation Based on V <sub>CCIO_PIO</sub> Voltages.....	39
2.5.7. I/O Standard Selection and I/O Bank Supply Compatibility Check.....	40
2.5.8. Simultaneous Switching Noise.....	40
2.5.9. HPS Shared I/O Requirements.....	40
2.5.10. Clocking Requirements.....	40
2.5.11. Clock Restrictions for GPIO Interfaces.....	40
2.5.12. SDM Shared I/O Requirements.....	41
2.5.13. Unused Pins.....	41
2.5.14. V <sub>CCIO_PIO</sub> Supply for Unused HSIO Banks.....	41
2.5.15. HSIO Pins During Power Sequencing.....	42
2.5.16. Drive Strength Requirement for HSIO Input Pins.....	42
2.5.17. Maximum DC Current Restrictions .....	43
2.5.18. 1.05 V, 1.1 V, or 1.2 V I/O Interface Voltage Level Compatibility.....	43
2.5.19. Connection to True Differential Signaling Input Buffers During Device Reconfiguration.....	44
2.5.20. LVSTL700 I/O Standards Differential Pin Pair Requirements.....	45
2.5.21. Implementing a Pseudo Open Drain.....	45
2.5.22. Allowed Duration for Using R <sub>T</sub> OCT.....	45
2.5.23. Single-Ended Strobe Signal Differential Pin Pair Restriction.....	46
2.5.24. Implementing SLVS-400 or DPHY I/O Standard with 1.1 V V <sub>CCIO_PIO</sub> .....	46
2.6. HSIO Simulation.....	46
2.6.1. IBIS Models—HSIO Support.....	47

2.6.2. IBIS-AMI Models.....	48
2.6.3. HSPICE Models.....	48
2.6.4. Net Length Reports.....	48
<b>3. Agilex 5 HVIO Banks.....</b>	<b>49</b>
3.1. HVIO Bank Overview.....	49
3.1.1. HVIO Bank Structure.....	50
3.1.2. HVIO Buffers and Registers.....	50
3.2. HVIO Features.....	51
3.2.1. Supported I/O Standards for HVIO Banks.....	52
3.2.2. Dedicated Features of HVIO Pins.....	52
3.2.3. HVIO Buffer Behavior.....	53
3.2.4. Programmable I/O Element Features for the HVIO Bank.....	53
3.3. HVIO Implementation Guide.....	54
3.3.1. I/O Assignments with the Quartus Prime Assignment Editor.....	54
3.3.2. Assigning Pin I/O Standards in the Quartus Prime Pin Planner.....	56
3.4. HVIO Design Guidelines.....	57
3.4.1. HVIO Pins During Power Sequencing.....	57
3.4.2. Unused HVIO Pins.....	57
3.4.3. $V_{CCIO\_HVIO}$ Supply for Unused HVIO Banks.....	58
3.4.4. Maximum DC Current Restrictions .....	58
3.5. HVIO Simulation.....	58
3.5.1. IBIS Models—HVIO Support.....	59
3.5.2. HSPICE Models.....	59
3.5.3. Net Length Reports.....	60
<b>4. Agilex 5 HPS I/O Banks.....</b>	<b>61</b>
4.1. HPS I/O Bank Overview.....	61
4.2. HPS I/O Features.....	61
4.2.1. Supported I/O Standards for HPS I/O Banks.....	62
4.2.2. Programmable I/O Element Features for the HPS I/O Bank.....	62
4.2.3. HPS I/O Buffer Behavior.....	63
4.3. HPS I/O Implementation Guide.....	63
4.3.1. Configuring Open Drain Feature for the HPS I/O.....	64
4.3.2. I/O Assignments with the Quartus Prime Assignment Editor.....	65
4.3.3. Assigning Pin I/O Standards in the Quartus Prime Pin Planner.....	67
4.4. HPS I/O Design Guidelines.....	67
4.4.1. HPS I/O Pins During Power Sequencing.....	67
4.4.2. HPS Shared I/O Requirements.....	68
4.5. HPS I/O Simulation.....	68
4.5.1. IBIS Models—HPS I/O Support.....	68
4.5.2. Net Length Reports.....	69
<b>5. Agilex 5 SDM I/O Banks.....</b>	<b>70</b>
5.1. SDM I/O Bank Overview.....	70
5.2. SDM I/O Features.....	70
5.2.1. Supported I/O Standards for SDM I/O Banks.....	71
5.2.2. SDM I/O Buffer Behavior.....	71
5.2.3. I/O Standards and Features for Configuration Pins.....	72
5.3. SDM I/O Design Guidelines.....	74
5.3.1. SDM I/O Pins During Power Sequencing.....	74
5.3.2. Avalon Streaming Interface Dedicated Configuration Pins.....	75

5.4. SDM I/O Simulation.....	75
5.4.1. IBIS Models—SDM I/O Support.....	75
5.4.2. Net Length Reports.....	76
<b>6. Agilex 5 I/O Troubleshooting Guidelines.....</b>	<b>77</b>
<b>7. GPIO FPGA IP.....</b>	<b>78</b>
7.1. Release Information for GPIO FPGA IP.....	78
7.2. Generating the GPIO FPGA IP.....	78
7.2.1. Altera FPGA IP Generation Output.....	80
7.3. GPIO FPGA IP Parameter Settings.....	83
7.3.1. Guideline: Swap datain_h and datain_l Ports in Migrated IP.....	84
7.4. GPIO FPGA IP Interface Signals.....	84
7.4.1. Shared Signals.....	87
7.4.2. Data Bit-Order for Data Interface.....	87
7.4.3. Input and Output Bus High and Low Bits.....	87
7.4.4. Data Interface Signals and Corresponding Clocks.....	88
7.5. GPIO FPGA IP Architecture.....	88
7.5.1. GPIO FPGA IP Data Paths.....	89
7.5.2. Register Packing.....	91
7.6. Verifying Resource Utilization and Design Performance.....	91
7.7. GPIO FPGA IP Timing.....	91
7.7.1. Timing Components.....	91
7.7.2. Delay Elements.....	93
7.7.3. Timing Analysis.....	93
7.7.4. Timing Closure Guidelines.....	96
7.8. GPIO FPGA IP Design Examples.....	96
7.8.1. GPIO FPGA IP Synthesizable Quartus Prime Design Example.....	97
7.8.2. GPIO FPGA IP Simulation Design Example.....	97
<b>8. Programmable I/O Features Description.....</b>	<b>99</b>
8.1. Programmable Pre-Emphasis.....	100
8.2. Programmable De-Emphasis.....	101
8.3. Programmable Differential Output Voltage.....	102
8.4. Continuous Time Linear Equalization.....	103
<b>9. Document Revision History for the General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs.....</b>	<b>104</b>

## 1. Agilex™ 5 General-Purpose I/O Overview

The Agilex™ 5 I/O system includes four types of I/O interfaces. Each I/O interface caters to different interfacing requirements.

**Table 1. Types of I/O Interfaces**

Interface Type	Features
High-speed I/O (HSIO)	<ul style="list-style-type: none"> <li>1.0 V, 1.05 V, 1.1 V, 1.2 V, and 1.3 V single-ended non-voltage referenced I/O standards.</li> <li>1.05 V, 1.1 V and 1.2 V single-ended and differential voltage referenced I/O standards.</li> <li>1.3 V true differential I/O compatible with LVDS, capable to interface with LVDS subsets such as: <ul style="list-style-type: none"> <li>— RSDS</li> <li>— Mini-LVDS</li> <li>— Any I/O standards using equivalent electrical specifications</li> </ul> </li> <li>External memory interfaces up to 1,866 MHz with a Hard Memory Controller (HMC).</li> <li>LVDS serializer/deserializer (SERDES) interface up to 1.6 Gbps.</li> <li>MIPI* D-PHY* interface up to 3.5 Gbps<sup>(1)</sup> per lane</li> </ul>
High-voltage I/O (HVIO)	1.8 V, 2.5 V, and 3.3 V single-ended non-voltage referenced JEDEC-compliant I/O standards.
Secure Device Manager (SDM) I/O	1.8 V single-ended non-voltage referenced I/O standard.
Hard Processor System (HPS) I/O	1.8 V single-ended non-voltage referenced I/O standard.

### Related Information

- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)
- [LVDS SERDES User Guide: Agilex 5 FPGAs and SoCs](#)
- [External Memory Interfaces \(EMIF\) IP User Guide: Agilex 5 FPGAs and SoCs](#)
- [General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs](#)  
Get the latest and previous versions of this user guide. If an IP or software version is not listed, the user guide for the previous IP or software version applies.
- [MIPI D-PHY specifications, MIPI Alliance website.](#)  
Provides more information about the standard and long reference channels.

<sup>(1)</sup> Up to 3.5 Gbps for standard reference channel, and up to 2.5 Gbps for long reference channel. For more information, refer to the MIPI D-PHY specifications and the Agilex 5 data sheet.

## 1.1. Package Selection and I/O Vertical Migration Support

In the following figures:

- The arrows indicate the package migration paths. The shades represent the devices included in each path.
- To achieve full I/O migration across devices in the same migration path, restrict I/Os and transceivers utilization to match the device with the lowest I/O and transceiver counts.

**Figure 1. Package Options, Migrations, and I/O Pins—D-Series**

Series	Device	Package	
		Key: HVIO / HSIO (LVDS) / HPSIO / Transceivers	
		Ball Pitch: Variable <sup>(1)</sup> Grid Array Pattern: Variable Pitch BGA VPBGA: Variable Pitch BGA	
		B23D 820-pin VPBGA 23 mm × 23 mm	B32B 1610-pin VPBGA 32 mm × 32 mm
D-Series	A5D 010	60 / 192 (96) / 48 / 8	60 / 384 (192) / 48 / 16
	A5D 025	60 / 192 (96) / 48 / 8	60 / 384 (192) / 48 / 16
	A5D 031	60 / 192 (96) / 48 / 8	60 / 384 (192) / 48 / 16
	A5D 051		60 / 384 (192) / 48 / 24
	A5D 064		60 / 384 (192) / 48 / 32

Note:

(1) The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable, ranging from 0.65 mm to 1.45 mm in a single package to ease signal routing. For more information, refer to the PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs.

**Figure 2. Package Options, Migrations, and I/O Pins—E-Series**

Series	Device	Package					
		Key: HVIO / HSIO (LVDS) / HPSIO / Transceivers					
		Ball Pitch: Variable <sup>(1)</sup> Grid Array Pattern: Variable Pitch BGA VPBGA: Variable Pitch BGA					
		M16A 896-pin MBGA 16 mm × 16 mm	B15A 351-pin VPBGA 15 mm × 15 mm	B18A 474-pin VPBGA 18 mm × 18 mm	B23B 795-pin VPBGA 23 mm × 23 mm	B23A 839-pin VPBGA 23 mm × 23 mm	B32A 1591-pin VPBGA 32 mm × 32 mm
E-Series	Device Group A	A5E 013A				120 / 96 (48) / 48 / 4	200 / 192 (96) / 48 / 4
		A5E 028A				120 / 96 (48) / 48 / 12	200 / 192 (96) / 48 / 12
		A5E 043A				120 / 96 (48) / 48 / 12	120 / 384 (192) / 48 / 16
		A5E 052A				120 / 96 (48) / 48 / 12	120 / 384 (192) / 48 / 24
		A5E 065A				120 / 96 (48) / 48 / 12	120 / 384 (192) / 48 / 24
	Device Group B	A5E 005B	80 / 72 (36) / 0 / 0	160 / 48 (24) / 0 / 0	159 / 96 (48) / 0 / 0		
		A5E 007B	80 / 72 (36) / 0 / 0	160 / 48 (24) / 0 / 0	159 / 96 (48) / 0 / 0		
		A5E 008B	40 / 192 (96) / 48 / 4		159 / 192 (96) / 48 / 0	120 / 96 (48) / 48 / 4	200 / 192 (96) / 48 / 4
		A5E 013B	40 / 192 (96) / 48 / 4		159 / 192 (96) / 48 / 0	120 / 96 (48) / 48 / 4	200 / 192 (96) / 48 / 4
		A5E 028B	40 / 192 (96) / 48 / 8		159 / 192 (96) / 48 / 0	120 / 96 (48) / 48 / 12	200 / 192 (96) / 48 / 12
		A5E 043B				120 / 96 (48) / 48 / 12	120 / 384 (192) / 48 / 16
		A5E 052B				120 / 96 (48) / 48 / 12	120 / 384 (192) / 48 / 24
		A5E 065B				120 / 96 (48) / 48 / 12	120 / 384 (192) / 48 / 24

Note:

(1) The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable, ranging from 0.65 mm to 1.45 mm in a single package to ease signal routing. For more information, refer to the PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs and Device Migration Guidelines: Agilex™ 5 FPGAs and SoCs E-Series.

**Note:**

For the VPBGA packages, The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable, ranging from 0.65 mm to 1.45 mm in a single package to ease signal routing. For more information, refer to the [PCB Design Guidelines \(HSSI, EMIF, MIPI, True Differential, PDN\) User Guide: Agilex 5 FPGAs and SoCs](#).

**Related Information**

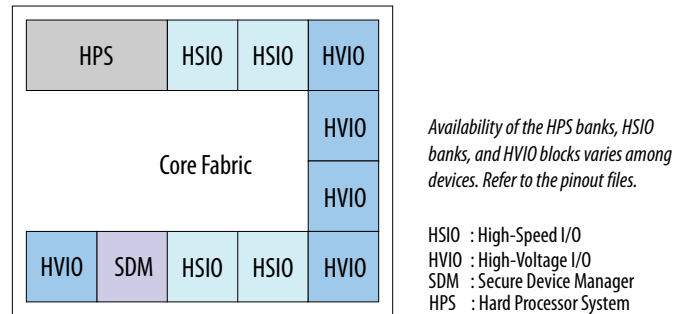
- [PCB Design Guidelines \(HSSI, EMIF, MIPI, True Differential, PDN\) User Guide: Agilex 5 FPGAs and SoCs](#)
- [Device Migration Guidelines: Agilex 5 FPGAs and SoCs E-Series](#)  
Provides more information about the device migration path.

## 1.2. Types of I/O Banks

The Agilex 5 devices contain four types of I/O banks: HSIO, HVIO, HPS, and SDM I/O banks.

**Figure 3. Locations of Different I/O Bank Types**

This figure shows the approximate locations of each I/O bank type in the Agilex 5 device. The figure shows the view of the die as shown in the Quartus® Prime **Chip Planner**. In the **Pin Planner**, this corresponds to the "Bottom View". Different device and package combinations have different number of I/O banks. Refer to the device pin-out files for available I/O banks and the locations of the SDM and HPS I/O banks for each device package.



Refer to the related information for the features and architectural descriptions of each I/O bank type.

### Related Information

- [Agilex 5 HSIO Banks](#) on page 9
- [Agilex 5 HVIO Banks](#) on page 49
- [Agilex 5 HPS I/O Banks](#) on page 61
- [Agilex 5 SDM I/O Banks](#) on page 70
- [Device Migration Guidelines: Agilex 5 FPGAs and SoCs E-Series](#)





## 2. Agilex 5 HSIO Banks

---

The HSIO banks are available in the Agilex 5 FPGAs.

The HSIO banks provide the I/O buffer and peripheral support for the following functions:

- General-purpose interfaces (GPIO mode)—with or without GPIO FPGA IP
- External memory interfaces (EMIF mode)—with External Memory Interfaces IP
- Parallel interfaces (PHYLITE mode)—with PHY Lite for Parallel Interfaces IP
- LVDS SERDES interfaces—with LVDS SERDES FPGA IP
- MIPI D-PHY interfaces—with MIPI DPHY IP

### Related Information

- [LVDS SERDES User Guide: Agilex 5 FPGAs and SoCs](#)
- [Types of I/O Banks on page 8](#)
- [Device Migration Guidelines: Agilex 5 FPGAs and SoCs E-Series](#)
- [External Memory Interfaces \(EMIF\) IP User Guide: Agilex 5 FPGAs and SoCs](#)
- [Placement Restrictions for True Differential and Single-Ended I/O Standards in the Same or Adjacent HSIO Bank on page 36](#)

### 2.1. HSIO Bank Overview

Each HSIO bank contains a top index sub-bank and a bottom index sub-bank.

- Top index sub-bank—the pin index numbers are 48 to 95.
- Bottom index sub-bank—the pin index numbers are 0 to 47.

Each sub-bank contains four I/O lanes. Each I/O lane has 12 I/O pins. Consequently, there are a total of 48 single-ended I/O pins or 24 true differential I/O pairs in each sub-bank.

If you use SERDES, you can configure each I/O lane to support a SERDES transmitter or receiver channel, with optional dynamic phase alignment (DPA), for:

- Up to six dedicated differential receiver input buffer pairs
- Up to six dedicated differential transmitter output buffer pairs

If you do not use SERDES, you can configure each true differential buffer as receiver or transmitter.

Additionally, each sub-bank also contains dedicated circuitries including:

- I/O PLL
- Hard memory controller
- On-chip termination (OCT) calibration blocks

The total number of HSIO banks varies across different device packages. Some HSIO banks are shared with the SDM and HPS function blocks. Refer to the device pin-out files for available I/O banks for each device package.

### Related Information

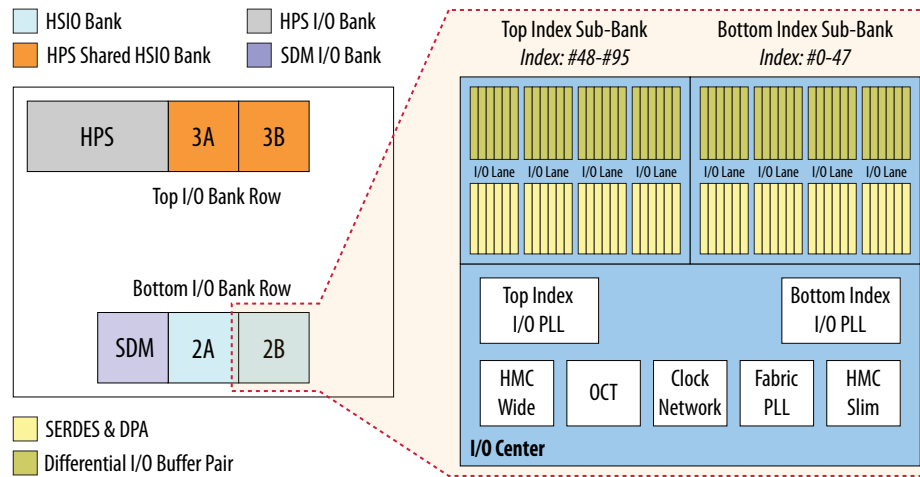
#### Agilex 5 Device Pin-Out Files

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

## 2.1.1. HSIO Bank Structure

**Figure 4. Agilex 5 HSIO Bank Structure (Die Top View)**

This figure shows the HSIO bank structure of the Agilex 5 device. The figure shows the view of the die as shown in the Quartus Prime **Chip Planner**. In the **Pin Planner**, this corresponds to the "Bottom View". Different device packages have different number of HSIO banks. Refer to the device pin-out files for available HSIO banks and the locations of the HPS shared HSIO banks for each device package.



### Related Information

#### Agilex 5 Device Pin-Out Files

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

## 2.1.2. HSIO Buffers and Registers

The I/O registers consist of three different paths.

- The input path for handling data from the input pin to the core
- The output path for handling data from the core to the output pin
- The output enable (OE) path for handling the OE signal to the output buffer

The I/O registers allow fast source-synchronous register-to-register transfers and resynchronizations. To use the I/O registers to implement double data rate (DDR) circuitry, you can use the GPIO FPGA IP.

The input and output paths contain the following blocks:

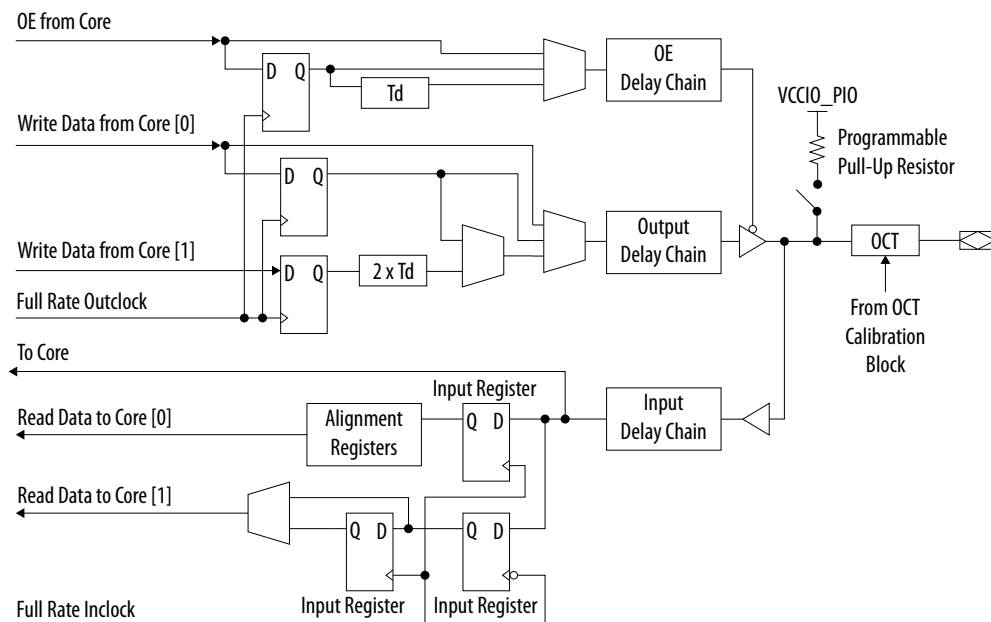
- Input registers:
  - Support full rate data transfer from the peripheral to the core
  - Support double or single data rate data captured from I/O buffer to the core
- Output registers:
  - Support full rate data transfer from the core to the peripheral
  - Support double or single data rate data transfer to the output pin
- OE registers:
  - Support the output enable signal from the core to the peripheral
  - Support double data rate or single data rate data transfer to the I/O pin

The input and output paths also support the following features:

- Clock enable
- Asynchronous or synchronous reset
- Bypass mode for input and output paths
- Delay chain on input and output paths

**Figure 5. I/O Element (IOE) Structure of Agilex 5 HSIO**

In this figure, "Td" is the delay block with fixed delay inserted to ensure correct timing of the DDR data transfer.



### Related Information

GPIO FPGA IP on page 78

## 2.2. HSIO Features

The I/O bank within the HSIO interface supports various differential and single-ended I/O standards to cater to different types of interfacing requirements.

- Single-ended LVCMOS for general purpose I/O interfacing.
- Single-ended and pseudo-differential voltage-referenced I/O standards for general purpose and external memory interfacing. The differential voltage-referenced output pins are not true differential output pins. The differential voltage-referenced I/O standards use two single-ended output pins with one of the output pins inverted.
- True differential I/O buffer pairs using the True Differential Signaling and SLVS-400 I/O standards. The True Differential Signaling I/O standard is compatible with the LVDS, RSDS, Mini-LVDS, and LVPECL I/O standards. One true differential buffer pair forms a true differential channel.

### Power Pins for the HSIO Buffers

The VCCIO\_PIO and VCCPT pins power the I/O buffers located in the I/O bank within the HSIO interface.

### HSIO Buffer Features

- Single-ended non-voltage referenced and voltage-referenced I/O standards
- Differential voltage-referenced I/O standards
- True differential transmitters and receivers
- Serializer/deserializer (SERDES)
- Programmable slew rate
- Programmable weak pull-up resistor
- Programmable differential output voltage ( $V_{OD}$ ) for true differential output buffers
- Programmable receiver equalization calibration
- On-chip series termination ( $R_S$  OCT)
- On-chip parallel termination ( $R_T$  OCT)
- On-chip differential termination ( $R_D$  OCT)
- Dynamic on-chip parallel termination
- Internally generated  $V_{REF}$
- Programmable pre-emphasis for true differential output buffer
- Programmable de-emphasis

### 2.2.1. Supported I/O Standards for HSIO Banks

The VCCIO\_PIO and VCCPT power supplies power the HSIO buffers. Each I/O sub-bank has its own VCCIO\_PIO power supply and supports only one I/O voltage.

The True Differential Signaling I/O standard is compatible with the LVDS, RSDS, Mini-LVDS, and LVPECL standards at a lower signal swing.

You can place the True Differential Signaling input buffer in a HSIO bank powered by 1.05 V, 1.1 V, 1.2 V and 1.3 V  $V_{CCIO\_PIO}$ . The maximum input voltage to the True Differential Signaling input buffer must not exceed the value of

$$\text{Maximum } V_{ICM} + \left( \frac{\text{Maximum } V_{ID}}{2} \right):$$

- For 1.05 V, 1.1 V, and 1.2 V  $V_{CCIO\_PIO}$ , the maximum input voltage is 1.177 V
- For 1.3 V  $V_{CCIO\_PIO}$  bank, the maximum input voltage depends on the termination:
  - On-chip differential termination ( $R_D$  OCT) enabled—maximum input voltage is 1.602 V
  - On-board differential termination with  $R_D$  OCT disabled—maximum input voltage is 1.427 V with  $V_{ICM}$  capped at 1.2 V

By default, the Quartus Prime software assigns 1.2 V to the  $V_{CCIO\_PIO}$  pin in unused I/O sub-banks.

**Table 2. HSIO Bank Supported I/O Standards**

This table lists the input and output voltages of a HSIO bank.

I/O Standard	$V_{CCIO\_PIO}$ (V)		$V_{CCPT}$ (V)	JEDEC Standard
	Input	Output		
1.3 V LVCMOS	1.3	1.3	1.8	—
1.2 V LVCMOS	1.2	1.2	1.8	JESD8-12A.01
1.1 V LVCMOS	1.1	1.1	1.8	—
1.05 V LVCMOS	1.05	1.05	1.8	—
1.0 V LVCMOS	1.0	1.0	1.8	—
SSTL-12 <sup>(2)</sup>	1.2	1.2	1.8	JESD79-4B
HSTL-12 <sup>(2)</sup>	1.2	1.2	1.8	JESD-16A
HSUL-12 <sup>(2)</sup>	1.2	1.2	1.8	JESD209-3C
POD12 <sup>(2)</sup>	1.2	1.2	1.8	JESD79-4B
POD11 <sup>(2)</sup>	1.1	1.1	1.8	JESD79-5
LVSTL11	1.1	1.1	1.8	JESD209-4C
LVSTL105	1.05	1.05	1.8	JESD209-5
LVSTL700 <sup>(4)</sup>	1.05	1.05	1.8	JESD209-4-1 JESD209-5
Differential SSTL-12 <sup>(2) (3)</sup>	1.2	1.2	1.8	JESD79-4B
Differential HSTL-12 <sup>(2) (3)</sup>	1.2	1.2	1.8	JESD8-16A
Differential HSUL-12 <sup>(2) (3)</sup>	1.2	1.2	1.8	JESD209-3C
Differential POD-12 <sup>(2) (3)</sup>	1.2	1.2	1.8	JESD79-4B
Differential POD11 <sup>(2) (3)</sup>	1.1	1.1	1.8	JESD79-5

*continued...*

<sup>(2)</sup> Input buffers are powered by 1.8 V  $V_{CCPT}$

<sup>(3)</sup> Uses two single-ended outputs with second output programmed as inverted.

I/O Standard	V <sub>CCIO_PIO</sub> (V)		V <sub>CCPT</sub> (V)	JEDEC Standard
	Input	Output		
Differential LVSTL11 <sup>(3)</sup>	1.1	1.1	1.8	JESD209-4C
Differential LVSTL105 <sup>(3)</sup>	1.05	1.05	1.8	JESD209-5
Differential LVSTL700 <sup>(4)</sup> <sup>(3)</sup>	1.05	1.05	1.8	JESD209-4-1 JESD209-5
SLVS-400 <sup>(4)</sup>	1.1/1.2	1.1/1.2	1.8	JESD8-13
DPHY <sup>(4)</sup>	1.1/1.2	1.1/1.2	1.8	—
True Differential Signaling <sup>(2)</sup>	1.05/1.1/1.2/1.3	1.3	1.8	—

#### Related Information

- [I/O Standards Specifications, Agilex 5 FPGAs and SoCs Device Data Sheet](#)  
Provides the electrical specifications for the supported I/O standards.
- [Assigning Pin I/O Standards in the Quartus Prime Assignment Editor](#) on page 18
- [Assigning Pin I/O Standards in the Quartus Prime Pin Planner](#) on page 20

## 2.2.2. HSIO Buffer Behavior

**Table 3. HSIO Pins Guideline for Different Pin States**

HSIO Pin State					
Not turned on	Powering up	Fully powered up	Configuration mode	User mode	Powering down
Either tri-state the pins or do not drive them with any external voltage.	<ul style="list-style-type: none"> <li>Pin voltage must not exceed V<sub>CCIO_PIO</sub> or 1.2 V, whichever is lower.<sup>(5)</sup></li> <li>After full V<sub>CCIO_PIO</sub> power up, the pins are tri-stated with weak pull-up enabled.</li> </ul>	All pins are tri-stated with weak pull-up enabled.	All pins are tri-stated with weak pull-up enabled.	Valid data transactions can be initiated.	<ul style="list-style-type: none"> <li>Pin voltage must not exceed V<sub>CCIO_PIO</sub> or 1.2 V, whichever is lower.<sup>(5)</sup></li> <li>When the V<sub>CCIO_PIO</sub> and V<sub>CC</sub> power rails are powering down, the I/O pin signals measure between ground and the V<sub>CCIO_PIO</sub> voltage levels.</li> </ul>

**Note:** After the Agilex 5 device fully powers up, the voltage levels for the HSIO pins must not exceed the DC input voltage (V<sub>I</sub>) value or the AC maximum allowed overshoot during transitions.

#### Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)

<sup>(4)</sup> Not supported in GPIO mode.

<sup>(5)</sup> V<sub>CCIO\_PIO</sub> refers to the real-time onboard voltage supply.

## 2.2.3. Programmable I/O Element Features for the HSIO Bank

**Table 4. Programmable Slew Rate, De-Emphasis, Receiver Equalization Calibration, and I/O Delay**

This table lists the I/O standards that the feature supports and the available settings for each I/O standard.

I/O Standard	Slew Rate Control	De-Emphasis	Receiver Equalization Calibration	I/O Delay <sup>(6)</sup>
<ul style="list-style-type: none"> <li>1.3 V LVCMOS</li> <li>1.2 V LVCMOS</li> <li>1.1 V LVCMOS</li> <li>1.05 V LVCMOS</li> <li>1.0 V LVCMOS</li> </ul>	<ul style="list-style-type: none"> <li>Fastest</li> <li>Fast</li> <li>Medium (Default)</li> <li>Slow</li> </ul>	—	Off	Refer to the device data sheet
<ul style="list-style-type: none"> <li>SSTL-12 / Differential SSTL-12</li> <li>HSTL-12 / Differential HSTL-12</li> <li>HSUL-12 / Differential HSUL-12</li> </ul>		<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Low LP</li> <li>Medium LP</li> <li>High LP</li> <li>Low CZ</li> <li>Medium CZ</li> <li>High CZ</li> </ul>	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Small</li> <li>Medium</li> <li>Large</li> </ul>	
<ul style="list-style-type: none"> <li>POD12 / Differential POD12</li> <li>POD11 / Differential POD11</li> <li>LVSTL11 / Differential LVSTL11</li> <li>LVSTL105 / Differential LVSTL105</li> <li>LVSTL700 / Differential LVSTL700</li> <li>SLVS-400</li> <li>DPHY</li> </ul>	<ul style="list-style-type: none"> <li>Fastest (Default)</li> <li>Fast</li> <li>Medium</li> <li>Slow</li> </ul>			
True Differential Signaling	—	—		

**Table 5. Programmable Weak Pull-Up Resistor**

This table lists the I/O standard that the features support and the available settings.

I/O Standard	Weak Pull-Up Resistor
<ul style="list-style-type: none"> <li>1.3 V LVCMOS</li> <li>1.2 V LVCMOS</li> <li>1.1 V LVCMOS</li> <li>1.05 V LVCMOS</li> <li>1.0 V LVCMOS</li> </ul>	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>On</li> </ul>

**Table 6. Programmable Pre-Emphasis and Differential Output Voltage**

This table lists the I/O standard that the features support and the available settings.

I/O Standard	Pre-Emphasis	Differential Output Voltage
True Differential Signaling	<ul style="list-style-type: none"> <li>Off</li> <li>On (Default)</li> </ul>	<ul style="list-style-type: none"> <li>Low</li> <li>Medium low</li> <li>Medium high (Default)</li> <li>High</li> </ul>

### Related Information

- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)
- [Programmable I/O Features Description](#) on page 99

<sup>(6)</sup> Delay chain is not supported in the LVDS SERDES receiver mode.

### 2.2.3.1. Guidelines: Programmable Output Slew Rate Control

**Table 7. Slew Rate Implementation and Mode Support**

Uncompensated slew rate is supported only for OCT without calibration. Compensated slew rate is supported only for OCT with calibration.

Slew Rate Setting	Implementation	Slew Rate Mode Support
<ul style="list-style-type: none"> <li>Fast</li> <li>Medium</li> <li>Slow</li> </ul>	GPIO mode	Supports only the uncompensated slew rate mode.
	<ul style="list-style-type: none"> <li>External memory interface</li> <li>PHY Lite</li> <li>MIPI D-PHY mode</li> </ul>	Supports only the compensated slew rate mode. The compensated slew rate mode achieves better slew rate control by reducing variation of the ramp rate.
Fastest	<ul style="list-style-type: none"> <li>GPIO mode</li> <li>External memory interface</li> <li>PHY Lite</li> <li>MIPI D-PHY mode</li> </ul>	Supports only the slew rate bypass mode. The implementation disables slew rate control and the buffer switches at the fastest ramp rate.

#### Related Information

[Programmable I/O Features Description](#) on page 99

### 2.2.3.2. Guidelines: Programmable Pull-Up Resistor

The programmable pull-up resistor feature is enabled by default on unused I/O pins in the HSIO bank.

#### Related Information

[Programmable I/O Features Description](#) on page 99

### 2.2.3.3. Guidelines: Programmable De-Emphasis

- The de-emphasis effect reduces eye height. If you use a non-default de-emphasis setting, perform an IBIS or HSPICE simulation to estimate the electrical performance of the I/O buffer.
- To get the optimal setting for your design, start the simulation with the lowest de-emphasis setting. From there, fine-tune the setting until you get the best signal integrity.
- If you use the compensated slew rate setting, de-emphasis is supported only in the following modes:
  - External memory interface
  - PHY Lite
  - MIPI D-PHY

#### Related Information

[Programmable I/O Features Description](#) on page 99



## 2.3. HSIO Implementation Guide

The Quartus Prime software provides tools for you to create, configure and compile your I/O design. Each tool provides different functions and supports different features to implement your I/O design.

**Table 8. Quartus Prime I/O Implementation Tools**

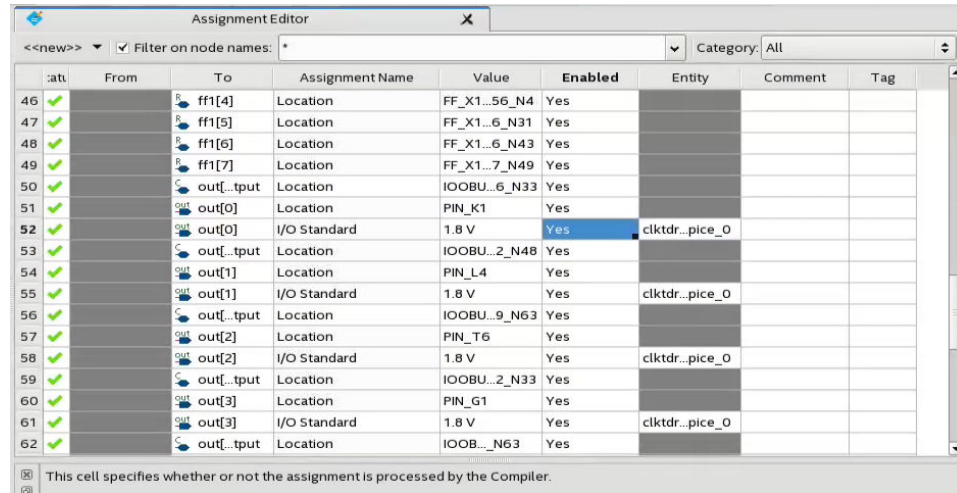
Tool	Functions	Supported Assignment	Supported I/O Standards
Assignment Editor	<ul style="list-style-type: none"> <li>View, create and edit assignments.</li> <li>The Quartus Prime software: <ul style="list-style-type: none"> <li>Dynamically validates your edits.</li> <li>Notify you of errors and warnings of invalid assignments.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>I/O standard</li> <li>Programmable slew rate control</li> <li>Programmable I/O delay</li> <li>Programmable weak pull-up resistor</li> <li>Programmable pre-emphasis</li> <li>Programmable de-emphasis</li> <li>Programmable <math>V_{OD}</math></li> <li>OCT</li> <li>Receiver equalization</li> <li>Fast input register</li> <li>Fast output enable register</li> <li>Fast output register</li> </ul>	<ul style="list-style-type: none"> <li>1.3 V LVCMOS</li> <li>1.2 V LVCMOS</li> <li>1.1 V LVCMOS</li> <li>1.05 V LVCMOS</li> <li>1.0 V LVCMOS</li> <li>SSTL-12</li> <li>HSTL-12</li> <li>HSUL-12</li> <li>POD12</li> <li>POD11</li> <li>LVSTL11</li> <li>LVSTL105</li> <li>LVSTL700</li> </ul>
Pin Planner	<ul style="list-style-type: none"> <li>Graphically represent pin locations on the device.</li> <li>With this tool, you can: <ul style="list-style-type: none"> <li>Perform initial pin planning.</li> <li>Locate, place, and assign I/O pins.</li> <li>Configure board trace models for pins you select for signal integrity evaluations.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>I/O standard</li> <li>Programmable slew rate control</li> <li>Programmable weak pull-up resistor</li> <li>OCT</li> <li>Fast input register</li> <li>Fast output enable register</li> <li>Fast output register</li> </ul>	<ul style="list-style-type: none"> <li>Differential SSTL-12</li> <li>Differential HSTL-12</li> <li>Differential HSUL-12</li> <li>Differential POD-12</li> <li>Differential POD11</li> <li>Differential LVSTL11</li> <li>Differential LVSTL105</li> <li>Differential LVSTL700</li> <li>SLVS-400</li> <li>DPHY</li> <li>True Differential Signaling</li> </ul>
GPIO FPGA IP	<ul style="list-style-type: none"> <li>Instantiate the IP.</li> <li>Customize your IP instance using parameters options.</li> </ul>	<ul style="list-style-type: none"> <li>SDR transfer</li> <li>DDIO transfer</li> <li>Output enable</li> </ul>	—

### 2.3.1. I/O Assignments with the Quartus Prime Assignment Editor

You can assign all instance-specific settings and constraints through the Quartus Prime Assignment Editor. You can filter assignments by node name or category.

**Figure 6. Quartus Prime Assignment Editor**

This figure shows an example of the user interface and does not represent actual components, features, or settings supported by Agilex 5 FPGAs.



	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
46	ff1[4]	Location	FF_X1...56_N4	Yes				
47	ff1[5]	Location	FF_X1...6_N31	Yes				
48	ff1[6]	Location	FF_X1...6_N43	Yes				
49	ff1[7]	Location	FF_X1...7_N49	Yes				
50	out[...tput	Location	IOOBU...6_N33	Yes				
51	out[0]	Location	PIN_K1	Yes				
52	out[0]	I/O Standard	1.8 V	Yes	clktdr...pice_0			
53	out[...tput	Location	IOOBU...2_N48	Yes				
54	out[1]	Location	PIN_L4	Yes				
55	out[1]	I/O Standard	1.8 V	Yes	clktdr...pice_0			
56	out[...tput	Location	IOOBU...9_N63	Yes				
57	out[2]	Location	PIN_T6	Yes				
58	out[2]	I/O Standard	1.8 V	Yes	clktdr...pice_0			
59	out[...tput	Location	IOOBU...2_N33	Yes				
60	out[3]	Location	PIN_G1	Yes				
61	out[3]	I/O Standard	1.8 V	Yes	clktdr...pice_0			
62	out[...tput	Location	IOOB...N63	Yes				

This cell specifies whether or not the assignment is processed by the Compiler.

#### 2.3.1.1. Assigning Pin I/O Standards in the Quartus Prime Assignment Editor

1. From the Quartus Prime menu, select **Assignments > Assignment Editor**
2. Under the **To** column, search for the pin that you want to configure.
3. Under the **Assignment Name** column, select **I/O Standard (Accepts wildcards)**.
4. Under the **Value** column, select the I/O standard that you want to assign to the pin.
5. From the Quartus Prime menu, select **File > Save**.

#### Related Information

[Supported I/O Standards for HSIO Banks](#) on page 12

#### 2.3.1.2. Assigning Programmable IOE Features in the Quartus Prime Assignment Editor

1. From the Quartus Prime menu, select **Assignments > Assignment Editor**
2. Under the **To** column, search for the pin that you want to configure.
3. Under the **Assignment Name** column, select a supported programmable IOE feature.
4. Under the **Value** column, select a supported value.
5. From the Quartus Prime menu, select **File > Save**.

### Related Information

[HSIO Programmable IOE Features Assignment Names and Settings](#) on page 19  
Provides a list of supported programmable IOE features for the HSIO, the assignment names, and supported values.

### 2.3.1.3. HSIO Programmable IOE Features Assignment Names and Settings

**Table 9. HSIO Programmable IOE Features Assignment Names and Settings**

This table lists the programmable IOE features assignment names and values that you can specify in the Quartus Prime Assignment Editor and Pin Planner tools.

Feature	Assignment Name	Supported Values
Slew rate control	<b>Slew Rate</b>	<ul style="list-style-type: none"> <li>• <b>0</b>—slow</li> <li>• <b>1</b>—medium</li> <li>• <b>2</b>—fast</li> <li>• <b>3</b>—fastest</li> </ul> For the default setting, refer to the related information.
I/O delay	<ul style="list-style-type: none"> <li>• <b>Input Delay Chain Setting</b></li> <li>• <b>Output Delay Chain Setting</b></li> <li>• <b>Output Enable Delay Chain Setting</b></li> </ul>	Refer to the device data sheet.
Weak pull-up resistor	<b>Weak Pull-Up Resistor</b>	<ul style="list-style-type: none"> <li>• <b>On</b></li> <li>• <b>Off</b> (default)</li> </ul>
Pre-emphasis	<b>Programmable Pre-emphasis</b>	<ul style="list-style-type: none"> <li>• <b>0</b>—off</li> <li>• <b>1</b>—on (default)</li> </ul>
De-emphasis	<b>Programmable De-emphasis</b>	<ul style="list-style-type: none"> <li>• <b>HIGH</b></li> <li>• <b>HIGH CONST Z</b></li> <li>• <b>LOW</b></li> <li>• <b>LOW CONST Z</b></li> <li>• <b>MEDIUM</b></li> <li>• <b>MEDIUM CONST Z</b></li> <li>• <b>OFF</b> (default)</li> </ul>
Receiver equalization calibration	<b>Receiver Equalization</b>	<ul style="list-style-type: none"> <li>• <b>OFF</b> (default)</li> <li>• <b>SMALL</b></li> <li>• <b>MEDIUM</b></li> <li>• <b>LARGE</b></li> </ul>
Differential output voltage	<b>Programmable Differential Output Voltage (VOD)</b>	<ul style="list-style-type: none"> <li>• <b>0</b>—low</li> <li>• <b>1</b>—medium low</li> <li>• <b>2</b>—medium high (default)</li> <li>• <b>3</b>—high</li> </ul>

### Related Information

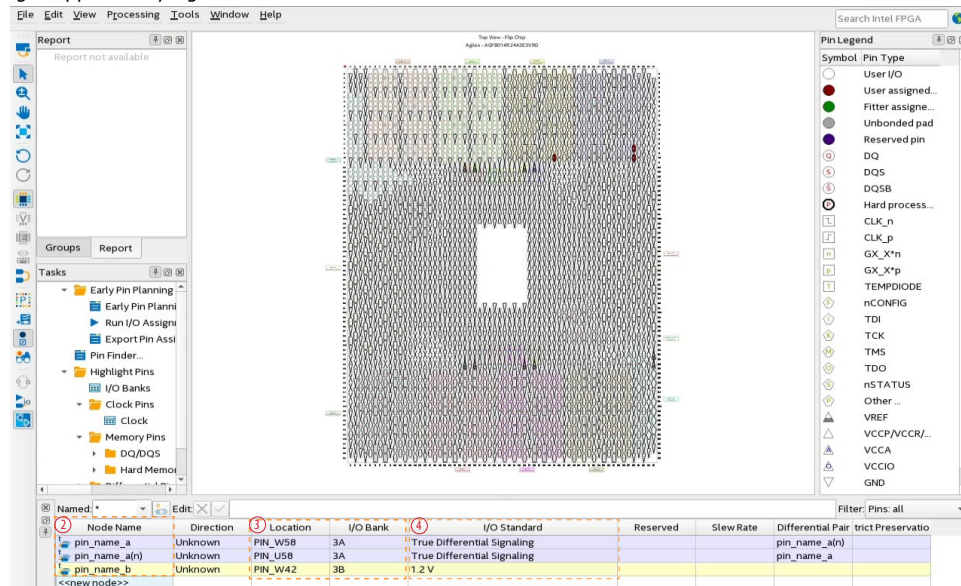
- [Programmable IOE Delay, Agilex 5 FPGAs and SoCs Device Data Sheet](#)  
Provides the input and output delay chains specifications.
- [Assigning Programmable IOE Features in the Quartus Prime Assignment Editor](#) on page 18

## 2.3.2. Assigning Pin I/O Standards in the Quartus Prime Pin Planner

You can use the Quartus Prime Pin Planner for I/O pin planning, assignment, and validation.

**Figure 7. Quartus Prime Pin Planner**

This figure shows an example of the user interface and does not represent actual components, features, or settings supported by Agilex 5 FPGAs.



1. From the Quartus Prime menu, select **Assignments > Pin Planner**.
2. Under the **Node Name** column in the **All Pins** box, look for the pin that you want to configure.
3. Under the **Location** column, select the specific pin location.  
The **I/O Bank** column displays the I/O bank name where the pin resides. The **Top View - Flip Chip** diagram shows the I/O banks in different colors.
4. Under the **I/O Standard** column, select the supported I/O standards that you want to assign to the pin.

If you select **True Differential Signaling**, the Pin Planner automatically adds a negative node with a specific pin location.

### Related Information

[Supported I/O Standards for HSIO Banks](#) on page 12

## 2.4. HSIO Termination

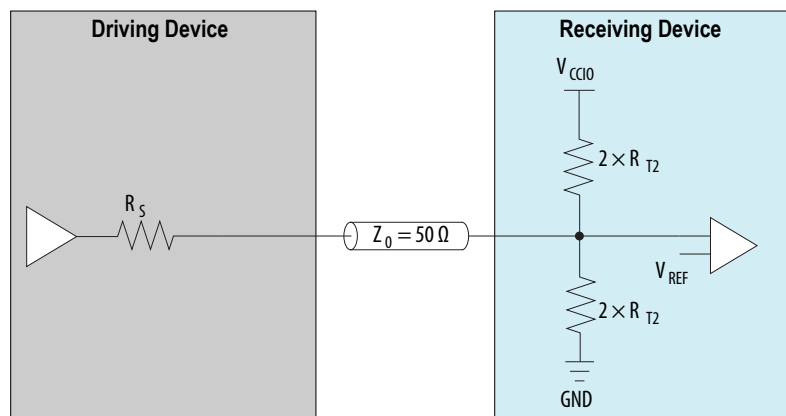
Agilex 5 devices support on-chip termination for single-ended and true differential I/O standards. The OCT maintains signal quality, saves board space, and reduces external component costs. You can also use external termination for the single-ended I/Os and true differential signaling I/Os.

### 2.4.1. Single-Ended I/O Termination in Agilex 5 Devices

Agilex 5 devices support on-chip termination for single-ended I/O standards. OCT helps to minimize reflections and improve electrical margins.

**Figure 8.  $R_S$  and  $R_T$  OCT**

This figure shows the single-ended termination schemes supported in Agilex 5 devices.  $R_{T2}$  is the dynamic parallel termination that switches on only when the device is receiving. In bidirectional applications,  $R_{T2}$  automatically switches on when the device is receiving and switches off when the device is driving.



#### 2.4.1.1. Single-Ended I/O Standards On-Chip Termination

Serial ( $R_S$ ) and parallel ( $R_T$ ) OCT provides I/O impedance matching and termination capabilities.

The OCT calibration circuit uses the impedance of the external resistor that is connected to the  $RZQ$  pin as reference. During calibration, the circuit continuously alters the impedance of the I/O buffer until the impedance reaches a predetermined ratio to the reference resistance.

The OCT with calibration feature is not supported in GPIO mode.

**Table 10. OCT Schemes Supported in Agilex 5 Devices**

Direction	OCT Scheme
Output	$R_S$ OCT with calibration
	$R_S$ OCT without calibration
Input	$R_T$ OCT with calibration
	$R_T$ OCT without calibration
Bidirectional	Dynamic $R_S$ and $R_T$ OCT

### 2.4.1.1.1. $R_S$ OCT

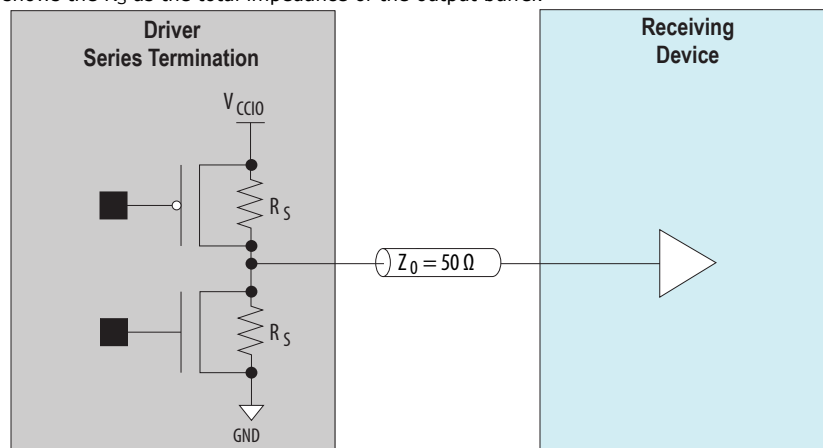
Agilex 5 devices support  $R_S$  OCT with and without calibration.

**Table 11.  $R_S$  OCT Schemes**

OCT Scheme	Description
$R_S$ without calibration	<ul style="list-style-type: none"> <li>Available on output buffer only.</li> <li>Driver-impedance matching provides the I/O driver with a controlled output impedance that closely matches the impedance of the transmission line.</li> </ul>
$R_S$ with calibration	<ul style="list-style-type: none"> <li>The <math>R_S</math> OCT calibration circuit uses the impedance of the external resistor connected to the RZQ pin as a reference.</li> <li>During calibration, the circuit continuously alters the impedance of the I/O buffer until the value reaches the target impedance, which is a predetermined ratio to the reference resistance.</li> <li>The calibration occurs at the end of the device configuration. When the calibration circuit finds the correct impedance, the circuit stops changing the characteristics of the drivers.</li> <li>In EMIF and MIPI D-PHY modes, you may trigger recalibration during user mode.</li> </ul>

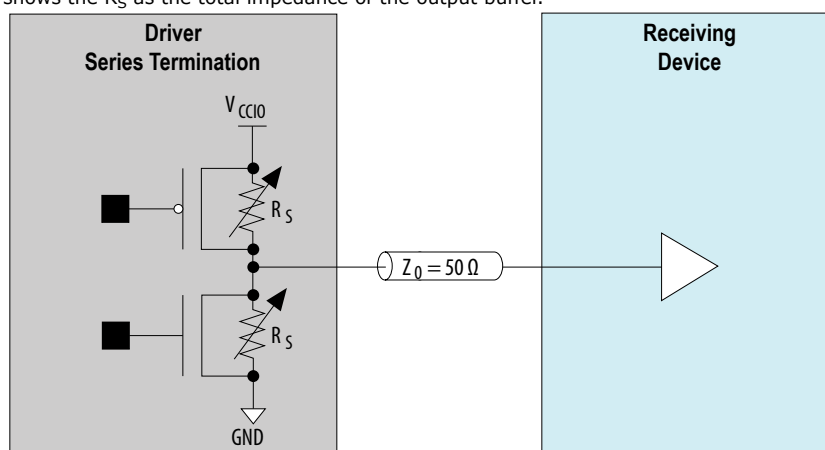
**Figure 9.  $R_S$  OCT without Calibration**

This figure shows the  $R_S$  as the total impedance of the output buffer.



**Figure 10.  $R_S$  OCT with Calibration**

This figure shows the  $R_S$  as the total impedance of the output buffer.



**Table 12. Selectable I/O Standards for  $R_S$  OCT for HSIO Banks**

The default values are in **bold** font.

I/O Standard	$R_S$ OCT without Calibration <sup>(7)</sup> ( $\Omega$ )	$R_S$ OCT with Calibration ( $\Omega$ )
1.3 V LVCMOS	34, <b>40</b>	—
1.2 V LVCMOS	34, <b>40</b>	—
1.1 V LVCMOS	34, <b>40</b>	—
1.05 V LVCMOS	34, <b>40</b>	—
1.0 V LVCMOS	34, <b>40</b>	—
SSTL-12	34, <b>40</b>	34, 40
HSTL-12	34, <b>40</b>	34, 40
HSUL-12	34, <b>40</b>	34, 40
POD12	<b>34</b> , 40	34, 40
POD11	<b>34</b> , 40	34, 40
LVSTL11	34, <b>40</b>	34, 40
LVSTL105	34, <b>40</b>	34, 40
LVSTL700	—	<b>40</b>
Differential SSTL-12	34, <b>40</b>	34, 40
Differential HSTL-12	34, <b>40</b>	34, 40
Differential HSUL-12	34, <b>40</b>	34, 40
Differential POD12	<b>34</b> , 40	34, 40
Differential POD11	<b>34</b> , 40	34, 40
Differential LVSTL11	34, <b>40</b>	34, 40

*continued...*

<sup>(7)</sup> Supported only in GPIO mode.

I/O Standard	R <sub>S</sub> OCT without Calibration <sup>(7)</sup> (Ω)	R <sub>S</sub> OCT with Calibration (Ω)
Differential LVSTL105	34, <b>40</b>	34, 40
Differential LVSTL700	—	<b>40</b>
SLVS-400	—	<b>45</b>
DPHY	—	<b>45</b>

### Related Information

[OCT Features Assignment Names and Settings](#) on page 32

---

<sup>(7)</sup> Supported only in GPIO mode.



#### 2.4.1.1.2. $R_T$ OCT

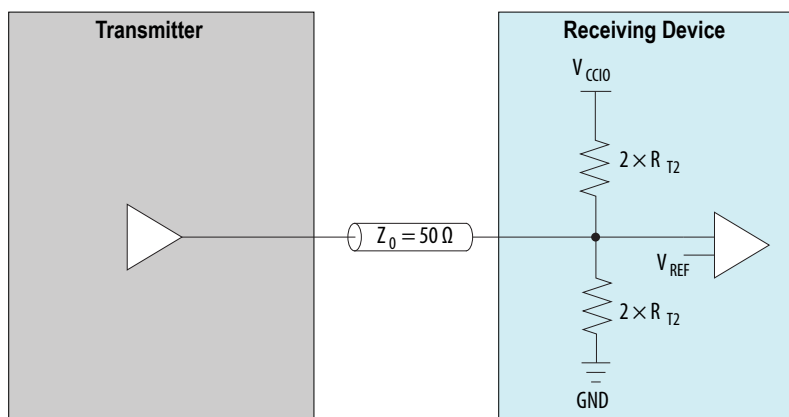
The Agilex 5 devices support  $R_T$  OCT with and without calibration.  $R_T$  OCT is available only for input and bidirectional pins. Output pins do not support  $R_T$  OCT.

You must disable  $R_T$  OCT for interfaces that require external termination circuitry near the receiver of the Agilex 5 device.

**Table 13.  $R_T$  OCT Schemes**

OCT Scheme	Description
$R_T$ OCT without calibration	<ul style="list-style-type: none"> <li>Available only on the input buffer.</li> <li>Receiver impedance matching provides the receiver with a controlled input impedance that closely matches the impedance of the transmission line.</li> </ul>
$R_T$ OCT with calibration	<ul style="list-style-type: none"> <li>The <math>R_T</math> OCT calibration circuit uses the impedance of the external resistor connected to the RZQ pin as a reference.</li> <li>During calibration, the circuit continuously alters the impedance of the I/O buffer until the value reaches the target impedance, which is a predetermined ratio to the reference resistance.</li> <li>The calibration occurs at the end of the device configuration. When the calibration circuit finds the correct impedance, the circuit stops changing the characteristics of the drivers.</li> <li>In EMIF and MIPI D-PHY modes, you may trigger recalibration during user mode.</li> </ul>

**Figure 11.  $R_T$  OCT with Calibration**



**Table 14. Selectable I/O Standards for  $R_T$  OCT with Calibration**

This table lists the output termination settings for calibrated OCT on different I/O standards. The default values are in **bold** font.

I/O Standard	$R_T$ OCT without Calibration <sup>(8)</sup> (Ω)	$R_T$ OCT with Calibration (Ω)
1.3 V LVCMOS	—	—
1.2 V LVCMOS	—	—
1.1 V LVCMOS	—	—
1.05 V LVCMOS	—	—
1.0 V LVCMOS	—	—
<i>continued...</i>		

<sup>(8)</sup> Supported only in GPIO mode.

I/O Standard	R <sub>T</sub> OCT without Calibration <sup>(8)</sup> (Ω)	R <sub>T</sub> OCT with Calibration (Ω)
SSTL-12	50	50, 60
HSTL-12	50	50, 60
HSUL-12	—	—
POD12	50	40, 50, 60
POD11	50	40, 50, 60
LVSTL11	50	40, 50, 60
LVSTL105	50	40, 50, 60
LVSTL700	—	40, 50, 60
Differential SSTL-12	50	50, 60
Differential HSTL-12	50	50, 60
Differential HSUL-12	—	—
Differential POD12	50	40, 50, 60
Differential POD11	50	40, 50, 60
Differential LVSTL11	50	40, 50, 60
Differential LVSTL105	50	40, 50, 60
Differential LVSTL700	—	40, 50, 60

### Related Information

OCT Features Assignment Names and Settings on page 32

#### 2.4.1.1.3. Dynamic OCT

Dynamic OCT is useful for terminating a high performance bidirectional path by optimizing signal integrity depending on data direction. Dynamic OCT reduces power usage because the termination switches on only during input operations.

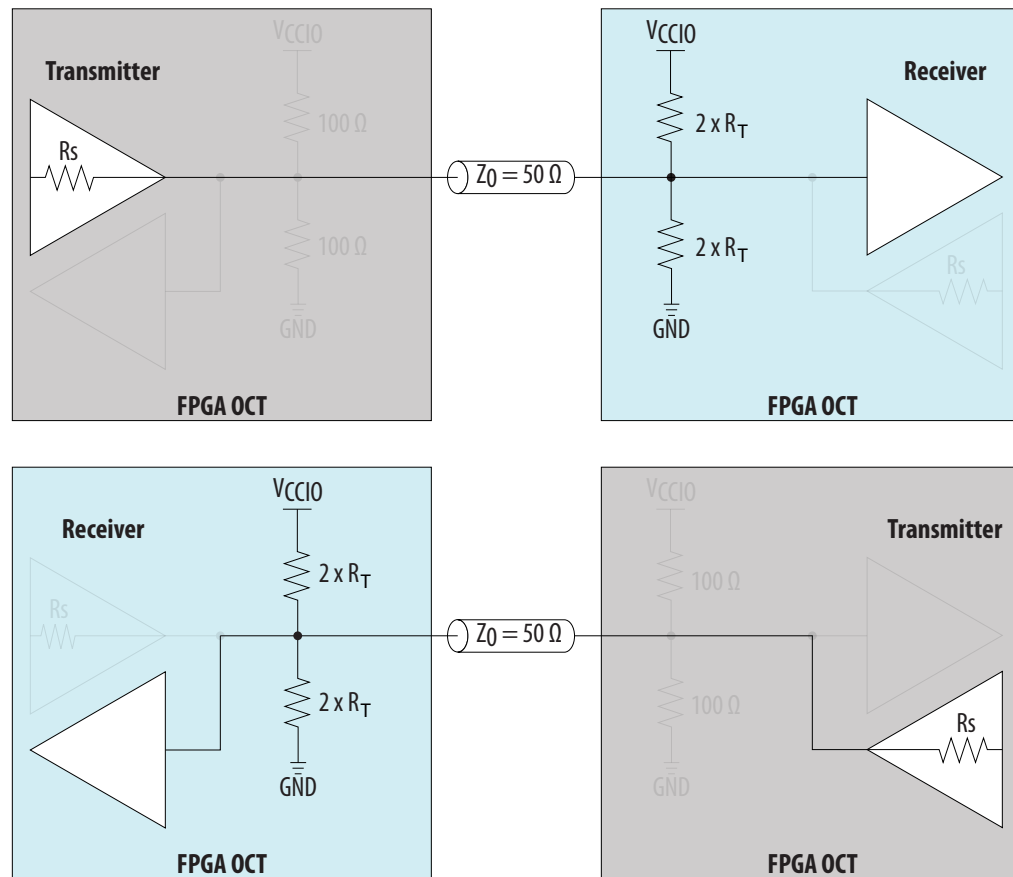
**Table 15. Dynamic OCT Based on Bidirectional I/O**

Dynamic R<sub>T</sub> OCT or R<sub>S</sub> OCT switches on or off based on whether the bidirectional I/O acts as a receiver or driver.

Dynamic OCT	Bidirectional I/O	State
Dynamic R <sub>T</sub> OCT	Receiver	On
	Driver	Off
Dynamic R <sub>S</sub> OCT	Receiver	Off
	Driver	On

<sup>(8)</sup> Supported only in GPIO mode.

Figure 12. Dynamic  $R_T$  OCT in Agilex 5 Devices



#### 2.4.1.2. OCT Calibration Block

You can calibrate the OCT using the OCT calibration block available in each HSIO bank. Only the 1.05 V, 1.1 V, and 1.2 V  $V_{CCIO\_PIO}$  banks can use the OCT calibration block.

The OCT calibration block can calibrate the I/O buffers located in the same HSIO banks only, except for DDR4 or DDR5 DIMM implementation. Examples:

- Non-DDR4 and non-DDR5 DIMM implementation—you can use the OCT calibration block in bank 2A to calibrate the I/O buffers in bank 2A only.
- DDR4 or DDR5 DIMM implementation that spans across banks 2A and 2B—you can use the OCT calibration block in either bank to calibrate the DDR4 or DDR5 DIMM I/O buffers in both banks.

The OCT calibration process uses the  $RZQ$  pin that is available in every HSIO sub-bank for series-calibrated and parallel-calibrated terminations.

- You can use the  $RZQ$  pin in one sub-bank to calibrate I/Os in the other sub-bank within the same HSIO bank. For example, you can use the  $RZQ$  pin in the bottom index sub-bank of bank 2B to calibrate the I/Os in the top index sub-bank of bank 2B. Both sub-bank must use the same  $V_{CCIO\_PIO}$  voltage value.
- The  $RZQ$  pin is a dual-purpose I/O pin and functions as a general-purpose I/O pin if you do not use the calibration circuit.
- The  $RZQ$  pin shares the same  $V_{CCIO\_PIO}$  supply voltage with the I/O sub-bank where the pin is located.

The OCT calibration block has an external 240  $\Omega$  reference resistor associated with it through the  $RZQ$  pin available in every sub-bank.

- Connect the  $RZQ$  pin to GND through an external 240  $\Omega$  resistor.
- For differential I/O standards, you must use the same  $RZQ$  resistor to calibrate both the positive and negative legs of the differential I/O pin.
- You can use each  $RZQ$  resistor to calibrate two  $R_S$  OCT settings and one  $R_T$  OCT setting for all I/O standards.

#### 2.4.1.3. Single-Ended I/O Standards External Termination

The SSTL, HSTL, POD, and LVSTL I/O standards require a termination voltage. The internally-generated reference voltage of the receiving device tracks the termination voltage of the transmitting device.

Altera recommends that you use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors required.

**Note:** You cannot use  $R_S$  and  $R_T$  OCT simultaneously. For more information, refer to the related information.

**Table 16. I/O Standards Required External Termination**

I/O Standard	External Termination Scheme
1.3 V LVCMOS	No on-board termination required
1.2 V LVCMOS	No on-board termination required
1.1 V LVCMOS	No on-board termination required
1.05 V LVCMOS	No on-board termination required
1.0 V LVCMOS	No on-board termination required
SSTL-12	Single-ended SSTL I/O standard termination
HSTL-12	Single-ended HSTL I/O standard termination
HSUL-12	No on-board termination required
POD12	Single-ended POD I/O standard termination
POD11	Single-ended POD I/O standard termination
LVSTL11	Single-ended LVSTL I/O standard termination
LVSTL105	Single-ended LVSTL I/O standard termination
continued...	

I/O Standard	External Termination Scheme
LVSTL700	Single-ended LVSTL I/O standard termination
Differential SSTL-12	Differential SSTL I/O standard termination
Differential HSTL-12	Differential HSTL I/O standard termination
Differential HSUL-12	No on-board termination required
Differential POD12	Differential POD I/O standard termination
Differential POD11	Differential POD I/O standard termination
Differential LVSTL11	Differential LVSTL I/O standard termination
Differential LVSTL105	Differential LVSTL I/O standard termination
Differential LVSTL700	Differential LVSTL I/O standard termination

**Figure 13. SSTL and HSTL I/O Standards External Termination**

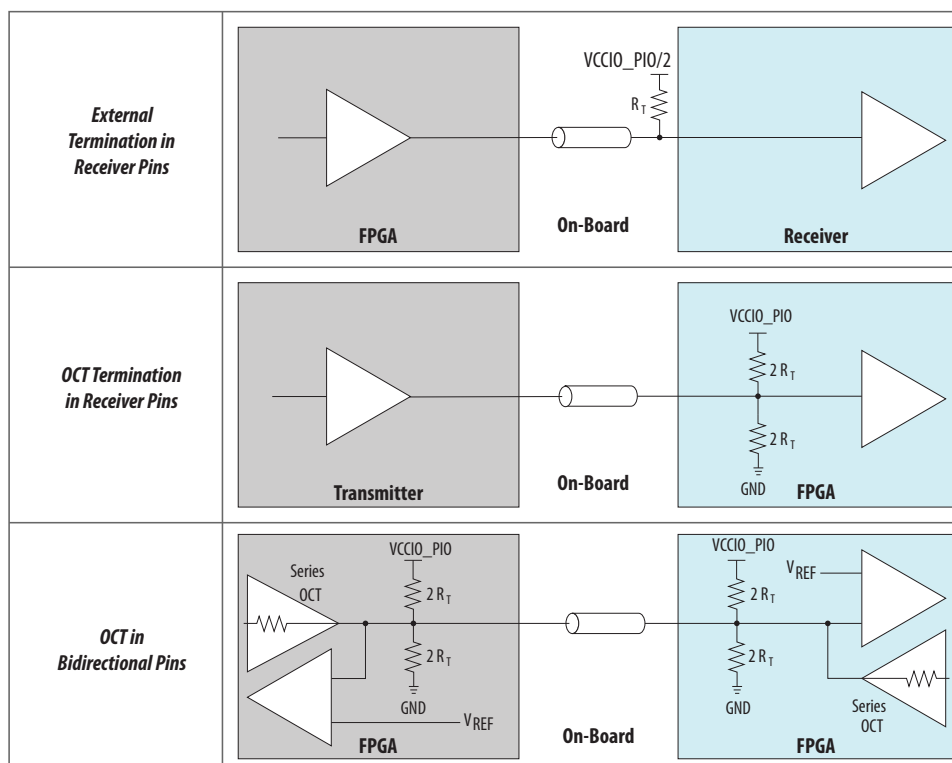


Figure 14. POD I/O Standards External Termination

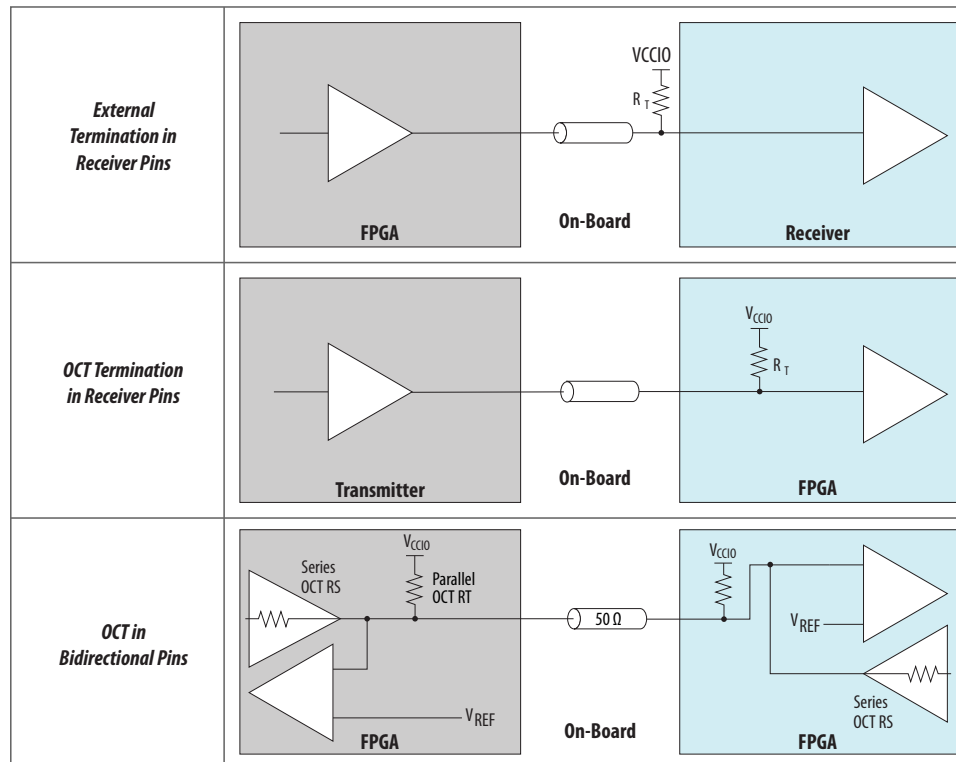
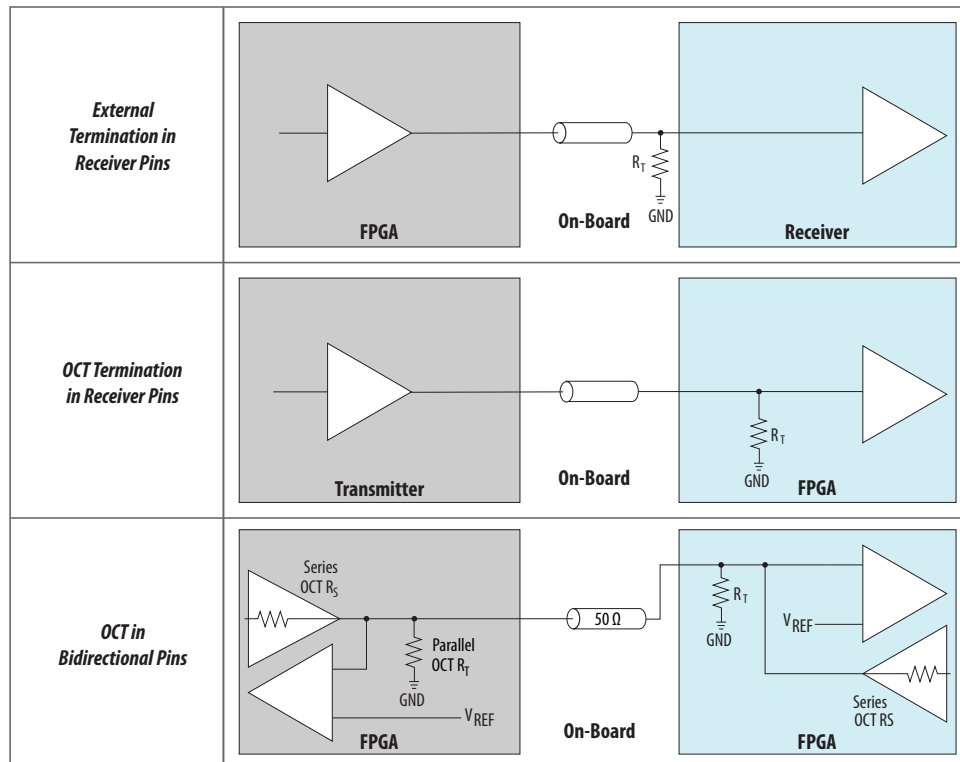


Figure 15. LVSTL I/O Standards External Termination



#### Related Information

Dynamic OCT on page 26

### 2.4.1.4. Single-Ended I/O Termination Implementation Guide

To implement I/O termination in your design, you can assign the termination for your pin using the Quartus Prime Assignment Editor or through the External Memory Interfaces IP and PHY Lite for Parallel Interfaces IP.

#### Related Information

Configuring OCT Using the Assignment Editor on page 31

#### 2.4.1.4.1. Configuring OCT Using the Assignment Editor

1. From the Quartus Prime menu, select **Assignments** ► **Assignment Editor**.
2. Under the **To** column, search for the pin that you want to configure.
3. Under the **Assignment Name** column, select a supported termination feature.
4. Under the **Value** column, select a supported value.
5. From the Quartus Prime menu, select **File** ► **Save**.

#### Related Information

Single-Ended I/O Termination Implementation Guide on page 31

#### 2.4.1.4.2. OCT Features Assignment Names and Settings

**Table 17. Agilex 5 FPGAs OCT Assignment Names and Settings**

OCT Feature	Assignment Name	Supported Values
$R_S$ with calibration	<b>Output Termination</b>	<ul style="list-style-type: none"> <li>Series 34 Ohm with Calibration</li> <li>Series 40 Ohm with Calibration</li> <li>Series 45 Ohm with Calibration</li> <li>Series 50 Ohm with Calibration</li> </ul>
$R_S$ without calibration	<b>Output Termination</b>	<ul style="list-style-type: none"> <li>Series 34 Ohm without Calibration</li> <li>Series 40 Ohm without Calibration</li> </ul>
$R_T$ with calibration	<b>Input Termination</b>	<ul style="list-style-type: none"> <li>Parallel 40 Ohm with Calibration</li> <li>Parallel 50 Ohm with Calibration</li> <li>Parallel 60 Ohm with Calibration</li> </ul>
$R_T$ without calibration	<b>Input Termination</b>	<ul style="list-style-type: none"> <li>Parallel 50 Ohm without Calibration</li> <li>Parallel 60 Ohm without Calibration</li> </ul>

#### Related Information

- [RS OCT](#) on page 22  
Lists the supported  $R_S$  OCT values for different I/O standards.
- [RT OCT](#) on page 25  
Lists the supported  $R_T$  OCT values for different I/O standards.

#### 2.4.2. True Differential Signaling I/O Termination in Agilex 5 Devices

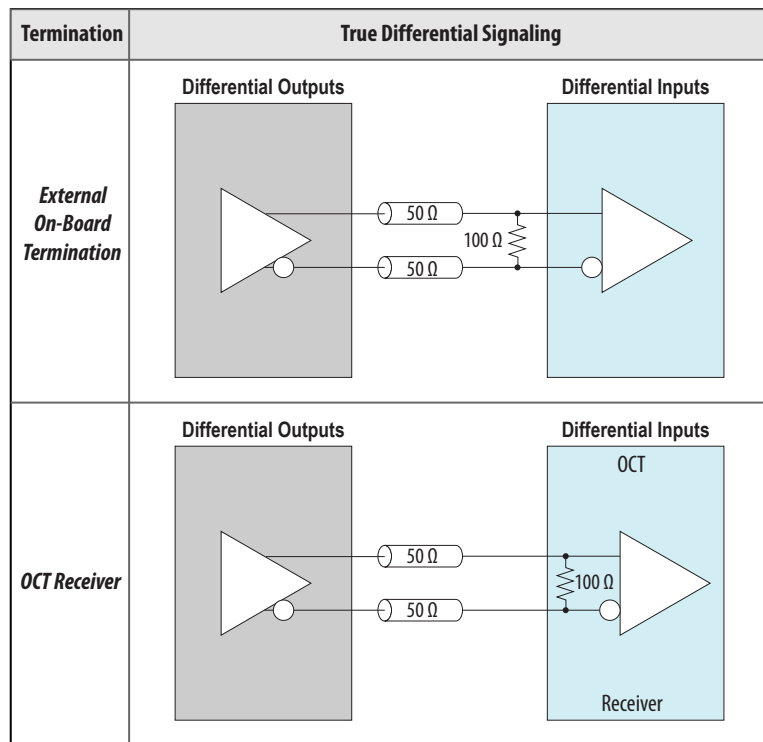
All HSIO banks have dedicated circuitry to support true differential I/O standards by using the True Differential Signaling, DPHY, or SLVS-400 differential buffers without resistor networks.

The True Differential Signaling buffer is compatible with the LVDS, RSDS, Mini-LVDS, and LVPECL standards. The True Differential Signaling, DPHY, and SLVS-400 buffers support 100  $\Omega$  differential on-chip termination ( $R_D$  OCT). If you use an SLVS-400 or DPHY receiver:

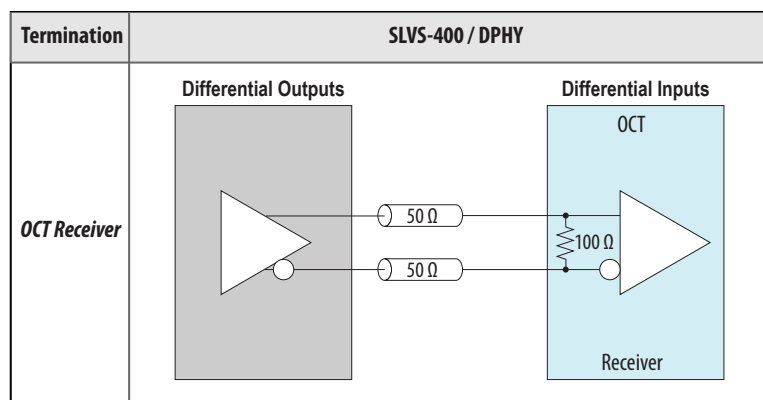
- The  $R_D$  OCT is calibrated and always enabled.
- You must connect a 240  $\Omega$  RZQ resistor



**Figure 16. True Differential Signaling I/O Standard Termination**



**Figure 17. SLVS-400 and DPHY I/O Standards Termination**



Use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors usage.

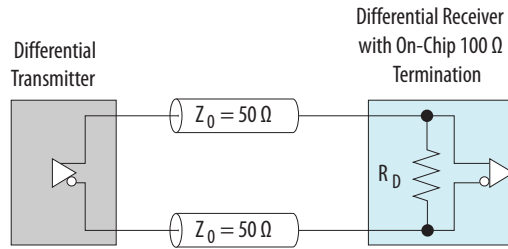
#### Related Information

- [Agilex 5 Device Pin-Out Files](#)  
Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.
- [AN 555: True Differential Signaling Termination and Biasing for Agilex 7 M-Series and Agilex 5 FPGAs](#)

### 2.4.2.1. True Differential Signaling I/O Standard On-Chip Termination

All I/O pins and dedicated clock input pins located in the HSIO banks of Agilex 5 devices support on-chip differential termination ( $R_D$  OCT). The Agilex 5 devices provide a  $100\ \Omega$  on-chip differential termination option on each differential receiver channel for the True Differential Signaling, DPHY, and SLVS-400 I/O standards.

**Figure 18. OCT for Differential I/O Termination**



#### 2.4.2.1.1. Configuring Differential Input $R_D$ OCT Using the Assignment Editor

**Table 18. Differential Input  $R_D$  OCT in Quartus Prime Assignment Editor Settings**

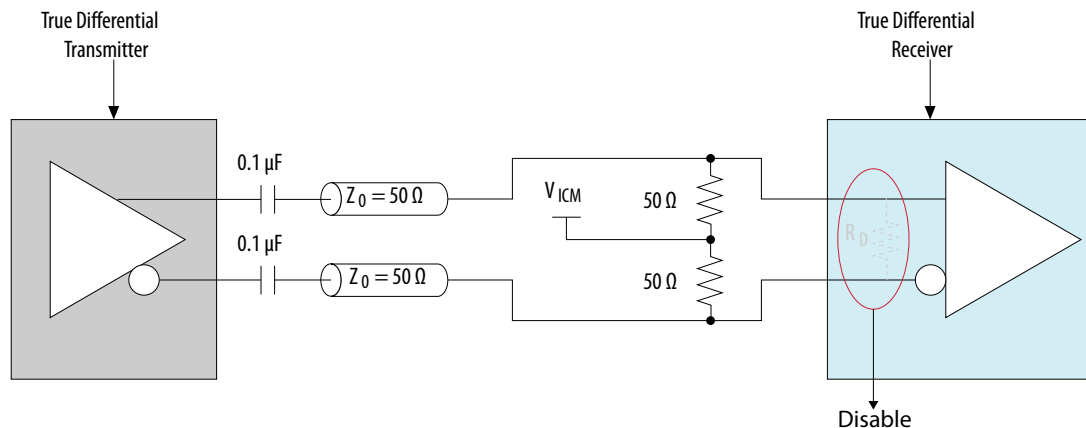
To	Assignment Name	Value
rx_in	Input Termination	Differential

1. From the Quartus Prime menu, select **Assignments > Assignment Editor**.
2. Under the **To** column, search for the input pin that you want to configure.
3. Under the **Assignment Name** column, select **Input Termination**.
4. Under the **Value** column, select **Differential**.
5. From the Quartus Prime menu, select **File > Save**.

#### 2.4.2.1.2. Guidelines: Differential Input $R_D$ OCT

Disable  $R_D$  OCT for interfaces that require external voltage bias circuitry near the true differential receivers of Agilex 5 devices.

**Figure 19. External Voltage Bias Circuitry with  $R_D$  OCT Disabled**



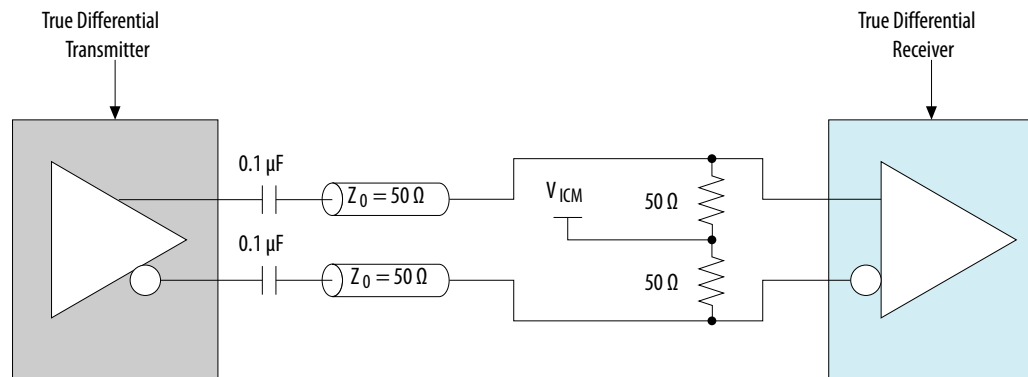
### 2.4.2.2. True Differential Signaling I/O Standard External Termination

Analyze the electrical specification requirement of the LVDS interface and ensure the common-mode voltage for your LVDS data rate conforms to the data sheet specification.

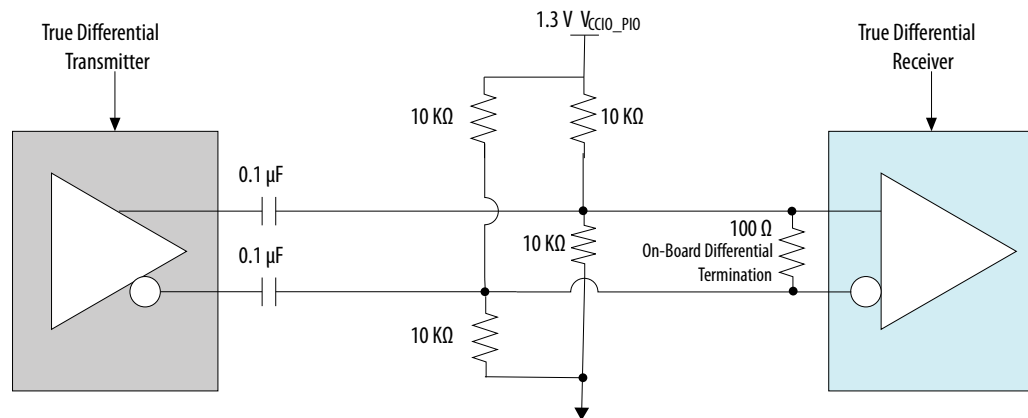
- Use AC coupling and external voltage bias circuitry if the common-mode voltage of the output buffer does not match the differential receiver input common-mode voltage.
- Consider using a dedicated  $V_{ICM}$  voltage supply for wide LVDS interfaces that share a common  $V_{ICM}$  reference voltage.

**Note:** Altera recommends that you use SPICE or IBIS models to verify your AC- or DC-coupled termination.

**Figure 20. Example of AC-Coupled External  $V_{ICM}$  Termination**



**Figure 21. Example of AC-Coupled External Termination for 1.3 V  $V_{CCIO\_PIO}$**



#### Related Information

- [HSIO Differential I/O Standards Specifications, Agilex 5 FPGAs and SoCs Device Data Sheet](#)  
Provides the  $V_{ICM}$  specifications for the True Differential Signaling I/O standard.
- [AN 555: True Differential Signaling Termination and Biasing for Agilex 7 M-Series and Agilex 5 FPGAs](#)

## 2.5. HSIO Design Guidelines

Different functions of the HSIO pins have different guidelines, placement restrictions, connection requirements, and clocking requirements.

### Related Information

[Pin Connection Guidelines: Agilex 5 FPGAs and SoCs](#)

Provides more information about each pin function.

### 2.5.1. I/O Standard Placement Restrictions for True Differential I/Os

Adhere to these placement guidelines for the true differential I/Os.

- Do not place LVSTL, SLVS-400, or DPHY I/O standard in the same I/O lane as the True Differential Signaling I/O standard.
- You can place True Differential Signaling I/O standard in the same I/O lane as LVSTL I/O standard only if you use the True Differential Signaling input as a reference clock.
- If you use the SLVS-400, DPHY, or 1.05 V, 1.1 V, or 1.2 V True Differential Signaling I/O standard, you can place only the LVCMOS I/O standard in the same I/O lane.

### 2.5.2. Placement Restrictions for True Differential and Single-Ended I/O Standards in the Same or Adjacent HSIO Bank

If you use true differential I/O standards and single-ended I/O standards in the same or adjacent HSIO banks, adhere to the following placement guidelines.

- Do not place true differential and toggling single-ended I/O standards in the combinations of locations listed in the following tables.
- The Quartus Prime software issues the following error messages:
  - Compilation error—violation of the same bank placement restriction.
  - Critical warning—assignment of true differential I/O standards to pin pairs with the following pin index numbers: 0 and 1, 6 and 7, 88 and 89, and 94 and 95.

From Quartus Prime software version 25.1.1 onwards, you can place true differential and single-ended I/O standards in the combinations of locations listed in the following table for the two scenarios listed below:

- The receiver equalization calibration is enabled for the affected true differential input buffers.
- The single-ended I/O is a non-toggling pin. You must use the following .qsf in your Quartus design to exclude the non-toggling pins in the Quartus Prime placement rules check:

```
set_instance_assignment -name TOGGLE_SPEED TOGGLE_SPEED_SLOW -to <pin name>
```

For example:

```
set_instance_assignment -name TOGGLE_SPEED TOGGLE_SPEED_SLOW -to din
```

**Table 19. Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in the Same HSIO Bank**

This table lists the combinations of pins and I/O standards not allowed in the same HSIO bank. Examples:

- If you place a true differential I/O standard in pin pair 10 and 11, do not place single-ended I/O standards in pins 8 or 19.
- If you place a single-ended I/O standard in pin 57 or 67, do not place a true differential I/O standard in pin pair 58 and 59.

Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)	
True Differential Pin Pair	Single-Ended Pin	True Differential Pin Pair	Single-Ended Pin	True Differential Pin Pair	Single-Ended Pin	True Differential Pin Pair	Single-Ended Pin
0 and 1	3, 4	24 and 25	27, 28	48 and 49	51, 52	72 and 73	75, 76
2 and 3	0	26 and 27	16, 24	50 and 51	40, 48	74 and 75	64, 72
4 and 5	1, 15	28 and 29	25, 39	52 and 53	49, 63	76 and 77	73, 87
6 and 7	9	30 and 31	22, 32	54 and 55	46, 56	78 and 79	70, 80
8 and 9	6, 11	32 and 33	31, 34	56 and 57	55, 58	80 and 81	79, 82
10 and 11	8, 19	34 and 35	33, 43	58 and 59	57, 67	82 and 83	81, 90
12 and 13	14, 17	36 and 37	38, 41	60 and 61	62, 65	84 and 85	86, 89
14 and 15	5, 12	38 and 39	29, 36	62 and 63	53, 60	86 and 87	77, 84
16 and 17	13, 26	40 and 41	37, 50	64 and 65	61, 74	88 and 89	85
18 and 19	10, 21	42 and 43	35, 45	66 and 67	59, 69	90 and 91	83, 92
20 and 21	18, 23	44 and 45	42, 47	68 and 69	66, 71	92 and 93	91, 94
22 and 23	20, 30	46 and 47	44, 54	70 and 71	68, 78	94 and 95	93

**Table 20. Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in Adjacent HSIO Banks**

This table lists the combinations of pins and I/O standards not allowed in adjacent HSIO banks. Examples:

- If you place a true differential I/O standard in pin pair 6 and 7 of bank 3B, do not place single-ended I/O standards in pin 95 of bank 3A.
- If you place a single-ended I/O standard in pin 2 of bank 2B, do not place a true differential I/O standard in pin pair 88 and 89 of bank 2A.

Combinations Not Allowed (Pin Index Number)				Combinations Not Allowed (Pin Index Number)			
True Differential		Single-Ended		True Differential		Single-Ended	
Bank	Pin Pair	Bank	Pin	Bank	Pin Pair	Bank	Pin
3A	88 and 89	3B	2	2A	88 and 89	2B	2
	94 and 95		7		94 and 95		7
3B	2 and 3	3A	88	2B	2 and 3	2A	88
	6 and 7		95		6 and 7		95

Refer to the related information for the figure showing the locations of the HSIO banks.

### Related Information

- [Agilex 5 Device Pin-Out Files](#)  
Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.
- [Agilex 5 HSIO Banks](#) on page 9

## 2.5.3. $V_{REF}$ Sources and Input Standards Grouping

Consider these  $V_{REF}$  sources guidelines.

Agilex 5 devices support internal  $V_{REF}$  sources. Each I/O lane in the bank also has its own internal  $V_{REF}$  generator. You can configure  $V_{REF}$  generator in the External Memory Interfaces IP and PHY Lite for Parallel Interfaces IP.

In each I/O lane, adhere to the input standards grouping to ensure all input pins in the I/O lane use the same internal  $V_{REF}$  source. If the mix of input standards in an I/O lane does not adhere to these groupings, Quartus Prime displays error messages during design compilation.

**Note:** Although the following table lists the groups based on  $V_{REF}$ , the final rules depend on implementation. For example, the PHY Lite interface uses one I/O standard per I/O lane. If you use HSTL-12 and SSTL-12 with the PHY Lite for Parallel Interfaces IP, assign each I/O standard in a different I/O lane.

**Table 21. Input Standards Groups Per I/O Lane**

Group	Input Standards Mix within I/O Lane
Group 1	<ul style="list-style-type: none"> <li>• POD12</li> <li>• 1.2 V True Differential Signaling</li> <li>• 1.2 V LVCMOS</li> <li>• Differential POD12</li> </ul>
Group 2	<ul style="list-style-type: none"> <li>• POD11</li> <li>• 1.1 V True Differential Signaling</li> <li>• 1.1 V LVCMOS</li> <li>• Differential POD11</li> </ul>
Group 3	<ul style="list-style-type: none"> <li>• SSTL-12</li> <li>• HSTL-12</li> <li>• HSUL-12</li> <li>• 1.2 V True Differential Signaling</li> <li>• 1.2 V LVCMOS</li> <li>• Differential SSTL-12</li> <li>• Differential HSTL-12</li> <li>• Differential HSUL-12</li> </ul>
Group 4	<ul style="list-style-type: none"> <li>• LVSTL11</li> <li>• 1.1 V LVCMOS</li> <li>• Differential LVSTL11</li> </ul>
Group 5	<ul style="list-style-type: none"> <li>• LVSTL105</li> <li>• LVSTL700</li> <li>• 1.05 V LVCMOS</li> <li>• Differential LVSTL105</li> <li>• Differential LVSTL700</li> </ul>

### Related Information

[I/O Standard Selection and I/O Bank Supply Compatibility Check](#) on page 40

## 2.5.4. HSIO Pin Restrictions for External Memory Interfaces

In specific external memory interface implementations, some HSIO pins are not usable. For details, refer to the External Memory Interfaces (EMIF) IP User Guide: Agilex 5 FPGAs and SoCs.

## 2.5.5. RZQ Pin Requirement

There is one RZQ pin per I/O sub-bank. The RZQ pins are dual-purpose pins, and can be used as GPIO if you do not use OCT calibration.

Adhere to the following guidelines if you use the RZQ pin:

- To use the RZQ pins for OCT calibration, connect a 240  $\Omega$  precision resistor with a  $\pm 1\%$  tolerance to the pins.
- You cannot place the RZQ pin in an I/O lane with any input standard except LVCMOS or True Differential Signaling input buffer.

## 2.5.6. I/O Standards Implementation Based on $V_{CCIO\_PIO}$ Voltages

The following guidelines apply to I/O standards based on the  $V_{CCIO\_PIO}$  voltages.

### 1.2 V, 1.1 V, or 1.05 V $V_{CCIO\_PIO}$

If you use a 1.2 V, 1.1 V, or 1.05 V  $V_{CCIO\_PIO}$ , you can implement single-ended non-voltage referenced and voltage-referenced I/O standards. The 1.2 V, 1.1 V, or 1.05 V buffer also supports differential voltage-referenced I/O and true differential input standards.

You can implement a mix of both voltage-referenced and non-voltage referenced I/O, and true differential input standards within the I/O bank if all the I/O standards support the  $V_{CCIO\_PIO}$  of the I/O bank.

### 1.3 V $V_{CCIO\_PIO}$

If you use a 1.3 V  $V_{CCIO\_PIO}$  voltage, you can implement both 1.3 V LVCMOS and True Differential Signaling I/O standards in the same I/O lane and sub-bank. The buffer can interface with upstream or downstream devices that are compatible with the Agilex 5 FPGAs electrical specifications.

If you use True Differential Signaling input, analyze the electrical specification requirement to implement your true differential receiver.

Implement DC coupling if the signal swing and  $V_{ICM}$  voltage requirement are within the Agilex 5 True Differential Signaling standard specification. Otherwise, implement AC coupling and external bias circuitry.

### Related Information

[I/O Standards Specifications, Agilex 5 FPGAs and SoCs Device Data Sheet](#)

Provides the electrical specifications for the supported I/O standards.

### 2.5.7. I/O Standard Selection and I/O Bank Supply Compatibility Check

- Select a suitable signaling type and I/O standard for each I/O pin. The I/O banks are located in rows along the top periphery and bottom periphery of the device. Each I/O bank has two sub-banks. Each sub-bank has its own PLL, DPA and SERDES circuitries, and individual  $V_{CCIO\_PIO}$  voltage rail.
- Ensure that the selected I/O standard is supported in the targeted I/O sub-bank.
- Place I/O pins that share the same  $V_{CCIO\_PIO}$  voltage levels in the same I/O sub-bank.
- Verify that all output signals in each I/O sub-bank are intended to drive out at the sub-bank's I/O voltage level.
- Verify that all voltage-referenced signals in each I/O lane are intended to use the same  $V_{REF}$  source by adhering to the voltage-referenced input standards grouping per I/O lane.

#### Related Information

[VREF Sources and Input Standards Grouping](#) on page 38

### 2.5.8. Simultaneous Switching Noise

Considering simultaneous switching noise (SSN) impact on the design, use differential I/O standards and lower voltage I/O standards for high-switching I/O pins. Place clock signals, RZQ pins, and asynchronous control signals near ground signals and away from large switching buses.

### 2.5.9. HPS Shared I/O Requirements

The HPS external memory interface uses I/O pins located in the HSIO bank instead of the HPS I/O bank. The  $V_{CCIO\_PIO}$  powers the HSIO bank instead of the 1.8 V  $V_{CCIO\_HPS}$ . For the location of the HPS shared HSIO pins, refer to device pin-out files.

#### Related Information

[Agilex 5 Device Pin-Out Files](#)

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

### 2.5.10. Clocking Requirements

In your clocking scheme, use the dedicated clock pins for I/O PLL reference clock or as output clock for better jitter performance.

You must use the True Differential Signaling input standard for the I/O PLL reference clock.

### 2.5.11. Clock Restrictions for GPIO Interfaces

Adhere to these clock sharing guidelines when designing with multiple TX or multiple RX registers in the same I/O lane.



- When placing multiple TX or multiple RX SDR registers in the same I/O lane, you must use the same reference clock to drive these TX or RX registers. This rule applies when the register packing option is enabled in your FPGA design.
- When placing multiple TX or multiple RX DDIO registers in the same I/O lane, you must use the same reference clock to drive these registers.

### 2.5.12. SDM Shared I/O Requirements

The Avalon® streaming interface ×16 configuration modes use the configuration pins located in an HSIO bank for device configuration. The V<sub>CCIO\_PIO</sub> voltage rail, instead of the V<sub>CCIO\_SDM</sub> voltage rail, powers the HSIO bank.

When you use Avalon streaming interface ×16 configuration scheme, Avalon streaming interface pins in the SDM shared IO bank are not usable as user I/Os for:

- Designs that use external partial reconfiguration, for example, designs that send partial reconfiguration bitstream using Avalon streaming interface pins.
- Designs that use the HPS.

#### Related Information

[Agilex 5 Configuration Pins, Device Configuration User Guide: Agilex 5 FPGAs and SoCs](#)

Provides more details about the I/O setting and restrictions on the pins during device configuration.

### 2.5.13. Unused Pins

Unused I/O pins are configured as input tri-stated with no weak pull-up. If the entire HSIO bank is unused, you may leave these pins floating, connected to V<sub>CCIO\_PIO</sub>, or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.

#### Related Information

[Agilex 5 Device Pin-Out Files](#)

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

### 2.5.14. V<sub>CCIO\_PIO</sub> Supply for Unused HSIO Banks

When the entire HSIO bank is unused, you may connect the V<sub>CCIO\_PIO</sub> pin of the unused HSIO bank to 0 V, 1.0 V, 1.05 V, 1.1 V, 1.2 V, or 1.3 V.

If only one of the sub-banks within the same HSIO bank is unused, you must connect the V<sub>CCIO\_PIO</sub> pin of the unused sub-bank to the same V<sub>CCIO\_PIO</sub> voltage level as the other actively utilized sub-bank. You must use following .qsf to assign the V<sub>CCIO\_PIO</sub> of the unused sub-bank to the intended voltage supply value.

```
set_global_assignment -name IOBANK_VCCIO <voltage supply> -section_id  
<sub_bank_name>
```

Example:

```
set_global_assignment -name IOBANK_VCCIO 1.1V -section_id 3B_B
```

### 2.5.15. HSIO Pins During Power Sequencing

Agilex 5 devices do not support hot-socketing and require a specific power sequence. Design your power supply solution to properly control the complete power sequence.

Adhere to the these guidelines to prevent unnecessary current draw on the I/O pins located in the HSIO banks. These guidelines apply for unpowered, power up to power-on reset (POR), POR delay, POR delay to configuration, configuration, initialization, user mode, and power down device states.

- The I/O pins in the HSIO banks can be tri-stated, driven to ground, or driven to the  $V_{CCIO\_PIO}$  level.
- While the device is powering up or down:
  - The input signals of an I/O pin, at all times, must not exceed the I/O buffer power supply rail of the bank where the I/O pin resides.
  - If you use a pin in a HSIO bank with 1.3 V  $V_{CCIO\_PIO}$ , the pin voltage must not exceed the  $V_{CCIO\_PIO}$  rail or 1.2 V, whichever is lower.
- While the device is powering up or powering down, the HSIO pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per HSIO bank.
- While the device is not turned on, tri-state the I/O pin and do not drive the pin with any external voltage.
- After the device fully powers up, the voltage levels for the HSIO pins must not exceed the DC input voltage ( $V_I$ ) value or the AC maximum allowed overshoot during transitions.

**Table 22. Guideline Examples**

Condition	Guideline
The $V_{CCIO\_PIO}$ pin ramps up and at period X, the $V_{CCIO\_PIO}$ voltage is 1.1 V.	At period X, keep the signals driven by the device connected to the HSIO I/O pin at a voltage of 1.1 V or lower.
The 1.3 V $V_{CCIO\_PIO}$ pin ramps up and the voltage continues to rise pass the 1.2 V level.	Keep the HSIO pin voltage at 1.2 V or lower until the device fully powers up.

### 2.5.16. Drive Strength Requirement for HSIO Input Pins

Each HSIO input pin with programmable pull-up feature turned on requires 1 mA of drive strength. The connected output buffer must provide a minimum of 1 mA to the pin.

If an output buffer drives two input pins, the output buffer must provide 2 mA to the input pins. Increase the drive strength current according to the number of input pins the output buffer drives.

If you connect an output buffer to multiple input pins and one of the input pins has programmable pull-up feature enabled, you must turn on the same programmable feature on all of the other input pins.

## 2.5.17. Maximum DC Current Restrictions

While using Agilex 5 HSIO pins, adhere to the maximum allowed duration of the per pin DC current limit.

**Table 23. Maximum Allowed Duration of DC Current Limit**

DC Current Limit	Maximum Allowed Duration (%)
$\pm 7.5$ mA	100%
$\pm 10$ mA	75%
$\pm 15$ mA	50%
More than $\pm 15$ mA	Not allowed

### Related Information

- [Absolute Maximum Ratings, Agilex 5 FPGAs and SoCs Device Data Sheet](#)  
Lists the absolute maximum ratings for DC output current.
- [DC Characteristics, Agilex 5 FPGAs and SoCs Device Data Sheet](#)  
Provides more information related to DC current specifications.

## 2.5.18. 1.05 V, 1.1 V, or 1.2 V I/O Interface Voltage Level Compatibility

Evaluate the electrical signal level compatibility between Agilex 5 1.05 V, 1.1 V, or 1.2 V output and the downstream device. Ensure that the  $V_{OH}$  and  $V_{OL}$  voltages of the 1.05 V, 1.1 V, or 1.2 V output buffer conform to the  $V_{IH}$  and  $V_{IL}$  specifications of the receiving buffer of the downstream device.

### Example 1. 1.2 V LVCMOS I/O Standard Voltage Swing Calculation

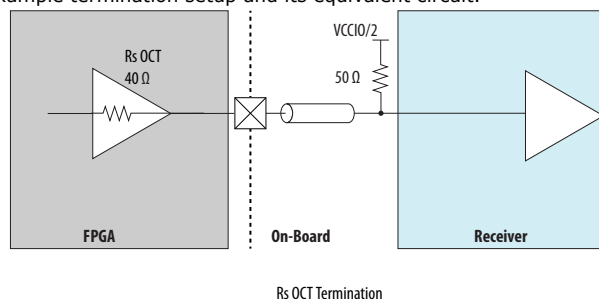
If you use the 1.2 V LVCMOS I/O standard, the output signal swings from 0 V to 1.2 V on a lossless transmission line with no external pull-up or pull-down component. Ensure that the  $V_{IH}$  or  $V_{IL}$  tolerance of the downstream connecting device can meet those conditions.

### Example 2. 1.2 V Voltage-Referenced I/O Standards Voltage Swing Calculation

If you use the 1.2 V voltage-referenced I/O standards, the output signal swing has a dependency on the external board termination or the internal termination of the receiver.

**Figure 22. Termination Setup Using 40  $\Omega$   $R_S$  OCT Driver with On-Board 50  $\Omega$  Pull-Up Resistor to  $V_{CCIO\_PIO}/2$**

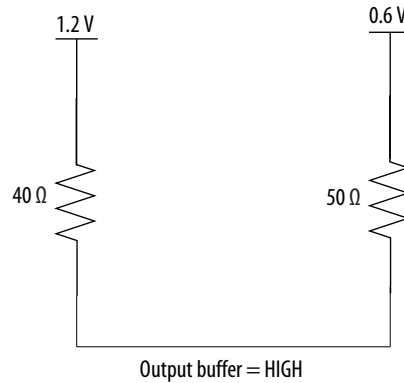
This figure shows an example termination setup and its equivalent circuit.



**Figure 23. Equivalent Circuit of the Example with Output Buffer Driving HIGH**

When the output buffer is driving HIGH, the pin voltage is 0.93 V based on voltage divider rule:

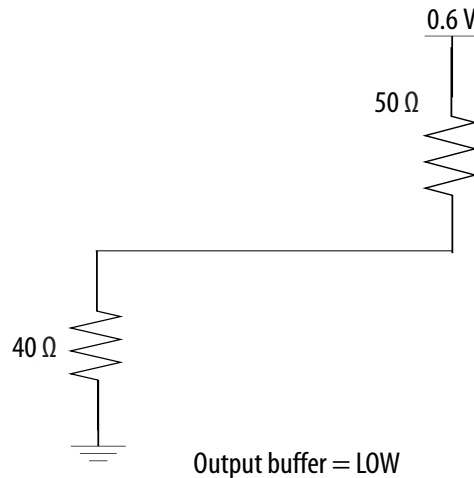
$$\left( \frac{1.2 \text{ V} - \text{Pin Voltage}}{40} = \frac{\text{Pin Voltage} - 0.6 \text{ V}}{50} \right).$$



**Figure 24. Equivalent Circuit of the Example with Output Buffer Driving LOW**

When the output buffer is driving LOW, the pin voltage is 0.27 V based on the voltage divider rule:

$$\left( \frac{0.6 \text{ V} - \text{Pin Voltage}}{50} = \frac{\text{Pin Voltage}}{40} \right).$$



### 2.5.19. Connection to True Differential Signaling Input Buffers During Device Reconfiguration

You can reconfigure Agilex 5 FPGAs at any time during user mode. Follow these guidelines for connection from an external device driving the True Differential Signaling input buffer during reconfiguration of Agilex 5 FPGAs.

**Table 24. True Differential Signaling Input Buffer Reconfiguration Guidelines**

True Differential Signaling Input Buffer Mode After Reconfiguration	External Connection Guidelines
Same mode as before FPGA reconfiguration	The external device can continue to drive the True Differential Signaling input buffer during reconfiguration of the FPGA.
Different mode after FPGA reconfiguration	<ul style="list-style-type: none"> <li>Before you start reconfiguration of the FPGA, ensure that the external device tri-states the connection.</li> <li>The external device can initiate a new connection to the True Differential Signaling input buffer after successful reconfiguration of the FPGA.</li> </ul>

## 2.5.20. LVSTL700 I/O Standards Differential Pin Pair Requirements

If you assign single-ended LVSTL700 I/O standard to the I/O buffer, assign LVSTL700, LVSTL11, or LVSTL105 I/O standard to the remaining leg of the I/O buffer pin pair. If the remaining positive or negative leg is unused, reserve the leg as an unused pin.

For example, if you assign the LVSTL700 I/O standard to pin function `DIFF2B_T_1P`, you must assign pin function `DIFF2B_T_1N` with LVSTL700, LVSTL11, or LVSTL105 I/O standard, or leave the pin as "unused".

### Related Information

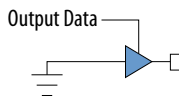
#### Agilex 5 Device Pin-Out Files

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

## 2.5.21. Implementing a Pseudo Open Drain

Apply this method to implement a pseudo open drain for Agilex 5 devices using the LVCMOS I/O standard.

**Figure 25. Pseudo Open Drain Connection**



1. Use the GPIO IP to initiate an output or bidirectional buffer with the OE turned on.
2. Connect the input port of the output buffer to the ground.
3. Connect the actual data signal to the OE port.

**Note:** Drive the buffer `LOW` before you switch the OE signal. When you switch the OE signal to `HIGH`, the output pin drives `LOW`. When you switch the OE signal to `LOW`, the output pin is tri-stated. You need an external pull-up circuitry to pull the connection to `HIGH`.

## 2.5.22. Allowed Duration for Using $R_T$ OCT

When you use  $R_T$  OCT, adhere to the maximum allowed duration for enabling the  $R_T$  OCT based on pin utilization per I/O bank.

This guideline applies to the following I/O standard when operating in GPIO or PHY Lite modes:

- SSTL-12 and Differential SSTL-12
- HSTL-12 and Differential HSTL-12
- HSUL-12 and Differential HSUL-12

**Table 25. Maximum Allowed  $R_T$  OCT Duration**

Number of Pins In Use Per I/O Bank (With $R_T$ OCT Turned On)	Maximum Allowed $R_T$ OCT Duration (%)
32	100
38	90
48	80
58	70
96	60

### 2.5.23. Single-Ended Strobe Signal Differential Pin Pair Restriction

If you use single-ended external memory interface or PHY Lite strobe signal, such as DQS, leave the remaining positive or negative leg of the differential pin pair as an unused pin.

For example, if you assign a single-ended external memory interface strobe signal to pin function DIFF2B\_T\_1P, ensure that the other leg of the pair, pin function DIFF2B\_T\_1N, is left unused.

#### Related Information

##### Agilex 5 Device Pin-Out Files

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

### 2.5.24. Implementing SLVS-400 or DPHY I/O Standard with 1.1 V $V_{CCIO\_PIO}$

If you use the SLVS-400 or DPHY I/O standard, Quartus Prime sets a default 1.2 V  $V_{CCIO\_PIO}$  to the sub-bank. To use SLVS-400 or DPHY at 1.1 V, set the sub-bank's  $V_{CCIO\_PIO}$  to 1.1 V through the Quartus Prime settings file (.qsf).

```
set_global_assignment -name IOBANK_VCCIO 1.1V -section_id <sub_bank_name>
```

Example: `set_global_assignment -name IOBANK_VCCIO 1.1V -section_id 3B_B`

## 2.6. HSIO Simulation

Altera provides several types of simulation models for Agilex 5 devices.

These simulation models are:

- Synopsys\* HSPICE\* models
- IBIS models
- IBIS AMI models

**Table 26. Simulation Models Descriptions**

Model	Supported I/O Type	Description
HSPICE	HSIO	<ul style="list-style-type: none"> <li>• Simulates actual transistor level design to obtain precise electrical simulation.</li> <li>• The syntax describes I/O buffers, board components and connections, and specific simulation parameters.</li> <li>• The model contains encrypted transistor and logic cell library models, output buffer circuit models for single-ended and differential I/Os, and sample SPICE decks for single-ended and differential I/Os.</li> <li>• The model requires a longer simulation time compared to the IBIS model.</li> </ul>
IBIS	HSIO	<ul style="list-style-type: none"> <li>• This is a behavioral model of the I/O buffers based on the I/V curve data derived from the HSPICE simulation.</li> <li>• The pre-emphasis feature is an example that can use the IBIS simulation model.</li> <li>• This model has a shorter simulation time compared to HSPICE.</li> <li>• The simulation model has less complexity compared to HSPICE models and supported by many simulation tools.</li> </ul>
IBIS AMI	Transceiver I/O	<ul style="list-style-type: none"> <li>• Algorithmic Modeling Interface (IBIS AMI) is a part of IBIS 5.0 specification for high-speed transmitter and receiver models that are supplied as executables in tools that support IBIS simulation.</li> <li>• This is an industry standard model methodology for high-speed link simulation applied to multi gigabit serial link channels.</li> <li>• This simulation model allows simulation of millions of bits in minutes, crosstalk and jitter analysis, detect data pattern dependencies, and able to model complex blocks such as equalization and CDR.</li> </ul>

### 2.6.1. IBIS Models—HSIO Support

You can use the Agilex 5 IBIS model to perform system-level simulations for various I/O configurations across three predefined process, voltage, and temperature settings.

The Agilex 5 IBIS model kit contains the following information:

- IBIS model file (.ibs)
- User guide that describes the model usage
- Model list sheet that lists the supported I/O feature for each model
- Package RLC report that provides the lumped package RLC values for each supported Agilex 5 variant

You can use the Agilex 5 IBIS model to simulate all valid I/O features configurations across all supported I/O standards:

- Slew rate
- Weak pull-up
- De-emphasis
- Pre-emphasis
- Differential output voltage

### Related Information

[IBIS Models for Intel® FPGA Devices](#)

## 2.6.2. IBIS-AMI Models

You can use the Agilex 5 IBIS AMI models to perform system-level simulations for DDR5 and LPDDR5 interfaces across three predefined process, voltage, and temperature settings.

## 2.6.3. HSPICE Models

You can use the Agilex 5 SPICE model to perform system-level simulations for various configurations. The SPICE kits provide models that support a wide variety of I/O features across process, voltage, and temperature (PVT)

Each SPICE kit contains the following items:

- Encrypted transistor and logic cell library models
- Encrypted input or output buffer circuit models for single-ended and differential I/Os
- Single-ended and differential sample SPICE decks
- User guide that describes the model usage

The HSPICE models provide options to simulate buffer behavior for the following I/O features:

- $R_S$  OCT with and without calibration
- $R_T$  OCT with calibration

### Related Information

[Accessing HSPICE Simulation Kits, Quartus Prime Pro Edition User Guide: PCB Design Tools](#)

## 2.6.4. Net Length Reports

The net length information consists of the package trace delay from the die pad to the package pin. Each pin in an FPGA package has its own net length information. This information is important for you to perform board trace compensation to optimize the channel-to-channel skew on your board design.

### Related Information

[Agilex 5 Device Package Net Length Report](#)

Downloads the net length reports for Agilex 5 devices.





## 3. Agilex 5 HVIO Banks

---

The HVIO banks are available in all Agilex 5 devices.

The HVIO banks provide single-ended I/O buffers that support 1.8 V, 2.5 V, or 3.3 V I/O voltages. You must assign all I/Os within one HVIO bank with the same I/O standard.

### Related Information

- [Types of I/O Banks](#) on page 8
- [Device Migration Guidelines: Agilex 5 FPGAs and SoCs E-Series](#)

### 3.1. HVIO Bank Overview

Each HVIO block contains two banks with 20 single-ended I/O pins in each bank.

*Note:* Bank 6D in the Agilex 5 B23B device package contains only 19 single-ended I/O pins.

Additionally, each HVIO block also contains dedicated fabric-feeding PLL.

The total number of HVIO banks varies across different device packages. Refer to the device pin-out files for the HVIO banks availability and locations in each device package.

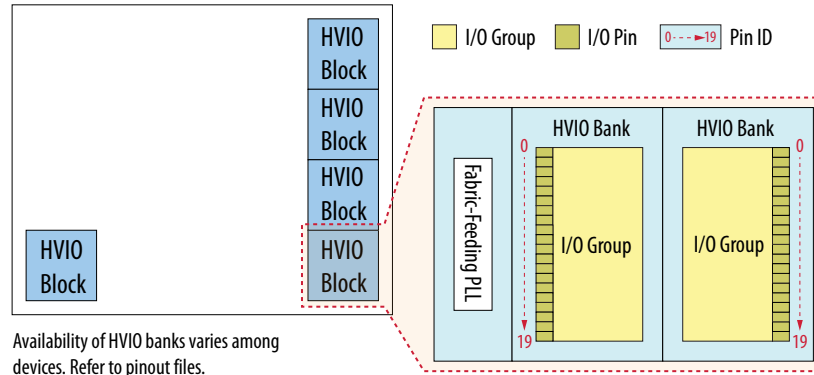
### Related Information

[Supported I/O Standards for HVIO Banks](#) on page 52

### 3.1.1. HVIO Bank Structure

**Figure 26. Agilex 5 HVIO Bank Structure (Die Top View)**

This figure shows the HVIO bank structure of the Agilex 5 device. The figure shows the view of the die as shown in the Quartus Prime **Chip Planner**. In the **Pin Planner**, this corresponds to the "Bottom View". Different device packages have different number of HVIO banks. Refer to the device pin-out files for HVIO banks availability and locations for each device package.



#### Related Information

##### Agilex 5 Device Pin-Out Files

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

### 3.1.2. HVIO Buffers and Registers

The I/O registers consist of three different paths.

- The input path for handling data from the input pin to the core
- The output path for handling data from the core to the output pin
- The output enable (OE) path for handling the OE signal to the output buffer

The I/O registers allow fast source-synchronous register-to-register transfers and resynchronizations. To use the I/O registers to implement DDR circuitry, you can use the GPIO FPGA IP.

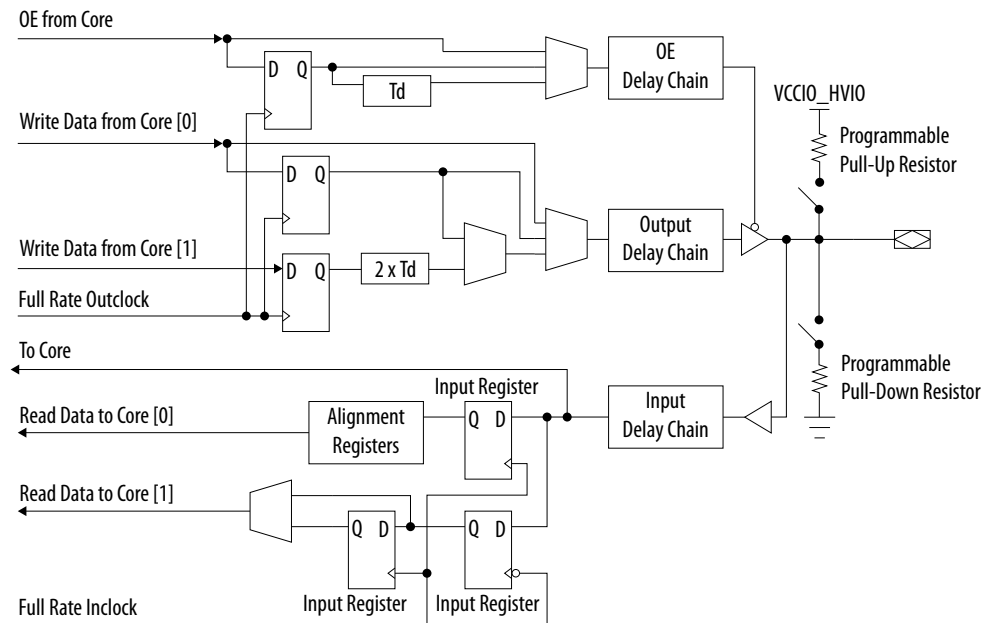
The input and output paths contain the following blocks:

- Input registers:
  - Support full rate data transfer from the periphery to the core
  - Support double or single data rate data captured from I/O buffer to the core
- Output registers:
  - Support full rate data transfer from the core to the periphery
  - Support double or single data rate data transfer to the output pin
- OE registers:
  - Support the output enable signal from the core to the periphery
  - Support double data rate or single data rate data transfer to the I/O pin

The input and output paths also support the following features:

- Clock enable
- Asynchronous or synchronous reset
- Delay chain on input and output paths

**Figure 27. I/O Element (IOE) Structure of Agilex 5 HVIO**



## 3.2. HVIO Features

The I/O bank within the HVIO interface supports 1.8 V, 2.5 V, and 3.3 V LVCMOS and LVTTTL I/O standards.

### Power Pins for the HVIO Buffers

The `VCCIO_HVIO` and `VCCPT_HVIO` pins power the I/O buffers located in the I/O bank within the HVIO interface.

### HVIO Buffer Features

- Single-ended I/O buffers—support LVCMOS and LVTTTL I/O standards
- Programmable current strength
- Programmable weak pull-up and pull-down resistor
- Programmable open-drain output
- Programmable delay chain

### Related Information

[Supported I/O Standards for HVIO Banks](#) on page 52

### 3.2.1. Supported I/O Standards for HVIO Banks

The  $V_{CCIO\_HVIO}$ ,  $V_{CCPT\_HVIO}$ , and  $V_{CC}$  power supplies power the HVIO buffers. Each HVIO bank has its own  $V_{CCIO\_HVIO}$  power supply, but shares  $V_{CCPT\_HVIO}$  and  $V_{CC}$  power supplies between the HVIO banks and with other blocks.

The HVIO bank supports 1.8 V, 2.5 V, and 3.3 V  $V_{CCIO\_HVIO}$ . In the bank, you can implement I/O standards that support the bank's  $V_{CCIO\_HVIO}$ .

**Table 27. HVIO Bank Supported I/O Standards**

This table lists the input and output voltages of a HVIO bank. To use the LVTTTL I/O standards on the hardware, assign the equivalent LVCMOS I/O standards in the Quartus Prime software.

I/O Standard	$V_{CCIO\_HVIO}$ (V)		$V_{CCPT\_HVIO}$ (V)	JEDEC Standard
	Input	Output		
1.8 V LVCMOS/LVTTTL	1.8	1.8	1.8	JESD8-31
2.5 V LVCMOS/LVTTTL	2.5	2.5	1.8	JESD8-12A.01
3.3 V LVCMOS/LVTTTL	3.3	3.3	1.8	JESD8-B

#### Related Information

- [I/O Standards Specifications, Agilex 5 FPGAs and SoCs Device Data Sheet](#)  
Provides the electrical specifications for the supported I/O standards.
- [Assigning Pin I/O Standards in the Quartus Prime Assignment Editor](#) on page 55
- [Assigning Pin I/O Standards in the Quartus Prime Pin Planner](#) on page 56

### 3.2.2. Dedicated Features of HVIO Pins

In the HVIO bank, each I/O pin provides dedicated features such as System PLL reference clock,  $\overline{PERST}$ , clock source for RGMII, and Fabric-Feeding I/O PLL.

For more information about the dedicated features of the HVIO pins refer to the related information.

#### Related Information

- [Agilex 5 Device Pin-Out Files](#)  
Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.
- [Pin Connection Guidelines: Agilex 5 FPGAs and SoCs](#)  
Provides more information about each pin function.
- [GTS Transceiver PHY User Guide](#)

### 3.2.3. HVIO Buffer Behavior

**Table 28. HVIO Pins Guideline for Different Pin States**

HVIO Pin State					
Not turned on	Powering up	Fully powered up	Configuration mode	User mode	Powering down
Either tristate the pins or do not drive them with any external voltage.	<ul style="list-style-type: none"> <li>Pin voltage must not exceed <math>V_{CCIO\_HVIO}^{(9)}</math></li> <li>After full <math>V_{CCIO\_HVIO}</math> power up, the pins are tri-stated.</li> </ul>	All pins are tri-stated.	All pins are tri-stated.	Valid data transactions can be initiated.	<ul style="list-style-type: none"> <li>Pin voltage must not exceed <math>V_{CCIO\_HVIO}^{(9)}</math></li> <li>When the <math>V_{CCIO\_HVIO}</math> and <math>V_{CC}</math> power rails are powering down, the I/O pin signals measure between ground and the <math>V_{CCIO\_HVIO}</math> voltage levels.</li> </ul>

**Note:** After the Agilex 5 device fully powers up, the voltage levels for the HVIO pins must not exceed the DC input voltage ( $V_I$ ) value or the AC maximum allowed overshoot during transitions.

#### Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)

### 3.2.4. Programmable I/O Element Features for the HVIO Bank

**Table 29. Programmable IOE Feature Settings for Agilex 5 HVIO Bank**

This table lists the I/O standards that the feature supports and the available settings for each I/O standard.

I/O Standard	Programmable IOE Feature			
	Current Strength	Weak Pull-up/Pull-down <sup>(10)</sup>	Open-Drain	I/O Delay
1.8 V LVCMOS	<ul style="list-style-type: none"> <li>3 mA</li> <li>6 mA</li> <li>9 mA</li> <li>12 mA (Default)</li> </ul>	<ul style="list-style-type: none"> <li>Disabled (Default)</li> <li>Weak pull-up with 20 k<math>\Omega</math> resistor</li> <li>Weak pull-down with 20 k<math>\Omega</math> resistor</li> </ul>	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled (Default)</li> </ul>	Refer to the device datasheet.
2.5 V LVCMOS				
3.3 V LVCMOS				

#### Related Information

- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)
- [Programmable I/O Features Description](#) on page 99

#### 3.2.4.1. Guidelines: Programmable Open-Drain Output

If you enable the open-drain output feature, follow these guidelines.

<sup>(9)</sup>  $V_{CCIO\_HVIO}$  refers to the onboard real-time voltage supply.

<sup>(10)</sup> The weak pull-up/pull-down feature is available only for the input buffer.

- Do not pull the output voltage higher than the  $V_I$  (DC) level.
- Intel recommends that you use an external pull-up resistor higher than 2 k $\Omega$ .

#### Related Information

[Programmable I/O Features Description](#) on page 99

### 3.3. HVIO Implementation Guide

The Quartus Prime software provides tools for you to create, configure and compile your I/O design. Each tool provides different functions and supports different features to implement your I/O design.

**Table 30. Quartus Prime I/O Implementation Tools**

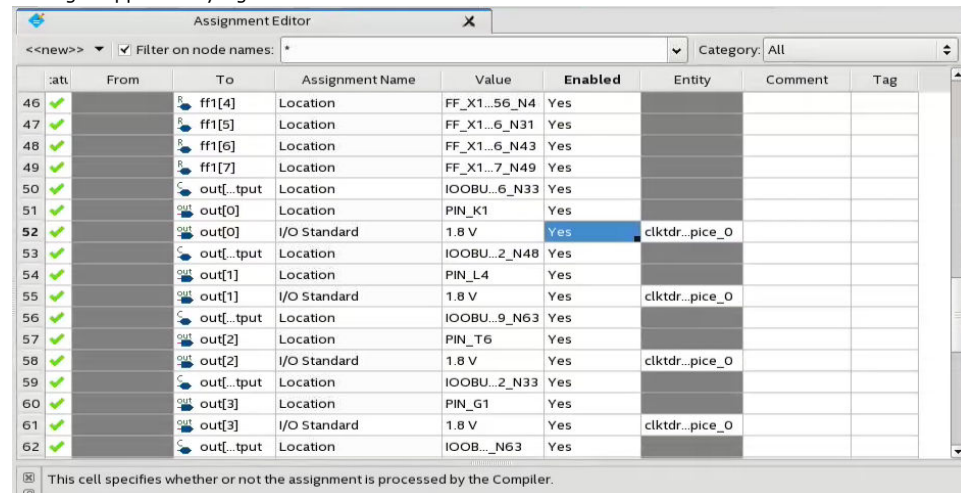
Tool	Functions	Supported Assignment	Supported I/O Standards
Assignment Editor	<ul style="list-style-type: none"> <li>• View, create and edit assignments.</li> <li>• The Quartus Prime software: <ul style="list-style-type: none"> <li>— Dynamically validates your edits.</li> <li>— Notify you of errors and warnings of invalid assignments.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• I/O standard</li> <li>• Programmable current strength</li> <li>• Programmable weak pull-up and pull-down resistor</li> </ul>	<ul style="list-style-type: none"> <li>• 1.8 V LVCMOS</li> <li>• 2.5 V LVCMOS</li> <li>• 3.3 V LVCMOS</li> </ul>
Pin Planner	<ul style="list-style-type: none"> <li>• Graphically represent pin locations on the device.</li> <li>• With this tool, you can: <ul style="list-style-type: none"> <li>— Perform initial pin planning.</li> <li>— Locate, place, and assign I/O pins.</li> <li>— Configure board trace models for pins you select for signal integrity evaluations.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• I/O standard</li> <li>• Programmable current strength</li> <li>• Programmable weak pull-up and pull-down resistor</li> </ul>	
GPIO FPGA IP	<ul style="list-style-type: none"> <li>• Instantiate the IP.</li> <li>• Customize your IP instance using parameters options.</li> </ul>	Programmable open-drain output	—

#### 3.3.1. I/O Assignments with the Quartus Prime Assignment Editor

You can assign all instance-specific settings and constraints through the Quartus Prime Assignment Editor. You can filter assignments by node name or category.

**Figure 28. Quartus Prime Assignment Editor**

This figure shows an example of the user interface and does not represent actual components, features, or settings supported by Agilex 5 FPGAs.



	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
46	✓	ff1[4]	Location	FF_X1...56_N4	Yes			
47	✓	ff1[5]	Location	FF_X1...6_N31	Yes			
48	✓	ff1[6]	Location	FF_X1...6_N43	Yes			
49	✓	ff1[7]	Location	FF_X1...7_N49	Yes			
50	✓	out[...tput	Location	IOOBU...6_N33	Yes			
51	✓	out[0]	Location	PIN_K1	Yes			
52	✓	out[0]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
53	✓	out[...tput	Location	IOOBU...2_N48	Yes			
54	✓	out[1]	Location	PIN_L4	Yes			
55	✓	out[1]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
56	✓	out[...tput	Location	IOOBU...9_N63	Yes			
57	✓	out[2]	Location	PIN_T6	Yes			
58	✓	out[2]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
59	✓	out[...tput	Location	IOOBU...2_N33	Yes			
60	✓	out[3]	Location	PIN_G1	Yes			
61	✓	out[3]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
62	✓	out[...tput	Location	IOOBU...N63	Yes			

☒ This cell specifies whether or not the assignment is processed by the Compiler.

### 3.3.1.1. Assigning Pin I/O Standards in the Quartus Prime Assignment Editor

1. From the Quartus Prime menu, select **Assignments > Assignment Editor**
2. Under the **To** column, search for the pin that you want to configure.
3. Under the **Assignment Name** column, select **I/O Standard (Accepts wildcards)**.
4. Under the **Value** column, select the I/O standard that you want to assign to the pin.
5. From the Quartus Prime menu, select **File > Save**.

#### Related Information

[Supported I/O Standards for HVIO Banks](#) on page 52

### 3.3.1.2. Assigning Programmable IOE Features in the Quartus Prime Assignment Editor

1. From the Quartus Prime menu, select **Assignments > Assignment Editor**
2. Under the **To** column, search for the pin that you want to configure.
3. Under the **Assignment Name** column, select a supported programmable IOE feature.
4. Under the **Value** column, select a supported value.
5. From the Quartus Prime menu, select **File > Save**.

#### Related Information

[HVIO Programmable IOE Features Assignment Names and Settings](#) on page 56  
Provides a list of supported programmable IOE features for the HVIO, the assignment names, and supported values.

### 3.3.1.3. HVIO Programmable IOE Features Assignment Names and Settings

**Table 31. HVIO Programmable IOE Features Assignment Names and Settings**

This table lists the programmable IOE features assignment names and values that you can specify in the Quartus Prime Assignment Editor and Pin Planner tools.

Feature	Assignment Name	Supported Values
Current strength	<b>Current Strength</b>	<ul style="list-style-type: none"> <li>3mA</li> <li>6mA</li> <li>9mA</li> <li>12mA (default)</li> </ul>
Weak pull-up/pull-down resistor <sup>(11)</sup>	<b>Weak Pull Up/Down</b>	<ul style="list-style-type: none"> <li>No Pull Up or Down (Default)</li> <li>Pull Down 20 kOhm</li> <li>Pull Up 20 kOhm</li> </ul>

#### Related Information

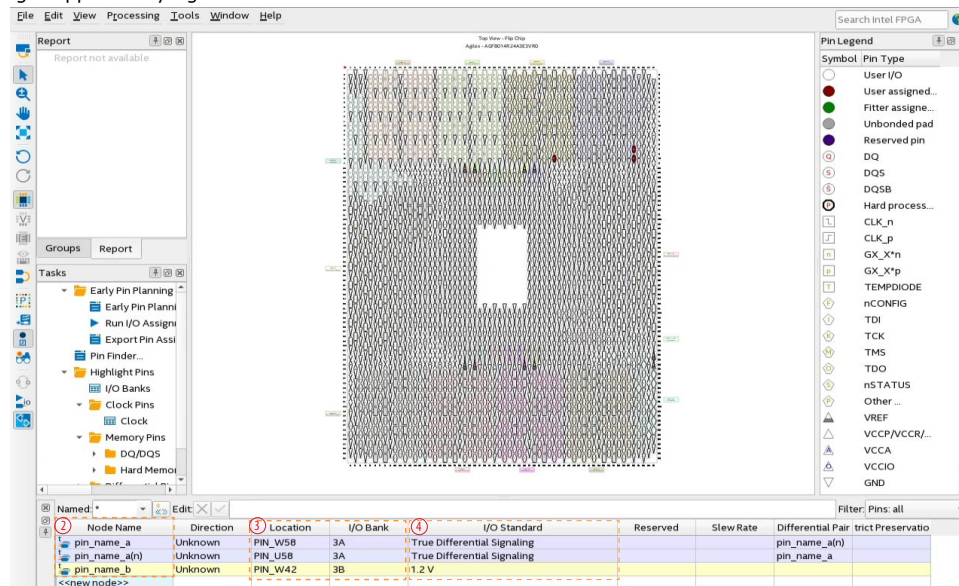
Assigning Programmable IOE Features in the Quartus Prime Assignment Editor on page 55

### 3.3.2. Assigning Pin I/O Standards in the Quartus Prime Pin Planner

You can use the Quartus Prime Pin Planner for I/O pin planning, assignment, and validation.

**Figure 29. Quartus Prime Pin Planner**

This figure shows an example of the user interface and does not represent actual components, features, or settings supported by Agilex 5 FPGAs.



<sup>(11)</sup> The weak pull-up/pull-down feature is available only for the input buffer.



1. From the Quartus Prime menu, select **Assignments > Pin Planner**.
2. Under the **Node Name** column in the **All Pins** box, look for the pin that you want to configure.
3. Under the **Location** column, select the specific pin location.  
The **I/O Bank** column displays the I/O bank name where the pin resides. The **Top View - Flip Chip** diagram shows the I/O banks in different colors.
4. Under the **I/O Standard** column, select the supported I/O standards that you want to assign to the pin.  
If you select **True Differential Signaling**, the Pin Planner automatically adds a negative node with a specific pin location.

#### Related Information

[Supported I/O Standards for HVIO Banks](#) on page 52

### 3.4. HVIO Design Guidelines

Different functions of the HVIO pins have different guidelines, placement restrictions, connection requirements, and clocking requirements.

#### 3.4.1. HVIO Pins During Power Sequencing

Agilex 5 devices do not support hot-socketing and require a specific power sequence. Design your power supply solution to properly control the complete power sequence.

Adhere to these guidelines to prevent unnecessary current draw on the I/O pins located in the HVIO banks. These guidelines apply for unpowered, power up to power-on reset (POR), POR delay, POR delay to configuration, configuration, initialization, user mode, and power down device states.

- The I/O pins in the HVIO banks can be tri-stated, driven to ground, or driven to the  $V_{CCIO\_HVIO}$  level.
- While the device is powering up or down, the input signals to an HVIO pin, at all times, must not exceed the  $V_{CCIO\_HVIO}$  rail.
- While the device is powering up, powering down, or not turned on, the HVIO pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per HVIO bank.
- After the device fully powers up, the voltage levels for the HVIO pins must not exceed the DC input voltage ( $V_I$ ) value or the AC maximum allowed overshoot during transitions.
- For more information, refer to the *Agilex 5 FPGAs and SoCs Pin Connection Guidelines* document.

**Table 32. Guideline Example**

Condition	Guideline
The $V_{CCIO\_HVIO}$ pin ramps up and at period X, the $V_{CCIO\_HVIO}$ voltage is 0.9 V.	At period X, keep the signals driven by the device connected to the HVIO I/O pin at a voltage of 0.9 V or lower.

#### 3.4.2. Unused HVIO Pins

Unused HVIO pins are configured as input tri-stated. You may leave these pins floating.

### 3.4.3. V<sub>CCIO\_HVIO</sub> Supply for Unused HVIO Banks

Connect the V<sub>CCIO\_HVIO</sub> of the unused HVIO bank to 0 V, 1.8 V, 2.5 V, or 3.3 V.

### 3.4.4. Maximum DC Current Restrictions

While using Agilex 5 HVIO pins, adhere to the maximum allowed duration of the per pin DC current limit for the specified current strength setting.

**Table 33. Maximum Allowed Durations of DC Current Limits Per Current Strength Setting**

Current Strength Setting	DC Current Limit	Maximum Allowed Duration (%)
12 mA	±8 mA	100%
	±10 mA	60%
	±12 mA	40%
	More than ±12 mA	Not allowed
9 mA	±6 mA	100%
	±7.5 mA	60%
	±9 mA	40%
	More than ±9 mA	Not allowed
6 mA	±4 mA	100%
	±5 mA	60%
	±6 mA	40%
	More than ±6 mA	Not allowed
3 mA	±2 mA	100%
	±2.5 mA	60%
	±3 mA	40%
	More than ±3 mA	Not allowed

## 3.5. HVIO Simulation

Altera provides simulation models for Agilex 5 devices.

These simulation models are:

- Synopsys HSPICE models
- IBIS models

**Table 34. Simulation Models Descriptions**

Model	Supported I/O Type	Description
HSPICE	HVIO	<ul style="list-style-type: none"><li>• Simulates actual transistor level design to obtain precise electrical simulation.</li><li>• The syntax describes I/O buffers, board components and connections, and specific simulation parameters.</li><li>• The model contains encrypted transistor and logic cell library models, output buffer circuit models for single-ended and differential I/Os, and sample SPICE decks for single-ended and differential I/Os.</li><li>• The model requires a longer simulation time compared to the IBIS model.</li></ul>
IBIS	HVIO	<ul style="list-style-type: none"><li>• This is a behavioral model of the I/O buffers based on the I/V curve data derived from the HSPICE simulation.</li><li>• The pre-emphasis feature is an example that can use the IBIS simulation model.</li><li>• This model has a shorter simulation time compared to HSPICE.</li><li>• The simulation model has less complexity compared to HSPICE models and supported by many simulation tools.</li></ul>

### 3.5.1. IBIS Models—HVIO Support

You can use the Agilex 5 IBIS model to perform system-level simulations for various I/O configurations across three predefined process, voltage, and temperature settings.

The Agilex 5 IBIS model kit contains the following information:

- IBIS model file (.ibs)
- User guide that describes the model usage
- Model list sheet that lists the supported I/O feature for each model
- Package RLC report that provides the lumped package RLC values for each supported Agilex 5 variant

You can use the Agilex 5 IBIS model to simulate all valid I/O features configurations across all supported I/O standards:

- Current strength
- Weak pull-up and pull-down
- Open-drain

### 3.5.2. HSPICE Models

You can use the Agilex 5 SPICE model to perform system-level simulations for various configurations. The SPICE kits provide models that support a wide variety of I/O features across process, voltage, and temperature (PVT)

Each SPICE kit contains the following items:

- Encrypted transistor and logic cell library models
- Encrypted input or output buffer circuit models for single-ended and differential I/Os
- Single-ended and differential sample SPICE decks
- User guide that describes the model usage

The HSPICE models provide options to simulate buffer behavior for the following I/O features:

- Current strength
- Weak pull-up and pull-down
- Open-drain

### 3.5.3. Net Length Reports

The net length information consists of the package trace delay from the die pad to the package pin. Each pin in an FPGA package has its own net length information. This information is important for you to perform board trace compensation to optimize the channel-to-channel skew on your board design.

#### Related Information

[Agilex 5 Device Package Net Length Report](#)

Downloads the net length reports for Agilex 5 devices.



## 4. Agilex 5 HPS I/O Banks

---

The HPS bank is available in the Agilex 5 SoCs. The HPS bank provides the I/O buffer and peripheral support to interface with the hard processor system (HPS).

### Related Information

- [Types of I/O Banks](#) on page 8
- [Device Migration Guidelines: Agilex 5 FPGAs and SoCs E-Series](#)

### 4.1. HPS I/O Bank Overview

The HPS I/O bank contains 48 I/O pins. You can use these I/O pins to access HPS features such as clocks, peripherals, mass storage flash, and JTAG.

### 4.2. HPS I/O Features

The I/O bank within the HPS interface supports single-ended IO standards.

#### Power Pins for the HPS I/O Buffers

The `VCCIO_HPS` pin powers the I/O buffers located in the HPS I/O bank within the HPS I/O interface.

#### HPS I/O Buffer Features

The HPS I/O buffer supports these features:

- Programmable current strength
- Programmable weak pull-up and pull-down resistor
- Programmable open-drain output
- Programmable slew rate
- Schmitt Trigger input buffer
- Programmable delay chain
- On-die termination impedance

### 4.2.1. Supported I/O Standards for HPS I/O Banks

The  $V_{CCIO\_HPS}$  power supply powers the HPS I/O buffer.

**Table 35. Agilex 5 HPS I/O Bank Supported I/O Standards**

I/O Standard	$V_{CCIO\_HPS}$ (V)	
	Input	Output
1.8 V LVCMOS	1.8	1.8

#### Related Information

- [I/O Standards Specifications, Agilex 5 FPGAs and SoCs Device Data Sheet](#)  
Provides the electrical specifications for the supported I/O standards.
- [Assigning Pin I/O Standards in the Quartus Prime Pin Planner](#) on page 67

### 4.2.2. Programmable I/O Element Features for the HPS I/O Bank

**Table 36. Programmable IOE Feature Settings for Agilex 5 HPS I/O Bank**

This table lists the supported IOE features for each I/O standards in the HPS I/O banks.

I/O Standard	Programmable IOE Feature						
	Current Strength	Slew Rate	Weak Pull-up/ Pull-down	Schmitt Trigger/ TTL Input	Open-Drain	I/O Delay	On-Die Termination Impedance
1.8 V LVCMOS	<ul style="list-style-type: none"> <li>• 2 mA</li> <li>• 4 mA</li> <li>• 6 mA</li> <li>• 8 mA (Default)</li> </ul>	<ul style="list-style-type: none"> <li>• Slow</li> <li>• Fast (Default)</li> </ul>	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Weak pull-up with 20 k<math>\Omega</math> resistor (Default)</li> <li>• Weak pull-up with 50 k<math>\Omega</math> resistor</li> <li>• Weak pull-up with 80 k<math>\Omega</math> resistor</li> <li>• Weak pull-down with 20 k<math>\Omega</math> resistor</li> <li>• Weak pull-down with 50 k<math>\Omega</math> resistor</li> <li>• Weak pull-down with 80 k<math>\Omega</math> resistor</li> </ul>	<ul style="list-style-type: none"> <li>• Schmitt Trigger (Default)</li> <li>• TTL</li> </ul>	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (Default)</li> </ul>	Refer to the device datasheet.	<ul style="list-style-type: none"> <li>• NMOS<sup>(12)</sup> (Default)</li> <li>• PMOS<sup>(13)</sup></li> </ul>

#### Related Information

- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)
- [Programmable I/O Features Description](#) on page 99
- [HPS Programmable I/O Timing Characteristics, Agilex 5 FPGAs and SoCs Device Data Sheet](#)

<sup>(12)</sup> On-die pull-down termination.

<sup>(13)</sup> On-die pull-up termination.

- [Hard Processor System Technical Reference Manual: Agilex 5 SoCs](#)

### 4.2.3. HPS I/O Buffer Behavior

**Table 37. HPS I/O Pins Guideline for Different Pin States**

HPS I/O Pin State					
Not turned on	Powering up	Fully powered up	HPS initialization	HPS boot completed	Powering down
Pin voltage must not exceed $V_{CCIO\_HPS}$ .	<ul style="list-style-type: none"> <li>Pin voltage must not exceed <math>V_{CCIO\_HPS}</math>.<sup>(14)</sup></li> <li>All pins are in undetermined state.</li> </ul>	All pins are configured as Schmitt Trigger input with 20 k $\Omega$ weak pull-up enabled.	All pins are configured as Schmitt Trigger input with 20 k $\Omega$ weak pull-up enabled.	Valid data transactions can be initiated.	<ul style="list-style-type: none"> <li>Pin voltage must not exceed <math>V_{CCIO\_HPS}</math>.<sup>(14)</sup></li> <li>All pins are in undetermined state.</li> </ul>

**Note:** After the Agilex 5 device fully powers up, the voltage levels for the HPS I/O pins must not exceed the DC input voltage ( $V_I$ ) value or the AC maximum allowed overshoot during transitions.

#### Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)

## 4.3. HPS I/O Implementation Guide

The Quartus Prime software provides tools for you to create, configure and compile your I/O design. Each tool provides different functions and supports different features to implement your I/O design.

**Table 38. Quartus Prime I/O Implementation Tools**

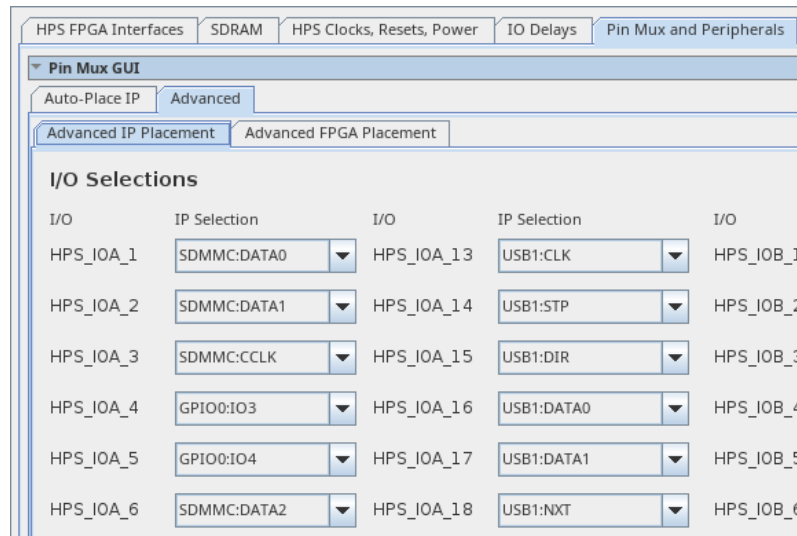
Tool	Functions	Supported Assignment	Supported I/O Standards
Assignment Editor	<ul style="list-style-type: none"> <li>View, create and edit assignments.</li> <li>The Quartus Prime software: <ul style="list-style-type: none"> <li>Dynamically validates your edits.</li> <li>Notify you of errors and warnings of invalid assignments.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>Programmable slew rate control</li> <li>Programmable current strength</li> <li>Programmable weak pull-up select</li> <li>Programmable weak pull-down select</li> <li>Schmitt Trigger</li> <li>On-die termination impedance</li> </ul>	1.8 V LVCMOS
Pin Planner	<ul style="list-style-type: none"> <li>Graphically represent pin locations on the device.</li> <li>With this tool, you can: <ul style="list-style-type: none"> <li>Perform initial pin planning.</li> <li>Configure board trace models for pins you select for signal integrity evaluations.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>Programmable slew rate control</li> <li>Programmable current strength</li> </ul>	
Hard Processor System FPGA IP	<ul style="list-style-type: none"> <li>Instantiate the IP.</li> <li>Customize your IP instance using parameters options.</li> </ul>	<ul style="list-style-type: none"> <li>Programmable open-drain output</li> <li>Programmable delay chain</li> </ul>	—

<sup>(14)</sup>  $V_{CCIO\_HPS}$  refers to the real-time onboard voltage supply.

### 4.3.1. Configuring Open Drain Feature for the HPS I/O

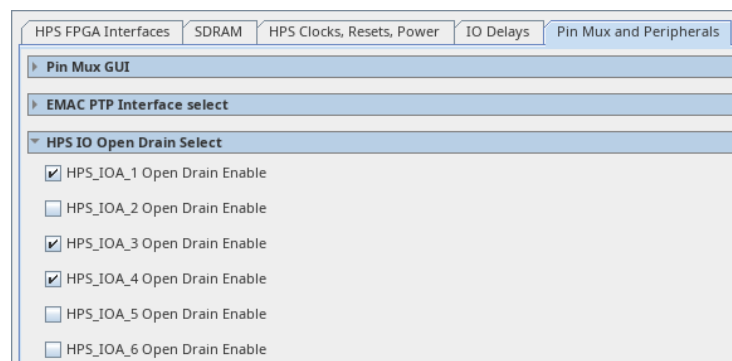
You can turn on the open drain feature for the HPS I/Os through the Hard Processor System FPGA IP in the Quartus Prime Platform Designer.

**Figure 30. Hard Processor System FPGA IP Parameter Editor**



1. From the Quartus Prime menu, select **Tools > Platform Designer**
2. Specify the **Quartus project** and **Platform Designer system**, then click **Open**.
3. In **Platform Designer**, open the Hard Processor System FPGA IP parameter editor.
4. Navigate to the **Pin Mux and Peripherals > Pin Mux GUI > Advanced > Advanced IP Placement** tab.
5. If you make any changes, click **Apply Selections**, then click **OK**.
6. Scroll down to the **HPS IO Open Drain Select** section.
7. Turn on the **HPS\_ION\_N Open Drain Enable** that you want.

**Figure 31. HPS IO Open Drain Select Section**



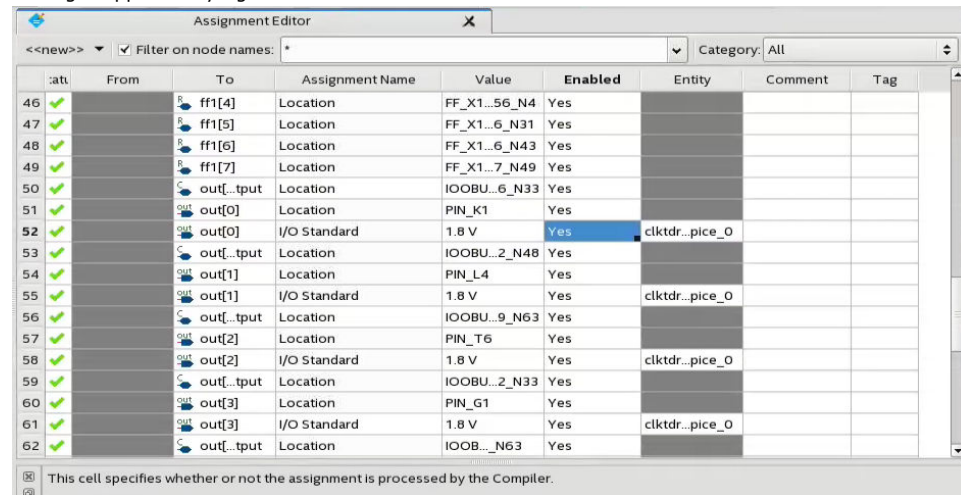


### 4.3.2. I/O Assignments with the Quartus Prime Assignment Editor

You can assign all instance-specific settings and constraints through the Quartus Prime Assignment Editor. You can filter assignments by node name or category.

**Figure 32. Quartus Prime Assignment Editor**

This figure shows an example of the user interface and does not represent actual components, features, or settings supported by Agilex 5 FPGAs.



	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
46	✓	ff1[4]	Location	FF_X1...56_N4	Yes			
47	✓	ff1[5]	Location	FF_X1...6_N31	Yes			
48	✓	ff1[6]	Location	FF_X1...6_N43	Yes			
49	✓	ff1[7]	Location	FF_X1...7_N49	Yes			
50	✓	out[...tput	Location	IOOBU...6_N33	Yes			
51	✓	out[0]	Location	PIN_K1	Yes			
52	✓	out[0]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
53	✓	out[...tput	Location	IOOBU...2_N48	Yes			
54	✓	out[1]	Location	PIN_L4	Yes			
55	✓	out[1]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
56	✓	out[...tput	Location	IOOBU...9_N63	Yes			
57	✓	out[2]	Location	PIN_T6	Yes			
58	✓	out[2]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
59	✓	out[...tput	Location	IOOBU...2_N33	Yes			
60	✓	out[3]	Location	PIN_G1	Yes			
61	✓	out[3]	I/O Standard	1.8 V	Yes	clktdr...pice_0		
62	✓	out[...tput	Location	IOOBU...N63	Yes			

This cell specifies whether or not the assignment is processed by the Compiler.

#### 4.3.2.1. Assigning Programmable IOE Features in the Quartus Prime Assignment Editor

1. From the Quartus Prime menu, select **Assignments > Assignment Editor**
2. Under the **To** column, search for the pin that you want to configure.
3. Under the **Assignment Name** column, select a supported programmable IOE feature.
4. Under the **Value** column, select a supported value.
5. From the Quartus Prime menu, select **File > Save**.

#### Related Information

[HPS I/O Programmable IOE Features Assignment Names and Settings](#) on page 66  
Provides a list of supported programmable IOE features for the HPS I/O, the assignment names, and supported values.

#### 4.3.2.2. HPS I/O Programmable IOE Features Assignment Names and Settings

**Table 39. HPS I/O Programmable IOE Features Assignment Names and Settings**

This table lists the programmable IOE features assignment names and values that you can specify in the Quartus Prime Assignment Editor and Pin Planner tools.

Feature	Assignment Name	Supported Values
Slew rate control	<b>Slew Rate</b>	<ul style="list-style-type: none"> <li>• <b>0</b>—slow</li> <li>• <b>1</b>—fast (default)</li> </ul>
<ul style="list-style-type: none"> <li>• Weak pull-up resistor</li> <li>• Weak pull-down resistor</li> </ul>	<b>Weak Pull-Up Resistor</b>	<ul style="list-style-type: none"> <li>• <b>On</b> (default)—turns on the weak pull-up or pull-down resistor</li> <li>• <b>Off</b>—turns off the weak pull-up or pull-down resistor</li> </ul>
	<b>Weak Pull Up/Down Select</b> <sup>(15)</sup>	<ul style="list-style-type: none"> <li>• <b>No Pull Up or Down</b></li> <li>• <b>Pull Down 20 kOhm</b></li> <li>• <b>Pull Down 50 kOhm</b></li> <li>• <b>Pull Down 80 kOhm</b></li> <li>• <b>Pull Up 20 kOhm</b> (default)</li> <li>• <b>Pull Up 50 kOhm</b></li> <li>• <b>Pull Up 80 kOhm</b></li> </ul>
Schmitt Trigger input buffer	<b>Schmitt Trigger</b>	<ul style="list-style-type: none"> <li>• <b>On</b> (default)</li> <li>• <b>Off</b></li> </ul>
Current strength	<b>Current Strength</b>	<ul style="list-style-type: none"> <li>• <b>2 mA</b></li> <li>• <b>4 mA</b></li> <li>• <b>6 mA</b></li> <li>• <b>8 mA</b> (default)</li> </ul>
On-die termination impedance	<b>HPS IO On-Die Termination Impedance</b>	<ul style="list-style-type: none"> <li>• <b>NMOS</b> (default)</li> <li>• <b>PMOS</b></li> </ul>

#### Related Information

[Assigning Programmable IOE Features in the Quartus Prime Assignment Editor](#) on page 65

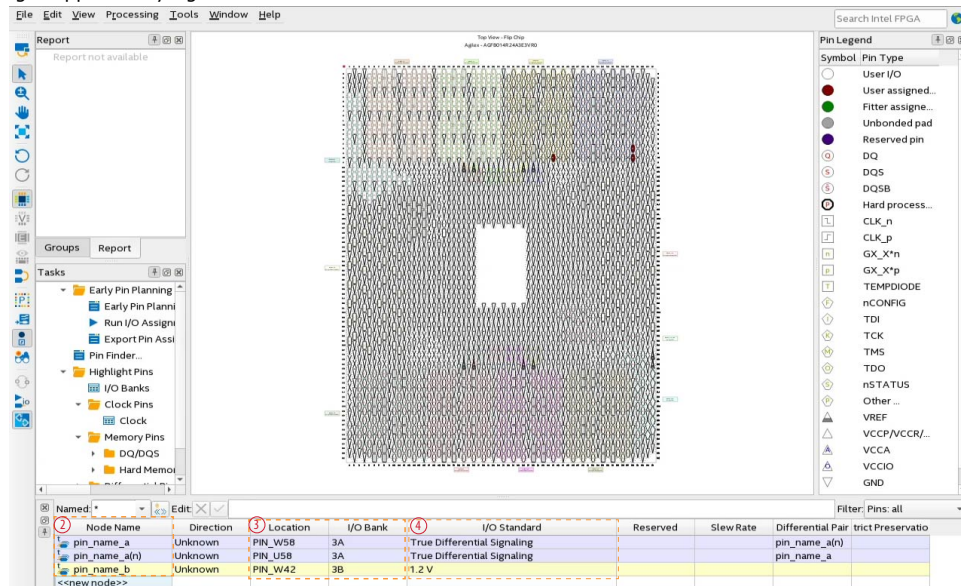
<sup>(15)</sup> You must use this together with the **Weak Pull-Up Resistor** assignment.

### 4.3.3. Assigning Pin I/O Standards in the Quartus Prime Pin Planner

You can use the Quartus Prime Pin Planner for I/O pin planning, assignment, and validation.

**Figure 33. Quartus Prime Pin Planner**

This figure shows an example of the user interface and does not represent actual components, features, or settings supported by Agilex 5 FPGAs.



1. From the Quartus Prime menu, select **Assignments > Pin Planner**.
2. Under the **Node Name** column in the **All Pins** box, look for the pin that you want to configure.
3. Under the **I/O Standard** column, select the supported I/O standards that you want to assign to the pin.

If you select **True Differential Signaling**, the Pin Planner automatically adds a negative node with a specific pin location.

#### Related Information

[Supported I/O Standards for HPS I/O Banks](#) on page 62

## 4.4. HPS I/O Design Guidelines

Different functions of the HPS I/O pins have different guidelines, placement restrictions, connection requirements, and clocking requirements.

### 4.4.1. HPS I/O Pins During Power Sequencing

Agilex 5 devices do not support hot-socketing and require a specific power sequence. Design your power supply solution to properly control the complete power sequence.

Adhere to these guidelines to prevent unnecessary current draw on the I/O pins located in the HPS I/O banks. These guidelines apply for unpowered, power up to POR, POR delay, POR delay to configuration, configuration, initialization, user mode, and power down device states.

- The I/O pins in the HPS I/O banks can be tri-stated, driven to ground, or driven to the  $V_{CCIO\_HPS}$  level.
- While the device is powering up or down, the input signals of an I/O pin, at all times, must not exceed the I/O buffer power supply rail of the bank where the I/O pin resides.
- While the device is powering up, powering down, or not turned on, the HPS I/O pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per HPS I/O bank.
- After the device fully powers up, the voltage levels for the HPS I/O pins must not exceed the DC input voltage ( $V_I$ ) value or the AC maximum allowed overshoot during transitions.

**Table 40. Guideline Example**

Condition	Guideline
The $V_{CCIO\_HPS}$ pin ramps up and at period X, the $V_{CCIO\_HPS}$ voltage is 0.9 V.	At period X, keep the signals driven by the device connected to the HPS I/O pin at a voltage of 0.9 V or lower.

#### 4.4.2. HPS Shared I/O Requirements

The HPS external memory interface uses I/O pins located in the HSIO bank instead of the HPS I/O bank. The  $V_{CCIO\_PIO}$  powers the HSIO bank instead of the 1.8 V  $V_{CCIO\_HPS}$ . For the location of the HPS shared HSIO pins, refer to device pin-out files.

##### Related Information

##### [Agilex 5 Device Pin-Out Files](#)

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

### 4.5. HPS I/O Simulation

You can use the Agilex 5 IBIS model to perform system-level simulations for various I/O configurations across three predefined process, voltage, and temperature settings.

#### 4.5.1. IBIS Models—HPS I/O Support

The Agilex 5 IBIS model kit contains the following information:

- IBIS model file (.ibs)
- User guide that describes the model usage
- Model list sheet that lists the supported I/O feature for each model
- Package RLC report that provides the lumped package RLC values for each supported Agilex 5 variant

You can use the Agilex 5 IBIS model to simulate all valid I/O features configurations across all supported I/O standards:

- Slew rate
- Weak pull-up
- Current strength
- Open drain

#### Related Information

[IBIS Models for Intel® FPGA Devices](#)

### 4.5.2. Net Length Reports

The net length information consists of the package trace delay from the die pad to the package pin. Each pin in an FPGA package has its own net length information. This information is important for you to perform board trace compensation to optimize the channel-to-channel skew on your board design.

#### Related Information

[Agilex 5 Device Package Net Length Report](#)

Downloads the net length reports for Agilex 5 devices.



## 5. Agilex 5 SDM I/O Banks

---

The SDM bank is available in the Agilex 5 FPGAs. The SDM bank provides the I/O buffer and peripheral support for device configuration and to interface with the secure device manager (SDM).

### Related Information

- [Types of I/O Banks](#) on page 8
- [Device Migration Guidelines: Agilex 5 FPGAs and SoCs E-Series](#)

### 5.1. SDM I/O Bank Overview

The SDM I/O bank contains 24 dedicated pins for device configuration purposes. The SDM I/O interfaces supports 1.8 V single-ended non-voltage referenced I/O standard for interfacing with the SDM.

The Agilex 5 pin-out files list the dedicated function of each pin in the SDM I/O bank.

### Related Information

#### [Agilex 5 Device Pin-Out Files](#)

Each device pinout file lists the available I/O banks for each package, the banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

### 5.2. SDM I/O Features

The I/O bank within the SDM interface supports single-ended IO standards.

#### Power Pins for the SDM I/O Buffers

The VCCIO\_SDM pin powers the I/O buffers located in the SDM I/O bank within the SDM I/O interface.

#### SDM I/O Buffer Features

The SDM I/O buffer is pre-configured with these features:

- Programmable current strength
- Programmable weak pull-up and pull-down resistor
- Programmable open-drain output
- Programmable slew rate
- Schmitt Trigger input buffer

### Related Information

Programmable I/O Features Description on page 99

## 5.2.1. Supported I/O Standards for SDM I/O Banks

The  $V_{CCIO\_SDM}$  power supply powers the SDM I/O buffer.

**Table 41. Agilex 5 SDM I/O Bank Supported I/O Standards**

I/O Standard	$V_{CCIO\_SDM}$ (V)	
	Input	Output
1.8 V LVCMOS	1.8	1.8

### Related Information

I/O Standards Specifications, Agilex 5 FPGAs and SoCs Device Data Sheet  
Provides the electrical specifications for the supported I/O standards.

## 5.2.2. SDM I/O Buffer Behavior

**Table 42. SDM I/O Pins Guideline for Different Pin States**

SDM I/O Pin State				
Not turned on	Powering up	Fully powered up	Configuration mode	Powering down
Pin voltage must not exceed $V_{CCIO\_SDM}$ .	<ul style="list-style-type: none"> <li>Pin voltage must not exceed <math>V_{CCIO\_SDM}</math>.<sup>(16)</sup></li> <li>All pins are in undetermined state, except these pins: <ul style="list-style-type: none"> <li>— VSIGP_0</li> <li>— VSIGP_1</li> <li>— VSIGN_0</li> <li>— VSIGN_1</li> <li>— RREF_SDM</li> </ul> </li> </ul>	Refer to the related information.	Refer to the related information.	<ul style="list-style-type: none"> <li>Pin voltage must not exceed <math>V_{CCIO\_SDM}</math>.<sup>(16)</sup></li> <li>All pins are in undetermined state, except these pins: <ul style="list-style-type: none"> <li>— VSIGP_0</li> <li>— VSIGP_1</li> <li>— VSIGN_0</li> <li>— VSIGN_1</li> <li>— RREF_SDM</li> </ul> </li> </ul>

### Related Information

- Agilex 5 FPGAs and SoCs Device Data Sheet
- Agilex 5 Configuration Timing Diagram, Device Configuration User Guide: Agilex 5 FPGAs and SoCs
- I/O Standards and Features for Configuration Pins on page 72  
Lists the pre-configured SDM I/O settings for each SDM pin across different device configurations modes and provides guidelines for the SDM I/O pins during configuration mode.

<sup>(16)</sup>  $V_{CCIO\_SDM}$  refers to the real-time onboard voltage supply.

### 5.2.3. I/O Standards and Features for Configuration Pins

The SDM pins have different I/O standards and features in different configuration schemes. You can assign the unused SDM pins for other functions in the Quartus Prime software.

**Table 43. Agilex 5 AS x4 Configuration Scheme—Dedicated Configuration Pins**

Pin Function	SDM I/O	Direction	I/O Standard	Schmitt Trigger/TTL Input	Weak Pull-Up/Pull-Down	Drive Strength	Open Drain	Slew Rate
AS_DATA1	SDM_IO1	Bidirectional	1.8 V LVCMOS	Schmitt Trigger	Disable	8 mA	Disable	Fast
AS_CLK	SDM_IO2	Output	1.8 V LVCMOS	—	—	8 mA	Disable	Fast
AS_DATA2	SDM_IO3	Bidirectional	1.8 V LVCMOS	Schmitt Trigger	Disable	8 mA	Disable	Fast
AS_DATA0	SDM_IO4	Bidirectional	1.8 V LVCMOS	Schmitt Trigger	Disable	8 mA	Disable	Fast
AS_nCS00	SDM_IO5	Output	1.8 V LVCMOS	—	—	8 mA	Disable	Fast
AS_DATA3	SDM_IO6	Bidirectional	1.8 V LVCMOS	Schmitt Trigger	Disable	8 mA	Disable	Fast
AS_nCS02	SDM_IO7	Output	1.8 V LVCMOS	—	—	8 mA	Disable	Fast
AS_nCS03	SDM_IO8	Output	1.8 V LVCMOS	—	—	8 mA	Disable	Fast
AS_nCS01	SDM_IO9	Output	1.8 V LVCMOS	—	—	8 mA	Disable	Fast
AS_nRST	SDM_IO15	Output	1.8 V LVCMOS	—	—	8 mA	Disable	Fast

**Table 44. Agilex 5 AS x4 Configuration Scheme—Unused Configuration Pins**

For the unused configuration pins, the drive strength, open drain, and slew rate settings are not applicable.

SDM I/O	Direction	I/O Standard	Schmitt Trigger/TTL Input	Weak Pull-Up/Pull-Down
SDM_IO0	Input	1.8 V LVCMOS	Schmitt Trigger	Weak pull-down with 20 kΩ resistor
SDM_IO10	Input	1.8 V LVCMOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor
SDM_IO11	Input	1.8 V LVCMOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor
SDM_IO12	Input	1.8 V LVCMOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor
SDM_IO13	Input	1.8 V LVCMOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor
SDM_IO14	Input	1.8 V LVCMOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor
SDM_IO16	Input	1.8 V LVCMOS	Schmitt Trigger	Weak pull-down with 20 kΩ resistor

**Table 45. Agilex 5 Avalon Streaming Interface x8 Configuration Scheme—Dedicated Configuration Pins**

Pin Function	SDM I/O	Direction	I/O Standard	Schmitt Trigger/TTL Input	Weak Pull-Up/Pull-Down	Drive Strength	Open Drain	Slew Rate
AVSTx8_DATA2	SDM_IO1	Input	1.8 V LVCMOS	Schmitt Trigger	Disable	—	—	—
AVSTx8_DATA0	SDM_IO2	Input	1.8 V LVCMOS	Schmitt Trigger	Disable	—	—	—

*continued...*



Pin Function	SDM I/O	Direction	I/O Standard	Schmitt Trigger/TTL Input	Weak Pull-Up/Pull-Down	Drive Strength	Open Drain	Slew Rate
AVSTx8_DATA3	SDM_IO3	Input	1.8 V LVC MOS	Schmitt Trigger	Disable	—	—	—
AVSTx8_DATA1	SDM_IO4	Input	1.8 V LVC MOS	Schmitt Trigger	Disable	—	—	—
AVSTx8_DATA4	SDM_IO6	Input	1.8 V LVC MOS	Schmitt Trigger	Disable	—	—	—
AVSTx8_READY	SDM_IO8	Output	1.8 V LVC MOS	—	—	8 mA	Disable	Fast
AVSTx8_DATA7	SDM_IO10	Input	1.8 V LVC MOS	Schmitt Trigger	Disable	—	—	—
AVSTx8_VALID	SDM_IO11	Input	1.8 V LVC MOS	Schmitt Trigger	Weak pull-down with 20 k $\Omega$ resistor	—	—	—
AVSTx8_DATA5	SDM_IO13	Input	1.8 V LVC MOS	Schmitt Trigger	Disable	—	—	—
AVSTx8_CLK	SDM_IO14	Input	1.8 V LVC MOS	Schmitt Trigger	Disable	—	—	—
AVSTx8_DATA6	SDM_IO15	Input	1.8 V LVC MOS	Schmitt Trigger	Disable	—	—	—

**Table 46. Agilex 5 Avalon Streaming Interface x8 Configuration Scheme—Unused Configuration Pins**

For the unused configuration pins, the drive strength, open drain, and slew rate settings are not applicable.

SDM I/O	Direction	I/O Standard	Schmitt Trigger/TTL Input	Weak Pull-Up/Pull-Down
SDM_IO0	Input	1.8 V LVC MOS	Schmitt Trigger	Weak pull-down with 20 k $\Omega$ resistor
SDM_IO5	Input	1.8 V LVC MOS	Schmitt Trigger	Weak pull-up with 20 k $\Omega$ resistor
SDM_IO7	Input	1.8 V LVC MOS	Schmitt Trigger	Weak pull-up with 20 k $\Omega$ resistor
SDM_IO9	Input	1.8 V LVC MOS	Schmitt Trigger	Weak pull-up with 20 k $\Omega$ resistor
SDM_IO12	Input	1.8 V LVC MOS	Schmitt Trigger	Weak pull-up with 20 k $\Omega$ resistor
SDM_IO16	Input	1.8 V LVC MOS	Schmitt Trigger	Weak pull-down with 20 k $\Omega$ resistor

**Table 47. Agilex 5 Avalon Streaming Interface x16 Configuration Scheme—Dedicated Configuration Pins**

For all pin functions in this table:

- The I/O location is the SDM shared GPIO bank.
- The weak pull-up or pull-down, and open drain options are not applicable.

Pin Function	Direction	I/O Standard	Drive Strength	Slew Rate
AVST_CLK	Input	1.2 V LVC MOS	—	—
AVST_READY	Output	1.2 V LVC MOS	Series 34 $\Omega$ OCT without calibration	Slow
AVST_VALID	Input	1.2 V LVC MOS	—	—
AVST_DATA	Input	1.2 V LVC MOS	—	—

**Table 48. Agilex 5 Optional Configuration Pins**

The SDM I/O for each pin function in this table is as assigned in the Quartus Prime configuration pins option.

Pin Function	Direction	I/O Standard	Schmitt Trigger/ TTL Input	Weak Pull-Up/ Pull-Down	Drive Strength	Open Drain	Slew Rate
PWRMGT_SCL	Bidirectional	1.8V LVC MOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor	2 mA	Enable	Slow
PWRMGT_SDA	Bidirectional	1.8V LVC MOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor	2 mA	Enable	Slow
PWRMGT_ALERT	Output	1.8V LVC MOS	—	—	2 mA	Enable	Slow
CONF_DONE	Output	1.8V LVC MOS	—	—	8 mA	Disable	Fast
INIT_DONE	Output	1.8V LVC MOS	—	—	8 mA	Disable	Fast
CvP_CONFDONE	Output	1.8V LVC MOS	—	—	8 mA	Disable	Fast
SEU_ERROR	Output	1.8V LVC MOS	—	—	8 mA	Disable	Fast
HPS_COLD_nRESET	Bidirectional	1.8V LVC MOS	Schmitt Trigger	Weak pull-up with 20 kΩ resistor	2 mA	Enable	Fast
Direct to factory image	Input	1.8V LVC MOS	Schmitt Trigger	Weak pull-down with 20 kΩ resistor	—	—	—
nCATTRIP	Output	1.8V LVC MOS	—	—	2 mA	Disable	Slow
TAMPERDETECTION	Output	1.8V LVC MOS	—	—	8 mA	Disable	Fast
TAMPERRESPONSESTATUS	Output	1.8V LVC MOS	—	—	8 mA	Disable	Fast

#### Related Information

- [Agilex 5 Configuration Pins, Device Configuration User Guide: Agilex 5 FPGAs and SoCs](#)  
Provides more information about the configuration pins in Agilex 5 devices.
- [SDM I/O Buffer Behavior](#) on page 71
- [IBIS Models—SDM I/O Support](#) on page 75
- [Avalon Streaming Interface Dedicated Configuration Pins](#) on page 75

## 5.3. SDM I/O Design Guidelines

Different functions of the SDM I/O pins have different guidelines, placement restrictions, connection requirements, and clocking requirements.

### 5.3.1. SDM I/O Pins During Power Sequencing

Agilex 5 devices do not support hot-socketing and require a specific power sequence. Design your power supply solution to properly control the complete power sequence.

Adhere to the guidelines to prevent unnecessary current draw on the I/O pins located in the SDM I/O banks. These guidelines apply for unpowered, power up to POR, POR delay, POR delay to configuration, configuration, initialization, user mode, and power down device states.

- The I/O pins in the SDM I/O banks can be tri-stated, driven to ground, or driven to the  $V_{CCIO\_SDM}$  level.
- While the device is powering up or down, the input signals of an I/O pin, at all times, must not exceed the I/O buffer power supply rail of the bank where the I/O pin resides.
- While the device is powering up, powering down, or not turned on, the SDM I/O pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per SDM I/O bank.
- After the device fully powers up, the voltage levels for the SDM I/O pins must not exceed the DC input voltage ( $V_I$ ) value or the AC maximum allowed overshoot during transitions.

**Table 49. Guideline Example**

Condition	Guideline
The $V_{CCIO\_SDM}$ pin ramps up and at period $X$ , the $V_{CCIO\_SDM}$ voltage is 0.9 V.	At period $X$ , keep the signals driven by the device connected to the SDM I/O pin at a voltage of 0.9 V or lower.

### 5.3.2. Avalon Streaming Interface Dedicated Configuration Pins

The Avalon streaming interface dedicated configuration pins are powered by bank 3AT. If you use the Avalon streaming interface  $\times 16$  configuration scheme, you must power bank 3AT with 1.2 V  $V_{CCIO\_PIO}$ .

#### Related Information

[I/O Standards and Features for Configuration Pins](#) on page 72

## 5.4. SDM I/O Simulation

You can use the Agilex 5 IBIS model to perform system-level simulations for various I/O configurations across three predefined process, voltage, and temperature settings.

### 5.4.1. IBIS Models—SDM I/O Support

The Agilex 5 IBIS model kit contains the following information:

- IBIS model file (.ibs)
- User guide that describes the model usage
- Model list sheet that lists the supported I/O feature for each model
- Package RLC report that provides the lumped package RLC values for each supported Agilex 5 variant

You can use the Agilex 5 IBIS model to simulate all valid I/O features configurations across all supported I/O standards:

- Slew rate
- Weak pull-up
- Weak pull-down
- Current strength

### Related Information

- [IBIS Models for Intel® FPGA Devices](#)
- [I/O Standards and Features for Configuration Pins](#) on page 72  
Lists the pre-configured SDM I/O settings for each SDM pin across different device configurations modes and provides guidelines for the SDM I/O pins during configuration mode.

## 5.4.2. Net Length Reports

The net length information consists of the package trace delay from the die pad to the package pin. Each pin in an FPGA package has its own net length information. This information is important for you to perform board trace compensation to optimize the channel-to-channel skew on your board design.

### Related Information

[Agilex 5 Device Package Net Length Report](#)

Downloads the net length reports for Agilex 5 devices.



## 6. Agilex 5 I/O Troubleshooting Guidelines

These debug guidelines are initial debug actions and do not necessarily resolve the failures in your designs.

**Table 50. GPIO Debug Guidelines**

This table lists the failure symptoms and the associated debug actions that you can take to identify the failure areas when you are designing GPIO systems with Agilex 5 devices.

Failure Symptoms	Recommended Debug Actions
1.2 V LVCMOS output at the entire bank does not reach 1.2 V. <i>Note:</i> Not applicable to the HVIO bank.	<ul style="list-style-type: none"> <li>Check the power-up and power-down sequences of each voltage rail with respect to time.</li> <li>Compare the power sequences as per recommendation in the <i>Power Management User Guide: Agilex 5 FPGAs and SoCs</i>.</li> <li>Verify the <math>V_{CCIO\_PIO}</math> voltage signal is 1.2 V.</li> </ul>
Quartus Prime software shows an error message to indicate incorrect I/O settings for $V_{CCIO}$ during design compilation. Error message example: Illegal constraint of I/O bank to the location <I/O bank>	Select the I/O pins specified in the error message and check the I/O settings for the pins.
Quartus Prime software shows illegal I/O error message during design compilation. Error message example: Programmable VOD option is set to 1 for pin <pin_name>, but setting is not supported by <I/O standard>	Select the I/O pins specified in the error message and set the pins to the correct I/O function. Refer to the device pin-outs file for more information about the pin functions.

## 7. GPIO FPGA IP

The GPIO FPGA IP provides features to support the device I/O blocks. You can use the Quartus Prime parameter editor to configure the GPIO FPGA IP.

### 7.1. Release Information for GPIO FPGA IP

Altera® FPGA IP versions match the Quartus Prime Design Suite software versions until v19.1. Starting in Quartus Prime Design Suite software version 19.2, the IP has a new versioning scheme.

The IP version (X.Y.Z) number can change with each Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

**Table 51. GPIO FPGA IP Current Release Information**

Item	Description
IP Version	23.0.0
Quartus Prime Version	25.1.1
Release Date	2025.08.04

#### Related Information

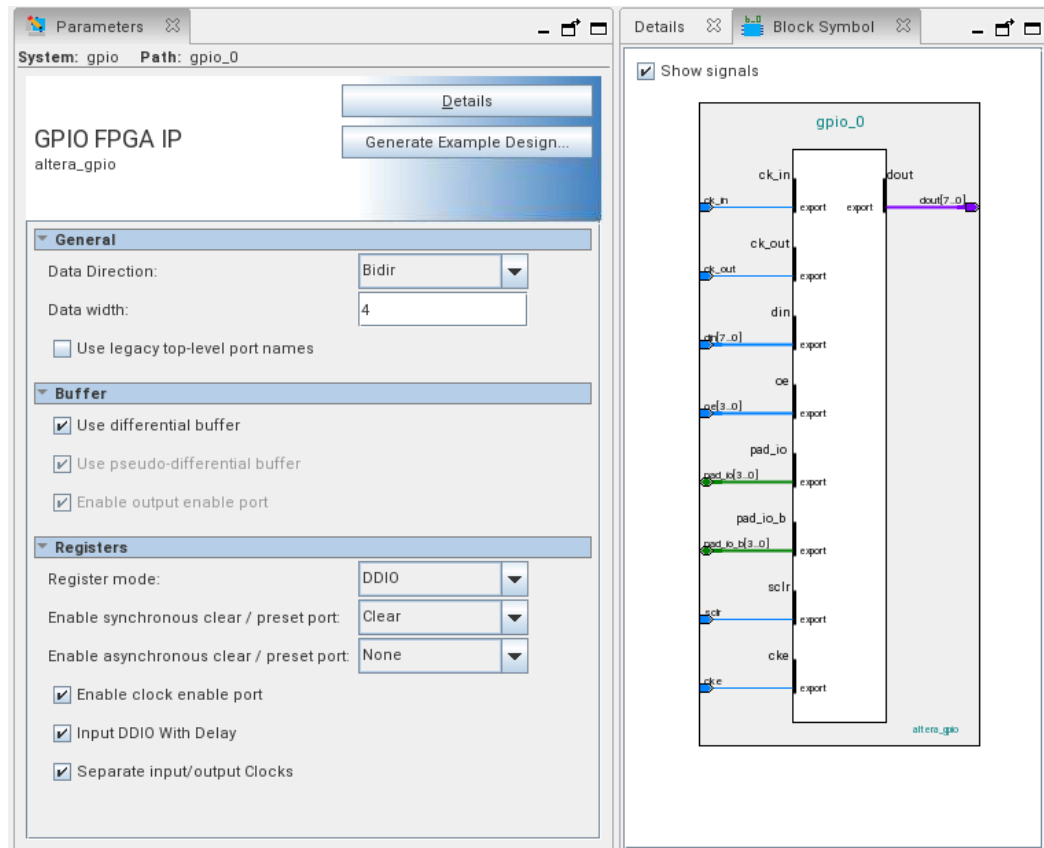
[GPIO FPGA IP Release Notes](#)

### 7.2. Generating the GPIO FPGA IP

Using the GPIO FPGA IP parameter editor, you can customize the IP settings and generate the IP variant files, simulation testbench, and HDL instantiation template.

Before you begin, create or open a Quartus Prime project.

Figure 34. GPIO FPGA IP Parameter Editor



1. In the **IP Catalog** window, double-click **GPIO FPGA IP**.  
The **Parameter Editor** window appears.
2. Specify a top-level name for your new IP variant and click **Create**.  
Do not include space and special characters in the name and file path.
3. Set the values in the **Parameters** tab.  
The **System Messages** tab displays errors and warning for the parameters settings.
4. From the **Parameter Editor** menu, select **File > Save**.  
The parameter editor saves the IP variant settings in the `<your_ip>.ip` file.
5. To generate the IP variant HDL files:
  - a. Click **Generate HDL**.  
The **Generation** window appears.
  - b. Specify the output file generation options and click **Generate**.  
The parameter editor generates the synthesis and simulation files as you specified, and automatically adds the `.ip` file of the variant to your project.
  - c. Click **Close**.
6. To generate a simulation testbench:

- a. From the **Parameter Editor** menu, select **Generate ► Generate Testbench System**.
  - b. Specify the testbench generation options and click **Generate**.
  - c. Click **Close**.
7. To generate an HDL instantiation template that you can copy and paste into your text editor:
- a. From the **Parameter Editor** menu, select **Generate ► Show Instantiation Template**.
  - b. Select the **HDL Language**.  
The code template appears in the **Example HDL** box.
  - c. Click **Copy** and then click **Close**.

After generating and instantiating your IP variant, assign appropriate pins to connect the ports.

### 7.2.1. Altera FPGA IP Generation Output

The Quartus Prime software generates the following output file structure for individual IPs that are not part of a Platform Designer system.



Figure 35. Individual IP Generation Output

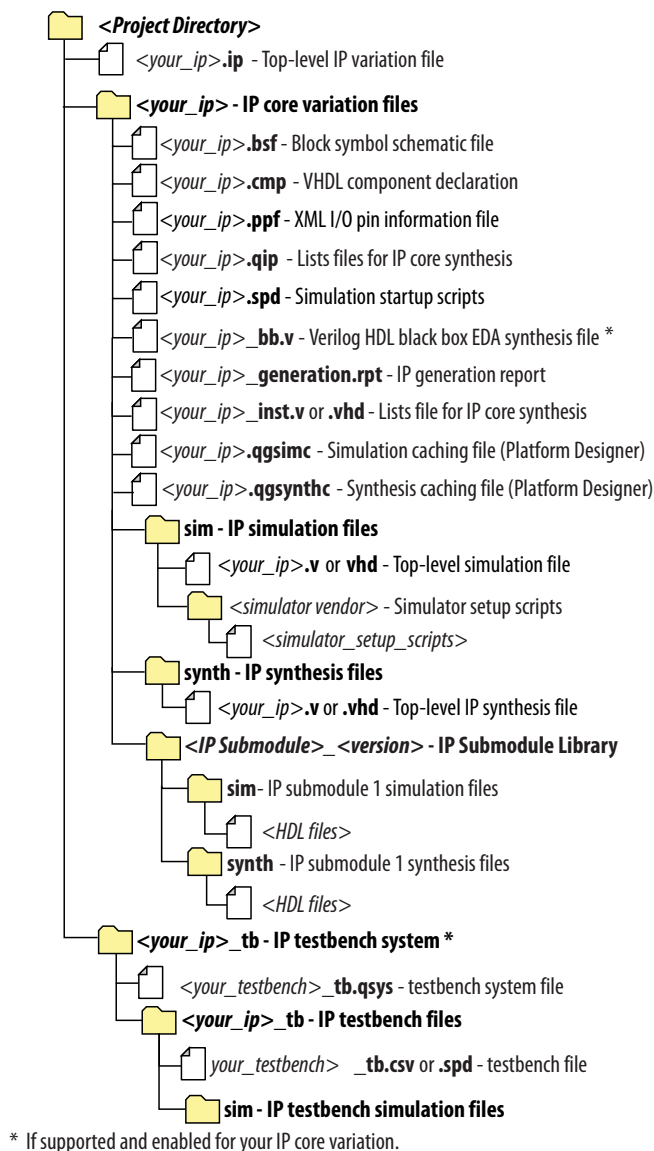


Table 52. Output Files of Altera FPGA IP Generation

File Name	Description
<code>&lt;your_ip&gt;.ip</code>	Top-level IP variation file that contains the parameterization of an IP in your project. If the IP variation is part of a Platform Designer system, the parameter editor also generates a <code>.qsys</code> file.
<code>&lt;your_ip&gt;.cmp</code>	The VHDL Component Declaration ( <code>.cmp</code> ) file is a text file that contains local generic and port definitions that you use in VHDL design files.
<code>&lt;your_ip&gt;_generation.rpt</code>	IP or Platform Designer generation log file. Displays a summary of the messages during IP generation.
continued...	

File Name	Description
<your_ip>.qgsimc (Platform Designer systems only)	Simulation caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP. This comparison determines if Platform Designer can skip regeneration of the HDL.
<your_ip>.qgsynth (Platform Designer systems only)	Synthesis caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP. This comparison determines if Platform Designer can skip regeneration of the HDL.
<your_ip>.csv	Contains information about the upgrade status of the IP component.
<your_ip>.bsf	A symbol representation of the IP variation for use in Block Diagram Files (.bdf).
<your_ip>.spd	Input file that ip-make-simscript requires to generate simulation scripts. The .spd file contains a list of files you generate for simulation, along with information about memories that you initialize.
<your_ip>.ppf	The Pin Planner File (.ppf) stores the port and node assignments for IP components you create for use with the Pin Planner.
<your_ip>_bb.v	Use the Verilog blackbox (_bb.v) file as an empty module declaration for use as a blackbox.
<your_ip>_inst.v or _inst.vhd	HDL example instantiation template. Copy and paste the contents of this file into your HDL file to instantiate the IP variation.
<your_ip>.regmap	If the IP contains register information, the Quartus Prime software generates the .regmap file. The .regmap file describes the register map information of master and slave interfaces. This file complements the .sopcinfo file by providing more detailed register information about the system. This file enables register display views and user customizable statistics in System Console.
<your_ip>.svd	Allows HPS System Debug tools to view the register maps of peripherals that connect to HPS within a Platform Designer system. During synthesis, the Quartus Prime software stores the .svd files for slave interface visible to the System Console masters in the .sof file in the debug session. System Console reads this section, which Platform Designer queries for register map information. For system slaves, Platform Designer accesses the registers by name.
<your_ip>.v <your_ip>.vhd	HDL files that instantiate each submodule or child IP for synthesis or simulation.
mentor/	Contains a msim_setup.tcl script to set up and run a ModelSim* simulation.
aldec/	Contains a Riviera-PRO* script rivierapro_setup.tcl to setup and run a simulation.
/synopsys/vcs /synopsys/vcsmx	Contains a shell script vcs_setup.sh to set up and run a VCS* simulation. Contains a shell script vcsmx_setup.sh and synopsys_sim.setup file to set up and run a VCS MX simulation.
/xcelium	Contains an Xcelium* Parallel simulator shell script xcelium_setup.sh and other setup files to set up and run a simulation.
/submodules	Contains HDL files for the IP submodule.
<IP submodule>/	Platform Designer generates /synth and /sim sub-directories for each IP submodule directory that Platform Designer generates.

## 7.3. GPIO FPGA IP Parameter Settings

You can set the parameter settings for the GPIO FPGA IP in the Quartus Prime software. There are three groups of options: **General**, **Buffer**, and **Registers**.

**Table 53. GPIO FPGA IP Parameters—General**

Parameter	Condition	Allowed Values	Description
<b>Data Direction</b>	—	<ul style="list-style-type: none"> <li>Input</li> <li>Output</li> <li>Bidir</li> </ul>	Specifies the data direction for the GPIO.
<b>Data width</b>	—	1 to 128	Specifies the data width.
<b>Use legacy top-level port names</b>	—	<ul style="list-style-type: none"> <li>On</li> <li>Off</li> </ul>	<p>Use same port names as in Stratix® V, Arria® V, and Cyclone® V devices.</p> <p>For example, dout becomes dataout_h and dataout_l, and din becomes datain_h and datain_l.</p> <p><i>Note:</i> The behavior of these ports are different than in the Stratix V, Arria V, and Cyclone V devices. For the migration guideline, refer to the related information.</p>

**Table 54. GPIO IP Parameters—Buffer**

Parameter	Condition	Allowed Values	Description
<b>Use differential buffer</b>	—	<ul style="list-style-type: none"> <li>On</li> <li>Off</li> </ul>	If turned on, enables differential I/O buffers.
<b>Use pseudo differential buffer</b>	<ul style="list-style-type: none"> <li><b>Data Direction</b> = Output</li> <li><b>Use differential buffer</b> = On</li> </ul>	<ul style="list-style-type: none"> <li>On</li> <li>Off</li> </ul>	<p>If turned on in output mode, enables pseudo differential output buffers.</p> <p>This option is automatically turned on for bidirectional mode if you turn on <b>Use differential buffer</b>.</p>
<b>Enable output enable port</b>	<b>Data Direction</b> = Output	<ul style="list-style-type: none"> <li>On</li> <li>Off</li> </ul>	If turned on, enables user input to the OE port. This option is automatically turned on for bidirectional mode.

**Table 55. GPIO IP Parameters—Registers**

Parameter	Condition	Allowed Values	Description
<b>Register mode</b>	—	<ul style="list-style-type: none"> <li>None</li> <li>Simple register</li> <li>DDIO</li> </ul>	<p>Specifies the register mode for the GPIO IP:</p> <ul style="list-style-type: none"> <li><b>None</b>—specifies a simple wire connection from/to the buffer.</li> <li><b>Simple register</b>—specifies that the DDIO is used as a simple register in single data-rate mode (SDR). The Fitter may pack this register in the I/O.</li> <li><b>DDIO</b>— specifies that the IP core uses the DDIO.</li> </ul>
<b>Enable synchronous clear / preset port</b>	<b>Register mode</b> = DDIO	<ul style="list-style-type: none"> <li>None</li> <li>Clear</li> <li>Preset</li> </ul>	<p>Specifies how to implement synchronous reset port.</p> <ul style="list-style-type: none"> <li><b>None</b>—Disables synchronous reset port.</li> <li><b>Clear</b>—Enables the SCLR port for synchronous clears.</li> <li><b>Preset</b>—Enables the SSET port for synchronous preset.</li> </ul>
continued...			

Parameter	Condition	Allowed Values	Description
Enable asynchronous clear / preset port	Register mode = DDIO	<ul style="list-style-type: none"> <li>None</li> <li>Clear</li> <li>Preset</li> </ul>	<p>Specifies how to implement asynchronous reset port.</p> <ul style="list-style-type: none"> <li><b>None</b>—Disables asynchronous reset port.</li> <li><b>Clear</b>—Enables the ACLR port for asynchronous clears.</li> <li><b>Preset</b>—Enables the ASET port for asynchronous preset.</li> </ul> <p>ACLR and ASET signals are active high.</p>
Enable clock enable ports	Register mode = DDIO	<ul style="list-style-type: none"> <li>On</li> <li>Off</li> </ul>	<ul style="list-style-type: none"> <li><b>On</b>—exposes the clock enable (CKE) port to allow you to control when data is clocked in or out. This signal prevents data from being passed through without your control.</li> <li><b>Off</b>—clock enable port is not exposed and data always pass through the register automatically.</li> </ul>
Input DDIO With Delay	<ul style="list-style-type: none"> <li><b>Data Direction</b> = Bidir</li> <li><b>Register mode</b> = DDIO</li> </ul>	<ul style="list-style-type: none"> <li>On</li> <li>Off</li> </ul>	If turned on, the I/O uses the DDIO with delay.
Separate input/output Clocks	<ul style="list-style-type: none"> <li><b>Data Direction</b> = Bidir</li> <li><b>Register mode</b> = Simple register or DDIO</li> </ul>	<ul style="list-style-type: none"> <li>On</li> <li>Off</li> </ul>	If turned on, enables separate clocks (CK_IN and CK_OUT) for the input and output paths in bidirectional mode.

#### Related Information

- [Input Path](#) on page 89  
Provides a figure showing the input path waveform.
- [Guideline: Swap datain\\_h and datain\\_l Ports in Migrated IP](#) on page 84

### 7.3.1. Guideline: Swap datain\_h and datain\_l Ports in Migrated IP

When you migrate your GPIO IP from previous devices to the GPIO IP, you can turn on **Use legacy top-level port names** option in the GPIO IP parameter editor. However, the behavior of these ports in the GPIO IP is different than in the IP used for the Stratix V, Arria V, and Cyclone V devices.

The GPIO IP drives these ports to the output registers on these clock edges:

- datain\_h—on the falling edge of outclock
- datain\_l—on the rising edge of outclock

If you migrated your GPIO IP from Stratix V, Arria V, and Cyclone V devices, swap the datain\_h and datain\_l ports when you instantiate the IP generated by the GPIO IP.

## 7.4. GPIO FPGA IP Interface Signals

Depending on the parameter settings you specify, different interface signals are available for the GPIO IP.

Figure 36. GPIO IP Interfaces



Figure 37. GPIO Interface Signals

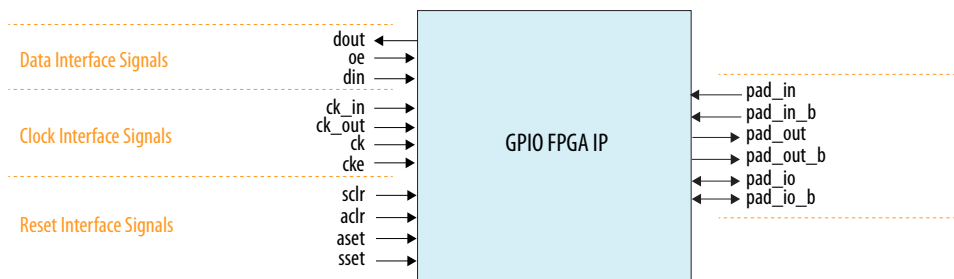


Table 56. Pad Interface Signals

The pad interface is the physical connection from the GPIO IP to the pad. This interface can be an input, output or bidirectional interface, depending on the IP configuration. In this table, *SIZE* is the data width specified in the IP parameter editor.

Signal Name	Direction	Description
pad_in[SIZE-1:0]	Input	Input signal from the pad.
pad_in_b[SIZE-1:0]	Input	Negative node of the differential input signal from the pad. This port is available if you turn on the <b>Use differential buffer</b> option.
pad_out[SIZE-1:0]	Output	Output signal to the pad.
pad_out_b[SIZE-1:0]	Output	Negative node of the differential output signal to the pad. This port is available if you turn on the <b>Use differential buffer</b> option.
pad_io[SIZE-1:0]	Bidirectional	Bidirectional signal connection with the pad.
pad_io_b[SIZE-1:0]	Bidirectional	Negative node of the differential bidirectional signal connection with the pad. This port is available if you turn on the <b>Use differential buffer</b> option.

**Table 57. Data Interface Signals**

The data interface is an input or output interface from the GPIO IP to the FPGA core. In this table, *SIZE* is the data width specified in the IP parameter editor.

Signal Name	Direction	Description
din[ <i>DATA_SIZE</i> -1:0]	Input	Data input from the FPGA core in output or bidirectional mode. <i>DATA_SIZE</i> depends on the register mode: <ul style="list-style-type: none"> <li>Bypass or simple register—<i>DATA_SIZE</i> = <i>SIZE</i></li> <li>DDIO—<i>DATA_SIZE</i> = 2 × <i>SIZE</i></li> </ul>
dout[ <i>DATA_SIZE</i> -1:0]	Output	Data output to the FPGA core in input or bidirectional mode, <i>DATA_SIZE</i> depends on the register mode: <ul style="list-style-type: none"> <li>Bypass or simple register—<i>DATA_SIZE</i> = <i>SIZE</i></li> <li>DDIO—<i>DATA_SIZE</i> = 2 × <i>SIZE</i></li> </ul>
oe[ <i>OE_SIZE</i> -1:0]	Input	OE input from the FPGA core in output mode with <b>Enable output enable port</b> turned on, or bidirectional mode. OE is active high. When transmitting data, set this signal to 1. When receiving data, set this signal to 0. <i>OE_SIZE</i> depends on the register mode: <ul style="list-style-type: none"> <li>Bypass or simple register—<i>DATA_SIZE</i> = <i>SIZE</i></li> <li>DDIO—<i>DATA_SIZE</i> = <i>SIZE</i></li> </ul>

**Table 58. Clock Interface Signals**

The clock interface is an input clock interface. It consists of different signals, depending on the configuration. The GPIO IP can have zero, one, two, or four clock inputs. Clock ports appear differently in different configurations to reflect the actual function performed by the clock signal.

Signal Name	Direction	Description
ck	Input	In input and output paths, this clock feeds a packed register or DDIO. In bidirectional mode, this clock is the unique clock for the input and output paths if you turn off the <b>Separate input/output Clocks</b> parameter.
ck_in	Input	In bidirectional mode, these clocks feed a packed register or DDIO in the input and output paths if you turn on the <b>Separate input/output Clocks</b> parameter.
ck_out		
cke	Input	Clock enable.

**Table 59. Reset Interface Signals**

The reset interface connects the GPIO IP core to the DDIOs.

Signal Name	Direction	Description
sclr	Input	Synchronous clear input. Not available if you select None or Preset for the <b>Enable synchronous clear / preset port</b> option.
aclr	Input	Asynchronous clear input. Active high. Not available if you select None or Preset for the <b>Enable asynchronous clear / preset port</b> option.
aset	Input	Asynchronous set input. Active high. Not available if you select None or Clear for the <b>Enable asynchronous clear / preset port</b> option.
sset	Input	Synchronous set input. Not available if you select None or Clear for the <b>Enable synchronous clear / preset port</b> option.

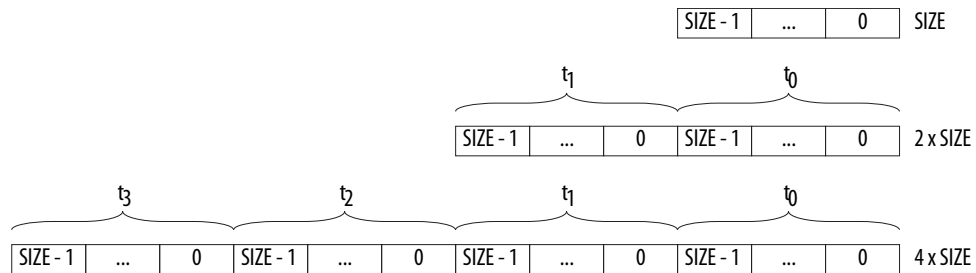
### 7.4.1. Shared Signals

- The input, output, and OE paths share the same clear and preset signals.
- The output and OE path shares the same clock signals.

### 7.4.2. Data Bit-Order for Data Interface

**Figure 38. Data Bit-Order Convention**

This figure shows the bit-order convention for the `din`, `dout` and `oe` data signals.



- If the data bus size value is `SIZE`, the LSB is at the right-most position.
- If the data bus size value is `2 x SIZE`, the bus is made of two words of `SIZE`.
- If the data bus size value is `4 x SIZE`, the bus is made of four words of `SIZE`.
- The LSB is in the right-most position of each word.
- The right-most word specifies the first word going out for output buses and the first word coming in for input buses.

#### Related Information

[Input Path](#) on page 89

### 7.4.3. Input and Output Bus High and Low Bits

The high and low bits in the input or output signals are included in the `din` and `dout` input and output buses.

#### Input Bus

For the `din` bus, if `datain_h` and `datain_l` are the high and low bits, with each width being `datain_width`:

- `datain_h = din[(2 x datain_width - 1):datain_width]`
- `datain_l = din[(datain_width - 1):0]`

For example, for `din[7:0] = 8'b11001010`:

- `datain_h = 4'b1100`
- `datain_l = 4'b1010`

### Output Bus

For the dout bus, if dataout\_h and dataout\_l are the high and low bits, with each width being dataout\_width:

- `dataout_h = dout[(2 × dataout_width - 1):dataout_width]`
- `dataout_l = dout[(dataout_width - 1):0]`

For example, for `dout[7:0] = 8'b11001010`:

- `dataout_h = 4'b1100`
- `dataout_l = 4'b1010`

## 7.4.4. Data Interface Signals and Corresponding Clocks

**Table 60. Data Interface Signals and Corresponding Clocks**

Parameter Configuration		Signal Name	Clock Signal Name
Separate input/output Clocks	Register mode		
Off	<ul style="list-style-type: none"> <li>• Simple Register</li> <li>• DDIO</li> </ul>	<ul style="list-style-type: none"> <li>• <code>din</code></li> <li>• <code>dout</code></li> <li>• <code>oe</code></li> <li>• All pad signals</li> </ul>	<code>ck</code>
	DDIO	<ul style="list-style-type: none"> <li>• <code>sclr</code></li> <li>• <code>sset</code></li> </ul>	
On	<ul style="list-style-type: none"> <li>• Simple Register</li> <li>• DDIO</li> </ul>	<code>din</code>	<code>ck_in</code>
		<ul style="list-style-type: none"> <li>• <code>dout</code></li> <li>• <code>oe</code></li> </ul>	<code>ck_out</code>
		All pad signals	<ul style="list-style-type: none"> <li>• Input path: <code>ck_in</code></li> <li>• Output path: <code>ck_out</code></li> </ul>
	DDIO	<ul style="list-style-type: none"> <li>• <code>sclr</code></li> <li>• <code>sset</code></li> </ul>	<ul style="list-style-type: none"> <li>• Input path: <code>ck_in</code></li> <li>• Output path: <code>ck_out</code></li> </ul>

## 7.5. GPIO FPGA IP Architecture

The GPIO IP supports the I/O components and features of the Agilex 5 devices. You can use the Quartus Prime parameter editor to configure the GPIO IP.

Components of the GPIO IP:

- Double data rate input/output (DDIO)—doubles the data-rate of a communication channel
- Delay chains—configure the delay chains to perform specific delay and assist in I/O timing closure
- I/O buffers—connect the pads to the FPGA



## 7.5.1. GPIO FPGA IP Data Paths

Figure 39. High-Level View of Single-Ended I/O

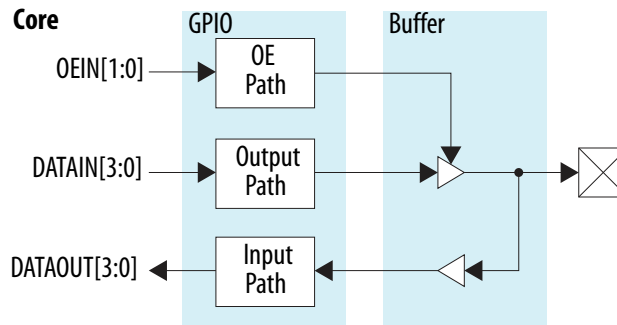


Table 61. GPIO IP Data Path Modes

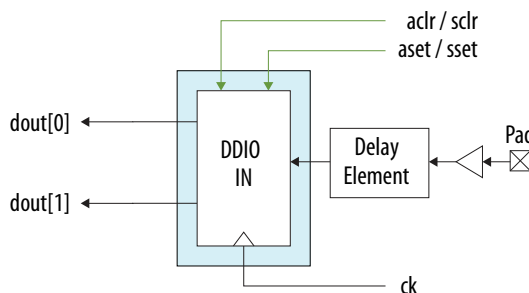
Data Path	Register Mode		
	Bypass	Simple Register	DDIO
Input	Data goes from the delay element to the core, bypassing all double data rate I/Os (DDIOs).	The DDIO operates as a simple register. The Fitter chooses whether to pack the register in the I/O or implement the register in the core, depending on the area and timing trade-offs.	The DDIO operates as a regular DDIO.
Output	Data goes from the core straight to the delay element, bypassing all DDIOs.		
Bidirectional	The output buffer drives both an output pin and an input buffer.	The DDIO operates as a simple register. The output buffer drives both an output pin and an input buffer.	The DDIO operates as a regular DDIO. The output buffer drives both an output pin and an input buffer. The input buffer drives a set of three flip-flops.

If you use asynchronous clear and preset signals, all DDIOs share these same signals.

### 7.5.1.1. Input Path

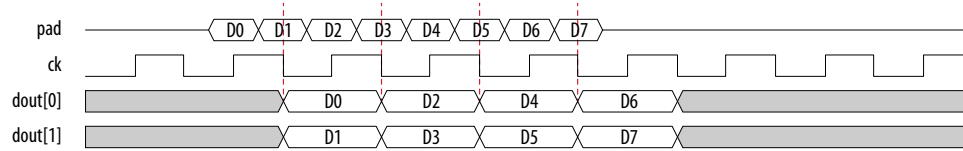
The pad sends data to the input buffer, and the input buffer feeds the delay element. After the data goes to the output of the delay element, the programmable bypass multiplexers select the features and paths to use.

Figure 40. Simplified View of Single-Ended HSIO Input Path



**Figure 41. Input Path Waveform in DDIO Mode**

The actual timing relationship between different signals may vary depending on the specific design, delays, and phases that you specify for the clock.



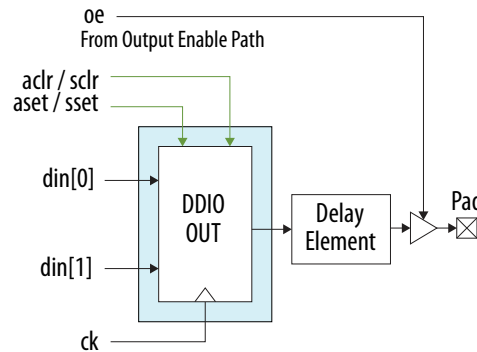
#### Related Information

[Data Bit-Order for Data Interface](#) on page 87

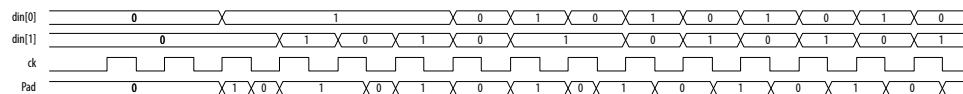
### 7.5.1.2. Output and Output Enable Paths

The output delay element sends data to the pad through the output buffer.

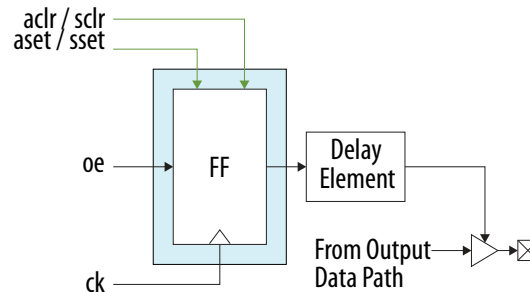
**Figure 42. Simplified View of Single-Ended HSIO Output Path**



**Figure 43. Output Path Waveform in DDIO Mode**



**Figure 44. Simplified View of Output Enable Path**



The difference between the output path and output enable (OE) path is that the OE path does not contain DDIO. To support packed-register implementations in the OE path, a simple register operates as DDIO.

## 7.5.2. Register Packing

The GPIO IP allows you to pack registers into the periphery to save area and resource utilization.

You can configure the DDIO on the input and output path as a flip flop by adding .qsf assignments.

**Table 62. Register Packing .qsf Assignments**

Path	.qsf Assignment
Input register packing	set_instance_assignment -name FAST_INPUT_REGISTER ON -to <path to register>
Output register packing	set_instance_assignment -name FAST_OUTPUT_REGISTER ON -to <path to register>
Output enable register packing	set_instance_assignment -name FAST_OUTPUT_ENABLE_REGISTER ON -to <path to register>

**Note:** The .qsf assignments do not guarantee register packing. However, these assignments enable the Fitter to find a legal placement. Otherwise, the Fitter keeps the flip flop in the core.

## 7.6. Verifying Resource Utilization and Design Performance

You can refer to the Quartus Prime compilation reports to get details about the resource usage and performance of your design.

1. From the Quartus Prime menu, select **Processing > Start Compilation** to run a full compilation.
2. Wait for the compilation to complete.
3. From the Quartus Prime menu, select **Processing > Compilation Report**.
4. Using the **Table of Contents**, navigate to **Fitter > Resource Section**.
  - a. To view the resource usage information, select **Resource Usage Summary**.
  - b. To view the resource utilization information, select **Resource Utilization by Entity**.

## 7.7. GPIO FPGA IP Timing

The performance of the GPIO IP depends on the I/O constraints and clock phases. To validate the timing for your GPIO configuration, Altera recommends that you use the Timing Analyzer.

### Related Information

[Using the Quartus Prime Timing Analyzer, Quartus Prime Pro Edition User Guide: Timing Analyzer](#)

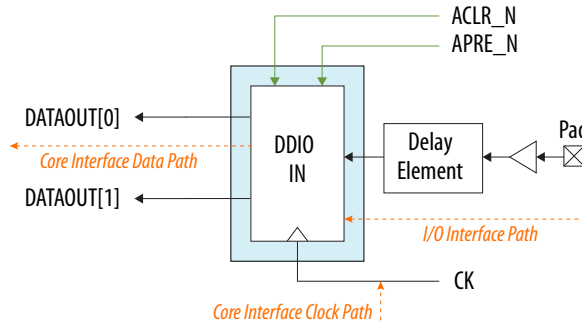
### 7.7.1. Timing Components

The GPIO IP timing components consist of two paths.

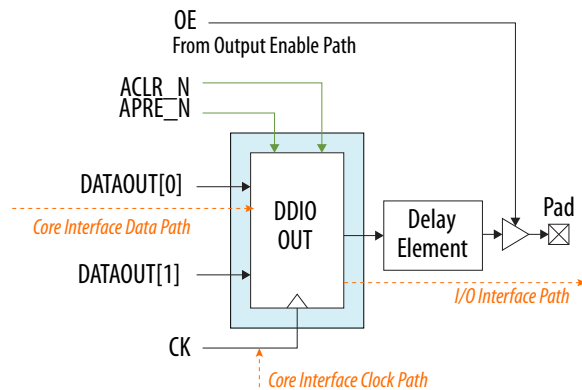
- I/O interface paths—from the FPGA to external receiving devices and from external transmitting devices to the FPGA.
- Core interface paths of data and clock—from the I/O to the core and from the core to I/O.

**Note:** The Timing Analyzer treats the path inside the DDIO\_IN and DDIO\_OUT blocks as black boxes.

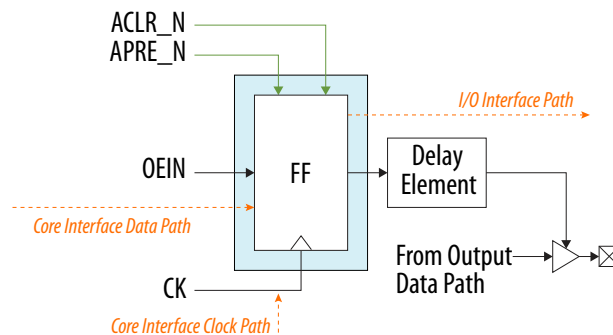
**Figure 45. Input Path Timing Components**



**Figure 46. Output Path Timing Components**



**Figure 47. Output Enable Path Timing Components**



## 7.7.2. Delay Elements

The Quartus Prime software does not automatically set delay elements to maximize slack in the I/O timing analysis. To close the timing or maximize slack, set the delay elements manually in the Quartus Prime settings file (.qsf).

**Table 63. Delay Elements .qsf Assignments**

Specify these assignments in the .qsf to access the delay elements.

Delay Element	.qsf Assignment
Input Delay Element	set_instance_assignment -to <PIN> -name INPUT_DELAY_CHAIN <0..63>
Output Delay Element	set_instance_assignment -to <PIN> -name OUTPUT_DELAY_CHAIN <0..15>
Output Enable Delay Element	set_instance_assignment -to <PIN> -name OE_DELAY_CHAIN <0..15>

The *Agilex 5 FPGAs and SoCs Device Data Sheet* provides information on delay chain specification and offset settings across fast and slow models.

- Fast model—Specifies the delay value when the maximum delay chain offset setting is selected using the fastest process.
- Slow model—Specifies the delay value when the maximum delay chain offset setting is selected using the slowest process within a specific speed grade.

For example, if you assign input delay chain setting to #10 using an Agilex 5 device with -1 speed grade:

- Minimum delay value =  $10 * \text{delay specification for fast model} / 63 = x \text{ ns}$
- Maximum delay value =  $10 * \text{delay specification for -1V slow model} / 63 = y \text{ ns}$

The input delay ranges from  $x \text{ ns}$  to  $y \text{ ns}$  when you select -1 device speed grade in your design.

**Note:** The IOE delay chains are not process, voltage and temperature (PVT) compensated, which means the delay chain value changes across PVT.

## 7.7.3. Timing Analysis

The Quartus Prime software does not automatically generate the SDC timing constraints for the GPIO IP. You must manually enter the timing constraints.

Follow the timing guidelines and examples to ensure that the Timing Analyzer analyzes the I/O timing correctly.

- To perform proper timing analysis for the I/O interface paths, specify the system level constraints of the data pins against the system clock pin in the .sdc file.
- To perform proper timing analysis for the core interface paths, define these clock settings in the .sdc file:
  - Clock to the core registers
  - Clock to the I/O registers for the simple register and DDIO modes

### Related Information

[AN 433: Constraining and Analyzing Source-Synchronous Interfaces](#)

Describes techniques for constraining and analyzing source-synchronous interfaces.

### 7.7.3.1. Single Data Rate Input Register

Figure 48. Single Data Rate Input Register

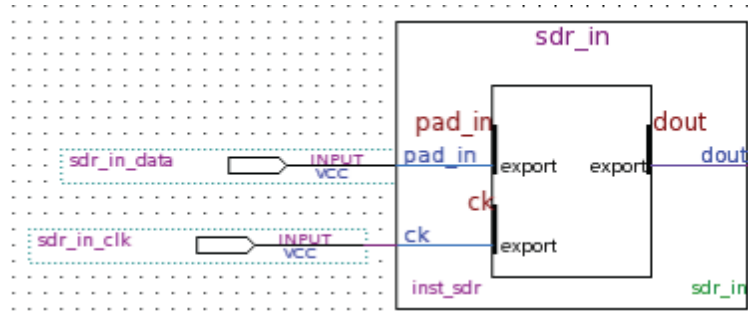


Table 64. Single Data Rate Input Register .sdc Command Examples

Command	Command Example	Description
create_clock	create_clock -name sdr_in_clk -period "100 MHz" sdr_in_clk	Creates clock setting for the input clock.
set_input_delay	set_input_delay -clock sdr_in_clk 0.15 sdr_in_data	Instructs the Timing Analyzer to analyze the timing of the input I/O with a 0.15 ns input delay.

### 7.7.3.2. DDIO Input Register

You can properly constrain the system by using a virtual clock to model the off-chip transmitter to the FPGA.

Figure 49. DDIO Input Register

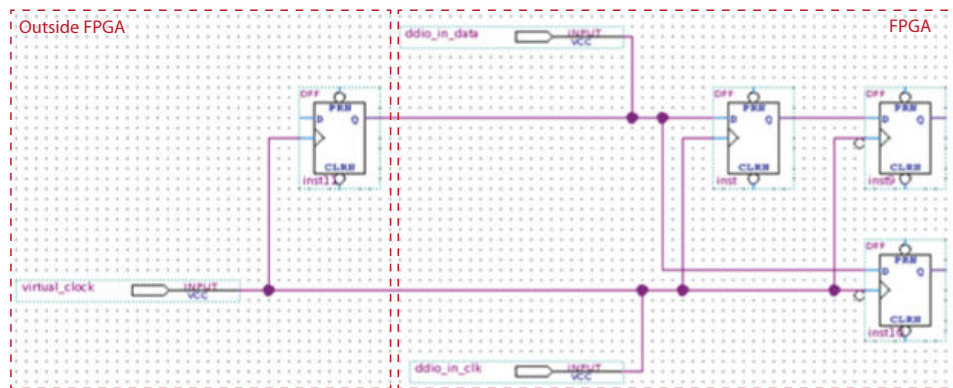


Table 65. DDIO Input Register .sdc Command Examples

Command	Command Example	Description
create_clock	create_clock -name virtual_clock -period "200 MHz"	Create clock setting for the virtual clock and the DDIO clock.
continued...		

Command	Command Example	Description
	create_clock -name ddio_in_clk -period "200 MHz" ddio_in_clk	
set_input_delay	set_input_delay -clock virtual_clock 0.25 ddio_in_data set_input_delay -add_delay -clock_fall -clock virtual_clock 0.25 ddio_in_data	Instruct the Timing Analyzer to analyze the positive clock edge and the negative clock edge of the transfer. Note the -add_delay in the second set_input_delay command.
set_false_path	set_false_path -fall_from virtual_clock -rise_to ddio_in_clk set_false_path -rise_from virtual_clock -fall_to ddio_in_clk	Instruct the Timing Analyzer to ignore the positive clock edge to the negative edge triggered register, and the negative clock edge to the positive edge triggered register.

### 7.7.3.3. Single Data Rate Output Register

Figure 50. Single Data Rate Output Register

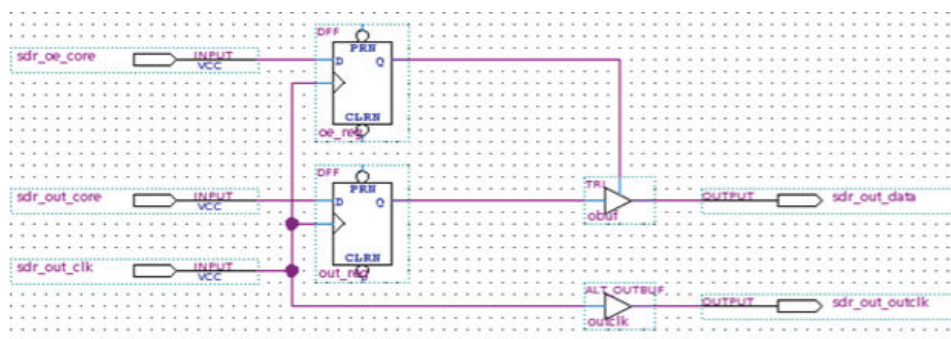


Table 66. Single Data Rate Output Register .sdc Command Examples

Command	Command Example	Description
create_clock and create_generated_ clock	create_clock -name sdr_out_clk -period "100 MHz" sdr_out_clk create_generated_clock -source sdr_out_clk -name sdr_out_outclk sdr_out_outclk	Generate the source clock and the output clock to transmit.
set_output_delay	set_output_delay -clock sdr_out_outclk 0.45 sdr_out_data	Instructs the Timing Analyzer to analyze the output data to transmit against the output clock to transmit.

### 7.7.3.4. DDIO Output Register

Table 67. DDIO Output Register .sdc Command Examples

Command	Command Example	Description
create_clock and create_generated_ clock	create_clock -name ddio_out_clk -period "200 MHz" ddio_out_clk	Generate the clocks to the DDIO and the clock to transmit.

*continued...*

Command	Command Example	Description
	<code>create_generated_clock -source ddio_out_clk -name ddio_out_outclk ddio_out_outclk</code>	
<code>set_output_delay</code>	<code>set_output_delay -clock ddio_out_outclk 0.55 ddio_out_data set_output_delay -add_delay -clock_fall -clock ddio_out_outclk 0.55 ddio_out_data</code>	Instruct the Timing Analyzer to analyze the positive and negative data against the output clock.
<code>set_false_path</code>	<code>set_false_path -rise_from ddio_out_clk -fall_to ddio_out_outclk set_false_path -fall_from ddio_out_clk -rise_to ddio_out_outclk</code>	Instruct the Timing Analyzer to ignore the rising edge of the source clock against the falling edge of the output clock, and the falling edge of source clock against rising edge of output clock

#### 7.7.4. Timing Closure Guidelines

For the GPIO input registers, the input I/O transfer is likely to fail the hold time if you do not set the input delay chain. This failure is caused by the clock delay being larger than the data delay.

However, if the I/O PLL drives the clocks of the GPIO input registers (simple register or DDIO mode), you can set the compensation mode to source synchronous mode. The Fitter automatically configures the I/O PLL to improve the setup and hold slack for the input I/O timing analysis.

For the GPIO output and output enable registers, you can add delay to the output data and clock using the output and output enable delay chains.

- If you observe setup time violation, you can increase the output clock delay chain setting.
- If you observe hold time violation, you can increase the output data delay chain setting.

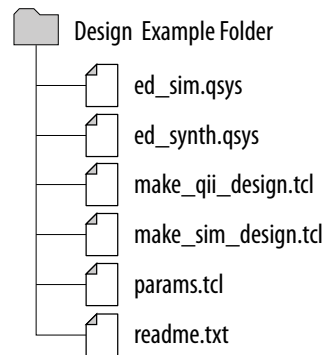
#### 7.8. GPIO FPGA IP Design Examples

The GPIO IP can generate design examples that match your IP configuration in the parameter editor. You can use these design examples as references for instantiating the IP and reviewing the expected behavior in simulations.

You can generate the design examples from the GPIO IP parameter editor. After you set the parameters that you want, click **Generate Example Design**. The IP parameter editor generates the design example source files in the directory you specify.



**Figure 51. Source Files in the Generated Design Example Directory**



**Note:** The `.qsys` files are for internal use during design example generation only. You cannot edit these `.qsys` files.

### 7.8.1. GPIO FPGA IP Synthesizable Quartus Prime Design Example

The synthesizable design example is a compilation-ready Platform Designer system that you can include in an Quartus Prime project.

#### Generating and Using the Design Example

To generate the synthesizable Quartus Prime design example from the source files, run the following command in the design example directory:

```
quartus_sh -t make_qii_design.tcl
```

To specify an exact device to use, run the following command:

```
quartus_sh -t make_qii_design.tcl [device_name]
```

The TCL script creates a `qii` directory that contains the `ed_synth.qpf` project file. You can open and compile this project in the Quartus Prime software.

### 7.8.2. GPIO FPGA IP Simulation Design Example

The simulation design example uses your GPIO IP parameter settings to build the IP instance connected to a simulation driver. The driver generates random traffic and internally checks the legality of the out going data.

Using the design example, you can run a simulation using a single command, depending on the simulator that you use. The simulation demonstrates how you can use the GPIO IP.

#### Generating and Using the Design Example

To generate the simulation design example from the source files for a Verilog simulator, run the following command in the design example directory:

```
quartus_sh -t make_sim_design.tcl
```

To generate the simulation design example from the source files for a VHDL simulator, run the following command in the design example directory:

```
quartus_sh -t make_sim_design.tcl VHDL
```

The TCL script creates a `sim` directory that contains subdirectories—one for each supported simulation tool. You can find the scripts for each simulation tool in the corresponding directories.

## 8. Programmable I/O Features Description

**Table 68. I/O Features and Description**

I/O Features	Description
Programmable Output Slew Rate Control	Each I/O pin contains a slew rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the signal. A faster slew rate provides high-speed transitions for high-performance systems while a slower slew rate reduces system noise and crosstalk but adds a nominal delay to the rising and falling edges.
Programmable IOE Delay	You can activate the programmable IOE delays to ensure zero hold time, minimize setup time, or increase the clock-to-output time. This feature helps read and write timing margins because it minimizes the uncertainties between signals on the bus. Each pin can have a different input delay from the pin-to-input register or a delay from output register-to-output pin values. This is to ensure that the signals within a bus have the same delay going into or out of the device.
Programmable Current Strength	You can assign current strength setting to the single-ended output buffer. For a list of I/O standards that support programmable current strength, refer to the related information. The current strength setting is not supported for: <ul style="list-style-type: none"> <li>• HSIO banks</li> <li>• Input-only pins</li> <li>• Pins with I/O standards that use true differential output buffers</li> <li>• Dedicated programming pins such as TDO</li> </ul>
Programmable Open-Drain Output	The programmable open-drain output provides a high-impedance state on output when logic to the output buffer is high. If logic to the output buffer is low, the output is low. You can attach several open-drain outputs to a wire. This connection type is like a logical OR function and is commonly called an active-low wired-OR circuit. If at least one of the outputs is in logic 0 state (active), the circuit sinks the current and brings the line to low voltage. You can use open-drain output if you are connecting multiple devices to a bus. For example, you can use the open-drain output for system-level control signals that can be asserted by any device or as an interrupt.
Programmable Pull-Up Resistor	Each I/O pin on supported banks provides an optional programmable pull-up resistor during user mode. The pull-up resistor weakly holds the I/O to the I/O bank power supply level.
Programmable Pull-Down Resistor	Each I/O pin on supported banks provides an optional programmable pull-down resistor during user mode. The pull-down resistor weakly holds the I/O to the ground level.
Programmable Pre-Emphasis	Pre-emphasis momentarily boosts the high-frequency component of the output signal during switching to increase the output slew rate. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line. For more information, refer to <a href="#">Programmable Pre-Emphasis</a> on page 100.
Programmable De-Emphasis	De-emphasis attenuates the I/O signal height when the symbol is longer than the specified duration. You can use de-emphasis to alter the signal amplitude to compensate for signal degradation over long transmission path. For more information, refer to <a href="#">Programmable De-Emphasis</a> on page 101.
Receiver Equalization Calibration	The FPGAs support Continuous Time Linear Equalization (CTLE) on all HSIO input buffers except for the 1.0 V, 1.05 V, 1.1 V, 1.2 V, and 1.3 V LVCMOS I/O standards. You can turn on CTLE for all external memory interface implementation except DDR5 and LPDDR5. For more information, refer to <a href="#">Continuous Time Linear Equalization</a> on page 103.
<i>continued...</i>	

I/O Features	Description
Programmable Differential Output Voltage	The programmable $V_{OD}$ settings allow you to adjust the output eye-opening to optimize the trace length and power consumption. A higher $V_{OD}$ swing improves voltage margins at the receiver end, and a smaller $V_{OD}$ swing reduces power consumption. For more information, refer to <a href="#">Programmable Differential Output Voltage</a> on page 102.
Schmitt Trigger	The Schmitt Trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt Triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This feature provides system noise tolerance on the device inputs but adds a small, nominal input delay.
On-Die Termination Impedance	The HPS and SDM input pins support on-die pull-up and pull-down termination. The on-die termination provides impedance matching and termination capabilities. You can enable this feature on input operations to minimize reflections and improve electrical margins.

#### Related Information

- [Programmable I/O Element Features for the HVIO Bank](#) on page 53
- [Programmable I/O Element Features for the HPS I/O Bank](#) on page 62

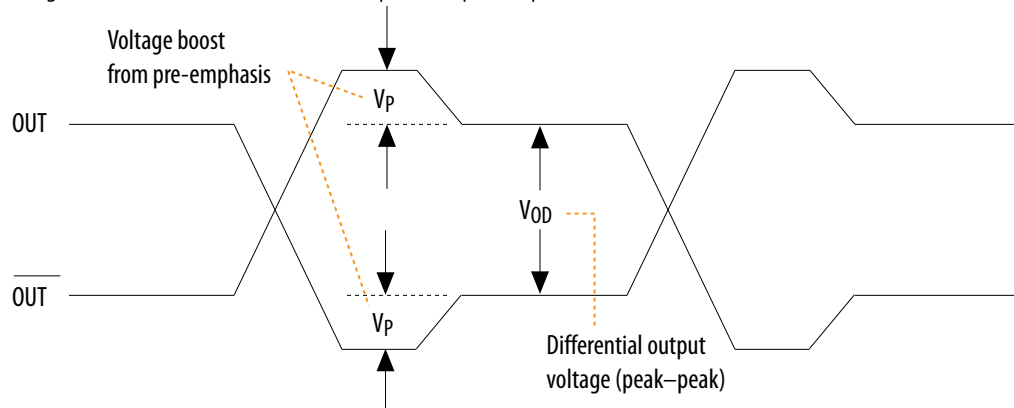
## 8.1. Programmable Pre-Emphasis

The  $V_{OD}$  setting and the output impedance of the driver set the output current limit of a high-speed transmission signal. At a high frequency, the slew rate may not be fast enough to reach the full  $V_{OD}$  level before the next edge, producing pattern-dependent jitter. With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate.

Pre-emphasis increases the amplitude of the high-frequency component of the output signal and thus helps to compensate for the frequency-dependent attenuation along the transmission line. The overshoot introduced by the extra current happens only during a change of state switching to increase the output slew rate and does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line.

**Figure 52. Programmable Pre-emphasis**

This figure shows the true differential output with pre-emphasis.



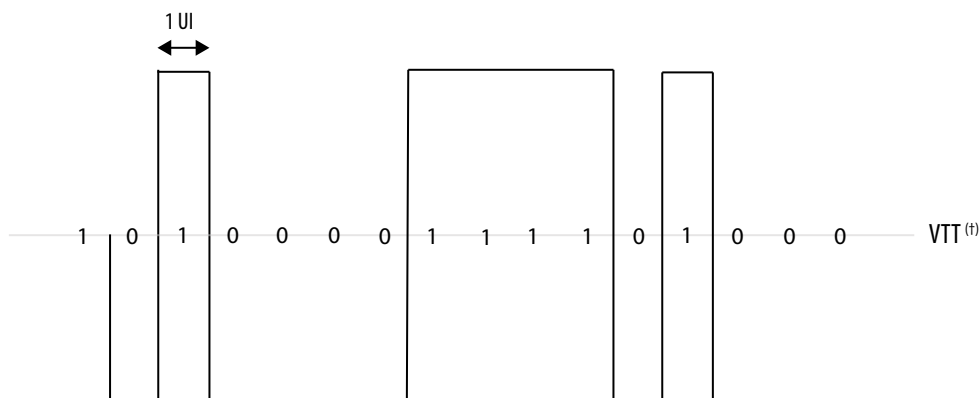
## 8.2. Programmable De-Emphasis

To compensate for signal degradation over long transmission path, you can alter the signal amplitude through the programmable de-emphasis feature.

**Table 69. Programmable De-Emphasis Feature Description**

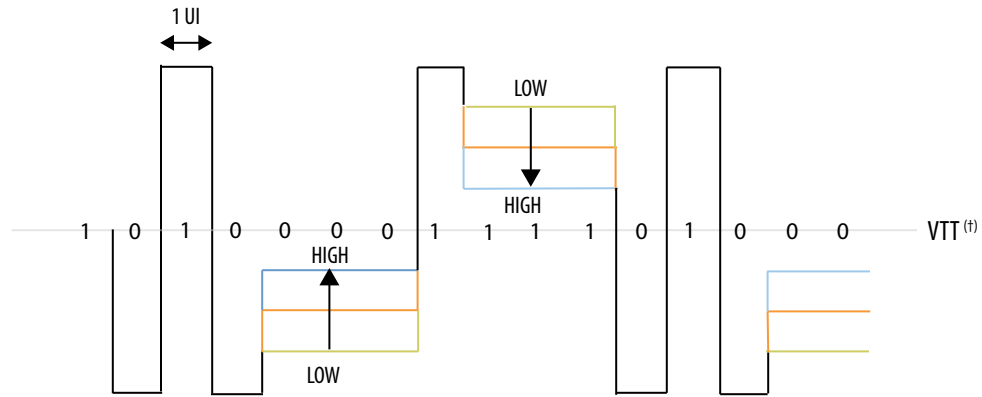
Item	Description
Availability	Available for the following I/O standards: <ul style="list-style-type: none"> <li>• SSTL-12 and Differential SSTL-12</li> <li>• HSTL-12 and Differential HSTL-12</li> <li>• HSUL-12 and Differential HSUL-12</li> <li>• POD 11 and Differential POD11</li> <li>• POD12 and Differential POD12</li> <li>• LVSTL11 and Differential LVSTL11</li> <li>• LVSTL105 and Differential LVSTL105</li> <li>• LVSTL700 and Differential LVSTL700</li> <li>• SLVS-400</li> <li>• DPHY</li> </ul>
Implementation	Two-tap de-emphasis implementation: <ul style="list-style-type: none"> <li>• A main tap</li> <li>• A delayed post tap at 1 UI</li> </ul>
Behavior	If turned on, the feature attenuates the I/O signal height, when the symbol is longer than 1 UI.
Types	<ul style="list-style-type: none"> <li>• Constant impedance de-emphasis: <ul style="list-style-type: none"> <li>— Provides double the effective equalization level of the low power de-emphasis.</li> <li>— Three equalization settings: low, medium, and high.</li> </ul> </li> <li>• Low power de-emphasis: <ul style="list-style-type: none"> <li>— Three equalization settings: low, medium, and high.</li> </ul> </li> </ul>
Recommendations	<ul style="list-style-type: none"> <li>• The de-emphasis effect reduces eye height. If you use a non-default de-emphasis setting, perform an IBIS or HSPICE simulation to estimate the I/O buffer's electrical performance.</li> <li>• To get the optimal setting for your design, start the simulation with the lowest de-emphasis setting. Then, fine-tune the setting until you get the best signal integrity condition.</li> </ul>

**Figure 53. De-Emphasis Off: Signal Attenuation for Supported I/O Standards**



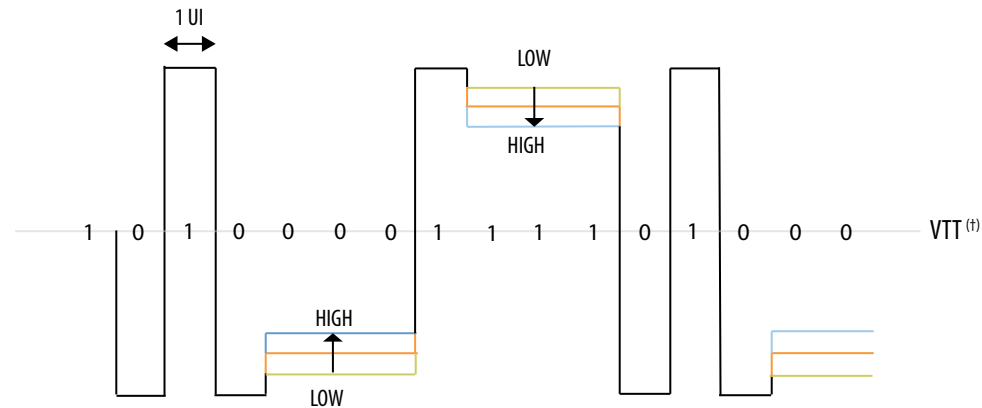
<sup>(†)</sup> Offset voltage has dependency on the board termination setup and voltages.

**Figure 54. Constant Impedance De-Emphasis: Signal Attenuation for Supported I/O Standards**



<sup>(†)</sup> Offset voltage has dependency on the board termination setup and voltages.

**Figure 55. Low Power De-Emphasis: Signal Attenuation for Supported I/O Standards**



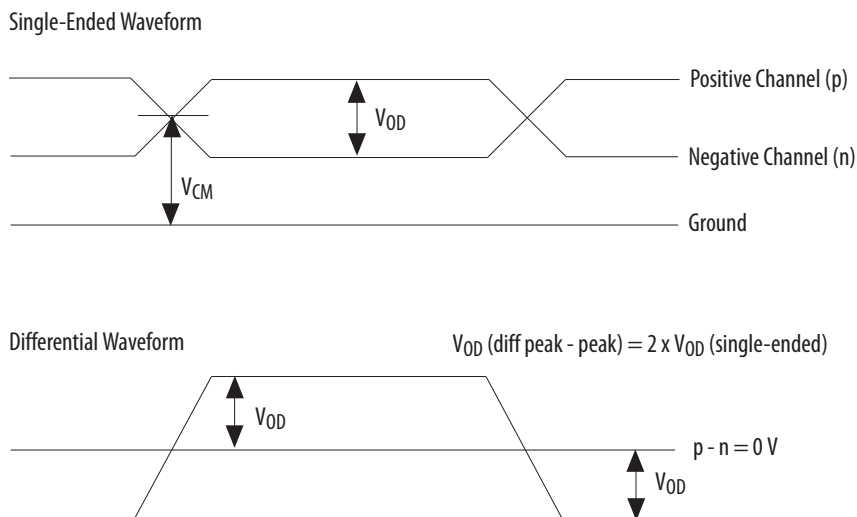
<sup>(†)</sup> Offset voltage has dependency on the board termination setup and voltages.

### 8.3. Programmable Differential Output Voltage

The programmable  $V_{OD}$  settings allow you to adjust the output eye-opening to optimize the trace length and power consumption. A higher  $V_{OD}$  swing improves voltage margins at the receiver end, and a smaller  $V_{OD}$  swing reduces power consumption. You can statically adjust the  $V_{OD}$  of the differential signal by changing the  $V_{OD}$  settings in the Quartus Prime software Assignment Editor.

**Figure 56. Differential  $V_{OD}$**

This figure shows the  $V_{OD}$  of the true differential output.



## 8.4. Continuous Time Linear Equalization

Each supported receiver uses a programmable equalization circuit that boosts the high-frequency gain of the incoming signal to compensate for the low-pass characteristics of the physical medium.

You can set this feature to automatically tune the receiver equalization settings based on the frequency content of the incoming signals. Through the automatic tuning, you can obtain the optimal CTLE settings.

The Agilex 5 FPGAs support a one-time receiver CTLE calibration. If you enable this feature, the calibration finds a stable receiver equalizer setting. Once found, the feature locks the equalizer value to the stable setting.

## 9. Document Revision History for the General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs

Document Version	Quartus Prime Version	Changes
2025.08.04	25.1.1	<ul style="list-style-type: none"> <li>Added new topic—<i>Clock Restrictions for GPIO Interfaces</i>.</li> <li>Updated <i>Placement Restrictions for True Differential and Single-Ended I/O Standards in the Same or Adjacent HSIO Bank</i>.</li> <li>Updated the note about <math>V_{REF}</math> <i>Sources and Input Standards Grouping</i>.</li> <li>Updated <i>Unused Pins</i>.</li> <li>Removed support for <i>Decision Feedback Equalization</i>.</li> <li>Added a note about package B23B in <i>HVIO Bank Overview</i>.</li> <li>Updated Table: <i>GPIO FPGA IP Current Release Information</i>.</li> <li>Updated the following IP names: <ul style="list-style-type: none"> <li>"Hard Processor System Intel Agilex 5 FPGA IP" to "Hard Processor System FPGA IP"</li> <li>"GPIO Intel® FPGA IP" to "GPIO FPGA IP"</li> </ul> </li> <li>Updated the note about the MIPI D-PHY interface in Table: <i>Types of I/O Interfaces</i>.</li> <li>Added the LVDS pin counts to the following figures: <ul style="list-style-type: none"> <li>Figure: <i>Package Options, Migrations, and I/O Pins—D-Series</i></li> <li>Figure: <i>Package Options, Migrations, and I/O Pins—E-Series</i></li> </ul> </li> <li>Updated the note about the Variable Pitch BGA (VPBGA) packaging throughout the document.</li> <li>Updated for latest branding standards.</li> </ul>
2025.02.17	24.3	Updated the guideline about the RZQ pin placement in <i>RZQ Pin Requirement</i> .
2024.10.07	24.3	<ul style="list-style-type: none"> <li>Updated the following figures: <ul style="list-style-type: none"> <li>Figure: <i>Package Options, Migrations, and I/O Pins—D-Series</i></li> <li>Figure: <i>Package Options, Migrations, and I/O Pins—E-Series</i></li> </ul> </li> <li>Updated the guidelines in <math>V_{CCIO\_PIO}</math> <i>Supply for Unused HSIO Banks</i>.</li> <li>Removed information about True Differential Signaling from Group 4 and 5 in Table: <i>Input Standards Groups Per I/O Lane</i>.</li> <li>Removed topic <i>Guidelines: Programmable Receiver Equalization Calibration</i>.</li> <li>Clarified that <math>V_{CCIO\_PIO}</math> refers to the real-time onboard voltage supply in <i>HSIO Buffer Behavior</i>.</li> <li>Updated <i>HVIO Buffer Behavior</i>: <ul style="list-style-type: none"> <li>Updated the HVIO pins guideline for the <b>Not turned on</b> pin state.</li> <li>Clarified that <math>V_{CCIO\_HVIO}</math> refers to the real-time onboard voltage supply.</li> </ul> </li> <li>Added the topic about assigning pin I/O standards in the Quartus Prime pin planner for the HVIO banks.</li> <li>Updated the guidelines for I/O pins in HVIO banks during power sequencing.</li> </ul>
continued...		



Document Version	Quartus Prime Version	Changes
		<ul style="list-style-type: none"><li>Clarified that <math>V_{CCIO\_HPS}</math> refers to the real-time onboard voltage supply in <i>HPS I/O Buffer Behavior</i>.</li><li>Clarified that <math>V_{CCIO\_SDM}</math> refers to the real-time onboard voltage supply in <i>SDM I/O Buffer Behavior</i>.</li><li>Added information about delay calculations in Delay Elements.</li></ul>
2024.04.05	24.1	Initial release.