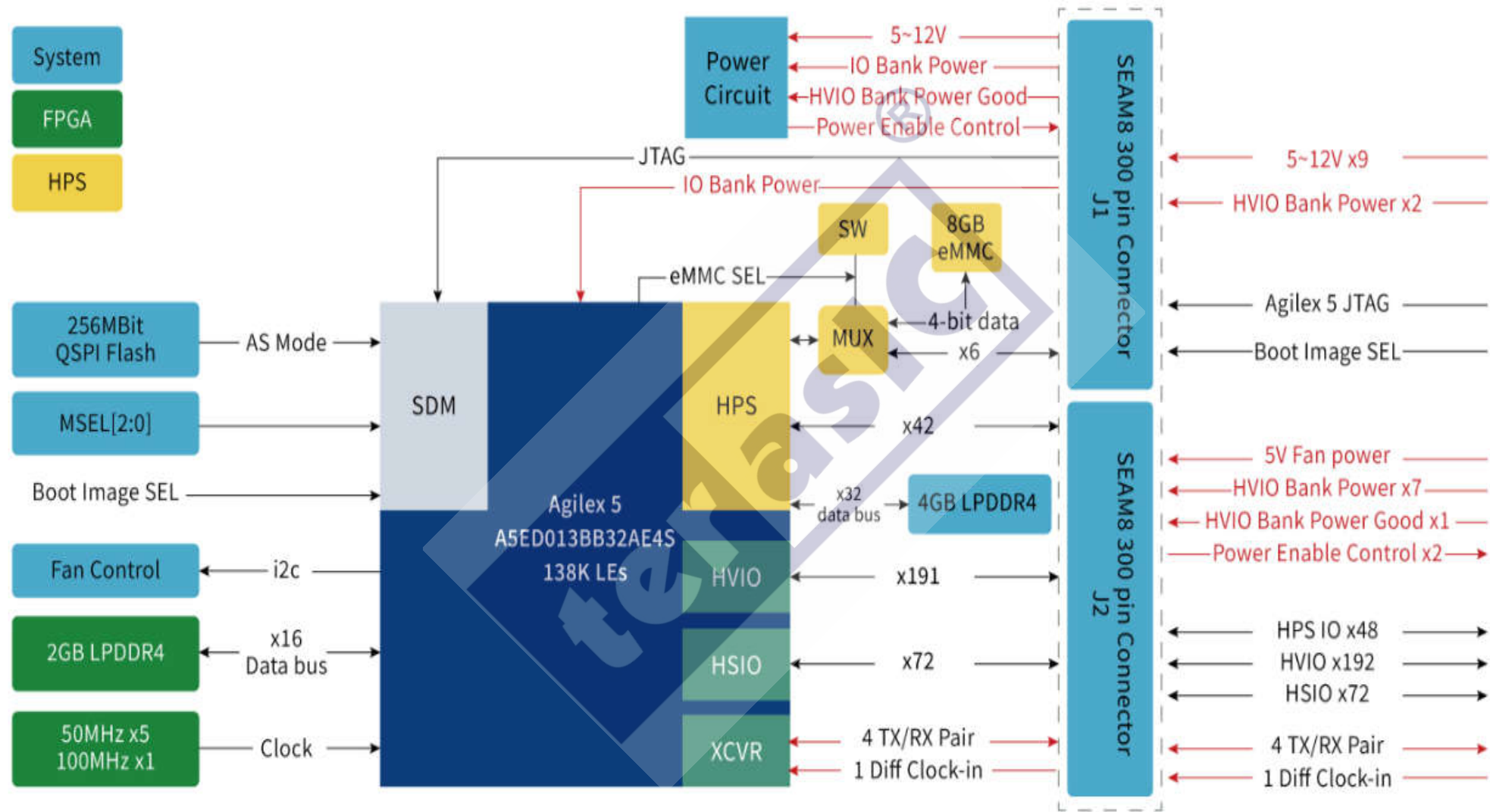


# Comet A13 SOM

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26	HPS eMMC, SDIO Port Expander		
27	6x50 B2B Connector, J1		
28	6x50 B2B Connector, J2		
29	FAN Control and Temperature Monitor		

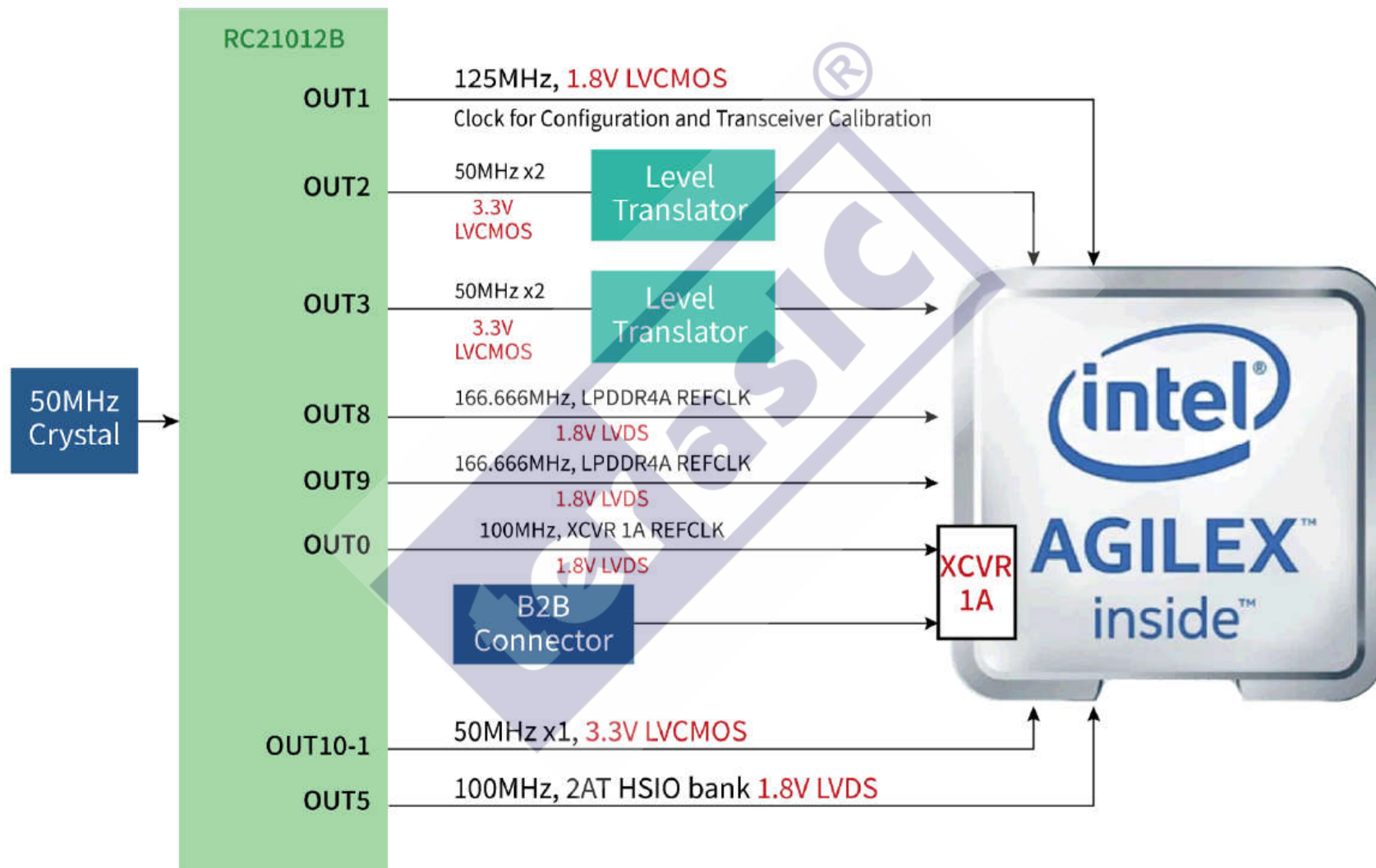
Block Diagram




# Clock Tree

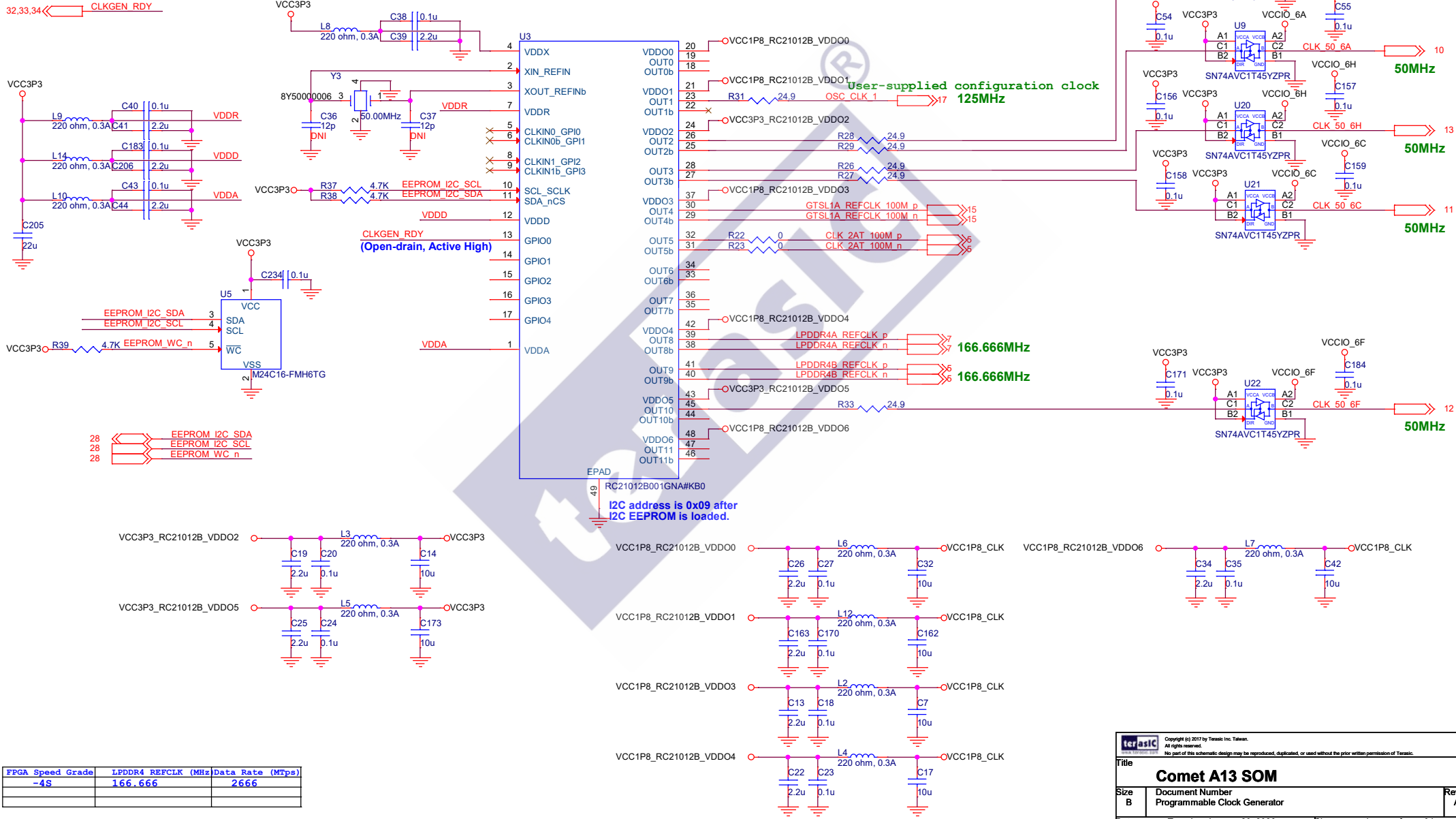
## 12-output Clock Generator

RC21012B001GNA#KB0

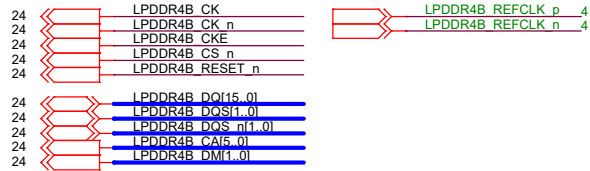


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Title <b>Comet A13 SOM</b>		
Size B	Document Number Clock Tree	Rev A
Date:	Tuesday, January 20, 2026	Sheet 3 of 34

# Programmable Clock Generator



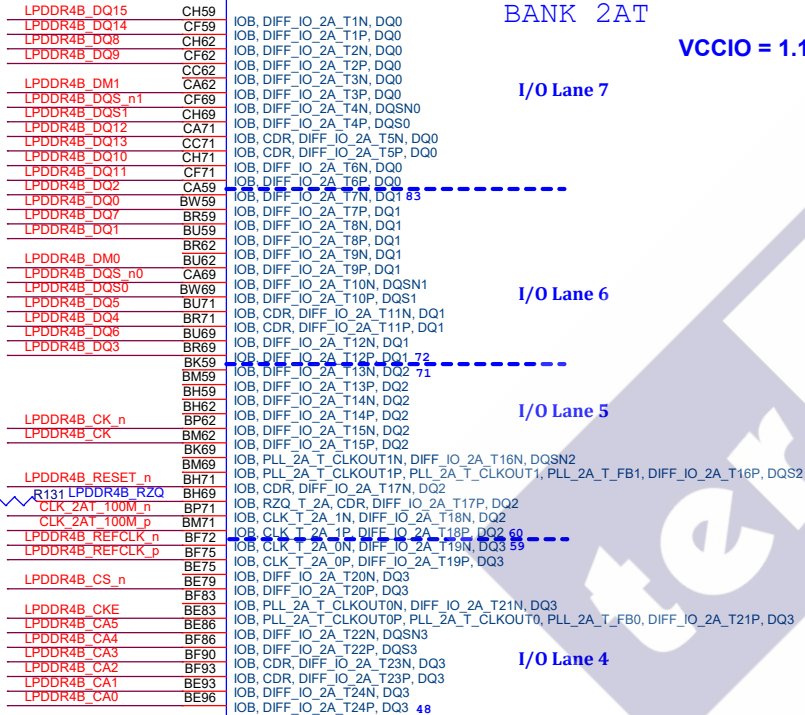
## LPDDR4B



CLK 2AT 100M p\_4  
CLK 2AT 100M n\_4

J1 HSIO 2AB A\_n[24:1]  
J1 HSIO 2AB A\_n[24:1]

U6C



BANK 2AT

VCCIO = 1.1V

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

BANK 2AB

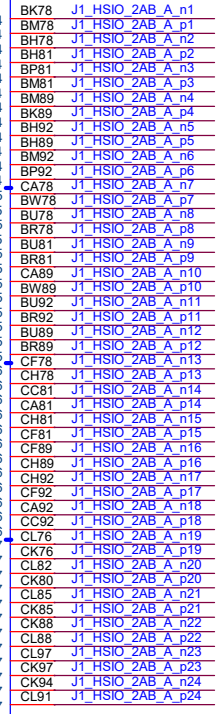
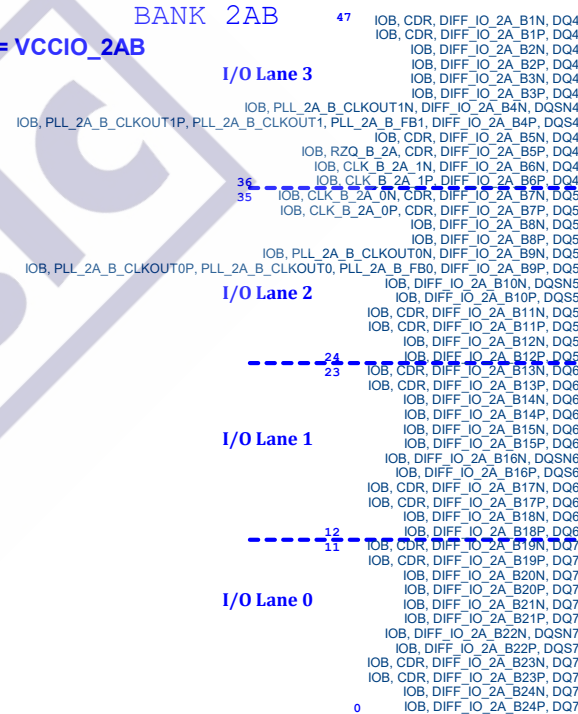
VCCIO = VCCIO\_2AB

I/O Lane 3


I/O Lane 2

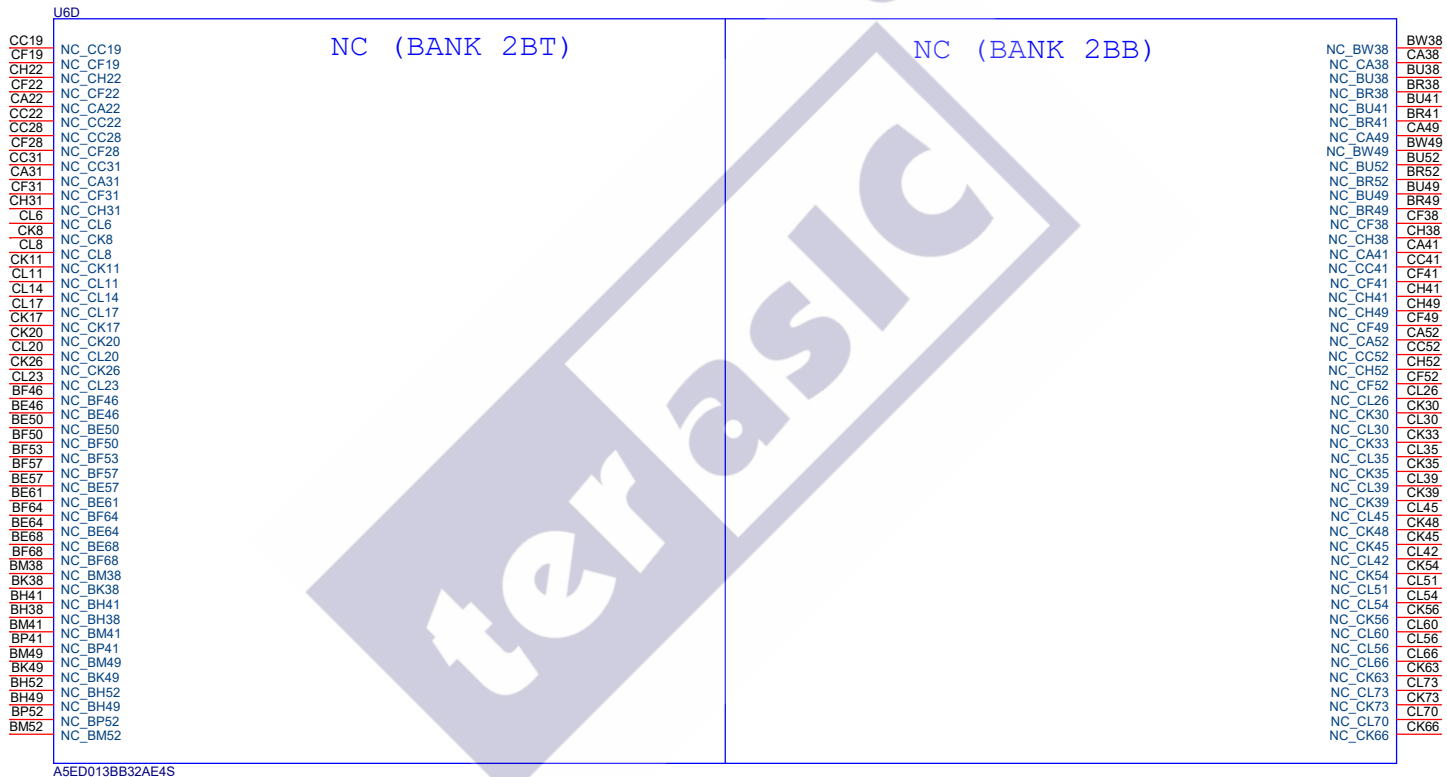
I/O Lane 1

I/O Lane 0




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Title <b>Comet A13 SOM</b>		
Size B	Document Number FPGA Bank 2A	Rev A
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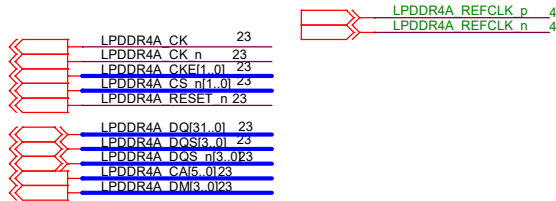


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Title <b>Comet A13 SOM</b>		
Size <b>B</b>	Document Number <b>FPGA NC (2B)</b>	Rev <b>A</b>
Date: <b>Tuesday, January 20, 2026</b>	Sheet <b>6</b>	of <b>34</b>



## LPDDR4A



U6E

VCCIO = 1.1V

BANK 3AT


BANK 3AB

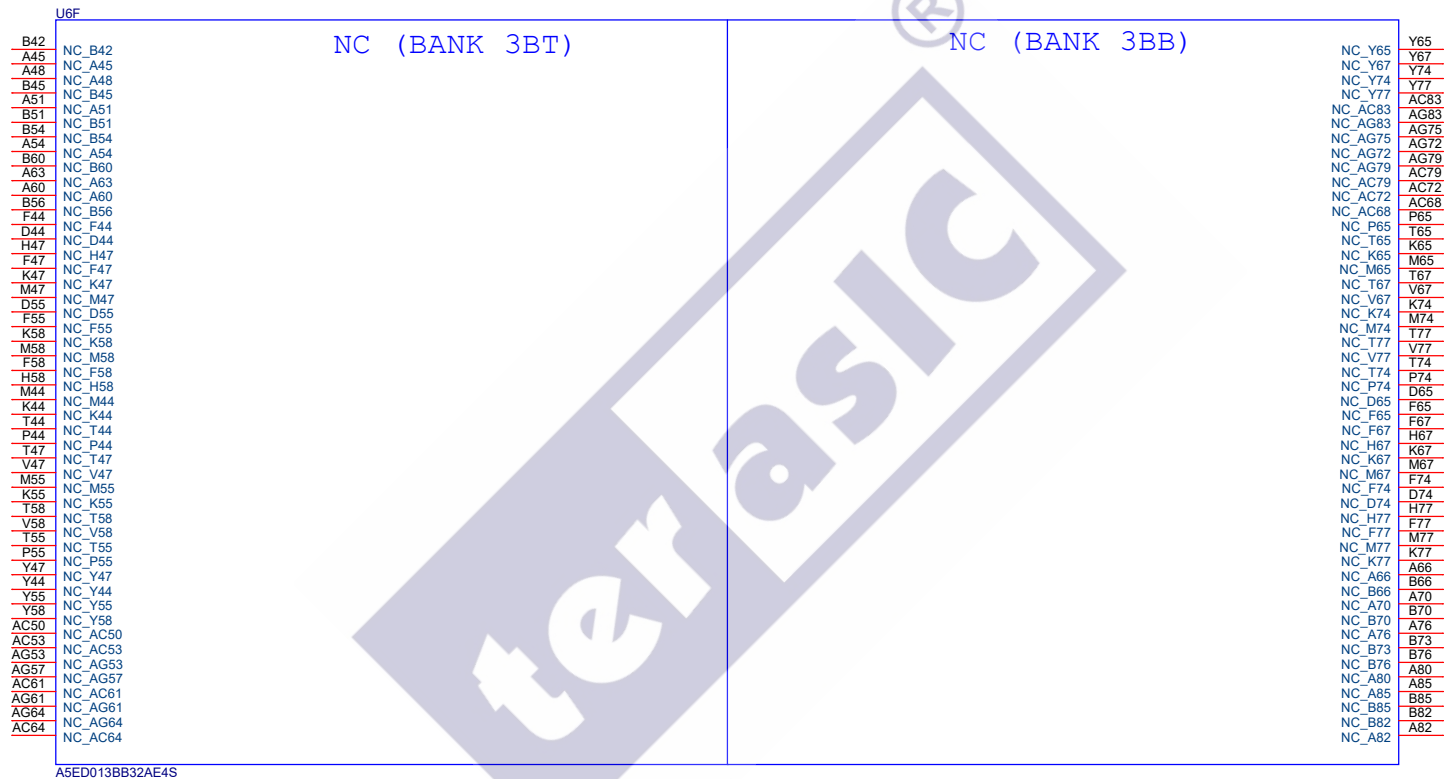
LPDDR4A_DQ17	A91
LPDDR4A_DQ16	B88
LPDDR4A_DQ22	A94
LPDDR4A_DQ23	B91
LPDDR4A_DM2	B97
LPDDR4A_DQS_n2	B101
LPDDR4A_DQS2	A101
LPDDR4A_DQ19	A110
LPDDR4A_DQ18	B106
LPDDR4A_DQ21	B103
LPDDR4A_DQ20	A106
LPDDR4A_DQ30	D84
LPDDR4A_DQ31	F84
LPDDR4A_DQ24	M87
LPDDR4A_DQ25	K87
LPDDR4A_DM3	F87
LPDDR4A_DQS_n3	D95
LPDDR4A_DQS3	F95
LPDDR4A_DQ26	K98
LPDDR4A_DQ29	M98
LPDDR4A_DQ28	F98
LPDDR4A_DQ27	H98
J2_HSIO_3AT_A_n13	P84
J2_HSIO_3AT_A_p13	T84
J2_HSIO_3AT_A_n14	M84
J2_HSIO_3AT_A_p14	K84
J2_HSIO_3AT_A_n15	T87
J2_HSIO_3AT_A_p15	V87
J2_HSIO_3AT_A_n16	M95
J2_HSIO_3AT_A_p16	K95
J2_HSIO_3AT_A_n17	T95
J2_HSIO_3AT_A_p17	P95
J2_HSIO_3AT_A_n18	T98
J2_HSIO_3AT_A_p18	V98
J2_HSIO_3AT_A_n19	Y84
J2_HSIO_3AT_A_p19	Y87
J2_HSIO_3AT_A_n20	Y95
J2_HSIO_3AT_A_p20	Y98
J2_HSIO_3AT_A_n21	AC86
J2_HSIO_3AT_A_p21	AC90
J2_HSIO_3AT_A_n22	AC93
J2_HSIO_3AT_A_p22	AC90
J2_HSIO_3AT_A_n23	AC96
J2_HSIO_3AT_A_p23	AC100
J2_HSIO_3AT_A_n24	AG104
J2_HSIO_3AT_A_p24	AG100



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Title <b>Comet A13 SOM</b>		
Size B	Document Number FPGA Bank 3A	Rev A
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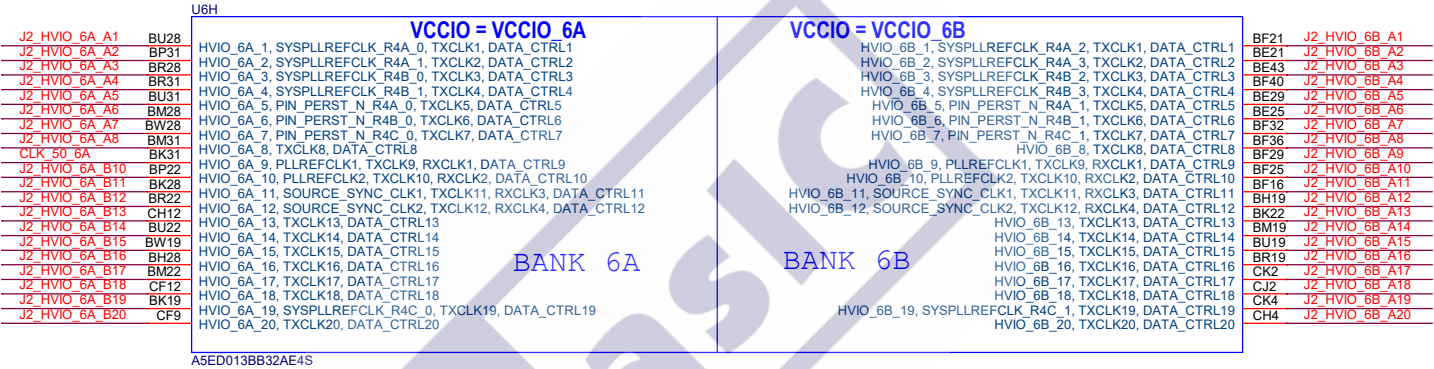
B2B Connector J1 Interface



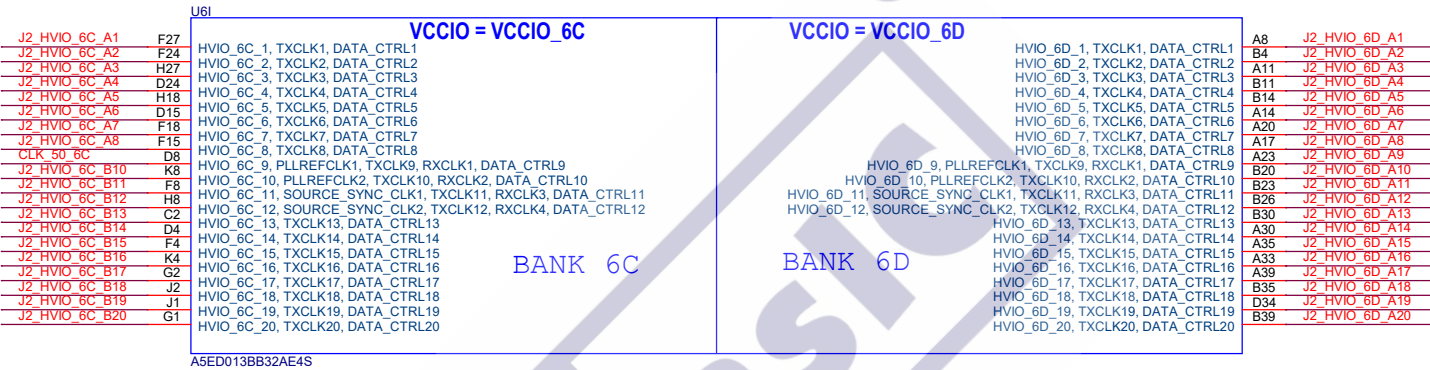
U6G			VCCIO = VCCIO_5A		VCCIO = VCCIO_5B			
J1 HVIO_5A_A1	CD134		HVIO_5A_1, SYSPLLREFCLK_L1A_0, TXCLK1, DATA_CTRL1		HVIO_5B_1, SYSPLLREFCLK_L1A_2, TXCLK1, DATA_CTRL1		BF111	J1 HVIO_5B_A1
J1 HVIO_5A_A2	CD135		HVIO_5A_2, SYSPLLREFCLK_L1A_1, TXCLK2, DATA_CTRL2		HVIO_5B_2, SYSPLLREFCLK_L1A_3, TXCLK2, DATA_CTRL2		BH109	J1 HVIO_5B_A2
J1 HVIO_5A_A3	CG134		HVIO_5A_3, SYSPLLREFCLK_L1B_0, TXCLK3, DATA_CTRL3		HVIO_5B_3, SYSPLLREFCLK_L1B_2, TXCLK3, DATA_CTRL3		BE115	J1 HVIO_5B_A3
J1 HVIO_5A_A4	CG135		HVIO_5A_4, SYSPLLREFCLK_L1B_1, TXCLK4, DATA_CTRL4		HVIO_5B_4, SYSPLLREFCLK_L1B_3, TXCLK4, DATA_CTRL4		BF115	J1 HVIO_5B_A4
J1 HVIO_5A_A5	CH132		HVIO_5A_5, PIN_PERST_N_CVP_L1A_0, TXCLK5, DATA_CTRL5		HVIO_5B_5, PIN_PERST_N_CVP_L1A_1, TXCLK5, DATA_CTRL5		BF107	J1 HVIO_5B_A5
J1 HVIO_5A_A6	CF132		HVIO_5A_6, PIN_PERST_N_CVP_L1B_0, TXCLK6, DATA_CTRL6		HVIO_5B_6, PIN_PERST_N_CVP_L1B_1, TXCLK6, DATA_CTRL6		BU109	J1 HVIO_5B_A6
J1 HVIO_5A_A7	CF128		HVIO_5A_7, PIN_PERST_N_CVP_L1C_0, TXCLK7, DATA_CTRL7		HVIO_5B_7, PIN_PERST_N_CVP_L1C_1, TXCLK7, DATA_CTRL7		BF104	J1 HVIO_5B_A7
J1 HVIO_5A_A8	CK134		HVIO_5A_8, TXCLK8, DATA_CTRL8		HVIO_5B_8, TXCLK8, DATA_CTRL8		BR109	J1 HVIO_5B_A8
CLK 50_5A	CH128		HVIO_5A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9		HVIO_5B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9		BE107	J1 HVIO_5B_A9
J1 HVIO_5A_B10	CL125		HVIO_5A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10		HVIO_5B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10		BK109	J1 HVIO_5B_A10
J1 HVIO_5A_B11	CF121		HVIO_5A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11		HVIO_5B_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11		BE111	J1 HVIO_5B_A11
J1 HVIO_5A_B12	CF118		HVIO_5A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12		HVIO_5B_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12		BM109	J1 HVIO_5B_A12
J1 HVIO_5A_B13	BU118		HVIO_5A_13, TXCLK13, DATA_CTRL13		HVIO_5B_13, TXCLK13, DATA_CTRL13		BR112	J1 HVIO_5B_A13
J1 HVIO_5A_B14	BR118		HVIO_5A_14, TXCLK14, DATA_CTRL14		HVIO_5B_14, TXCLK14, DATA_CTRL14		BK118	J1 HVIO_5B_A14
J1 HVIO_5A_B15	CA118		HVIO_5A_15, TXCLK15, DATA_CTRL15		HVIO_5B_15, TXCLK15, DATA_CTRL15		BM118	J1 HVIO_5B_A15
J1 HVIO_5A_B16	BW118		HVIO_5A_16, TXCLK16, DATA_CTRL16		HVIO_5B_16, TXCLK16, DATA_CTRL16		BP112	J1 HVIO_5B_A16
J1 HVIO_5A_B17	CL128		HVIO_5A_17, TXCLK17, DATA_CTRL17		HVIO_5B_17, TXCLK17, DATA_CTRL17		BM112	J1 HVIO_5B_A17
J1 HVIO_5A_B18	CL130		HVIO_5A_18, TXCLK18, DATA_CTRL18		HVIO_5B_18, TXCLK18, DATA_CTRL18		BK112	J1 HVIO_5B_A18
J1 HVIO_5A_B19	CK125		HVIO_5A_19, SYSPLLREFCLK_L1C_0, TXCLK19, DATA_CTRL19		HVIO_5B_19, SYSPLLREFCLK_L1C_1, TXCLK19, DATA_CTRL19		BH118	J1 HVIO_5B_A19
J1 HVIO_5A_B20	CK128		HVIO_5A_20, TXCLK20, DATA_CTRL20		HVIO_5B_20, TXCLK20, DATA_CTRL20		BF120	J1 HVIO_5B_A20

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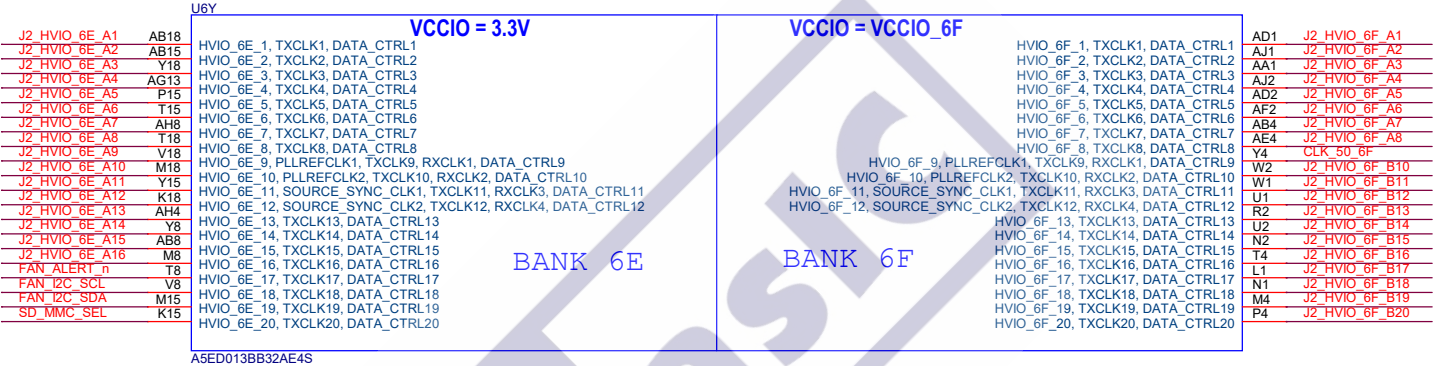
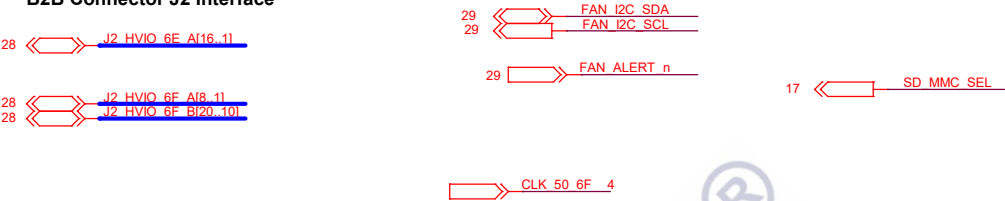
B2B Connector J2 Interface



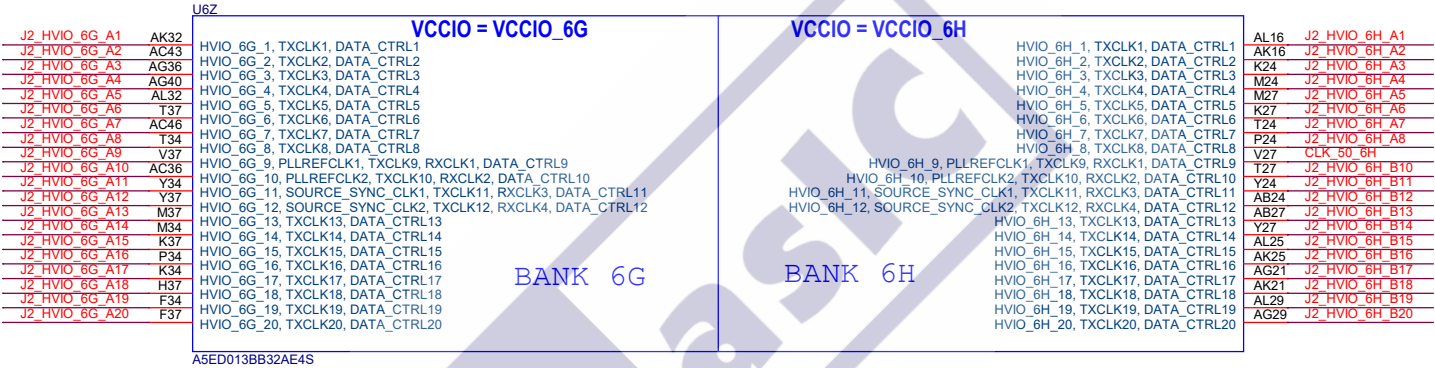
B2B Connector J2 Interface



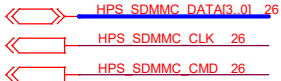
B2B Connector J2 Interface




B2B Connector J2 Interface

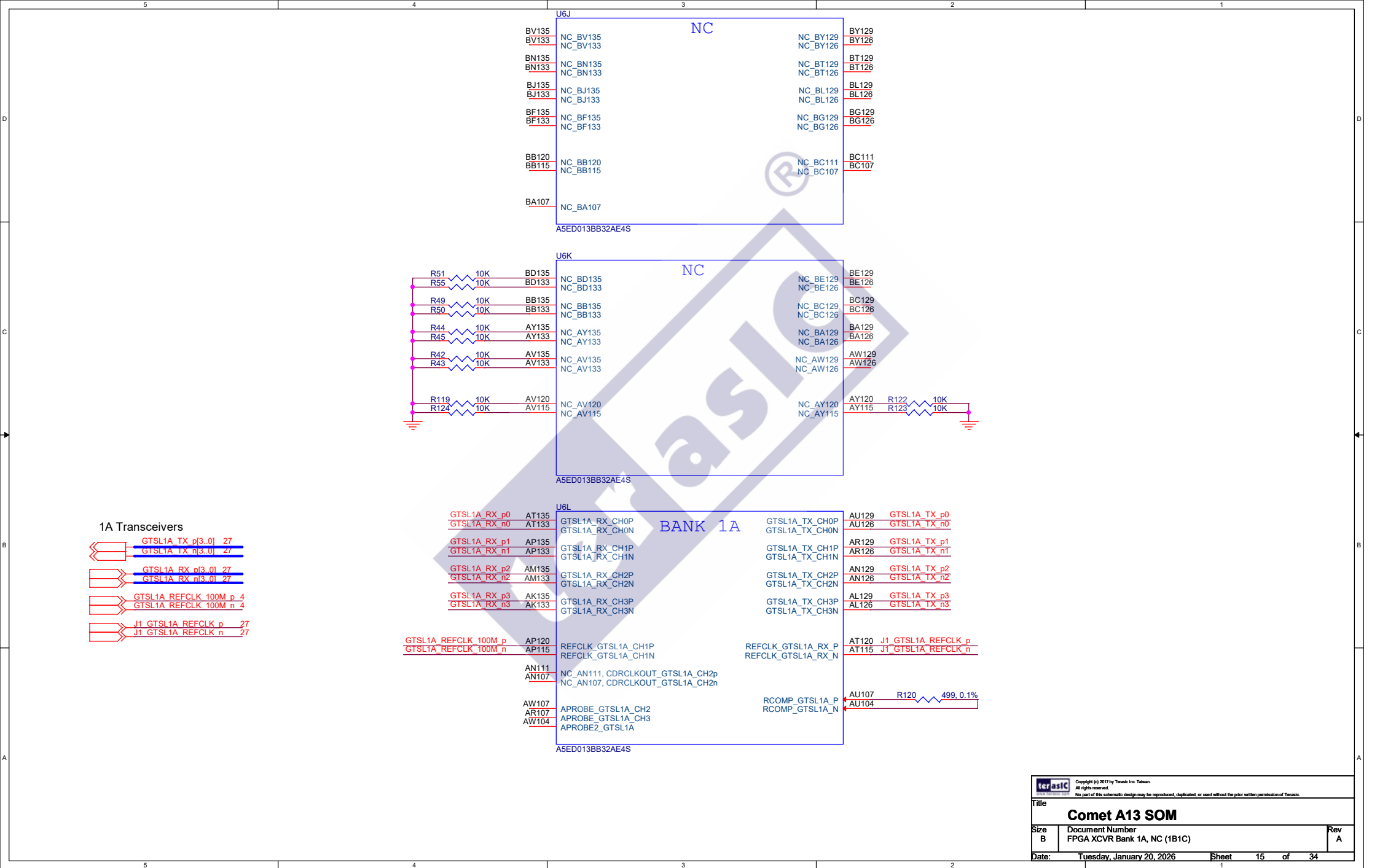


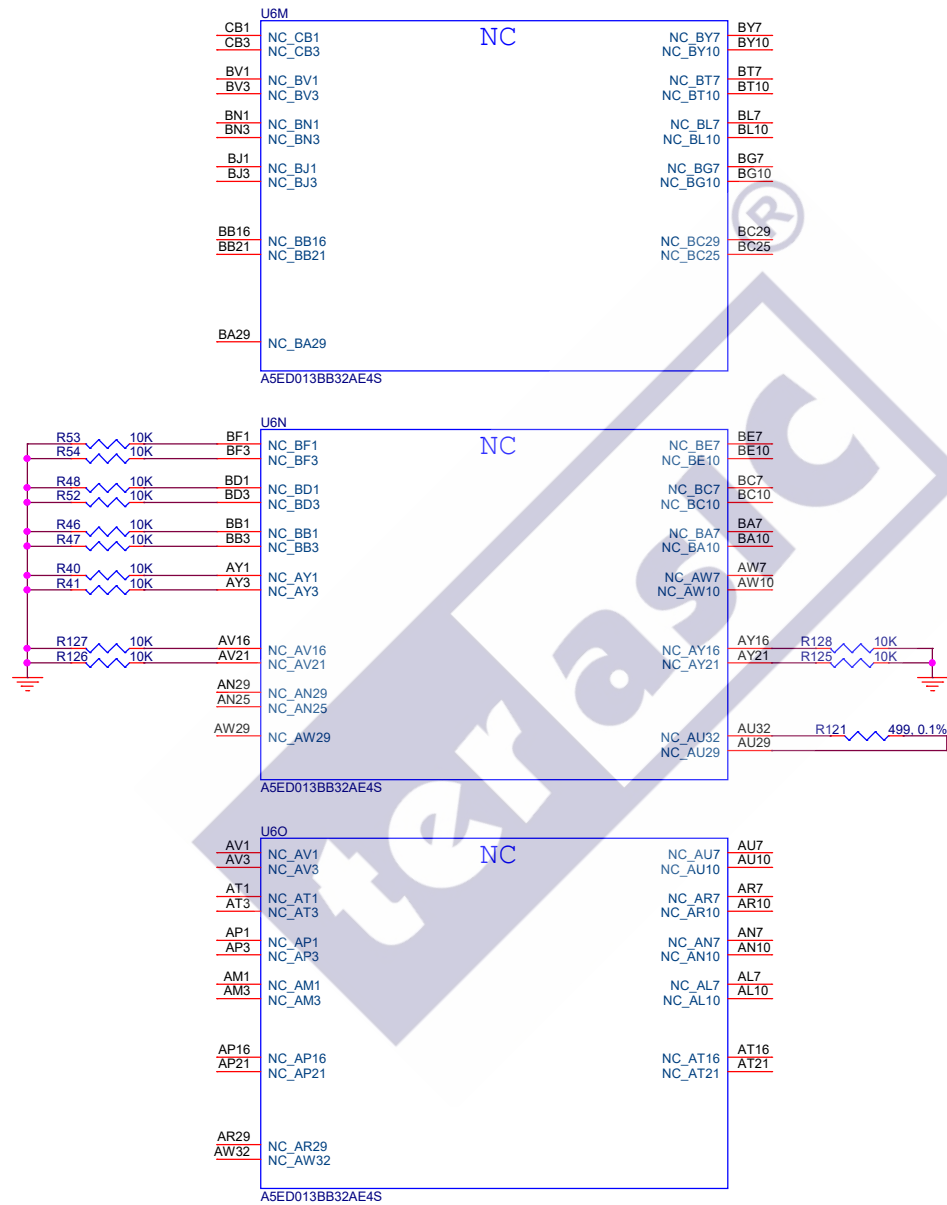
SD/eMMC Interface



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Title			
Comet A13 SOM			
Size	Document Number		Rev
B	FPGA Bank HPS		A
Date:	Tuesday, January 20, 2026	Sheet	14 of 34







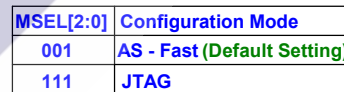
AG JTAG TCK 27  
AG JTAG TMS 27  
AG JTAG TDI 27  
AG JTAG TDO 27

Image\_Factory 27

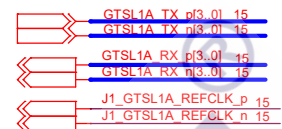
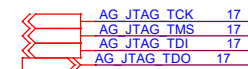
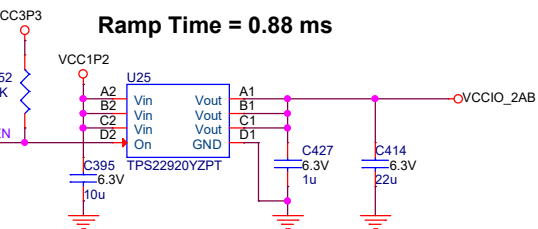
AS RST n 25

TEMPDIODE FPGA p29  
TEMPDIODE FPGA n29

FPGA AS CLK	25
FPGA AS DATA0	25
FPGA AS DATA1	25
FPGA AS DATA2	25
FPGA AS DATA3	25
FPGA nCS0	25



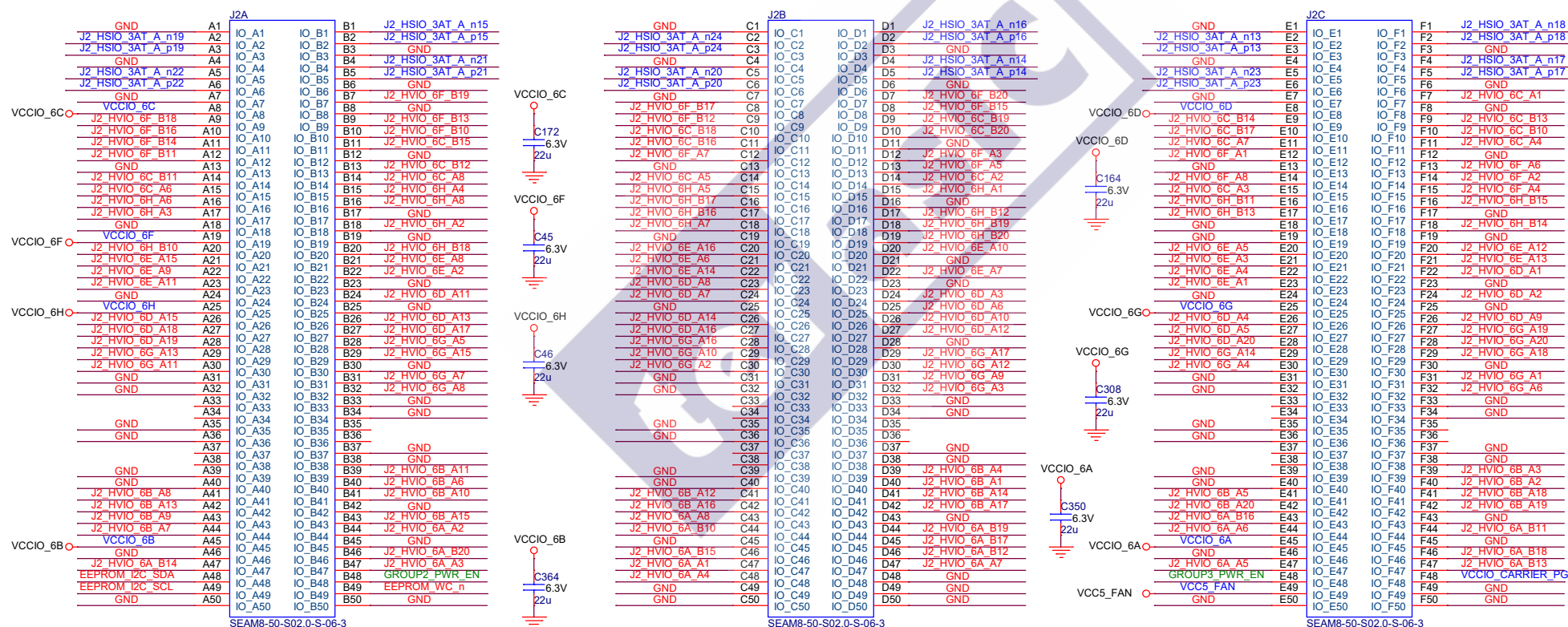
SDMMC Bus Device select	
SW1.2 Position	Target device
OFF	eMMC
ON	SD Card



34 VCCIO CARRIER PG

GROUP3 PWR EN 31.33.34

EEPROM I2C SDA  
EEPROM I2C SCL  
EEPROM WC\_n



Title **Comet A13 SOM**

Size	Document Number
B	6x50 B2B Connector, J2

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