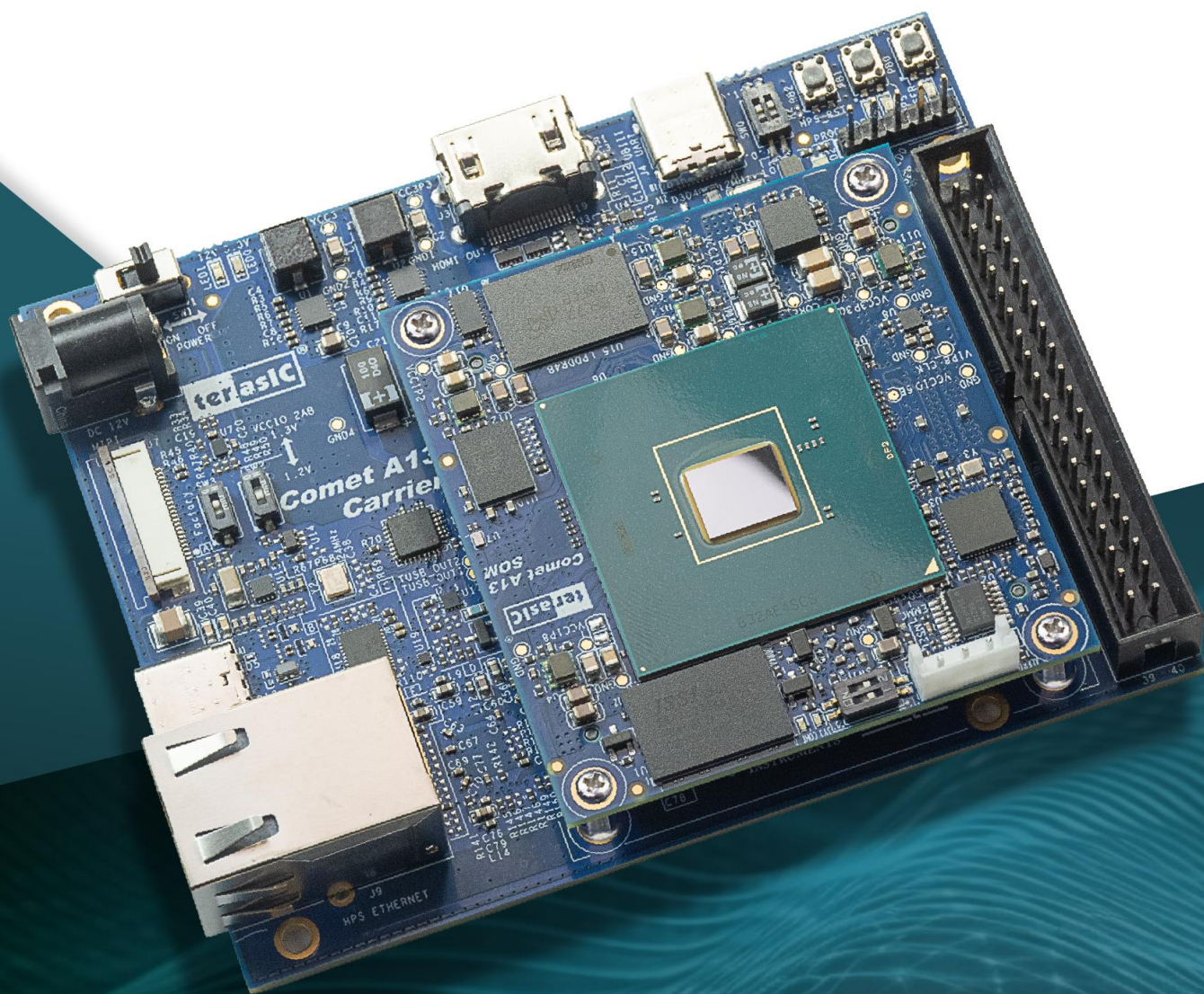


Comet-A13 Evaluation Kit



User Manual

CONTENTS

FPGA

Chapter 1	Overview	2
1.1	General Description	2
1.2	Key Features.....	2
1.3	Block Diagram	3
Chapter 2	Board Components	4
2.1	Overview	4
2.2	Power Input and Switch	5
2.3	Setup and Status Components	5
2.4	Reset Device.....	7
2.5	Clock Tree	8
2.6	USB Blaster III.....	8
2.7	General User I/O	9
2.8	2x20 GPIO Expansion Header	11
2.9	MIPI Connector.....	12
2.10	HDMI TX.....	14
2.11	HPS Gigabit Ethernet	15
2.12	HPS USB.....	17
2.13	USB to UART	19
2.14	HPS MicroSD Card.....	20
2.15	6x50 B2B Connector.....	20
Chapter 3	Board Assembly and Disassembly	22
Chapter 4	Additional Information.....	23
4.1	Getting Help.....	23



Chapter 1

Overview

This chapter provides an overview of the Comet A13 EVK's Carrier board and installation guide.

1.1 General Description

The Comet A13 Evaluation Kit (EVK) consists of a Comet A13 System on Module (SoM) and a Comet A13 Carrier Board (see **Figure 1-1**). The SoM is installed onto the carrier board via two SEAM8 connectors.

This manual focuses primarily on the features, interface specifications, and usage of the Comet A13 Carrier Board. For detailed information regarding the Comet A13 SoM, please refer to the dedicated Comet A13 SoM User Manual.

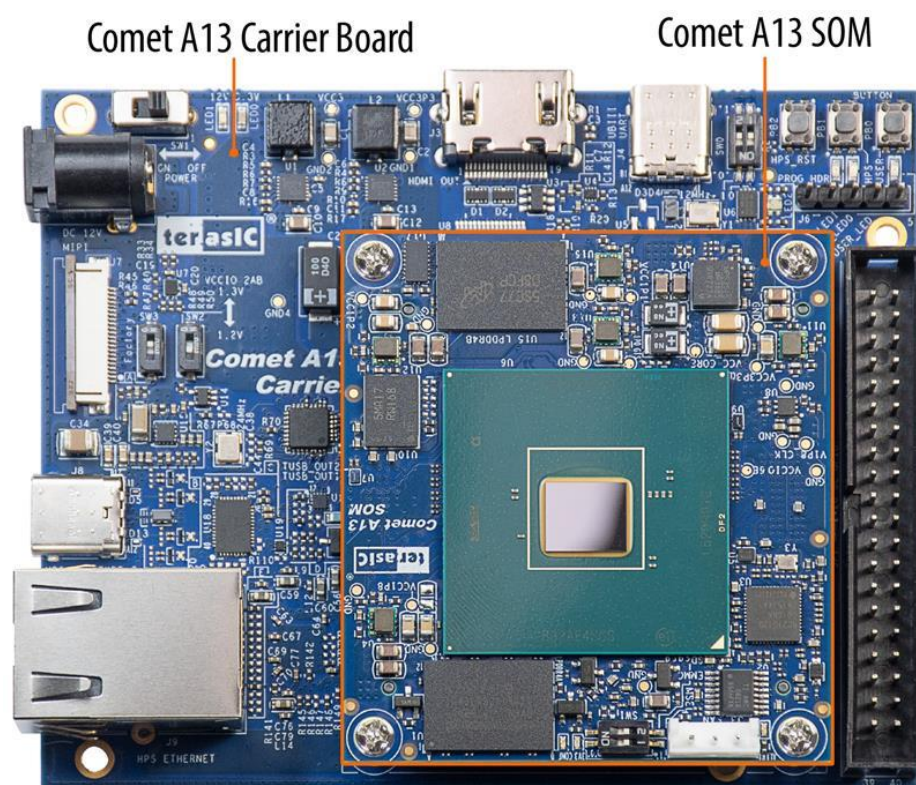


Figure 1-1 The Comet A13 Evaluation Kit

1.2 Key Features

The following hardware is implemented on the Comet A13 Carrier board:

- **Carrier Board System:**
 - On-Board USB Blaster III

- 12V DC Jack power input
 - Dual SEAF8 300-pin Connector (6x50 pin) for Module installation
 - Board Size: 80mm x 100mm
- Carrier Board FPGA Subsystem:
 - LED x1, Switch x2, Button x1
 - HDMI Out (1080P)
 - One 22-pin MIPI Connector (4 Data Lane) for CSI2 Camera
 - One 3.3V 2x20 DE-GPIO Header
 - Carrier Board HPS Subsystem:
 - LED x2, Button x1
 - UART Port (Type-C Connector)
 - Gigabit Ethernet PHY via RJ45
 - MicroSD Socket
 - HPS Cold Reset Button

1.3 Block Diagram

Figure 1-2 shows the block diagram of the Comet A13 Carrier board.

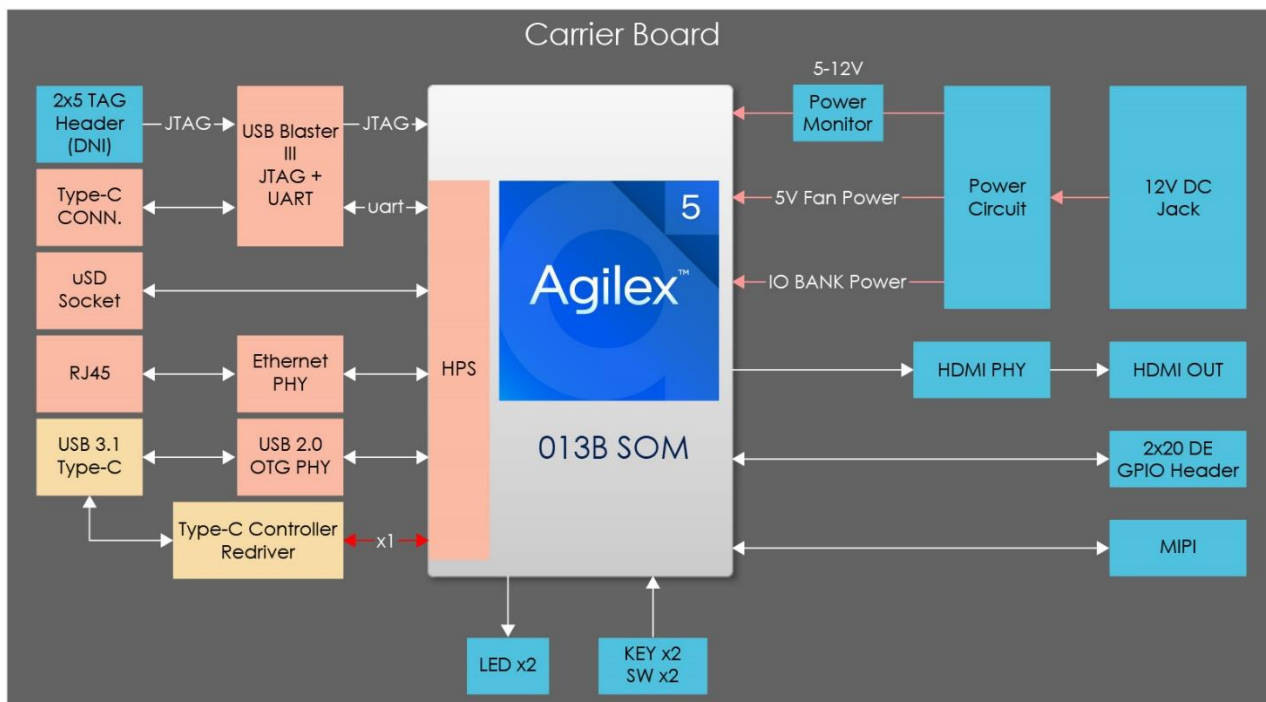


Figure 1-2 Block Diagram of the Comet A13 Carrier Board

Chapter 2

Board Components

This chapter introduces all the important components on the Comet A13 Carrier board.

2.1 Overview

Figure 2-1 is the top view of the Comet A13 Carrier board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

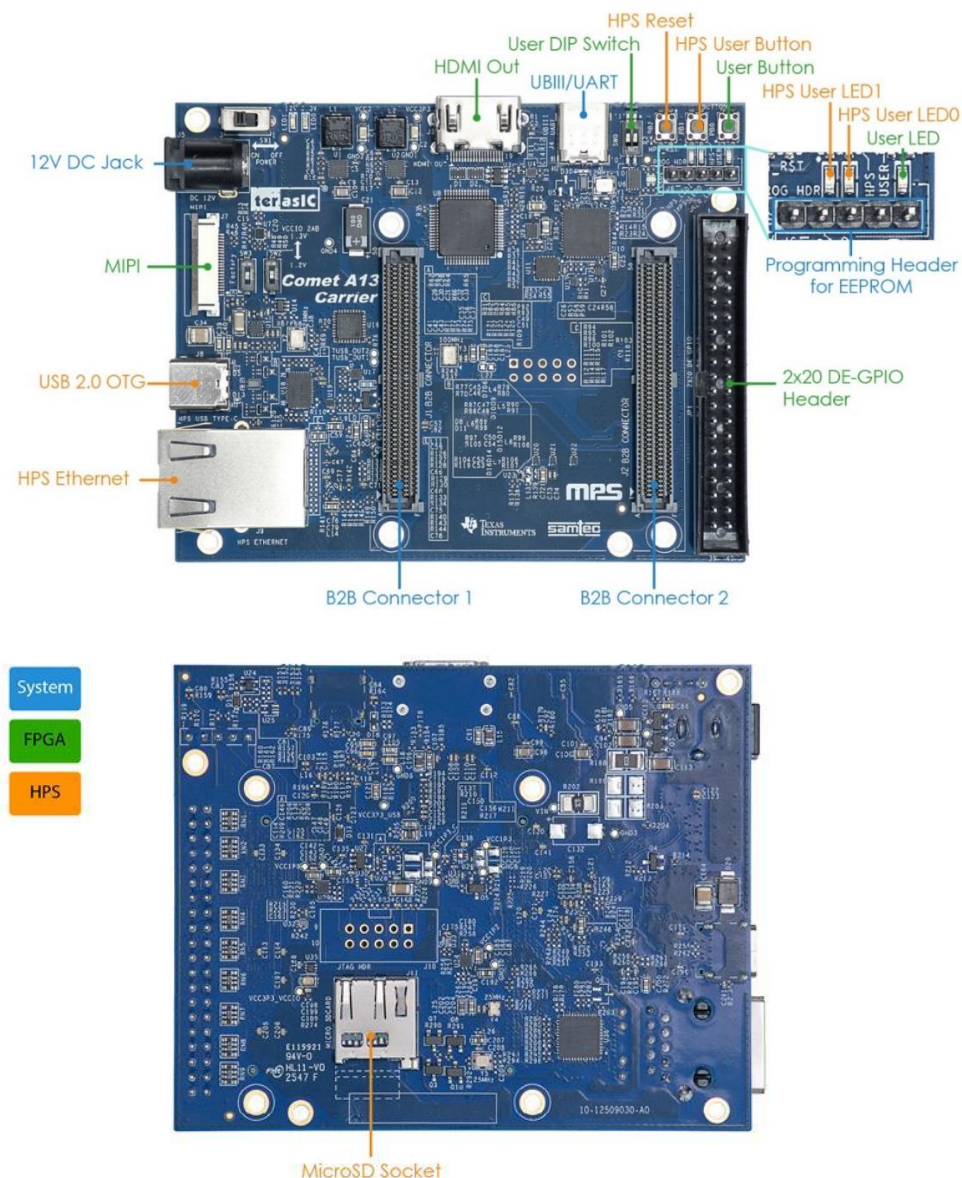


Figure 2-1 Comet A13 Carrier Board Layout

2.2 Power Input and Switch

This carrier board supports external power supply for power input. Power can be provided by connecting a standalone external power supply unit (PSU) to the onboard 12V DC Jack.

Figure 2-2 illustrates the locations of the 12V DC Jack and power switch.

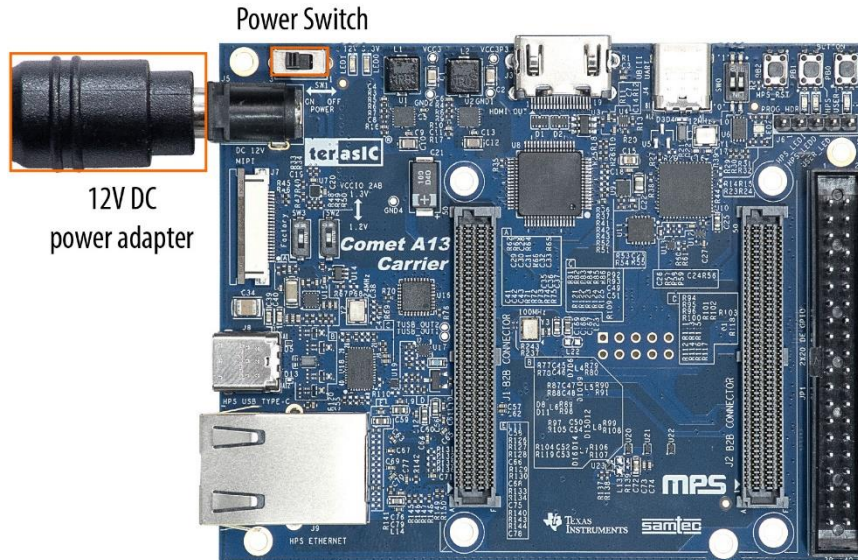


Figure 2-2 Key connectors and switches for power

2.3 Setup and Status Components

This section will introduce the use of the switch for setup on the carrier board, as well as a description of the various status LEDs.

■ Status LED

The Comet A13 carrier board includes board-specific status LEDs to indicate board status. **Figure 2-3** and **Figure 2-4** shows the location of all these status LED. Please refer to **Table 2-1** for the description of the LED indicators and **Table 2-2** for USB blaster III RGB LED.

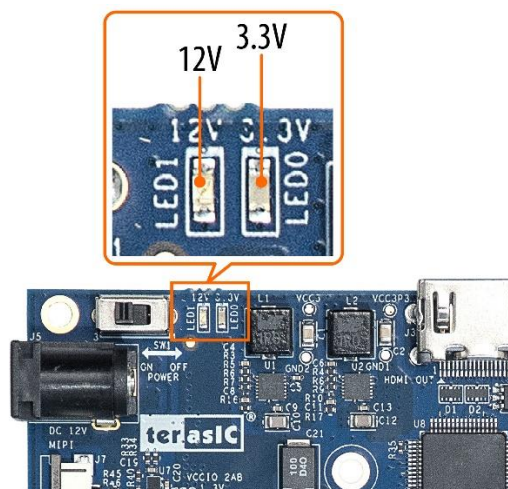


Figure 2-3 Power Status LED

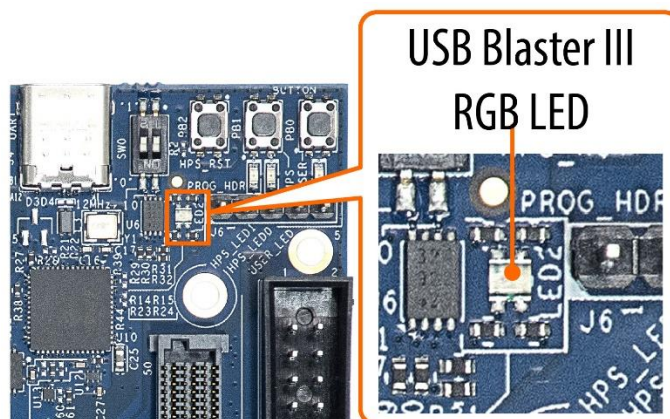


Figure 2-4 USB Blaster III Status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
LED1	12V	Illuminates when 12-V power is active.
LED0	3.3V	Illuminates when 3.3-V power is active.

Table 2-2 Status of USB Blaster III RGB LED

Color	Meaning
Off	No power / not connected / suspend mode
Blue	Connected, not in use
Green	Connected, an application is using JTAG, no traffic
Green flickering	Connected, data is moving through the JTAG interface
Purple flashing	Identify function has been triggered on this cable

■ VCCIO_2AB Select Switch

The Comet A13 SoM FPGA 2AB bank supports both 1.2V and 1.3V I/O standards on this EVK board. The 1.2V power is supplied by the SoM itself, while the 1.3V power is provided by the carrier board. When users need to use LVDS TX function on VCCIO_2AB bank, the I/O standard should be set to 1.3V. If only LVDS RX is used, set it as 1.2V. **Figure 2-5** shows the position of the SW2. When SW2 is set to ON position, the I/O standard is 1.3V, it's default set to OFF position for 1.2V I/O standard.

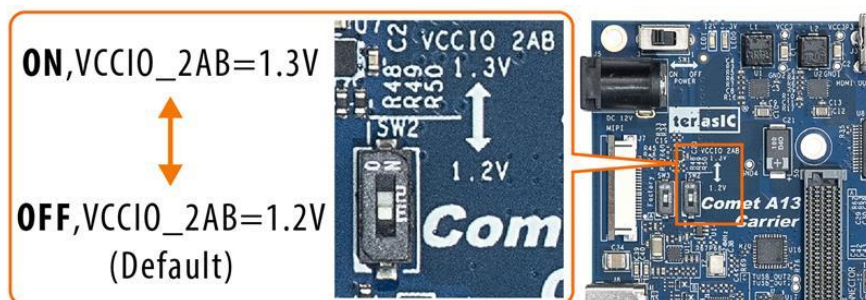


Figure 2-5 VCCIO_2AB I/O standard setting switch

■ Factory Image Switch

The factory switch SW3 on the carrier board can control the FPGA in ASx4 mode to select which image (factory or application user image) of the QSPI Flash to read the configuration file from after the board is powered. When the user switches the factory switch to the ON position, the FPGA will read the factory default FPGA code in the flash to boot the FPGA, GHRD application code is selected when SW3 is set to OFF position. **Figure 2-6** shows the position of this switch on the board.

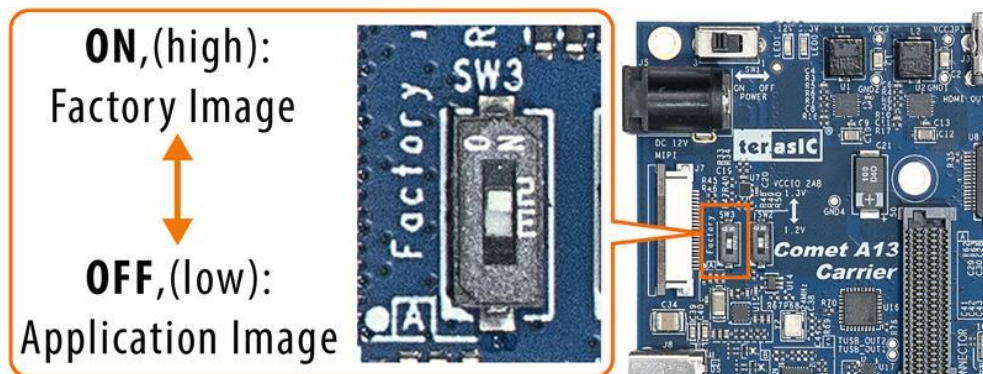


Figure 2-6 Boot Image Select Switch

2.4 Reset Device

The carrier board provides a HPS cold reset button (PB2), HPS_RST, as shown in **Figure 2-7** below. It's used to cold reset to the HPS, Ethernet PHY and USB host device. Active low input which resets all HPS logics that can be reset. **Figure 2-8** is the HPS reset tree for Comet A13 evaluation kit.

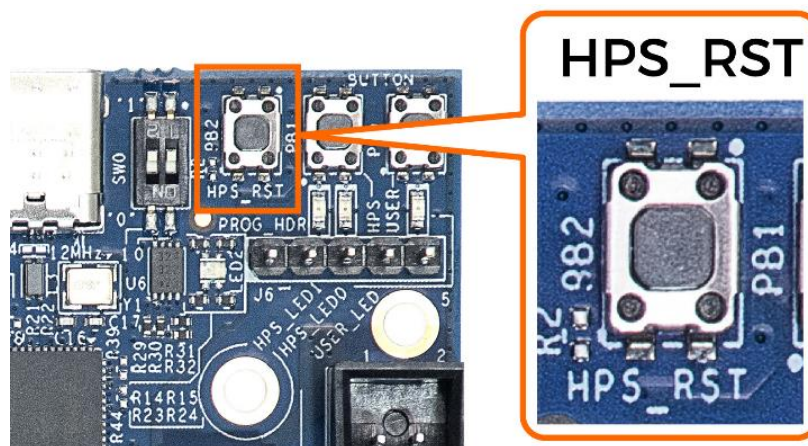


Figure 2-7 Position of the HPS_RST button

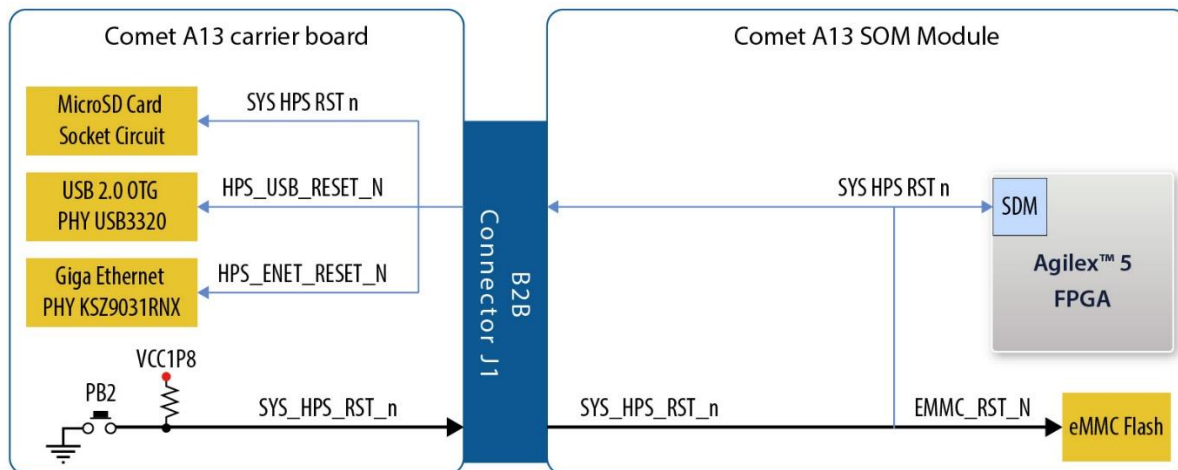


Figure 2-8 HPS reset tree on Comet A13 evaluation kit

2.5 Clock Tree

The clock tree design of the Comet A13 Carrier Board is primarily composed of two on-board oscillators (see **Figure 2-9**). Its purpose is to provide precise reference clocks for the SOM module and high-speed transceiver interfaces. The function of each clock is as follows:

- **100 MHz Clock:** This clock signal (CLK_100_p/n) is routed through pins E39/E38 of the B2B Connector J1 to the FPGA on the Comet A13 SoM module, serving as its primary reference clock source.
- **25MHz Clock:** This clock signal (HPS_OSC_CLK) is routed through pins C10 of the B2B Connector J1 to the FPGA on the Comet A13 SoM module, serving only for HPS.

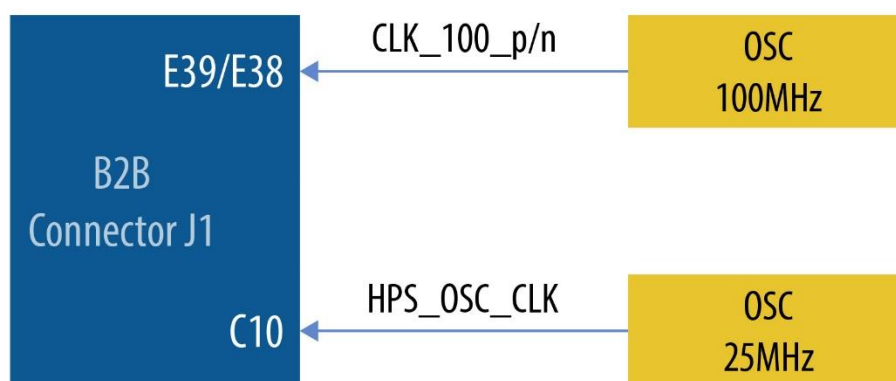


Figure 2-9 Clock tree of the Carrier Board

2.6 USB Blaster III

The board features a built-in Altera USB Blaster III circuit. Its USB interface is connected to the USB Type-C port via the on-board USB hub, while the JTAG signals are routed to the SOM (System on Module) through the B2B Connector J1.

Figure 2-10 provides the block diagram for the on-board USB Blaster III circuitry. **Figure 2-11** shows the physical locations of the USB Type-C connector.

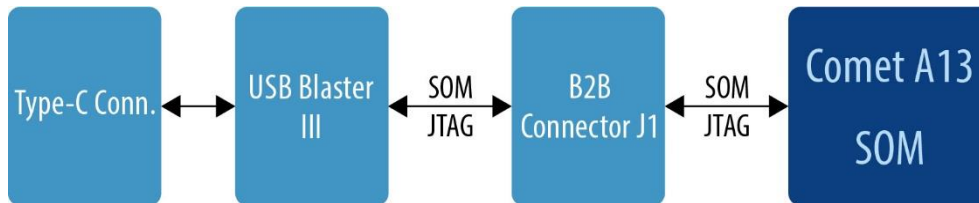


Figure 2-10 Block diagram of the USB Blaster III circuit

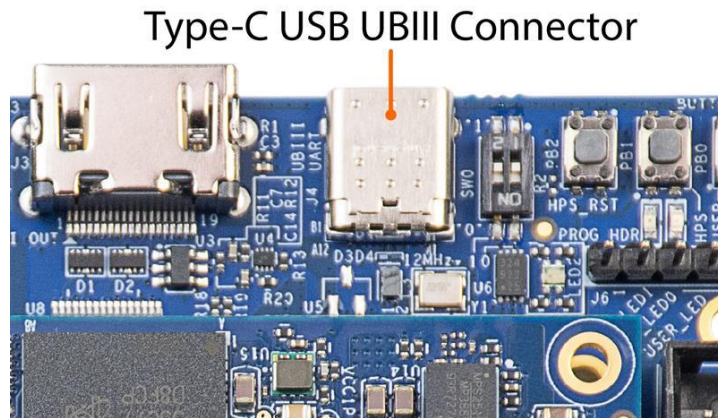


Figure 2-11 Location of the USB Type-C connector

2.7 General User I/O

This section describes the user I/O interfaces of the FPGA and HPS fabric on the carrier board. Please note that the HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. **Figure 2-12** shows the position of all these components and interface.

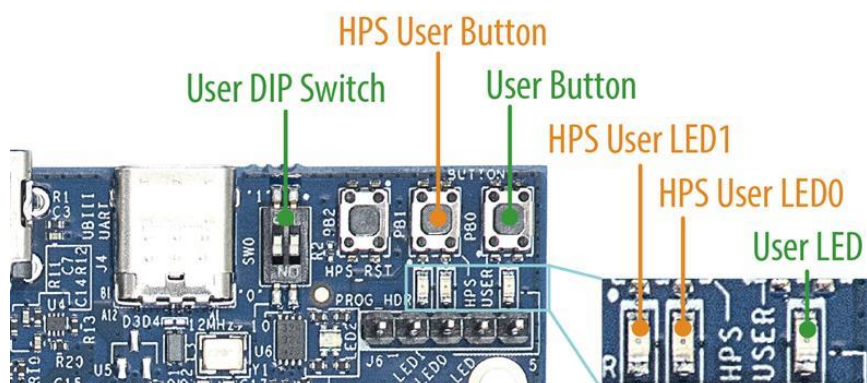


Figure 2-12 Position of all the general user components

■ User Push-buttons

The carrier board includes one FPGA and one HPS fabric user defined push-buttons that allow users to interact with the Agilex 5 SoC device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-3** lists the board references, signal names and their corresponding Agilex 5 SoC device pin numbers for the two push-buttons.

Table 2-3 Push-button (FPGA and HPS) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
PB0	USER_BUTTON	High Logic Level when the button is not pressed	3.3-V LVCMOS	J1_C29	BK112
PB1	HPS_KEY		1.8V	J1_E3	B134

■ DIP Switch

There is one two-positions slide switches on the FPGA fabric to provide additional FPGA input control. When a position of dip switch is in the ON position or the OFF position, it provides a low logic level or a high logic level to the Agilex SoC FPGA, respectively. **Table 2-4** lists the signal names and their corresponding Agilex SoC device pin numbers.

Table 2-4 Dip Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
SW0.1	USER_SW0	High logic level when SW in the OFF position.	3.3-V LVCMOS	J1_B31	BP112
SW0.2	USER_SW1		3.3-V LVCMOS	J1_C31	BM112

■ User LEDs

The FPGA board consists of one FPGA fabric and two HPS fabric user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Agilex SoC FPGA. Each LED is driven directly by the FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA and HPS that are connected to the LEDs is given in **Table 2-5**.

Table 2-5 Pin Assignments of User LEDs

Board Reference	Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
USER_LED	USER_LED	Driving a logic 0 on the I/O port turns the LED ON.	3.3-V LVCMOS	J1_C29	BH118
HPS_LED0	HPS_LED0		1.8-V	J1_A4	W135
HPS_LED1	HPS_LED1	Driving a logic 1 on the I/O port turns the LED OFF.	1.8-V	J1_A2	U135

2.8 2x20 GPIO Expansion Header

The board has one 40-pin expansion header. It has 36 user pins connected to the Agilex 5 SoC FPGA through the B2B connector J2. It also comes with DC +5V (VCC5), DC +3.3V (VCC3P3), and two GND pins. The maximum power consumption allowed for a daughter card connected to one GPIO ports is shown in **Table 2-6**.

Table 2-6 Voltage and Max. Current Limit of Expansion Header

Supplied Voltage	Max. Current Limit
5V	1A
3.3V	1.5A

Each pin on the expansion header is connected to two diodes and a resistor for protection against high or low voltage level. **Figure 2-13** shows the protection circuitry applied to all 36 data pins.

Table 2-7 shows the pin assignment of the GPIO header.

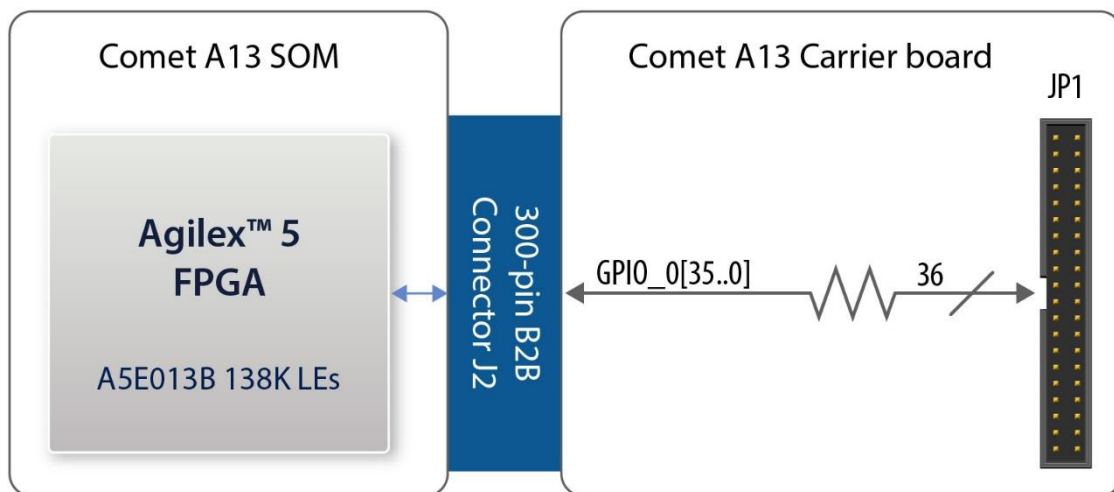


Figure 2-13 Connections between the GPIO header and Agilex 5 SoC FPGA

Table 2-7 Pin Assignment of Expansion Header

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	FPGA Pin Number
GPIO[0]	GPIO Connection[0]	3.3-V LVCMOS	J2_B19	PIN_BF29
GPIO[1]	GPIO Connection[1]	3.3-V LVCMOS	J2_D17	PIN_BF21
GPIO[2]	GPIO Connection[2]	3.3-V LVCMOS	J2_B27	PIN_BP22
GPIO[3]	GPIO Connection[3]	3.3-V LVCMOS	J2_C18	PIN_BE43
GPIO[4]	GPIO Connection[4]	3.3-V LVCMOS	J2_D18	PIN_BF40
GPIO[5]	GPIO Connection[5]	3.3-V LVCMOS	J2_A20	PIN_BE29
GPIO[6]	GPIO Connection[6]	3.3-V LVCMOS	J2_B20	PIN_BE25
GPIO[7]	GPIO Connection[7]	3.3-V LVCMOS	J2_B21	PIN_BF32
GPIO[8]	GPIO Connection[8]	3.3-V LVCMOS	J2_A22	PIN_BF36
GPIO[9]	GPIO Connection[9]	3.3-V LVCMOS	J2_C20	PIN_BF25

GPIO[10]	GPIO Connection[10]	3.3-V LVCMOS	J2_A23	PIN_BF16
GPIO[11]	GPIO Connection[11]	3.3-V LVCMOS	J2_C21	PIN_BH19
GPIO[12]	GPIO Connection[12]	3.3-V LVCMOS	J2_C22	PIN_BK22
GPIO[13]	GPIO Connection[13]	3.3-V LVCMOS	J2_A24	PIN_BM19
GPIO[14]	GPIO Connection[14]	3.3-V LVCMOS	J2_B23	PIN_BU19
GPIO[15]	GPIO Connection[15]	3.3-V LVCMOS	J2_D21	PIN_BR19
GPIO[16]	GPIO Connection[16]	3.3-V LVCMOS	J2_B24	PIN_CK2
GPIO[17]	GPIO Connection[17]	3.3-V LVCMOS	J2_D22	PIN_CJ2
GPIO[18]	GPIO Connection[18]	3.3-V LVCMOS	J2_B25	PIN_BU28
GPIO[19]	GPIO Connection[19]	3.3-V LVCMOS	J2_C24	PIN_BP31
GPIO[20]	GPIO Connection[20]	3.3-V LVCMOS	J2_C25	PIN_BR28
GPIO[21]	GPIO Connection[21]	3.3-V LVCMOS	J2_C26	PIN_BR31
GPIO[22]	GPIO Connection[22]	3.3-V LVCMOS	J2_D25	PIN_BU31
GPIO[23]	GPIO Connection[23]	3.3-V LVCMOS	J2_C28	PIN_BM28
GPIO[24]	GPIO Connection[24]	3.3-V LVCMOS	J2_C29	PIN_BW28
GPIO[25]	GPIO Connection[25]	3.3-V LVCMOS	J2_D26	PIN_BM31
GPIO[26]	GPIO Connection[26]	3.3-V LVCMOS	J2_D29	PIN_BK28
GPIO[27]	GPIO Connection[27]	3.3-V LVCMOS	J2_D30	PIN_BR22
GPIO[28]	GPIO Connection[28]	3.3-V LVCMOS	J2_A26	PIN_CH12
GPIO[29]	GPIO Connection[29]	3.3-V LVCMOS	J2_A27	PIN_BU22
GPIO[30]	GPIO Connection[30]	3.3-V LVCMOS	J2_A28	PIN_BW19
GPIO[31]	GPIO Connection[31]	3.3-V LVCMOS	J2_B28	PIN_BH28
GPIO[32]	GPIO Connection[32]	3.3-V LVCMOS	J2_A30	PIN_BM22
GPIO[33]	GPIO Connection[33]	3.3-V LVCMOS	J2_A31	PIN_CF12
GPIO[34]	GPIO Connection[34]	3.3-V LVCMOS	J2_B29	PIN_BK19
GPIO[35]	GPIO Connection[35]	3.3-V LVCMOS	J2_B31	PIN_CF9

2.9 MIPI Connector

The Agilex 5 devices offer native mobile industry processor interface (MIPI) D-PHY. This support complies to MIPI D-PHY version 2.5, and allows transmission or reception of data with MIPI D-PHY interfaces. It provides the PHY-protocol interface (PPI) to connect with camera serial interface (CSI) and display serial interface (DSI) applications.

The carrier board also provides one 22-pin FPC connectors (1 lane clock and 4 lane data for each), allowing users to connect MIPI interface cameras and display devices through FPC cable (see **Figure 2-14**). Users can use this connector and camera cable to connect to camera devices such as Raspberry Pi camera module to form a camera input application. In addition, it can also be connected with the display device such as Raspberry Pi MIPI Displayer module to implement a display application.

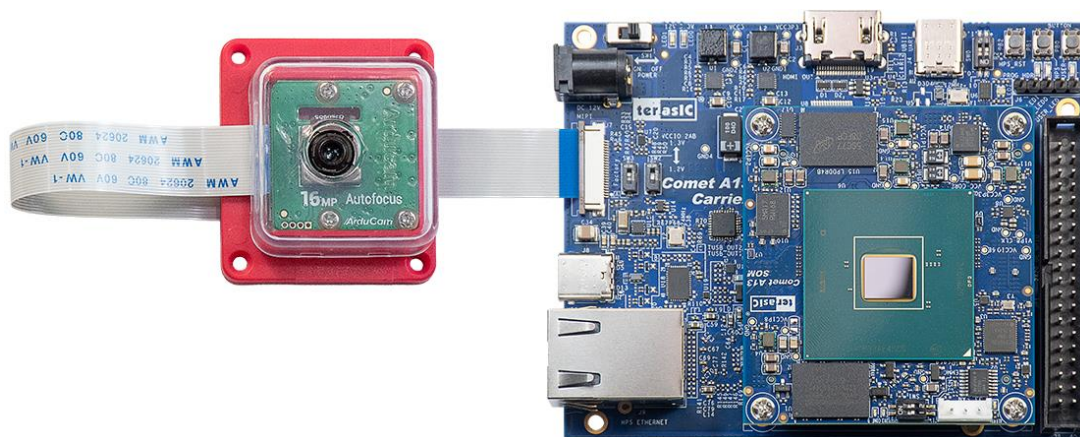


Figure 2-14 MIPI camera module connects to the carrier board via cable

See **Figure 2-15** shows the connections between the FPGA and 22-pin MIPI connector. **Table 2-8** shows the pin assignment of 22-pin MIPI connector.

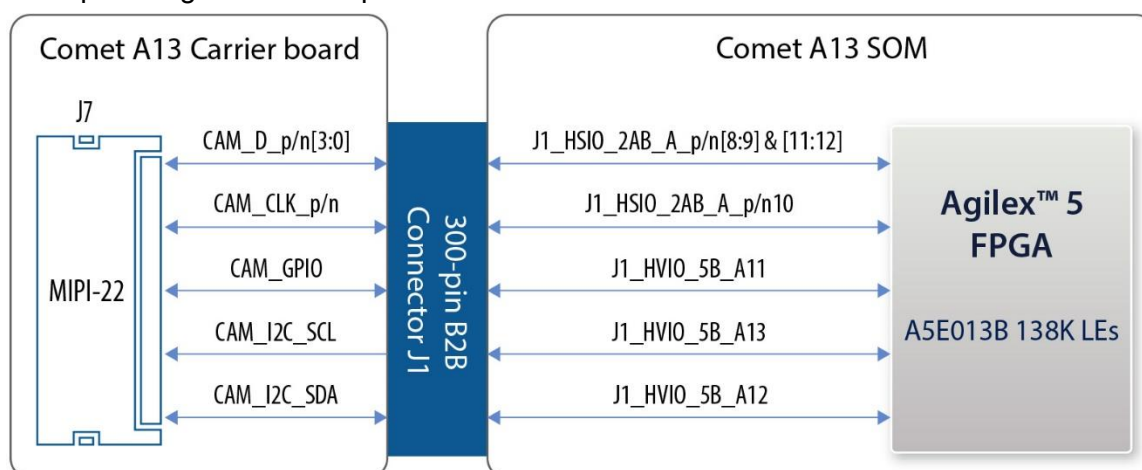


Figure 2-15 Connection between the MIPI connector and Agilex 5 FPGA

Table 2-8 MIPI connector pin assignments, schematic signal names, and functions

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A13 SoM FPGA Pin Num.
CAM_CLK_p	MIPI Clock positive	DPHY	J1_B42	PIN_BW89
CAM_CLK_n	MIPI Clock negative	DPHY	J1_B41	PIN_CA89
CAM_D_p[0]	MIPI Data 0 positive	DPHY	J1_F37	PIN_BR89
CAM_D_p[1]	MIPI Data 1 positive	DPHY	J1_F40	PIN_BR92
CAM_D_p[2]	MIPI Data 2 positive	DPHY	J1_E36	PIN_BR81
CAM_D_p[3]	MIPI Data 3 positive	DPHY	J1_B39	PIN_BR78
CAM_D_n[0]	MIPI Data 0 negative	DPHY	J1_F36	PIN_BU89
CAM_D_n[1]	MIPI Data 1 negative	DPHY	J1_F39	PIN_BU92
CAM_D_n[2]	MIPI Data 2 negative	DPHY	J1_E35	PIN_BU81
CAM_D_n[3]	MIPI Data 3 negative	DPHY	J1_B38	PIN_BU78
CAM_I2C_SCL	I2C clock	3.3-V LVCMOS	J1_A31	PIN_BR112

CAM_I2C_SDA	I2C data	3.3-V LVCMOS	J1_C30	PIN_BM109
CAM_GPIO	GPIO signal	3.3-V LVCMOS	J1_C26	PIN_BE111
CAM_RZQ0	External reference ball for output drive calibration	1.2V		PIN_BH89

2.10 HDMI TX

The development board provides a high performance DVI-compliant digital transmitter via the TI TFP410, which incorporates DVI v1.0 features and supports pixel rates up to 165MHz, including 1080p and WUXGA at 60Hz. The TFP410 is controlled via a serial I2C bus interface, which is connected to pins on the Agilex 5 SoC FPGA and output via HDMI TX interface on Comet A13 carrier board. A schematic diagram of the circuitry is shown in **Figure 2-16**. Detailed information on using the TFP410 is available on the manufacturer's website, or under the Datasheets\HDMI folder in the Comet A13 carrier board System CD.

Table 2-9 lists the HDMI Interface pin assignments and signal names relative to the FPGA.

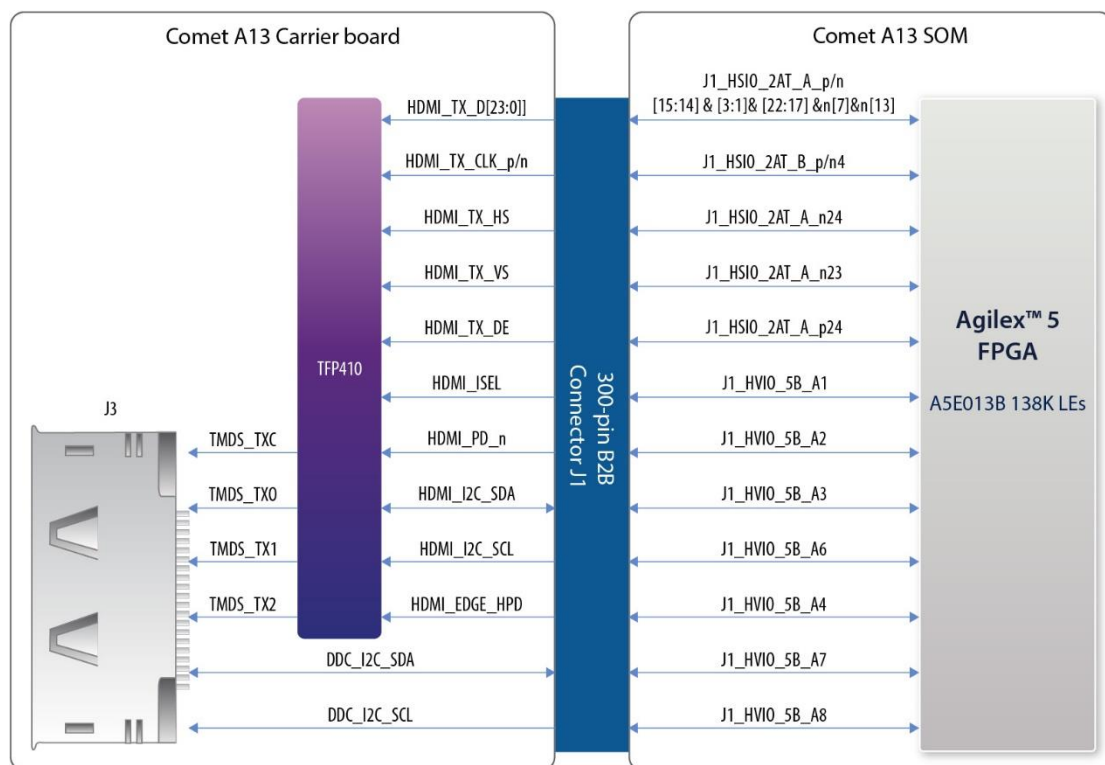


Figure 2-16 Connections between the FPGA and DVI Transmitter Chip

Table 2-9 Pin Assignment of HDMI

Schematic Signal Name	Description	I/O Standard	Comet A13 FPGA Pin Num.
HDMI_TX_D[0]	Video Data bus	1.2 V	PIN_BK78
HDMI_TX_D[1]	Video Data bus	1.2 V	PIN_BM78
HDMI_TX_D[2]	Video Data bus	1.2 V	PIN_BH78
HDMI_TX_D[3]	Video Data bus	1.2 V	PIN_BH81
HDMI_TX_D[4]	Video Data bus	1.2 V	PIN_BP81
HDMI_TX_D[5]	Video Data bus	1.2 V	PIN_BM81

HDMI_TX_D[6]	Video Data bus	1.2 V	PIN_CC81
HDMI_TX_D[7]	Video Data bus	1.2 V	PIN_CA81
HDMI_TX_D[8]	Video Data bus	1.2 V	PIN_CA78
HDMI_TX_D[9]	Video Data bus	1.2 V	PIN_CF78
HDMI_TX_D[10]	Video Data bus	1.2 V	PIN_CL82
HDMI_TX_D[11]	Video Data bus	1.2 V	PIN_CH81
HDMI_TX_D[12]	Video Data bus	1.2 V	PIN_CF81
HDMI_TX_D[13]	Video Data bus	1.2 V	PIN_CL85
HDMI_TX_D[14]	Video Data bus	1.2 V	PIN_CK85
HDMI_TX_D[15]	Video Data bus	1.2 V	PIN_CH92
HDMI_TX_D[16]	Video Data bus	1.2 V	PIN_CF92
HDMI_TX_D[17]	Video Data bus	1.2 V	PIN_CA92
HDMI_TX_D[18]	Video Data bus	1.2 V	PIN_CC92
HDMI_TX_D[19]	Video Data bus	1.2 V	PIN_CL76
HDMI_TX_D[20]	Video Data bus	1.2 V	PIN_CK76
HDMI_TX_D[21]	Video Data bus	1.2 V	PIN_CK80
HDMI_TX_D[22]	Video Data bus	1.2 V	PIN_CK88
HDMI_TX_D[23]	Video Data bus	1.2 V	PIN_CL88
DDC_I2C_SCL	Serial Port Data Clock to Sink	3.3-V LVCMOS	PIN_BR109
DDC_I2C_SDA	Serial Port Data Input/Output to Sink	3.3-V LVCMOS	PIN_BF104
HDMI_I2C_SCL	FPGA I2C Clock	3.3-V LVCMOS	PIN_BU109
HDMI_I2C_SDA	FPGA I2C Data	3.3-V LVCMOS	PIN_BE115
HDMI_TX_HS	Horizontal Synchronization	1.2 V	PIN_CK94
HDMI_TX_VS	Vertical Synchronization	1.2 V	PIN_CL97
HDMI_TX_DE	Data Enable Signal for Digital Video	1.2 V	PIN_CL91
HDMI_TX_CLK_p	HDMI transmitter clock	DIFFERENTIAL 1.2-V SSTL	PIN_BK89
HDMI_EDGE_HPD	Edge select/hot plug input	3.3-V LVCMOS	PIN_BF115
HDMI_ISEL	I ² C interface select/I ² C reset	3.3-V LVCMOS	PIN_BF111
HDMI_PD_n	Power down (active low)	3.3-V LVCMOS	PIN_BH109

2.11 HPS Gigabit Ethernet

The carrier board provides one Ethernet port for users. The Gigabit Ethernet port is connected to the Micrel KSZ9031RN PHY and provided to HPS fabric. Below here is the detailed information about the port.

The board supports Gigabit Ethernet transfer by an external Micrel KSZ9031RN PHY chip and HPS Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface. **Figure 2-17** shows the connections between the Comet A13 SoM module, 300-pin B2B J1 connector and RJ-45 connectors.

For more information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, which are available on the manufacturer's website.

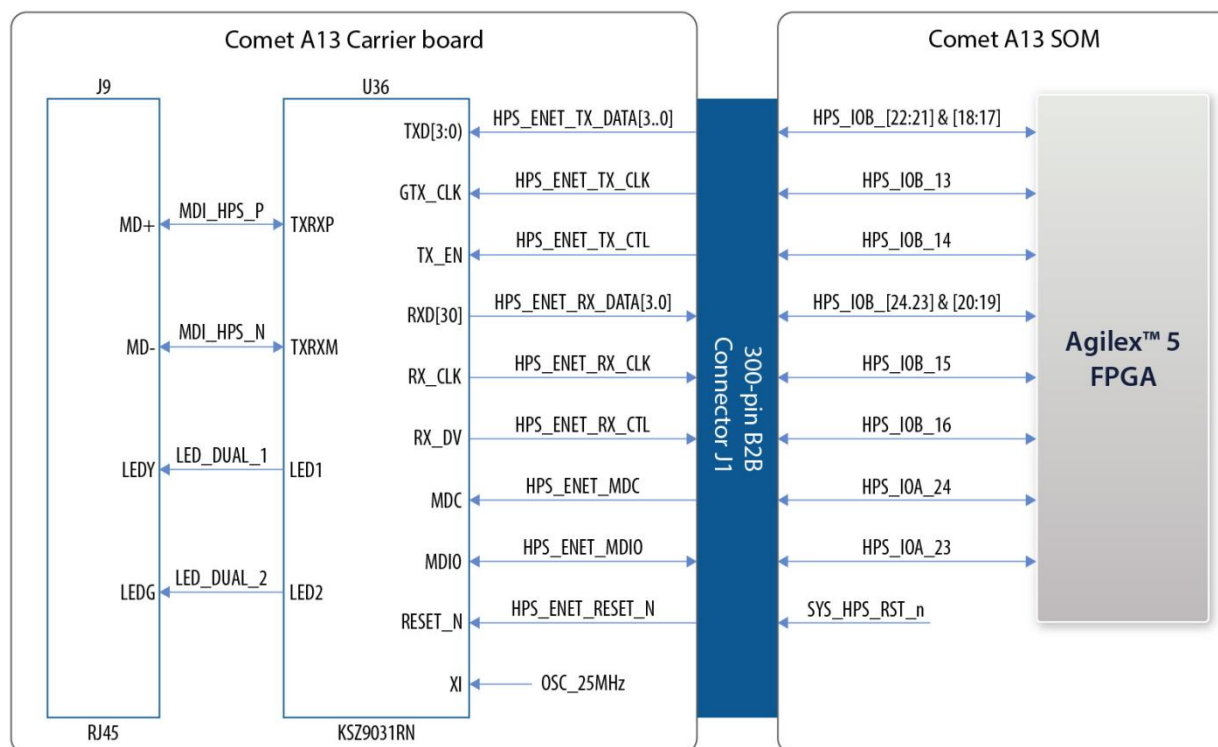


Figure 2-17 Connection between the RJ45 connector and Agilex 5 SoC FPGA

There are two LEDs, a green LED (LEDG) and a yellow LED (LEDY), which represent the status of the Ethernet PHY (KSZ9031RN). The LED control signals are connected to the LEDs on the RJ45 connector. The state and the definition of LEDG and LEDY are listed in **Table 2-10**. For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-10 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	Link / Activity (RX, TX)

Table 2-11 Pin Assignment of Gigabit Ethernet PHY and HPS on Comet A13 SoM

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A13 FPGA Pin Num.
HPS_ENET_TX_CTL	GMII and MII transmit enable	1.8 V	J1_E5	PIN_K127
HPS_ENET_TX_DATA[0]	GMII and MII transmit data[0]	1.8 V	J1_F7	PIN_K124
HPS_ENET_TX_DATA[1]	GMII and MII transmit data[1]	1.8 V	J1_C7	PIN_Y127

■ USB 3.1 interface for HPS

This board implements USB3.1 interface through FPGA's GTS transceiver (HPS to FPGA), redrive IC and USB type-c connector. It can operate in Host or Device models.

Table 2-2-12 lists the pin assignment of USB3.1 interface connected to the FPGA.

Table 2-2-12 Pin Assignment of USB 3.1 interface

Schematic Signal Name	Description	I/O Standard	B2B Connect or Pin Number	Comet A13 FPGA Pin Num.
HPS_USB3_REFCLK_100M_p	USB 3.1 interface reference clock	CML	J1_E18	PIN_AT120
HPS_USB3_REFCLK_100M_n			J1_E17	PIN_AT115
USB3_SS_TX_p	Differential positive output for USB port	HIGH SPEED DIFFERENTIAL I/O	J1_F16	PIN_AN129
USB3_SS_TX_n	Differential negative output for USB port		J1_F15	PIN_AN126
USB3_SS_RX_p	Differential positive input for USB port		J1_16	PIN_AM135
USB3_SS_RX_n	Differential negative input for USB port		J1_15	PIN_AM133
USB_FLT_n	Low when VCONN over-current fault is detected.	1.2 V	J1_F29	PIN_CF118
VBUS_DET	VBUS detection	1.2 V	J1_E25	PIN_BU118
VBUS_CTRL	To control whether if the VBUS power of Type-C connector J16 should output.	1.2 V	J1_E27	PIN_CA118
USB31_ID	Asserted low when the CC pins detect device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).	1.2 V	J1_F27	PIN_A60

■ USB 2.0 interface for HPS

The board also provides USB interfaces using the SMSC USB3320 controller. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device models. **Table 2-13** lists the pin assignment of USB2.0 interface connected to the FPGA.

Table 2-13 Pin Assignment of USB 2.0 interface

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A13 FPGA Pin Num.
HPS_USB_CLK	Reference Clock Output	1.8 V	J1_C6	PIN_P132
HPS_USB_DATA[0]	HPS USB_DATA[0]	1.8 V	J1_A10	PIN_AD135
HPS_USB_DATA[1]	HPS USB_DATA[1]	1.8 V	J1_C2	PIN_M132
HPS_USB_DATA[2]	HPS USB_DATA[2]	1.8 V	J1_D3	PIN_K132
HPS_USB_DATA[3]	HPS USB_DATA[3]	1.8 V	J1_B7	PIN_AG129
HPS_USB_DATA[4]	HPS USB_DATA[4]	1.8 V	J1_D2	PIN_J134
HPS_USB_DATA[5]	HPS USB_DATA[5]	1.8 V	J1_B10	PIN_AG120
HPS_USB_DATA[6]	HPS USB_DATA[6]	1.8 V	J1_E4	PIN_G134
HPS_USB_DATA[7]	HPS USB_DATA[7]	1.8 V	J1_F2	PIN_G135
HPS_USB_DIR	Direction of the Data Bus	1.8 V	J1_D4	PIN_J135
HPS_USB_NXT	Throttle the Data	1.8 V	J1_A6	PIN_AD134

HPS_USB_STP	Stop Data Stream on the Bus	1.8 V	J1_C3	PIN_L135
-------------	-----------------------------	-------	-------	----------

2.13 USB to UART

The Carrier board provides a UART interface, which is primarily used for communication with the HPS (Hard Processor System) on the SOM. It allows users to access the HPS console, view boot messages, execute Linux commands, and perform software debugging. This serves as the primary channel for interacting with the operating system.

The interface is implemented via the FT2232H chip in the USB Blaster III circuit. Connect a USB cable between the Comet A13 Carrier board's Type-C connector J4 and the host enables both USB Blaster III and HPS UART functions. Serial driver will be installed at the same time when the USB Blaster III driver is installed. After connecting the USB cable, normally USB Blaster III and a COM port number will both show in PC Device Manager. **Figure 2-19** shows the connections between the Agilex 5 SoC FPGA, FT2232H chip and the USB Type-C connector. **Table 2-14** lists the pin assignments of the HPS UART interface connected to the SoC FPGA.

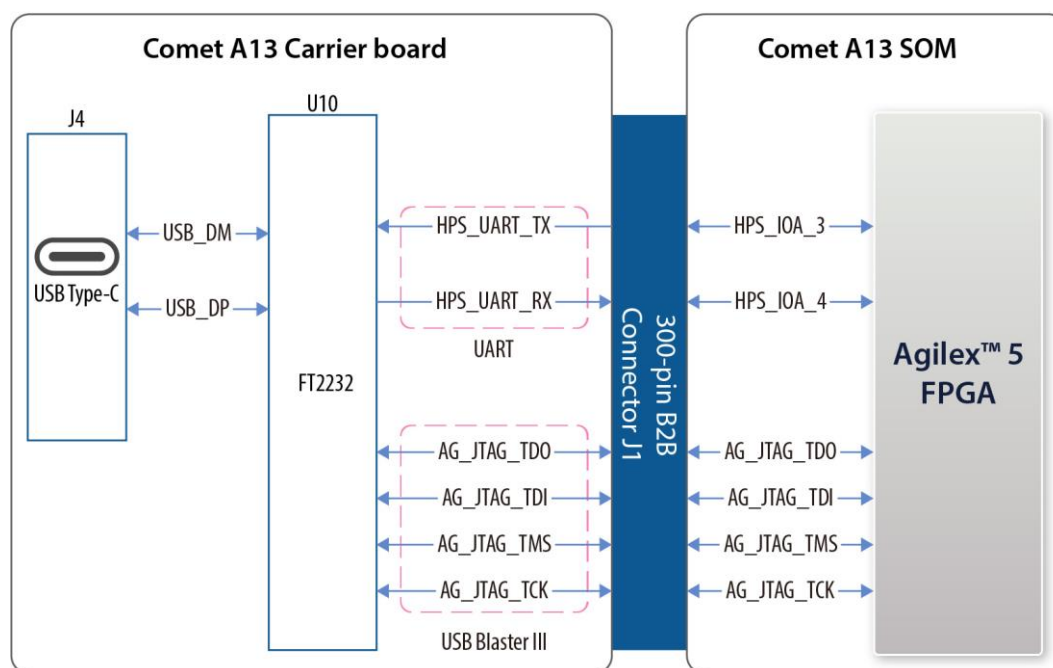


Figure 2-19 Block diagram of the HPS USB UART interface

Table 2-14 Pin Assignment of HPS UART

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A13 FPGA Pin Num.
HPS_UART_TX	UART Transmitter	1.8-V	J1_A5	PIN_W134
HPS_UART_RX	UART Receiver	1.8-V	J1_A9	PIN_AK115

2.14 HPS MicroSD Card

The Comet A13 carrier board provides Micro SD Card with x4 data lines for HPS fabric in the FPGA (See **Figure 2-20**). Users can choose it for HPS boot/data/system storage. Please note that the switch SW1 on the Comet A13 SoM module can help the user select which device (Micro SD Card or eMMC) will be used for HPS fabric. **Table 2-15** lists the pin assignment of Micro SD card socket to the HPS.

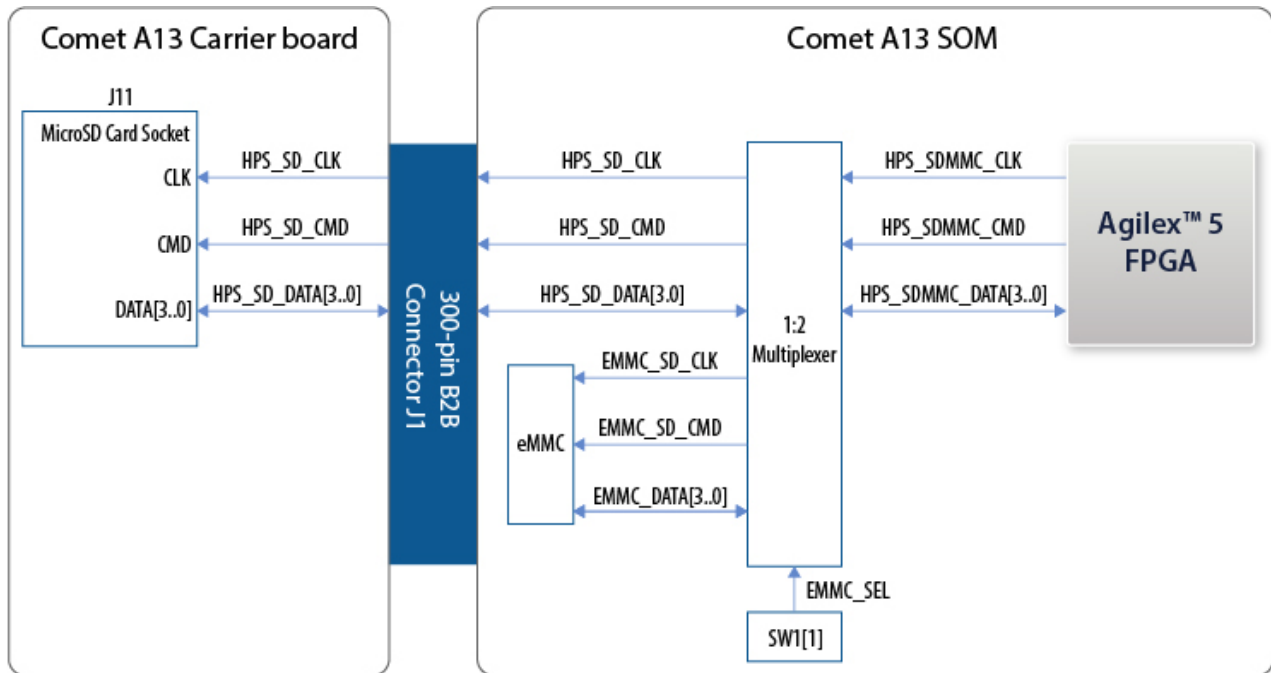


Figure 2-20 Connections between Micro SD card socket and Agilex 5 SoC FPGA

Table 2-15 The pin assignment of Micro SD card socket

Schematic Signal Name	Description	I/O Standard	B2B Connector Pin Number	Comet A13 FPGA Pin Num.
HPS_SD_CLK	HPS SD Clock	1.8 V	J1_B6	PIN_D132
HPS_SD_CMD	HPS SD Command Line	1.8 V	J1_A8	PIN_AB132
HPS_SD_DATA[0]	HPS SD_DATA[0]	1.8 V	J1_C9	PIN_E135
HPS_SD_DATA[1]	HPS SD_DATA[1]	1.8 V	J1_B9	PIN_F132
HPS_SD_DATA[2]	HPS SD_DATA[2]	1.8 V	J1_F9	PIN_AA135
HPS_SD_DATA[3]	HPS SD_DATA[3]	1.8 V	J1_E8	PIN_V127

2.15 6x50 B2B Connector

This carrier board is equipped with two 6x50 B2B connectors J1 & J2 for interfacing with Comet A13 SoM. The functionality is partitioned between the two connectors to separate power/control from the high-speed data paths, optimizing for signal integrity.

■ J1 Connector (Primarily for System Control, HPS I/O and High-Speed Data)

This connector primarily extends system control, HPS peripherals, and auxiliary signals from the carrier board to the SOM.

- **Power Delivery:** Serves as the primary power input for the SOM, supplying VIN, VCCIO_5A & 5B & 2AB and VCCIO_2AB_1V2_EN from the carrier board.
- **HPS Peripherals:** Extends interfaces from the SOM's Hard Processor System (HPS), such as UART, USB OTG 2.0, USB 3.1, SD card and Gigabit Ethernet, making them physically accessible to the user via connectors on the carrier board.
- **System Control & Debug:** Carries the SOM JTAG interface and other board-to-board control signals.
- **Auxiliary Signals for High-Speed Interfaces:** Transmits the **reference clocks and data bus** for interfaces like HDMI-TX, MIPI and Ethernet.

■ J2 Connector (Primarily for Power)

This connector is dedicated to provide power to the FPGA for the SoM module.

- **Power Delivery:** Serves as the primary power input for the SOM, supplying VIN, VCCIO_6A & 6B & 6C & 6D & 6F & 6G & 6H, GROUP2_PWR_EN, GROUP3_PWR_EN, VCCIO_CARRIER_PG and VCC5_FAN from the carrier board.
- **GPIO Data:** Connects the user I/Os for the 2x20 GPIO interfaces.
- **EEPROM Programming Signals:** Includes EEPROM_I2C_SDA, EEPROM_I2C_SCL and EEPROM_WC_N signals directly routed to the 1x5 programming header on the carrier board for EEPROM programming.

Figure 2-21 shows the interfaces connected to the J1 and J2 connectors.

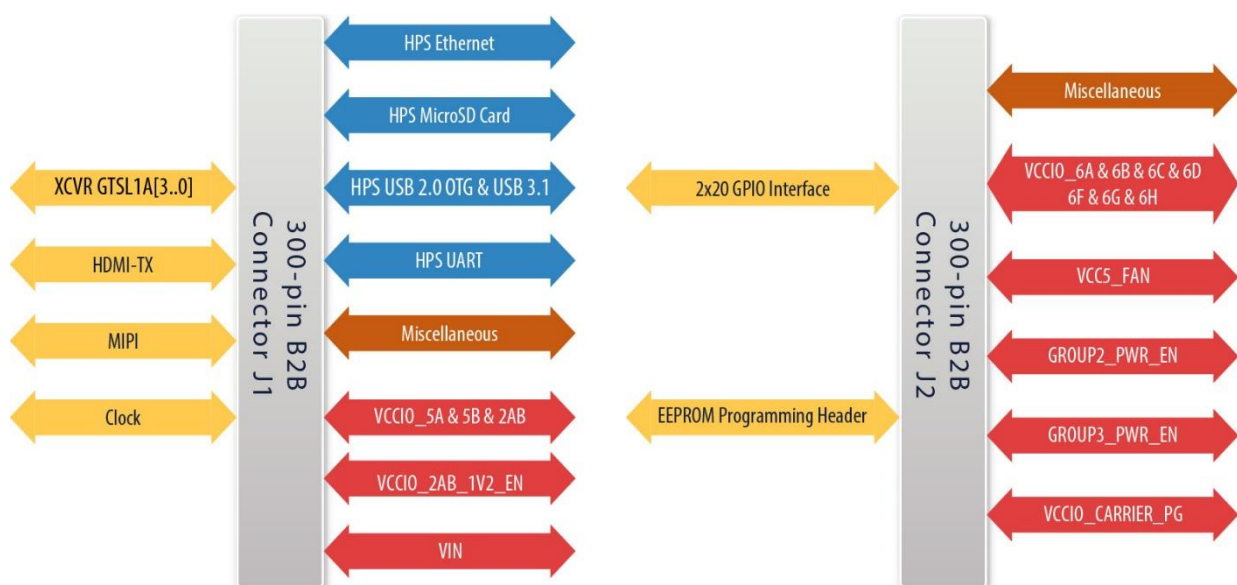


Figure 2-21 Interfaces connected to the J1 and J2 connectors.

Chapter 3

Board Assembly and Disassembly

This chapter explains how to assemble and disassemble the Comet A13 SOM and Terasic Comet A13 carrier board.

The video in the link below demonstrates how to install the Comet A13 SOM onto the carrier board, as well as the reverse process of removing it.

<https://youtu.be/-NdPe7jFcs>

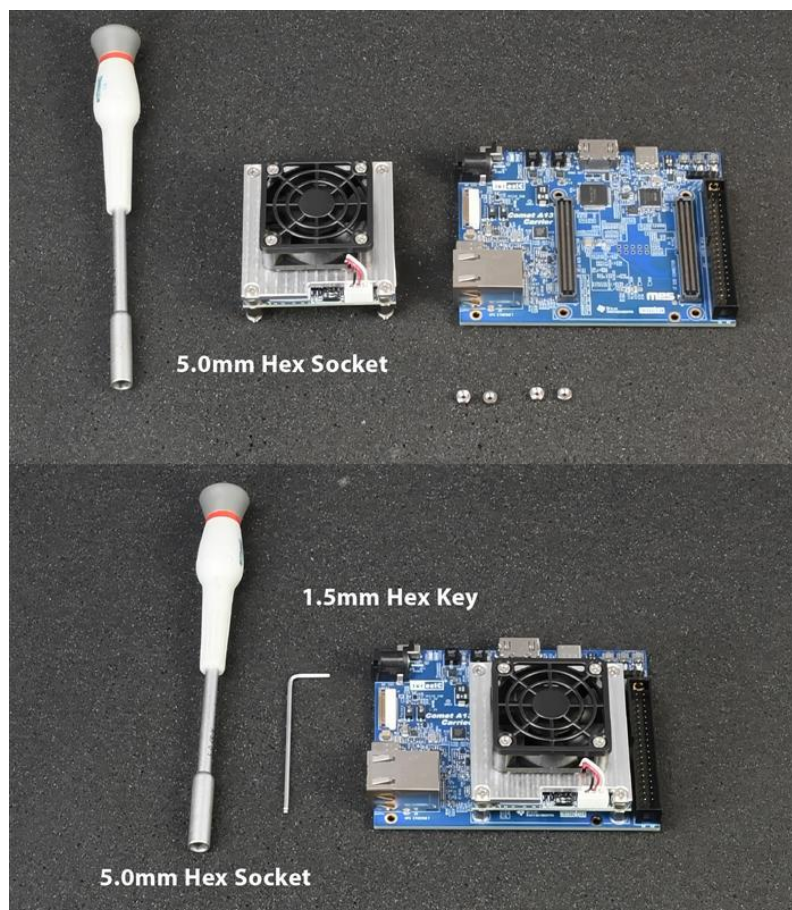


Figure 3-1 Video for installing and removing SOM and Carrier board

Chapter 4

Additional Information

4.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ **Terasic Technologies**

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

■ **Revision History**

Date	Version	Changes
2026.01	First publication	