



MPM3685

2.7-16V, 15A Step-Down Power Module

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPM3685 is an easy-to-use, fully integrated, step-down, DC/DC power module. MPM3685 offers a complete power solution that achieves up to 20A of peak current. It integrates a DC/DC converter, power inductor, and passive components. The MPM3685 can deliver output current over a wide input supply range with excellent load and line regulation.

The MPM3685 uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz easily with the MODE configuration, allowing the MPM3685 frequency to remain constant regardless of the input and output voltages.

The MPM3685 features configurable soft-start time with one capacitor. An open-drain power good signal indicates that the output voltage is within the nominal voltage range.

The MPM3685 has fully integrated, non-latched protection features including over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP).

The MPM3685 is available in a compact FCM ECLGA-33 (5mmx5mmx2.76mm) package.

FEATURES

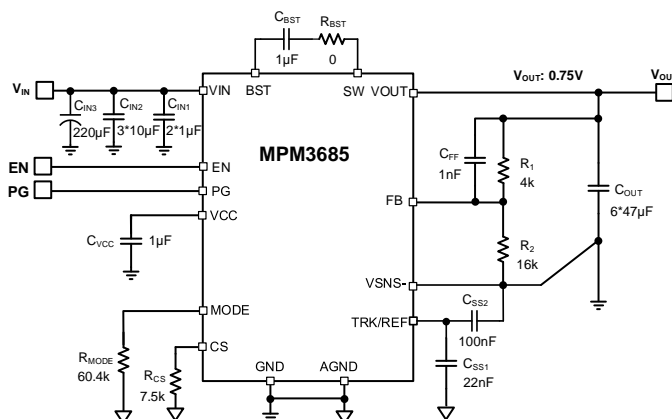
- Wide Input Voltage Range
 - 2.7V to 16V with External 3.3V Vcc
 - 4V to 16V with Internal or External Vcc
- Output Range: 0.6V to 5.5V
- 15A Continuous Output Current, Peak 20A
- Differential Output Voltage Remote Sense
- Adaptive Constant-on-Time (COT) for Ultrafast Transient Response
- Selectable Pulse Skip or Forced Continuous Conduction Mode (CCM) Operation
- Output Voltage Tracking
- Output Voltage Discharge
- PG Active Clamped Low Level during Power Failure
- Configurable Soft-Start Time
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVLO, Thermal Shutdown, and OVP

APPLICATIONS

- Telecom and Networking Systems
- Base Stations
- Industrial Systems
- Servers & Storage
- FPGA & ASIC Cards

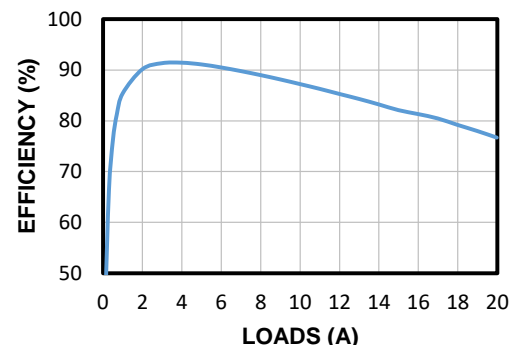
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TYPICAL APPLICATION



Efficiency vs Load

$V_{IN} = 3.3V, V_{OUT} = 0.75V, f_{SW} = 1000kHz$



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3685GPU	ECLGA (5mmx5mmx2.76mm)	See Below	3

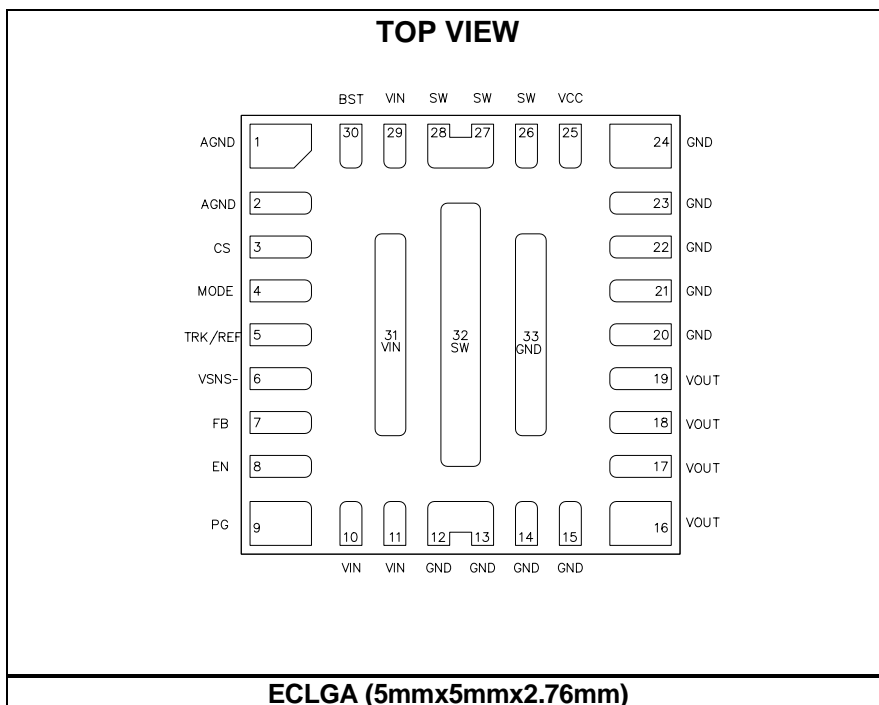
* For Tray, add suffix -T (e.g. MPM3685GPU-T).

TOP MARKING

MP**SY****YW**
MP**3685**
LLLLLLL
M

MPS: MPS prefix
 YY: Year code
 WW: Week code
 MP3685: Part number
 LLLLLLL: Lot number
 M: Module

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1, 2	AGND	Analog ground. Select AGND as the control circuit reference point and AGND need to be connected to GND when layout.
3	CS	Current limit. Connect a resistor to ground to set the current limit trip point.
4	MODE	Operation mode selection. Program MODE to select CCM, pulse-skip mode, and the operating switching frequency.
5	TRK/REF	External tracking voltage input. The output voltage tracks the TRK/REF input signal. Decouple TRK/REF with a ceramic capacitor as close to TRK/REF as possible. The capacitance of this capacitor determines the soft-start time. Refer to the Application Section for detail.
6	VSNS-	Differential remote sense negative input. Connect the VSNS- pin to the negative side of the voltage sense point. Short VSNS- to GND if not used.
7	FB	Feedback (Differential remote sense positive input). An external resistor divider from the output to VSNS- (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	Enable. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator. EN should be pulled up only when Vin exceeds Vin UVLO. Drive EN low to turn off the regulator. Connect EN to VIN through a resistive voltage divider for automatic start-up. Do not float EN.
9	PG	Power good output. PGOOD is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate a logic high signal if the output voltage is within regulation. Besides, a 0.1uF capacitor and a 1kΩ resistor are suggested to be placed close to PG Pin if Vout is greater than 2.5V, more details is shown in Figure 12-Figure 14. There is a delay of about 0.9ms between the time $FB \geq 92.5\%$ and PGOOD pulling high.
10, 11, 29, 31	VIN	Input voltage. VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed at VIN to decouple the input rail. Use wide PCB traces to make the connection.
12, 13, 14, 15, 20, 21, 22, 23, 24, 33	GND	System ground. GND is the reference ground of the regulated output voltage and requires careful consideration during the PCB layout. Use wide PCB traces to make the connection.
16, 17, 18, 19	VOUT	Module voltage output node. Use wide PCB traces to make the connection.
25	VCC	Internal 3.3V LDO output. The driver and control circuits are powered from the VCC voltage. Use a 1μF decoupling ceramic capacitor placed as close to the VCC pin as possible to decouple VCC. Capacitors with X7R or X5R grade dielectrics are recommended due to their stable temperature characteristics.
26, 27, 28, 32	SW	Switch output. Connect the SW pin to bootstrap capacitor (C _{BST}).
30	BST	Bootstrap. Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.

**ABSOLUTE MAXIMUM RATINGS** ⁽¹⁾

Supply voltage (V_{IN} to GND).....	-0.3V to 18V
$V_{SW(DC)}$ to GND.....	-0.3V to $V_{IN} + 0.3V$
V_{SW} (25ns) to GND.....	-5V to 25V
V_{OUT}	6.5V
V_{CC}	4.5V
All other pins.....	-0.3V to +4.3V
Continuous power dissipation ($T_A = +25^\circ C$) ⁽²⁾⁽⁵⁾	
.....	14.9W
Junction temperature	170°C
Lead temperature	260°C
Storage temperature	-55°C to +170°C

ESD Ratings

Human body model (HBM)	$\pm 2kV$
Charged device model (CDM)	$\pm 2kV$

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{IN})	4V to 16V
$V_{IN(DC)} - V_{SW(DC)}$	-0.3V to $V_{IN} + 0.3V$
$V_{SW(DC)}$	-0.3V to $V_{IN} + 0.3V$
Output voltage (V_{OUT})	0.6V to 5.5V
External VCC bias (V_{CC_EXT}).....	3.12V to 3.6V
EN voltage ⁽⁴⁾ (V_{EN})	3.6V
Operating junction temp (T_J).	-40°C to +125°C

Thermal Resistance ⁽⁵⁾	θ_{JA}	θ_{JB}
EVM3685-PU-00A.....	9.7.....	6.8... °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) EN pin has zener diode embedded for clamping the voltage at 3.6V. Please refer to the Operation Section for current limitation.
- 5) The thermal parameter is based on tests on MPS's evaluation board (EVM3685-PU-00A,) under no airflow cooling conditions in a standard enclosure. The board size is 10cm x 10cm, 4-layer, 2Oz for each layer.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C ⁽⁷⁾, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I _{IN}	V _{EN} = 0V		11	30	μA
Supply current (quiescent)	I _{IN}	V _{EN} = 2V, V _{FB} = 0.62V		650	850	μA
MOSFET						
Switch leakage	SW _{LKG_HS}	V _{EN} = 0V, V _{SW} = 0V		0	10	μA
	SW _{LKG_LS}	V _{EN} = 0V, V _{SW} = 12V		0	30	
Current Limit						
Current limit threshold	V _{LIM}		1.15	1.2	1.25	V
I _{CS} to I _{OUT} ratio	I _{CS} /I _{OUT}	I _{OUT} ≥ 2A	9	10	11	μA/A
Low-side negative current limit	I _{LIM_NEG}			-18		A
Negative current limit time out ⁽⁶⁾	t _{NCL_Timer}			200		ns
Switching Frequency						
Switching frequency ⁽⁶⁾	f _{SW}	MODE = GND, I _{OUT} = 0A, V _{OUT} = 1V	480	600	720	kHz
		MODE = 30.1kΩ, I _{OUT} = 0A, V _{OUT} = 1V	680	800	920	kHz
		MODE = 60.4 kΩ, I _{OUT} = 0A, V _{OUT} = 1V	850	1000	1150	kHz
Minimum on time ⁽⁶⁾	T _{ON_MIN}	V _{FB} = 500mV			50	ns
Minimum off time ⁽⁶⁾	T _{OFF_MIN}	V _{FB} = 500mV			180	ns
Over-Voltage and Under-Voltage Protection						
OVP threshold	V _{OVP}		113%	116%	119%	V _{REF}
UVP threshold	V _{UVP}		77%	80%	83%	V _{REF}
Feedback Voltage and Soft Start						
Feedback voltage	V _{REF}	T _J = -40°C to +125°C	594	600	606	mV
		T _J = 0°C to +70°C	597	600	603	mV
TRK/REF sourcing current	I _{TRACK_Source}	V _{TRK/REF} = 0V		42		μA
TRK/REF sinking current	I _{TRACK_Sink}	V _{TRK/REF} = 1V		12		μA
Soft-start time	t _{SS} , From 10%- 90% V _{REF}	C _{TRACK} = 1nF, T _J = +25°C	0.55	0.8	1.25	ms
Error Amplifier						
Error amplifier offset	V _{OS}		-3	0	3	mV
Feedback current	I _{FB}	V _{FB} = REF		50	100	nA

ELECTRICAL CHARACTERISTICS (continued) $V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁷⁾, typical value is tested at $T_J = +25^{\circ}C$, unless otherwise noted.

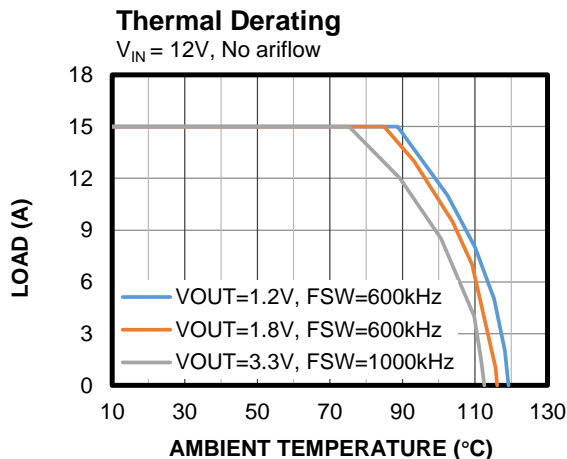
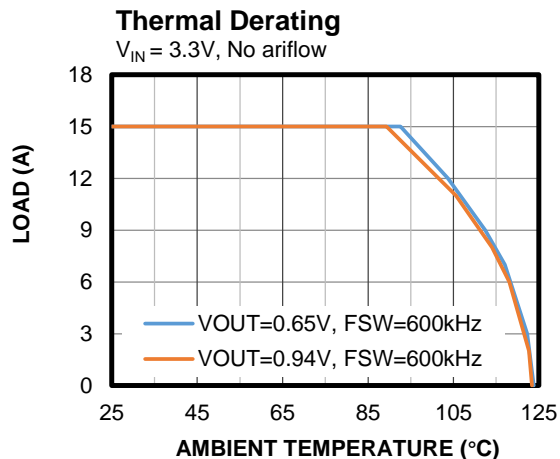
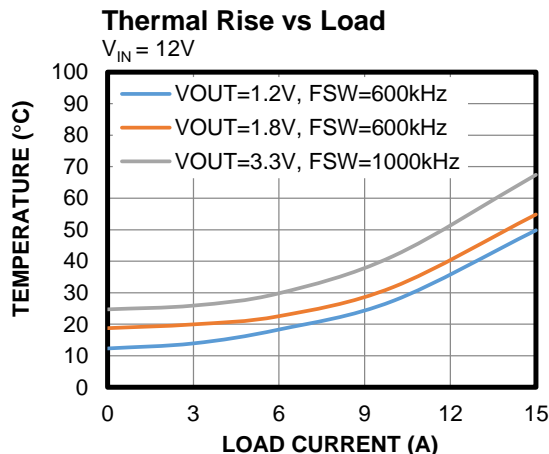
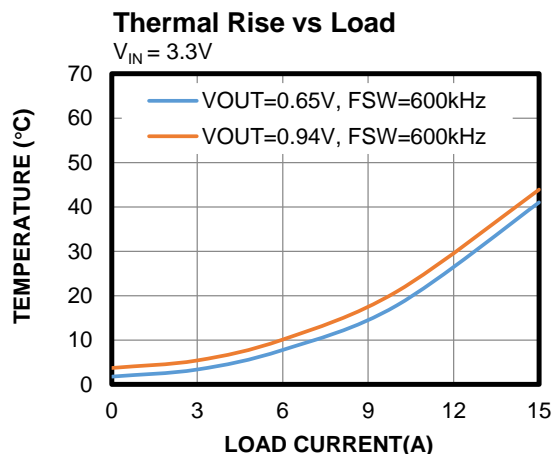
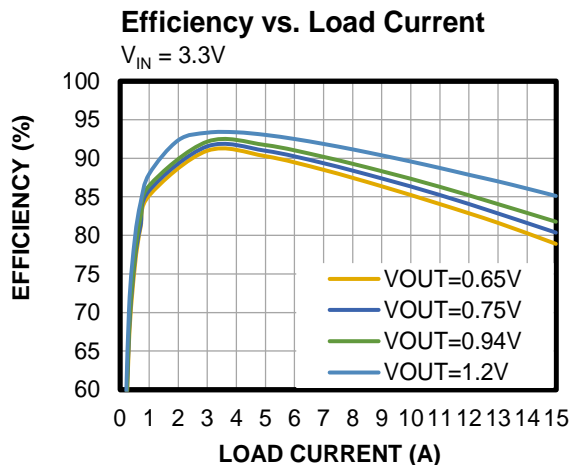
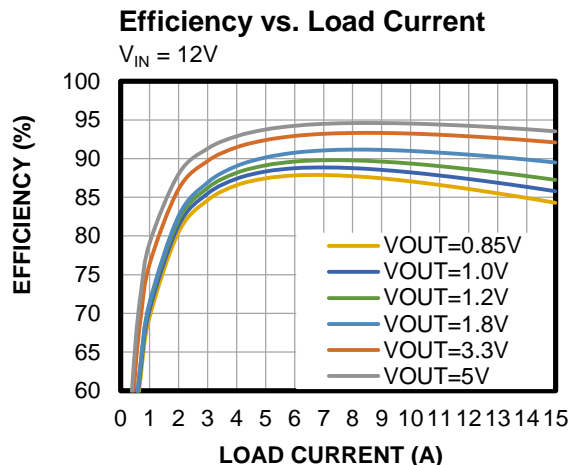
Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
Enable input rising threshold	VIH _{EN}		1.17	1.22	1.27	V
Enable hysteresis	V _{EN-HYS}			200		mV
Enable input current	I _{EN}	V _{EN} = 2V		0		μA
VIN UVLO						
VIN under-voltage lockout threshold rising	VIN _{Vth_Rise}	V _{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout threshold falling	VIN _{vth_Fall}		1.55	1.85	2.15	
VCC Regulator						
VCC under-voltage lockout threshold rising	VCC _{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold falling	VCC _{vth_Fall}		2.35	2.5	2.65	V
VCC regulator	V _{CC}		2.88	3.0	3.12	V
VCC load regulation		I _{cc} = 25mA		0.5		%
Power Good						
Power good high threshold	PG _{Vth_Hi_Rise}	FB from low to high	89.5%	92.5%	95.5%	V _{REF}
Power good low threshold	PG _{Vth_Lo_Rise}	FB from low to high	113%	116%	119%	V _{REF}
	PG _{Vth_Lo_Fall}	FB from high to low	77%	80%	83%	V _{REF}
Power good low to high delay	PG _{Td}	T _J = 25°C	0.63	0.9	1.17	ms
Power good sink current capability	V _{PG}	I _{PG} = 10mA			0.5	V
Power good leakage current	I _{PG_LEAK}	V _{PG} = 3.3V			3	μA
Power good low-level output voltage	V _{OL_100}	V _{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor @ 25°C		650	800	mV
	V _{OL_10}	V _{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor @ 25°C		750	900	mV
Thermal Protection						
Thermal shutdown ⁽⁶⁾	T _{SD}			160		°C
Thermal shutdown hysteresis ⁽⁶⁾				30		°C

Notes:

- 6) Guaranteed by sample characterization. Not tested in production.
7) Guaranteed by over-temperature (OT) correlation. Not tested in production

TYPICAL PERFORMANCE CHARACTERISTICS

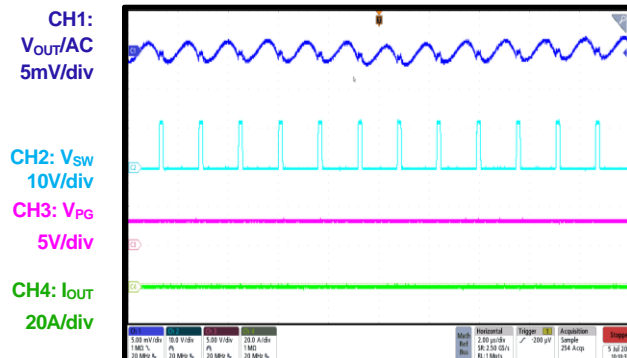
$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $C_{OUT} = 10 \times 47\mu F$ ceramic, FCCM, $F_{SW} = 600kHz$, $T_A = 25^\circ C$, unless otherwise noted.



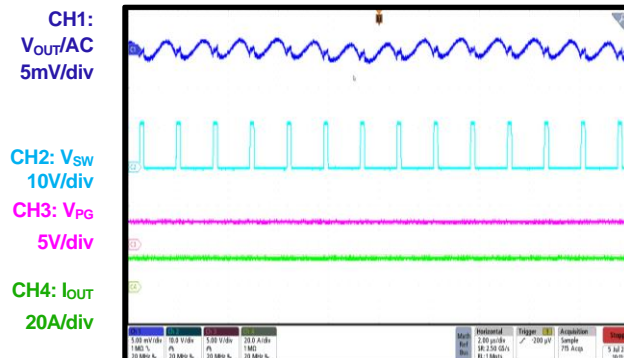
TYPICAL PERFORMANCE CHARACTERISTICS

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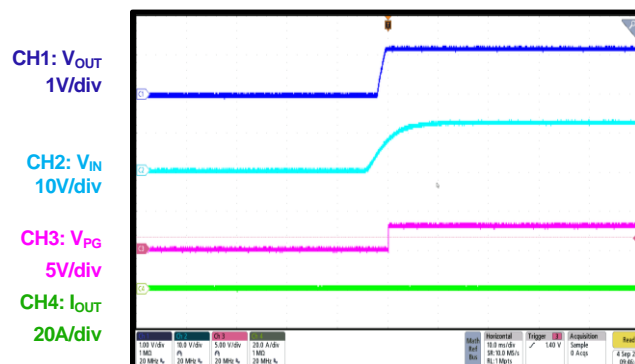
Steady State

 $I_O = 0A$ 

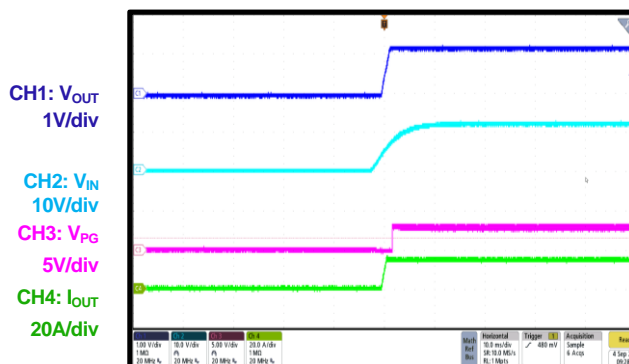
Steady State

 $I_O = 15A$ 

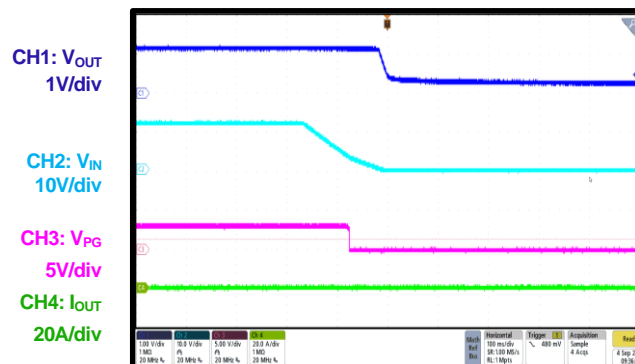
VIN start up

 $I_O = 0A$ 

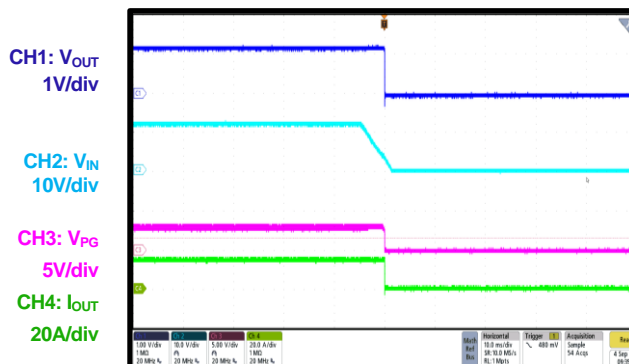
VIN start up

 $I_O = 15A$ 

VIN shutdown

 $I_O = 0A$ 

VIN shutdown

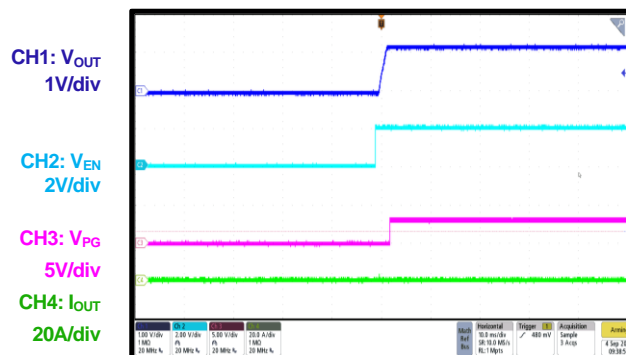
 $I_O = 15A$ 

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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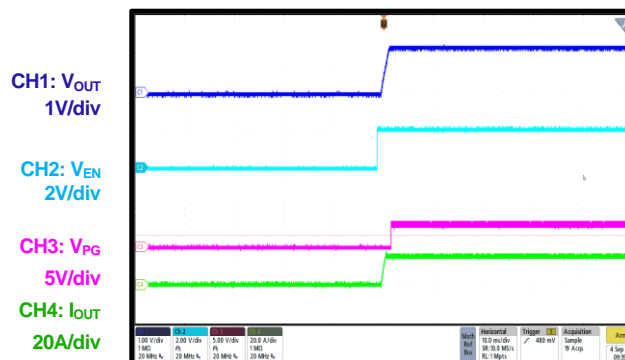
EN Startup

$I_O = 0A$



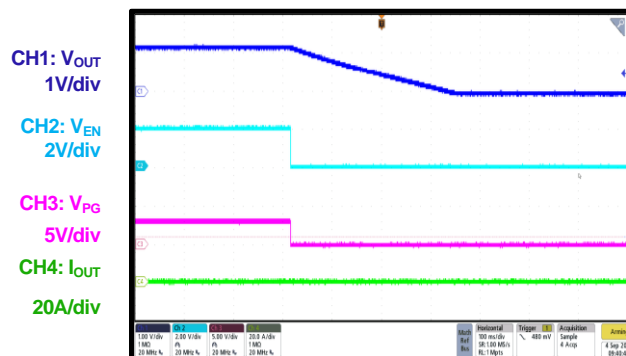
EN Startup

$I_O = 15A$



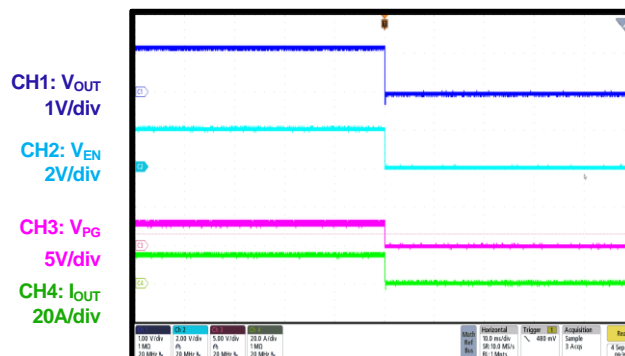
EN shutdown

$I_O = 0A$



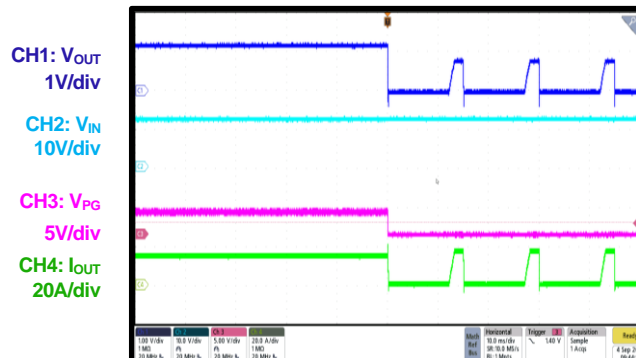
EN shutdown

$I_O = 15A$



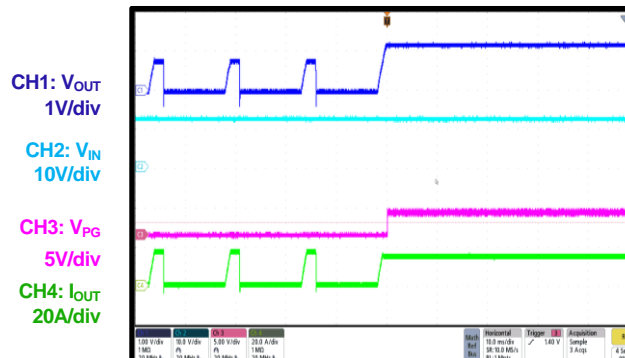
SCP Entry

$I_O = 15A$



SCP Recovery

$I_O = 15A$



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

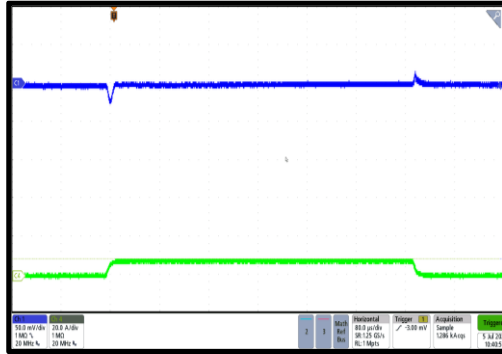
$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $C_{OUT} = 10 \times 47\mu F$ ceramic, FCCM, $F_{sw} = 600kHz$, $T_A = 25^\circ C$, unless otherwise noted.

load transient

$I_O = 0A-7.5A$, E-load, $2.5A/us$

CH1:
 V_{OUT}/AC
50mV/div

CH4: I_{OUT}
20A/div

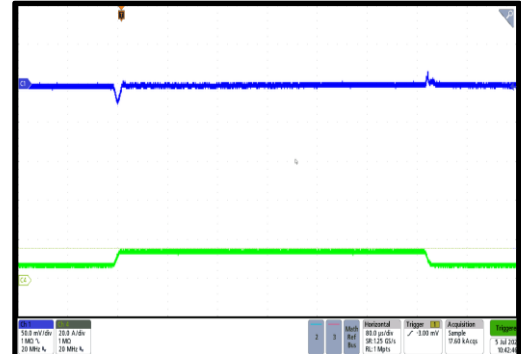


load transient

$I_O = 7.5A-15A$, E-load, $2.5A/us$

CH1:
 V_{OUT}/AC
50mV/div

CH4: I_{OUT}
20A/div



BLOCK DIAGRAM

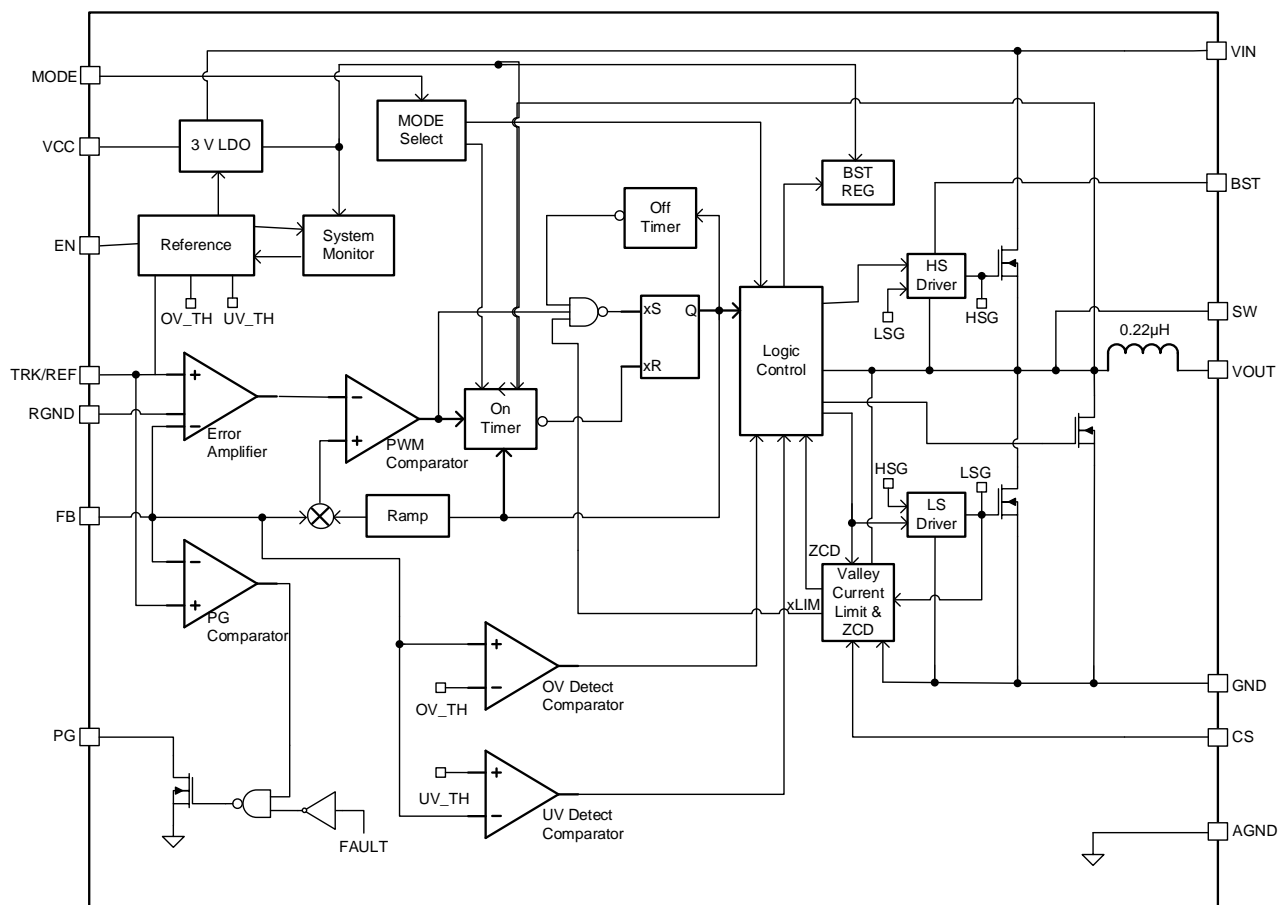


Figure 1: Functional Block Diagram

OPERATION

Constant-on-Time (COT) Control

The MPM3685 employs constant-on-time (COT) control to achieve a fast load transient response. Figure 2 details the control stage of the MPM3685.

The operational amplifier (AMP) corrects any error voltage between FB and V_{REF} . With the help of AMP, the MPM3685 can provide excellent load regulation over the entire load range, regardless of whether it is operating in forced continuous conduction mode (CCM) or pulse-skip mode.

The dedicated VSNS- pin helps to provide feedback remote GND sensing. The pair of the remote sense trace should be kept in low impedance to achieve the best performance.

The MPM3685 uses internal ramp compensation to support low ESR MLCC output capacitor solutions. The adaptive, internal ramp is optimized so that the MPM3685 is stable in the entire operating input and output voltage ranges with a proper design of the output L/C filter.

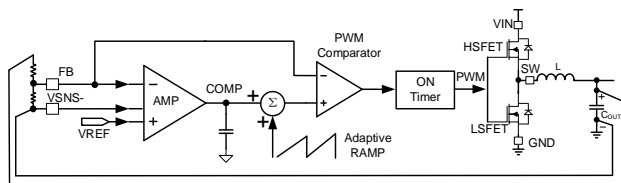


Figure 2: COT Control

Pulse-Width Modulation (PWM) Operation

Figure 3 shows how the pulse-width modulation (PWM) is generated. AMP corrects any error between FB and REF and generates a fairly smooth DC voltage (COMP). The internal ramp is superimposed onto COMP, and the superimposed COMP is compared with the FB signal. Whenever FB drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off and turns on again when FB drops below the superimposed COMP. By repeating this operation, the MPM3685 regulates the output voltage. The

integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and GND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot through. To avoid shoot through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

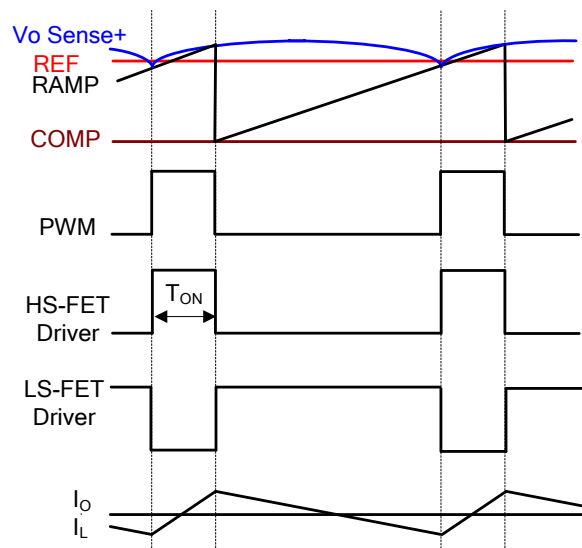


Figure 3: Heavy-Load Operation (PWM)

Continuous Conduction Mode (CCM) Operation

CCM occurs when the output current is high and the inductor current is always above zero amps. The MPM3685 can also be configured to operate in forced CCM operation when the output current is low (see the Mode Selection section for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), so the output ripple remains almost constant throughout the entire load range.

Pulse-Skip Operation

At light-load condition, the MPM3685 can be configured to work in pulse-skip mode to optimize the efficiency. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MPM3685 transitions from CCM to pulse-skip mode if it is configured to do so (see the Mode Selection section for details).

Figure 4 shows pulse-skip mode operation in light-load condition. When FB drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse-skip mode operation, FB will not reach the superimposed COMP while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Z) when the inductor current reaches zero. A current modulator takes over control of the LS-FET and limits the inductor current below -1mA. Therefore, the output capacitors discharge slowly to GND through the LS-FET. In light-load condition, the HS-FET is not turned on as frequently in pulse-skip mode as it is in forced CCM. As a result, the efficiency in pulse-skip mode is improved greatly compared to that in forced CCM operation.

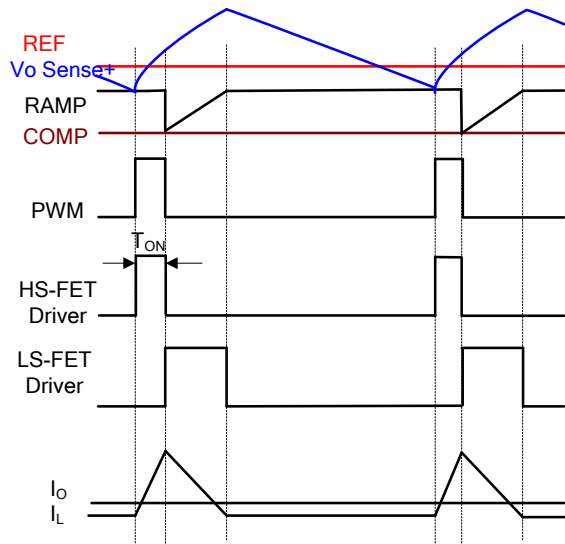


Figure 4: Pulse-Skip Mode at Light Load

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter, and the HS-FET is turned on more frequently. Therefore, the switching frequency increases accordingly. The output current reaches critical levels when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Output Voltage Tracking and Reference

Where F_{SW} represents the switching frequency, and $L=0.22\mu H$ represents the inductance of the integrated inductor.

The MPM3685 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MPM3685 can be configured to operate in forced CCM, even in a light-load condition (see Table 1).

Mode Selection

The MPM3685 provides both forced CCM operation and pulse-skip mode of operation under light-load condition. The MPM3685 has three options for switching frequency selection (600kHz, 800kHz, and 1000kHz). Select the operation mode under light-load condition and the switching frequency by choosing the value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: MODE Selection

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
243kΩ (±20%) to GND	Pulse skip	800kHz
121kΩ (±20%) to GND	Pulse skip	1000kHz
AGND	Forced CCM	600kHz
30.1kΩ (±20%) to GND	Forced CCM	800kHz
60.4kΩ (±20%) to GND	Forced CCM	1000kHz

Soft Start (SS)

The MPM3685 has a 1ms the minimum soft-start time (t_{ss}). Connect a soft-start capacitor (CSS) between the TRK/REF and VSNS- pins to increase t_{ss} .

The value of the soft-starting capacitor C_{SS} is determined by:

$$C_{SS}(\text{nF}) = \frac{t_{ss}(\text{ms}) \times 36\mu\text{A}}{0.6(\text{V})} \quad (2)$$

CSS can also be calculated with Equation (3):

$$C_{SS} = C_{SS1} + C_{SS2} \quad (3)$$

Where C_{SS2} is $\geq 22\text{nF}$.

The MPM3685 provides an analog input pin (TRK/REF) to track another power supply or accept an external reference. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MPM3685 output voltage. The FB voltage follows this external voltage signal exactly, and the soft-start settings are ignored. The TRK/REF input signal can be in the range of 0.3V to 1.4V. During the initial start-up, the TRK/REF must first reach 600mV or above to ensure proper operation. Afterward, it can be any value between 0.3V and 1.4V.

Pre-Bias Start-Up

The MPM3685 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the TRK/REF pin exceeds the sensed output voltage at FB pin. Before the TRK/REF voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop-in pre-biased level is negligible.

Current Sense and Over-Current Protection (OCP)

The MPM3685 features on-die current sensing and programmable over-current protection threshold for the inductor valley current.

The over-current protection is active when MPM3685 is enabled. During the LS-FET on state, the inductor current is sensed and mirrored to CS pin with the ratio of G_{CS} . By connecting a resistor (R_{CS}) between the CS and AGND pins, a V_{CS} voltage is generated which is proportional to the inductor current cycle-by-cycle. The HS-FET is allowed to turn on only when the V_{CS} voltage is below the internal over-current protection voltage threshold (V_{OCP}) (during the LS-FET on state) to limit the inductor valley current cycle-by-cycle.

The current limit threshold (R_{CS}) can be calculated with Equation (4):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIMIT} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times f_{SW}})} \quad (4)$$

Where $V_{OCP}=1.2V$, $G_{CS}=10\mu A/A$, $L=0.22\mu H$, and I_{LIMIT} is the desired output current limit (A).

It should be noted that the MPM3685 provides accurate cycle-by-cycle over-current protection for the inductor valley current. However, the conversion between the inductor valley current and the output current may involve error introduced by the tolerance of the integrated inductor and switching frequency variation due to the COT operation.

OCP hiccup is active 3ms after the MPM3685 is enabled. Once OCP hiccup is active, if the MPM3685 detects an over-current condition for 31 consecutive cycles, it enters hiccup mode. In hiccup mode, the MPM3685 latches off the HS-FET immediately and latches off the LS-FET after zero-current detection (ZCD) is detected. Meanwhile, the TRK/REF capacitor is discharged as well. After about 11ms, the MPM3685 attempts to soft start automatically. If the over-current condition still remains after 3ms, the MPM3685 repeats this operation cycle until the over-current condition is removed and the output voltage rises back to the regulation level smoothly.

Negative Inductor Current Limit

When the LS-FET detects a -18A (typical) current, the MPM3685 turns off the LS-FET for 200ns to limit the negative current.

Over-Voltage Protection (OVP)

The MPM3685 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides hiccup over-voltage protection (OVP) mode.

If the FB voltage exceeds 116% of the REF voltage, OVP is triggered. PG is pulled down until it reaches the low-side negative current limit (NOCP). Then the LS-FET is turned off momentarily for 200ns. The HS-FET is turned on during this period. After 200ns, the LS-FET is turned on again. The MPM3685 repeats this operation to discharge any over-voltage on the output. The MPM3685 exits OVP discharge mode when the feedback voltage drops below 105%*REF.

Over-Temperature Protection (OTP)

The MPM3685 has an over-temperature protection (OTP). The MPM3685 monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off and discharges the TRK/REF capacitors. OTP is a non-latch protection. There is a hysteresis of about 30°C. Once the junction temperature drops to about 130°C, a soft start is initiated.

The OTP function is effective once the MPM3685 is enabled.

Power Good (PG)

The MPM3685 has a power good (PG) output. PG is the open drain of a MOSFET. Connect PG to VCC or another external voltage source (less than 3.6V) through a pull-up resistor (typically 10kΩ). Besides, a 0.1μF capacitor and a 1kΩ resistor are suggested to be placed close to PG Pin if Vout is greater than 2.5V, more details is shown in Figure 12-Figure 14. After applying the input voltage, the MOSFET turns on, so PG is pulled to GND before TRK/REF is ready. After the FB voltage reaches 92.5% of the REF voltage, PG is pulled high after a 0.8ms delay.

When the FB voltage drops to 80 percent of the REF voltage or exceeds 116 percent of the nominal REF voltage, PG is pulled low, PG can be pulled high again after FB voltage increases to 92.5 percent of the REF voltage or drops to 101 percent of the REF voltage.

If the input supply fails to power the MPM3685, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the pull-up current is shown in Figure 5.

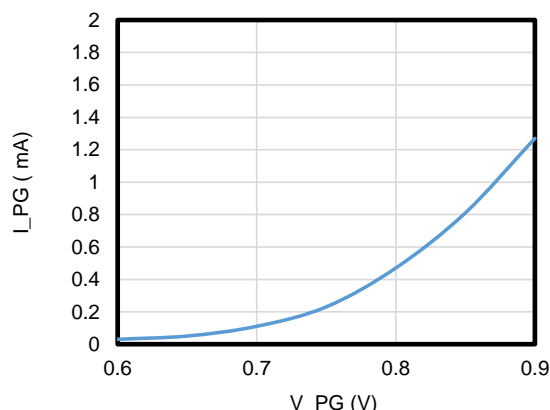


Figure 5: PG Clamped Voltage vs. Pull-Up Current

EN Configuration

The MPM3685 turns on when EN goes high. The MPM3685 turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MPM3685. EN should be pulled up only when Vin exceeds Vin UVLO.

The MPM3685 provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage at which the MPM3685 is enabled.

This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible under-voltage lockout (UVLO) bouncing during power-up and power-down. The resistor divider values can be determined by Equation (5):

$$V_{IN_START}(V) = V_{IH_EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (5)$$

Where V_{IH_EN} is 1.22V, typically.

R_{UP} and R_{DOWN} should be chosen so that the EN voltage does not exceed 3.6V when VIN reaches the maximum value.

APPLICATION INFORMATION

Setting the Output Voltage

The circuit connection is shown in Figure 6.

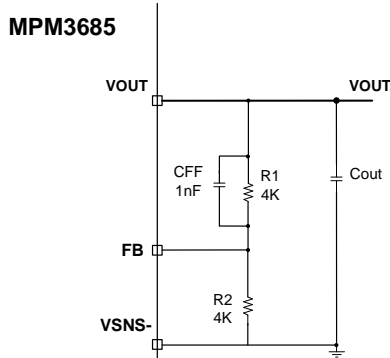


Figure 6: Circuit Connection

R2 can be determined with Equation (6):

$$R_2(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_1(k\Omega) \quad (6)$$

Where $V_{REF}=0.6V$.

For the best load transient response, place a feed-forward capacitor (C_{FF}) in parallel to R_1 . R_1 and C_{FF} add an extra zero to the system, which improves loop response. R_1 and C_{FF} are selected so that the zero is between 20kHz and 60kHz. This zero can be calculated with Equation (7):

$$f_z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (7)$$

Table 3 shows the values of feedback resistors and feedforward capacitor for common output voltages.

Table 3: Common Output Voltages

V _{OUT} (V)	C _{FF} (nF)	R ₁ (kΩ)	R ₂ (kΩ)
0.75	1	4	16
1.0	1	4	6
1.2	1	4	4
1.8	1	4	2
3.3	0.068	9	2
5	0.068	9.76	1.33

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down

converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During the layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (11):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (11)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors. Estimate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (12)$$

**PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE**

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (13)$$

Where L is fixed at 0.22μH internally.

The ESR dominates the switching frequency impedance for the POSCAP capacitors. For simplification, the output ripple can be approximated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (14)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 7, Figure 8 and follow the guidelines below.

1. Place the input MLCC capacitors as close to the VIN and GND pins as possible.
2. Place all signal traces far away from SW.
3. Maximize the VIN and GND copper plane to minimize parasitic impedance.
4. Ensure that the high-current paths (GND, VIN, and VOUT) have short, direct, and wide traces.
5. Place as many GND vias as possible to close GND to minimize both the parasitic impedance and thermal resistance.
6. Place the external feedback resistors next to FB.
7. Keep the feedback network away from the switching node.
8. If VIA has to be placed on PG pad, place it at least 10mm away from the positive side of the 1st input decoupling capacitor close to the IC. This is to prevent noise coupling from the high-speed switching Vin node.

■ Pad ■ Top Layer ■ Bottom Layer ● Via

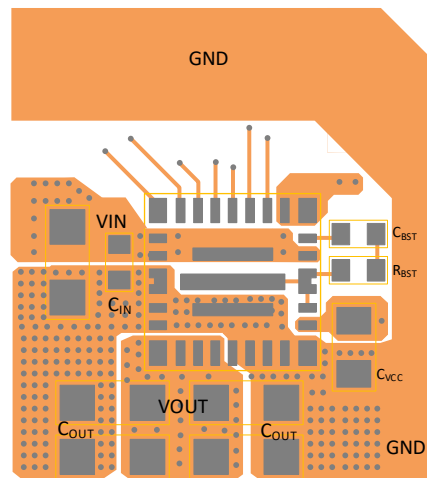


Figure 7: Recommended PCB Layout (Top)

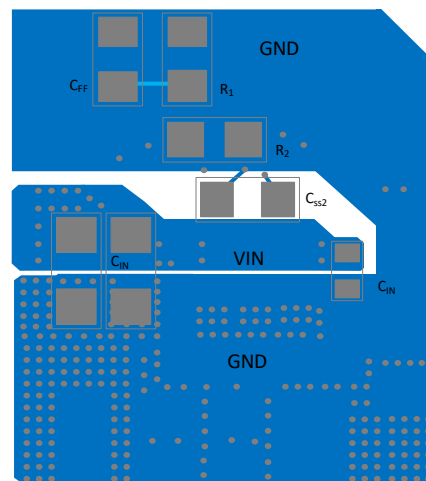


Figure 8: Recommended PCB Layout (Bottom)

TYPICAL APPLICATION CIRCUITS

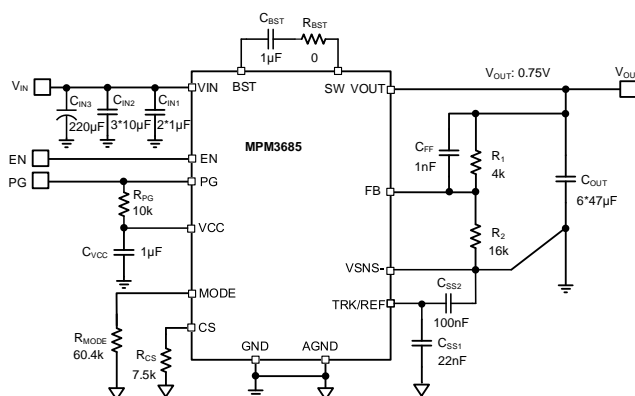


Figure 9: 0.75V Output Application Circuit

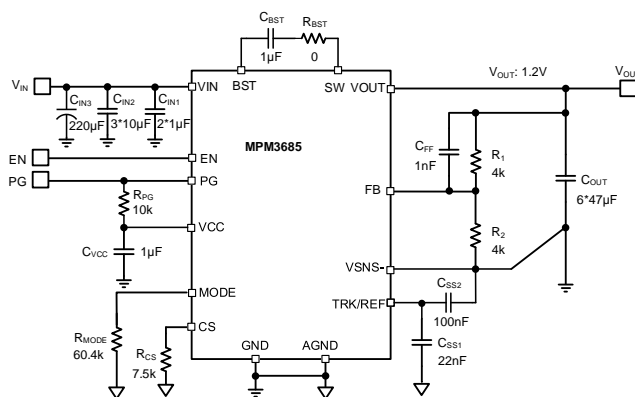


Figure 10: 1.2V Output Application Circuit

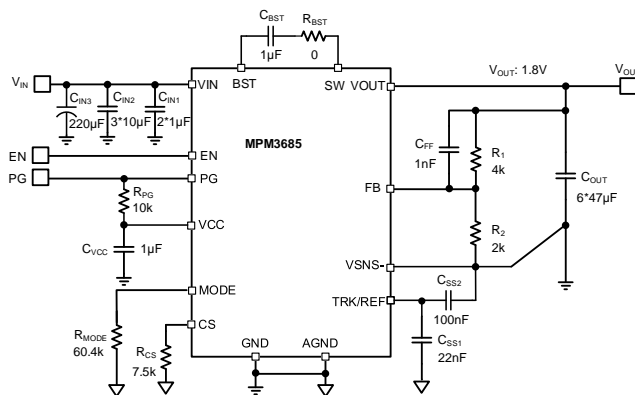


Figure 11: 1.8V Output Application Circuit

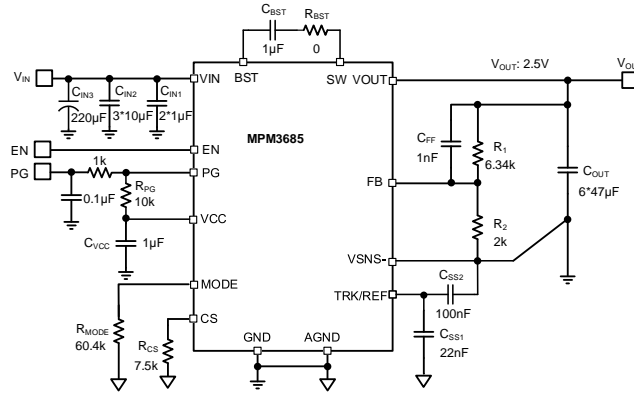


Figure 12: 2.5V Output Application Circuit

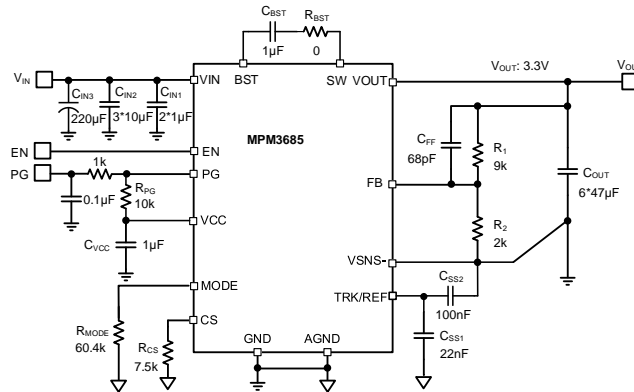


Figure 13: 3.3V Output Application Circuit

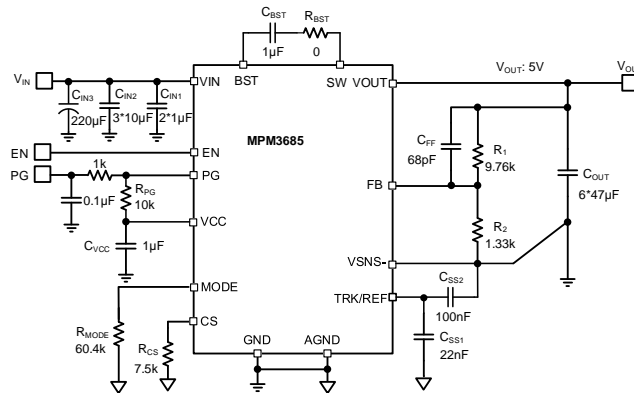
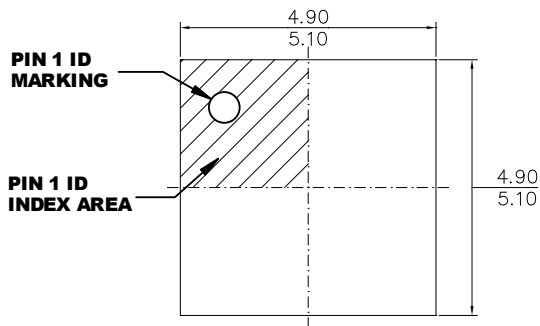


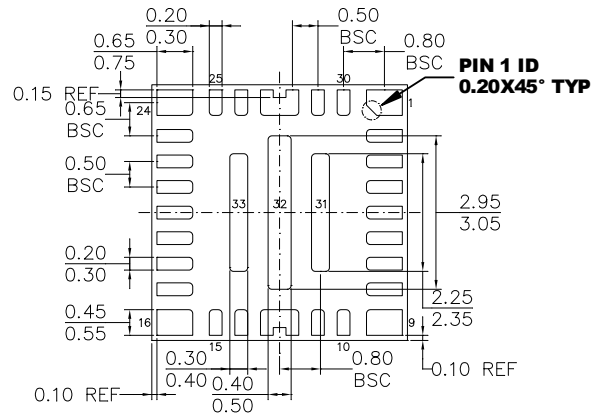
Figure 14: 5V Output Application Circuit

PACKAGE INFORMATION

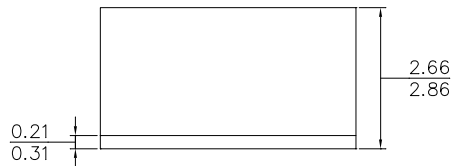
ECLGA (5mmx5mmx2.76mm)



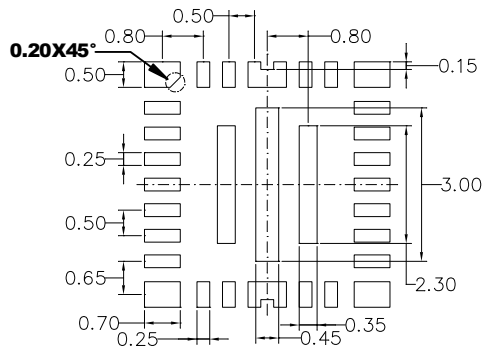
TOP VIEW



BOTTOM VIEW



SIDE VIEW

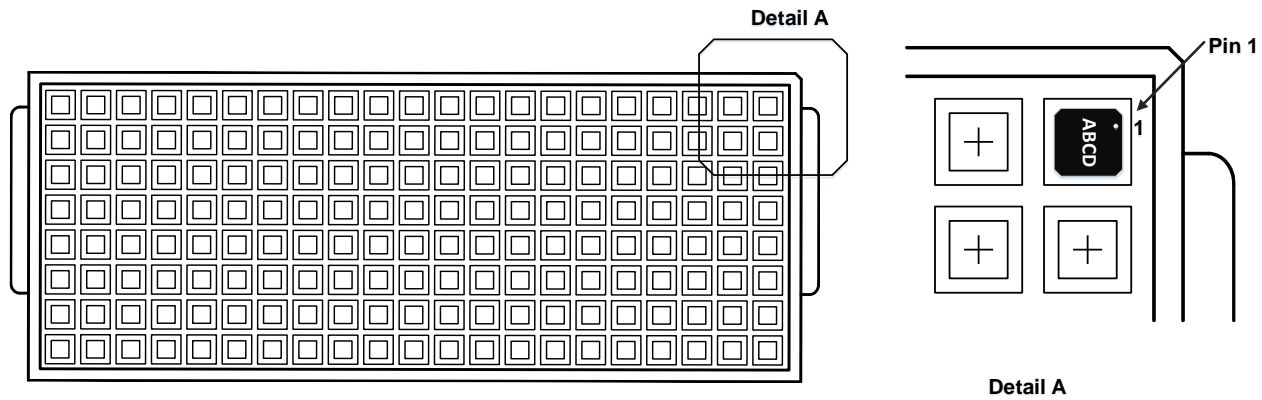


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.**
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION

**Note:**

This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width and height.

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3685GPU-T	ECLGA (5mmx5mmx2.76mm)	N/A	N/A	490	N/A	N/A	N/A

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