

# Pin Connection Guidelines

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## Agilex™ 5 FPGAs and SoCs

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## 1. Pin Connection Guidelines: Agilex™ 5 FPGAs and SoCs

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## 1.1. Pin Connection Guideline Status for Agilex™ 5 Devices

**Note:** The pin connection guideline statuses in this document represent the full Agilex™ 5 device family, which includes packages still in development. For the data sheet status of a specific Agilex 5 device series, refer to the *Agilex 5 FPGAs and SoCs Device Data Sheet*. For the Agilex 5 device pin-out status, refer to the device pin-out file.

The following descriptors designate the status level currently applicable to the relevant variant:

- Preliminary: Information in this document is **subject to change**. Intended for pre-production development, for production designs use with caution.
- Final: Information in this document is intended for use in **production design**.

**Table 1. Pin Connection Guideline Status for Agilex 5 Devices**

Tile	Status
Core Pins	Preliminary
HPS Pins	Preliminary
GTS Transceiver Pins	Preliminary
HVIO Pins	Preliminary

### Related Information

- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)
- [Agilex 5 Device Pin-Out Files](#)

## 1.2. Agilex 5 FPGA Core Pins

### 1.2.1. Clock and PLL Pins

**Note:** Altera recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 2. Clock and PLL Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK_[T,B]_2[A,B]_[0:1] [p,n] CLK_[T,B]_3[A,B]_[0:1] [p,n]	I/O, Clock Input	<p>Dual-purpose I/O pins that can be used for data inputs or outputs. On-chip termination such as differential input termination (<math>R_D</math> OCT), parallel termination (<math>R_T</math> OCT), and series termination (<math>R_S</math> OCT) are supported on these pins. For more information about the supported pins, refer to the device pin-out file.</p> <p>When you do not use these pins as dedicated clock pins, you can use them as regular I/O pins.</p> <p>Supported I/O standards:</p> <ul style="list-style-type: none"> <li>• 1.0 V</li> <li>• 1.05 V</li> <li>• 1.1 V</li> <li>• 1.2 V</li> <li>• 1.3 V</li> </ul> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p>	If the entire HSIO bank is unused, you may leave these pins floating, connected to <code>VCCIO_PIO</code> , or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.
PLL_[2] [A,B]_[T,B]_FB[0:1] PLL_[3] [A,B]_[T,B]_FB[0:1]	I/O, Clock Input	<p>Dual-purpose I/O pins that can be used as single-ended inputs, single-ended outputs, or external feedback input pins. For more information about the supported pins, refer to the device pin-out file.</p>	If the entire HSIO bank is unused, you may leave these pins floating, connected to <code>VCCIO_PIO</code> , or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		<p>Supported I/O standards:</p> <ul style="list-style-type: none"> <li>• 1.0 V</li> <li>• 1.05 V</li> <li>• 1.1 V</li> <li>• 1.2 V</li> <li>• 1.3 V</li> </ul> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p>	
PLL_[2] [A,B]_[T,B]_CLKOUT[0:1] [p,n] PLL_[3] [A,B]_[T,B]_CLKOUT[0:1] [p,n]	I/O, Clock Output	<p>I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.</p> <p>For more information about the supported pins, refer to the device pin-out file.</p> <p>Supported I/O standards:</p> <ul style="list-style-type: none"> <li>• 1.0 V</li> <li>• 1.05 V</li> <li>• 1.1 V</li> <li>• 1.2 V</li> <li>• 1.3 V</li> </ul> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p>	<p>If the entire HSIO bank is unused, you may leave these pins floating, connected to VCCIO_PIO, or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.</p>

### Related Information

- [Agilex 5 Device Pin-Out Files](#)
- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)

## 1.2.2. Dedicated Configuration/JTAG Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 3. Dedicated Configuration/JTAG Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
TCK	Input	Dedicated JTAG test clock input pin located in the Secure Device Manager (SDM) bank. You can also use this pin to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> section. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-down resistor. JTAG clock speed is 33 MHz for JTAG split mode. In the JTAG split mode, the SDM JTAG mode is independent of the HPS JTAG. JTAG clock speed is 22 MHz for JTAG daisy-chain mode. In the JTAG daisy-chain mode, the HPS DAP TAP is daisy chained with the SDM mTAP.	Connect this pin through a 1-kΩ pull-down resistor to GND. If you plan to use either the attestation or Black Key Provisioning (BKP) security features, or both, do not connect this pin to GND. Connect the TCK pin to the VCCIO_SDM supply using a 10-kΩ pull-up resistor.
TMS	Input	Dedicated JTAG test mode select input pin located in the SDM bank. You can also use this pin to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> section. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor.	Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_SDM supply. If the JTAG interface is not used, connect the TMS pin to the VCCIO_SDM supply using a 1-kΩ resistor.
TDO	Output	Dedicated JTAG test data output pin located in the SDM bank. You can also use this pin to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> section. This pin supports the 1.8-V single-ended I/O standard.	If the JTAG interface is not used, leave the TDO pin unconnected.
TDI	Input	Dedicated JTAG test data input pin located in the SDM bank. You can also use this pin to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> section. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor.	Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_SDM supply. If the JTAG interface is not used, connect the TDI pin to the VCCIO_SDM supply using a 1-kΩ resistor.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
nSTATUS	Output	<p>Configuration status pin. This pin is used for synchronization with the configuration host driving nCONFIG and to report errors.</p> <p>This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor. The drive strength is 8 mA.</p> <p><b>Attention:</b> Ensure that during power up, no external component drives the nSTATUS signal low.</p>	<p>When you are using the Avalon® streaming configuration scheme, connect this pin to the configuration host.</p> <p>For other configuration schemes, use this pin to monitor the configuration status.</p> <p>You must pull up this pin through a 10-kΩ resistor to VCCIO_SDM for all configuration schemes.</p>
nCONFIG	Input	<p>The nCONFIG pin is used to clear the device and prepare for reconfiguration.</p> <p>This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor.</p>	<p>When you use the Avalon streaming configuration scheme, connect this pin to the configuration host.</p> <p>When you use other configuration schemes, pull this pin to VCCIO_SDM through an external 10-KΩ pull-up resistor. Use this pin to restart configuration by driving it low and then high again. Ensure that you follow all the requirements for the nCONFIG operation as specified in the <i>Device Configuration User Guide: Agilex 5 FPGAs and SoCs</i>.</p>
OSC_CLK_1	Input	<p>Reference clock source for SDM PLL.</p> <p>Use this pin as the clock for device configuration and transceiver calibration.</p> <p>This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-down resistor.</p>	<p>If you use transceivers, MIPI, EMIF, and PHY Lite interfaces, you must provide an external clock source to this pin.</p> <p>If you choose to use either the external clock source for configuration or instantiate any transceivers, MIPI, EMIF, and PHY Lite interfaces in your design, or both, you must provide a 25-MHz, 100-MHz, or 125-MHz free-running clock source to this pin and enable it in the Quartus Prime software when you compile your design.</p> <p>If you are using the internal oscillator for configuration and do not instantiate any transceivers, MIPI, EMIF, and PHY Lite interfaces in your design, leave this pin unconnected.</p>

### Related Information

- [Device Configuration User Guide: Agilex 5 FPGAs and SoCs](#)
- [HPS JTAG Pins](#) on page 45

### 1.2.3. Optional/Dual-Purpose Configuration Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Attention:** There are pins usage restriction for dual-purpose pins in the Avalon streaming interface x16 mode, refer to the *Device Configuration User Guide: Agilex 5 FPGAs and SoCs* for more details.

**Table 4. Optional/Dual-Purpose Configuration Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
AVST_DATA[15:0]	I/O, Input	<p>Dual-purpose configuration data input pins. Use the AVST_DATA[15:0] pins for Avalon streaming interface x16 mode.</p> <p>This pin supports the 1.2-V LVCMOS I/O standard only if you are using Avalon streaming interface x16 configuration scheme.</p> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p> <p><b>Attention:</b> Access to the I/O pins located in bank 3AT with pin index [91...95] is not allowed for the Avalon streaming interface x16 configuration scheme. You must leave these pins unconnected. For more information, refer to the device pin mapping files to identify the exact pin location.</p>	If these pins are not used as the dual-purpose pins and they are not used as I/O pins, leave these pins unconnected.
AVST_READY (3ATbank)	I/O, Output	<p>Dual-purpose Avalon streaming interface data ready output pin. Use the AVST_READY (3ATbank) pin for the Avalon streaming interface x16 configuration schemes.</p> <p>You cannot use this pin as a user I/O pin if you are using the Avalon streaming interface x16 configuration scheme.</p> <p>This pin supports the 1.2-V LVCMOS I/O standard only if you are using Avalon streaming interface x16 configuration scheme.</p>	Connect this pin to the ready signal input of the external configuration controller when configuring using the Avalon streaming x16 interface.

*continued...*

Pin Name	Pin Functions	Pin Description	Connection Guidelines
		These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> .	
AVST_CLK (3ATbank)	I/O, Input	<p>Dual-purpose Avalon streaming interface clock input pin. Use the AVST_CLK (3ATbank) for the Avalon streaming interface x16 configuration schemes.</p> <p>You can also use this pin as a user I/O pin after configuration. This pin supports the 1.2-V LVCMOS I/O standard only if you are using Avalon streaming interface x16 configuration scheme.</p> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p>	<p>Connect this pin to the clock signal of the external configuration controller when configuring using the Avalon streaming x16 interface.</p> <p>Connect unused pins as defined in the Quartus Prime software.</p>
AVST_VALID (3ATbank)	I/O, Input	<p>Dual-purpose configuration data valid pin. Use the AVST_VALID (3ATbank) pin for the Avalon streaming interface x16 configuration schemes.</p> <p>You can also use this pin as a user I/O pin after configuration. This pin supports the 1.2-V LVCMOS I/O standard only if you are using Avalon streaming interface x16 configuration scheme.</p> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p>	<p>Connect this pin to the data valid signal of the external configuration controller when configuring using the Avalon streaming x16 interface.</p> <p>Connect unused pins as defined in the Quartus Prime software.</p>

### Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)

### 1.2.4. Differential I/O Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 5. Differential I/O Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DIFF_IO_[2][A,B]_[T,B] [1:24][p,n] DIFF_IO_[3][A,B]_[T,B] [1:24][p,n]	I/O, RX/TX channel	<p>These are LVDS SERDES channels on HSIO banks. If these pins are not used in LVDS SERDES implementation, these pins are available as user I/O pins.</p> <p>Supported I/O standards:</p> <ul style="list-style-type: none"> <li>1.3-V I/O standard for true differential I/O</li> <li>1.3-V I/O standard for single-ended non-voltage referenced I/O</li> <li>1.2-V I/O standard for single-ended voltage referenced and non-voltage referenced I/O</li> <li>1.2-V I/O standard for differential voltage referenced I/O</li> <li>1.2-V I/O standard for true differential I/O</li> <li>1.1-V I/O standard for single-ended voltage referenced and non-voltage referenced I/O</li> <li>1.1-V I/O standard for differential voltage referenced I/O</li> <li>1.1-V I/O standard for true differential I/O</li> <li>1.05-V I/O standard for single-ended voltage referenced and non-voltage referenced I/O</li> <li>1.05-V I/O standard for differential voltage referenced input</li> <li>1.05-V I/O standard for true differential I/O</li> <li>1.0-V I/O standard for non-voltage referenced I/O</li> </ul> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p> <p>For more information about the I/O placement guidelines, refer to the <i>General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs</i>.</p>	<p>Connect unused pins as defined in the Quartus Prime software.</p> <p>If the entire HSIO bank is unused, you may leave these pins floating, connected to VCCIO_PIO, or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.</p>

#### Related Information

- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)
- [General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs](#)

## 1.2.5. External Memory Interface Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 6. External Memory Interface Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQS[0:63]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry. Supported I/O standards: <ul style="list-style-type: none"> <li>• POD 1.2-V I/O standard</li> <li>• SSTL 1.2-V I/O standard</li> <li>• POD 1.1-V I/O standard</li> <li>• LVSTL 1.1-V I/O standard</li> <li>• LVSTL 1.05-V I/O standard</li> <li>• LVSTL700</li> </ul>	Connect unused pins as defined in the Quartus Prime software. If the entire HSIO bank is unused, you may leave these pins floating, connected to VCCIO_PIO, or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.
DQSn[0:63]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry. Supported I/O standards: <ul style="list-style-type: none"> <li>• POD 1.2-V I/O standard</li> <li>• SSTL 1.2-V I/O standard</li> <li>• POD 1.1-V I/O standard</li> <li>• LVSTL 1.1-V I/O standard</li> <li>• LVSTL 1.05-V I/O standard</li> <li>• LVSTL700</li> </ul>	Connect unused pins as defined in the Quartus Prime software. If the entire HSIO bank is unused, you may leave these pins floating, connected to VCCIO_PIO, or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.
DQ[0:63]	I/O, bidirectional	Optional data signal for use in external memory interfacing. Analyze the available DQ pins across all pertinent DQS columns in the device pin-out file.	Connect unused pins as defined in the Quartus Prime software. If the entire HSIO bank is unused, you may leave these pins floating, connected to VCCIO_PIO, or connected to a tri-stated upstream or downstream I/O pin. If the unused pins reside in an active HSIO bank, you may leave these pins floating or connected to a tri-stated upstream or downstream I/O pin.

*continued...*

Pin Name	Pin Functions	Pin Description	Connection Guidelines
		<p>Supported I/O standards:</p> <ul style="list-style-type: none"> <li>• POD 1.2-V I/O standard</li> <li>• SSTL 1.2-V I/O standard</li> <li>• POD 1.1-V I/O standard</li> <li>• LVSTL 1.1-V I/O standard</li> <li>• LVSTL 1.05-V I/O standard</li> <li>• LVSTL700</li> </ul> <p>For the DQ pin swapping guidelines, refer to the <i>External Memory Interfaces (EMIF) IP User Guide: Agilex 5 FPGA and SoCs</i>.</p>	

#### Related Information

- [Agilex 5 Device Pin-Out Files](#)
- [External Memory Interfaces \(EMIF\) IP User Guide: Agilex 5 FPGA and SoCs](#)

## 1.2.6. Voltage Sensor and Voltage Reference Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 7. Voltage Sensor and Voltage Reference Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VREFP_ADC	Input	Dedicated precision analog voltage reference.	Tie the VREFP_ADC pin to an external 1.25 V accurate reference source ( $\pm 0.1\%$ ) for better ADC performance. Treat the VREFP_ADC as an analog signal together with the VREFN_ADC signal that provides a differential 1.25 V voltage. If no external reference is supplied, always connect the VREFP_ADC pin to GND. An on-chip reference source ( $\pm 2\%$ ) is activated if the external voltage reference source is disabled. Do not drive the VREFP_ADC pin until the VCCADC power rail has reached 1.62 V to prevent damage.
VREFN_ADC	Input		Tie the VREFN_ADC pin to the GND for better ADC performance. Treat VREFN_ADC as an analog signal together with the VREFP_ADC signal that provides a differential 1.25 V voltage. If no external reference is supplied, always connect the VREFN_ADC pin to GND.
VSIGP_[0,1]	Input	Analog differential inputs pins used with the voltage sensor inside the FPGA to monitor external analog voltages.	Tie these pins to GND if you do not use the voltage sensor feature. For more information about the usage of these pins, refer to the <i>Power Management User Guide: Agilex 5 FPGAs and SoCs</i> . Do not drive the VSIGP and VSIGN pins until the VCCADC power rail has reached 1.62 V to prevent damage.
VSIGN_[0,1]	Input		

### Related Information

Power Management User Guide: Agilex 5 FPGAs and SoCs

### 1.2.7. Remote Temperature Sensing Diode Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 8. Remote Temperature Sensing Diode Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
TEMPDIODE0A [p, n]	Input	These pins connect to the internal temperature sensing diodes in the FPGA core and corner areas of the FPGA.	Connect these pins to an external temperature sensing device to allow sensing of the FPGA's temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave these pins unconnected. For more information about the locations and channel numbers of the temperature sensors, refer to the <i>Agilex 5 Sensor Monitoring System</i> chapter in the <i>Power Management User Guide: Agilex 5 FPGAs and SoCs</i> .

#### Related Information

[Agilex 5 Sensor Monitoring System, Power Management User Guide: Agilex 5 FPGAs and SoCs](#)



### 1.2.8. Reference Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 9. Reference Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RZQ_[T,B]_2[A,B] RZQ_[T,B]_3[A,B]	I/O	<p>Reference pins for I/O banks. The RZQ pins share the same VCCIO_PIO with the I/O bank where they are located.</p> <p>Connect the external precision resistor to the designated pin within the bank. If not required, this pin is a regular I/O pin. These pins support 1.3-V, 1.2-V, 1.1-V, 1.05-V, and 1.0-V I/O standard.</p> <p>These pins support the programmable pull-up resistor. For more information, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p> <p>For more information about the supported pins, refer to the device pin-out file.</p>	<p>When using OCT, tie these pins to GND through a 240-Ω resistor.</p> <p>When you do not use these pins as dedicated input for the external precision resistor or as I/O pins, leave these pins unconnected.</p>

#### Related Information

- [Agilex 5 Device Pin-Out Files](#)
- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)

### 1.2.9. HVIO GPIO Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 10. HVIO GPIO Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
HVIO_5[A,B]_[1:20] HVIO_6[A,B,C,D,E,F,G,H]_[1:20]	I/O	General-purpose input/output pins. Support I/O standards: <ul style="list-style-type: none"> <li>• 1.8-V LVCMOS I/O standard</li> <li>• 1.8-V LVTTL I/O standard</li> <li>• 2.5-V LVCMOS I/O standard</li> <li>• 2.5-V LVTTL I/O standard</li> <li>• 3.3-V LVCMOS I/O standard</li> <li>• 3.3-V LVTTL I/O standard</li> </ul>	Connect unused pins as defined in the Quartus Prime software.

## 1.2.10. HVIO Optional Function Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Note:** Agilex 5 FPGA HVIO supports RGMII at 1.8 V.

**Table 11. HVIO Optional Function Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
PLLREFCLK[1,2]	Input	Reference clock input pins for IOPLL.	Provide a single-ended external clock source to this pin. Connect unused pins as defined in the Quartus Prime software.
SOURCE_SYNC_CLK[1,2]	Input	Reference clock input pins to Fabric Core or RGMII interface. These pins can be used as RGMII receive clock when you have RGMII interface connected with the HVIO bank on board.	Provide a single-ended external clock source to this pin when the pin is used as a reference clock. Connect with RGMII_RX_CLK from Ethernet PHY when this pin is used as a RGMII receive clock. You can only use one of the two pins at a time as RGMII_RX_CLK. Connect unused pins as defined in the Quartus Prime software.
SYSPLLREFCLK_L1[A,B,C,D][0:1] SYSPLLREFCLK_R4[A,B,C,D][0:1]	Input	Reference clock input pins for system PLL in the GTS transceiver banks. You can also use the system PLL for the core fabric if it is unused by the GTS transceiver.	Provide a single-ended external clock source to this pin. Connect unused pins as defined in the Quartus Prime software.
PIN_PERST_N_CVP_L1[A,B,C,D][0,1] PIN_PERST_N_R4[A,B,C,D][0,1]	Input	Dual-purpose pin functions as user I/O pin or PCIe* platform reset pin. Two reset pins available for each GTS bank, select either one of the pins. For ES device, if one PERST pin is selected as reset signal for GTS, the unused PERST pin for the same GTS bank must be left floating. When used as PCIe platform reset, connect this pin to the system PCIe nPERST signal. When the pin is low, the transceivers are in reset. When the pin is high, the transceivers are out of reset.	Reset input in PCIe case. For ES device, if one PERST pin is selected as reset signal for GTS, the unused PERST pin for the same GTS bank must be left floating. In a PCIe adapter card implementation, connect this signal from the PCIe edge connector to each GTS PCIe reset input pin. You must pull up the 3.3-V PCIe nPERST signal on the adapter card. If the pin is assigned to PIN_PERST in the Quartus Prime IP but GTS is unused, tie to GND.

*continued...*

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			<p>If VCCIO_HVIO is 1.8-V or 2.5-V, use a level translator to fan out and change the 3.3-V open-drain nPERST signal from the PCIe connector to this pin of each GTS transceiver that is used on the board.</p> <p>In case when one reset pin controls multiple PCIe IPs in bifurcation mode, ensure that this signal is deasserted high after all IPs reference clocks are stable.</p>
TXCLK[1:20]	Output	Transmit clock. These pins can be used as RGMII transmit clock when you have RGMII interface connected with HVIO bank on board.	Connect unused pins as defined in the Quartus Prime software.
RXCLK[1:4]	Input	Reference clock input pins for the fabric core.	Provide a single-ended external clock source to this pin. Connect unused pins as defined in the Quartus Prime software.
Data_Ctrl[1:20]	Input/Output	Data and control signal. These pins can be used as RGMII data and control signal when you have RGMII interface connected with HVIO bank on board.	<p>When these pins are used as RGMII receive data (RXD) or RGMII transmit data (TXD), you must assign the 4 pins for RXD or TXD in groups of 4. For example, [1:4], [5:8], [9:12], [13:16], and [17:20].</p> <p>Connect unused pins as defined in the Quartus Prime software.</p>

### Related Information

[GTS Transceiver PHY User Guide: Agilex 5 FPGAs and SoCs](#)

### 1.2.11. No Connect and DNU Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 12. No Connect and DNU Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, GND, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration, you have the option to connect these pins to either power, GND, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.

### 1.2.12. Power Supply Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Note:** Altera recommends you to generate a .pin file from the Quartus Prime Fitter to verify power pin assignment. Altera also recommends using this .pin file to determine if it is safe to power down or ground certain power supplies for your specific design. This step informs you to make the appropriate design choices for unused power supplies for your design.

**Table 13. Power Supply Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCP	Power	VCCP supplies power to the periphery.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the <i>Electrical Characteristics</i> section in the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> . Use the Power and Thermal Calculator and the Quartus Prime Power Analyzer to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.
VCC	Power	VCC supplies power to the core.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the <i>Electrical Characteristics</i> section in the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> . Use the Power and Thermal Calculator and the Quartus Prime Power Analyzer to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.
continued...			

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCPT	Power	Power supply for the IOPLL, programmable power technology, and I/O pre-drivers.	<p>Connect VCCPT to a 1.8-V low noise switching regulator. You have the option to source the following from the same regulator as VCCPT:</p> <ul style="list-style-type: none"> <li>VCCIO_SDM, VCCIO_HPS, and VCCPT_HVIO</li> <li>VCCPLL_SDM, VCCPLL_HPS, and VCCADC with proper isolation filtering</li> </ul> <p>Voltage spike ringing may be observed on VCCPT during device power-down sequencing if VCC is powered down before VCCPT, with the magnitude of the voltage spike ringing higher than VCCPT. This is the expected behavior and causes neither any functional failure nor reliability concerns to the device.</p> <p>For more details about the decoupling recommendations for this voltage rail, refer to the <i>Power Distribution Network Design Guidelines</i> section in the <i>PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex 5 FPGAs and SoCs</i>.</p> <p>For the power rail sharing, refer to the <a href="#">Power Supply Sharing Guidelines for Agilex 5 Devices</a> section.</p>
VCCRCORE	Power	Power supply for programmable power technology.	<p>Connect the VCCRCORE to 1.2-V power supply.</p> <p>You have the option to source VCCRCORE from the same regulator as VCCIO_PIO when you are using 1.2 V for VCCIO_PIO.</p>
VCCH_SDM	Power	Voltage rail sense.	<p>You must connect this sense to the VCCERT_GTS (1.0 V) rail for the Agilex 5 device with transceiver and connect this sense to VCCL_SDM for the device without transceiver.</p>
VCCIO_PIO_2[A,B]T VCCIO_PIO_2[A,B]B VCCIO_PIO_3[A,B]T VCCIO_PIO_3[A,B]B	Power	<p>These are the supply voltage pins for the HSIO banks. Each sub-bank can support a different voltage level.</p> <p>Supported VCCIO standards include the following:</p> <ul style="list-style-type: none"> <li>1.0-V</li> <li>1.05-V</li> <li>1.1-V</li> <li>1.2-V</li> <li>1.3-V</li> </ul> <p>For more information about the supported pins, refer to the device pin-out file.</p>	<p>Connect these pins to a 1.0 V, 1.05 V, 1.1 V, 1.2 V, or 1.3 V power supplies, depending on the I/O standard required by the specific sub-bank.</p> <p>When the entire HSIO bank is unused, you may connect the VCCIO_PIO of the unused HSIO bank to GND, 1.0 V, 1.05 V, 1.1 V, 1.2 V, or 1.3 V.</p> <p>If only one of the sub-bank within the same HSIO bank is unused, you must connect the VCCIO_PIO of the unused sub-bank to the same VCCIO_PIO voltage level as the other actively utilized sub-bank.</p> <p>Do not leave the VCCIO_PIO floating.</p>

*continued...*

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			<p>For the voltage tolerance (<math>\pm 3\%</math> or <math>\pm 5\%</math>) in different use cases, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i>.</p> <p>For production device, you have option to connect VCCIO_PIO_T and VCCIO_PIO_B in the same I/O bank with different voltage level, for example, VCCIO_PIO_2AT (1.2 V) and VCCIO_PIO_2AB (1.1 V). For ES device, you must connect VCCIO_PIO_T and VCCIO_PIO_B in the same I/O bank with the same voltage level, for example, VCCIO_PIO_2AT (1.2 V) and VCCIO_PIO_2AB (1.2 V).</p> <p>If you have LVDS TX signals on the sub-bank of your board, the VCCIO_PIO of this sub-bank must be connected to 1.3 V.</p> <p>During the power-up sequence only, a transient current whose magnitude is less than the VCCIO_PIO operating static current may be observed as the VCCIO_PIO transistors become operational. This is the expected behavior and causes neither any functional failure nor reliability concerns to the device if the power-up or power-down sequence is followed.</p> <p>For more details, refer to the <i>Power Management User Guide: Agilex 5 FPGAs and SoCs</i> and <i>General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs</i>.</p> <p>For the power rail sharing, refer to the <a href="#">Power Supply Sharing Guidelines for Agilex 5 Devices</a> section.</p>
VCCIO_PIO_SDM	Power	VCCIO_PIO voltage rail sense line.	<p>Connect these pins to VCCIO_PIO_3AT as 1.2 V when you use Avalon streaming interface x16 for FPGA configuration. Connect these pins to VCCRCORE if you do not use Avalon streaming interface x16 for FPGA configuration.</p>
VCCIO_SDM	Power	Configuration pins power supply.	<p>Connect these pins to a 1.8-V power supply.</p> <p>For more details about the decoupling recommendations for this voltage rail, refer to the <i>Power Distribution Network Design Guidelines</i> section in the <i>PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex 5 FPGAs and SoCs</i>.</p> <p>For the power rail sharing, refer to the <a href="#">Power Supply Sharing Guidelines for Agilex 5 Devices</a> section.</p>
VCCPLLDIG_SDM	Power	SDM block PLL power pins.	<p>VCCPLLDIG_SDM must be sourced from the same regulator as VCCCL_SDM with proper isolation filtering.</p>
continued...			



Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCCL_SDM	Power	SDM power supply.	For the devices with speed grade -1V, -2V, -2E, -3V, and -4S, connect these pins to a 0.8-V power supply. For the devices with speed grade -5S, connect these pins to a 0.78-V power supply. For the devices with speed grade -6S and -6X, connect these pins to 0.75-V power supply.
VCCBAT	Power	Battery back-up power supply for device security Advanced Encryption Standard, Battery-backed RAM (AES BBRAM) key register.	<p>When using the device security AES BBRAM key, connect this pin to a non-volatile battery power source in the range of 1.0 V to 1.8 V. A series RC (R=10 kΩ, C=1 μF) circuit must be added to the VCCBAT rail. Connect a 10-kΩ resistor in series between the battery power source and VCCBAT. The 1-uF capacitor is connected between VCCPT and GND.</p> <p>For more information about the schematic diagram, refer to the <i>Power Distribution Network Design Guidelines</i> section in the <i>PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex 5 FPGAs and SoCs</i>.</p> <p>Provide a minimum decoupling of 47 nF for the VCCBAT power rail near the VCCBAT pin.</p> <p>When not using the AES BBRAM key, tie this pin to ground.</p>
VCCPLL_SDM	Power	VCCPLL_SDM supplies analog power to the SDM block PLLs.	<p>With proper isolation filtering, you have the option to source VCCPLL_SDM from the same regulator as VCCPT.</p> <p>Decoupling for these pins depends on the design decoupling requirements of the specific board.</p>
GND	Ground	Device ground pins.	Connect all GND pins to the board ground plane.
VCCLSENSE	Output	Differential sense line to external regulator.	<p>VCCLSENSE and GNDSENSE are differential remote sense pins for the VCC power. Connect the differential remote sense lines of your regulators to the respective VCCLSENSE and GNDSENSE pins. This compensates for the DC IR drop associated with the PCB and device package from the VCC power. Route these connections as differential pair traces and keep them isolated from any other noise source.</p> <p>You must connect the VCCLSENSE and GNDSENSE lines to the regulator's remote sense inputs. Altera strongly recommends connecting the VCCLSENSE and GNDSENSE lines to the regulator's remote sense inputs. If the remote sense is unused, then connect VCCLSENSE to VCC and tie GNDSENSE to GND.</p>
GNDSENSE			
continued...			

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCADC	Power	ADC power pin for the voltage sensors.	You must supply a low noise 1.8-V power supply to this pin if you are using the internal voltage sensors of the Agilex 5 device. Tie this pin to VCCPT with proper isolation filtering.
VCCFUSEWR_SDM	Power	The required power supply to program (write) the optional, one-time programmable eFuses. These eFuses are an integral part of the Agilex 5 security architecture.	Connect this pin to 1.8-V. You must source VCCFUSEWR_SDM and VCCPT from the same 1.8-V regulator.
VCCPT_HVIO	Power	Pre-driver analog power supply pin for HVIO.	Connect these pins to a 1.8-V power supply. You must share the same regulator with VCCPT.
VCCIO_HVIO	Power	Buffer analog power supply pin for HVIO.	You can connect these pins to a 1.8-V, 2.5-V, or 3.3-V power supply.
VCCL_ADC_SDM	Power	HPS DSU and periphery voltage sense.	For the range of the VCCL_ADC_SDM power supply voltage, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> . VCCL_ADC_SDM can be shared with VCC. Do not leave the VCCL_ADC_SDM floating or connected to GND.
VCC_IO_SDM	Power	SDM block I/O digital supply voltage sense.	For the range of the VCC_IO_SDM power supply voltage, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> . VCC_IO_SDM can be shared with VCC. Do not leave the VCC_IO_SDM floating or connected to GND.

### Related Information

- [Agilex 5 Device Pin-Out Files](#)
- [Agilex 5 FPGAs and SoCs Device Data Sheet](#)
- [General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs](#)
- [Power Management User Guide: Agilex 5 FPGAs and SoCs](#)
- [Power Distribution Network Design Guidelines, PCB Design Guidelines \(HSSI, EMIF, MIPI, True Differential, PDN\) User Guide: Agilex 5 FPGAs and SoCs](#)

### 1.2.13. Secure Device Manager (SDM) Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 14. SDM Pins**

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
RREF_SDM	Reference resistor input for the PLLs of the SDM interface.	—	Input to read reference resistance	Connect a 2-kΩ ±1% resistor to GND.
SDM_IO0	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO1	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA2	Connect this pin to the data2 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
		3'b001 or 3'b011	AS_DATA1	Connect this pin to the data1 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO2	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA0	Connect this pin to the data0 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
		3'b001 or 3'b011	AS_CLK	Connect this pin to the clock input of the QSPI flash device when configuring from the QSPI flash device.

*continued...*

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO3	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA3	Connect this pin to the data3 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
		3'b001 or 3'b011	AS_DATA2	Connect this pin to the data2 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO4	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA1	Connect this pin to the data1 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
		3'b001 or 3'b011	AS_DATA0	Connect this pin to the data0 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO5	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions as MSEL[0] during power up and reset to determine the configuration scheme. Once the pin completes the MSEL function, it then functions according to the configuration scheme you have selected.	—	MSEL[0]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCS00	Connect this pin to the nCS input of the first QSPI flash device when configuring from QSPI flash devices.
continued...				

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
	For more information, refer to the <i>Device Configuration User Guide: Agilex 5 FPGAs and SoCs</i> .	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO6	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA4	Connect this pin to the data4 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
		3'b001 or 3'b011	AS_DATA3	Connect this pin to the data3 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO7	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions as MSEL[1] during power up to determines the configuration scheme. Once the pin completes the MSEL function, it then functions according to the configuration scheme you have selected. For more information, refer to the <i>Device Configuration User Guide: Agilex 5 FPGAs and SoCs</i> .	—	MSEL[1]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCS02	Connect this pin to the nCS input of the third QSPI flash device when you use cascaded QSPI flash devices for HPS application and with Mailbox Client IP or HPS as data storage.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO8	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_READY	Connect this pin to the ready signal output of the external configuration controller when configuring using the Avalon streaming x8 interface.
continued...				

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		3'b001 or 3'b011	AS_nCS03	Connect this pin to the nCS input of the fourth QSPI flash device when you use cascaded QSPI flash devices for HPS application and with Mailbox Client IP or HPS as data storage. Connect with a 1-kΩ pull-up resistor to VCCIO_SDM.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO9	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions as MSEL[2] during power up to determines the configuration scheme. Once the pin completes the MSEL function, it then functions according to the configuration scheme you have selected. For more information, refer to the <i>Device Configuration User Guide: Agilex 5 FPGAs and SoCs</i> .	—	MSEL[2]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCS01	Connect this pin to the nCS input of the second QSPI flash device when you use cascaded QSPI flash devices for HPS application and with Mailbox Client IP or HPS as data storage.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO10	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA7	Connect this pin to the data7 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO11	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.	3'b110	AVSTx8_VALID	Connect this pin to the data valid pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
continued...				

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
	This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO12	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.	—	Any MSEL setting	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO13	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA5	Connect this pin to the data5 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO14	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_CLK	Connect this pin to the clock output of an external configuration controller when configuring using the Avalon streaming x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO15	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA6	Connect this pin to the data6 pin of an external configuration controller when configuring using the Avalon streaming x8 interface.
continued...				

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		3'b001 or 3'b011	AS_nRST	Connect this pin to the reset pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.
SDM_IO16	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> section.

### Related Information

Device Configuration User Guide: Agilex 5 FPGAs and SoCs



### 1.2.14. Secure Device Manager (SDM) Optional Signal Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 15. SDM Optional Signal Pins**

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes		
			ASx4	AVSTx8	AVSTx16
PWRMGT_SCL	PMBus Power Management Clock. This pin is used as the clock pin for the PMBus interface.	This pin requires a pull-up resistor to the 1.8-V VCCIO_SDM supply. Altera recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V. Connect this pin to the PMBus clock pin of your regulator. When a -V or -E power option device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the external master controller for the PMBus slave mode.	SDM_IO0 SDM_IO14	SDM_IO0	SDM_IO0 SDM_IO14
continued...					

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes		
			ASx4	AVSTx8	AVSTx16
		<i>Note:</i> Altera recommends holding the voltage level translators disabled by default to ensure that bus contention, excessive currents, or oscillations do not occur during FPGA rails ramp up or down.			
PWRMGT_SDA	PMBus Power Management Clock. This pin is used as the clock pin for the PMBus interface.	<p>This pin requires a pull-up resistor to the 1.8-V VCCIO_SDM supply. Altera recommends a pull-up value of 5.1-k<math>\Omega</math> to 10-k<math>\Omega</math> depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V. Connect this pin to the PMBus data pin of your regulator.</p> <p>When a Agilex 5 -V or -E power option device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the external master controller for the PMBus slave mode.</p> <p><i>Note:</i> Altera recommends holding the voltage level translators disabled by default to ensure that bus contention, excessive currents, or oscillations do not occur during FPGA rails ramp up or down.</p>	SDM_IO11 SDM_IO12 SDM_IO16	SDM_IO12 SDM_IO16	SDM_IO11 SDM_IO12 SDM_IO16
continued...					

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes		
			ASx4	AVSTx8	AVSTx16
PWRMGT_ALERT	PMBus Power Management Alert. This pin is used as the ALERT function for the PMBus interface when the Agilex 5 -V or -E power option device is the PMBus slave.	This pin requires a pull-up resistor to the 1.8-V VCCIO_SDM supply. Altera recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V. You must connect this pin to the PMBus ALERT pin of the external master controller.  When using the SmartVID feature with the Agilex 5 -V or -E power option device as a PMBus slave, you must connect the PWRMGT_ALERT signal along with the PWRMGT_SCL and PWRMGT_SDA signals to the PMBus master device to complete the SmartVID power management interface. The PMBus master device reads the VID codes from the Agilex 5 slave and programs the voltage regulator to output the correct VID voltage.  <i>Note:</i> Altera recommends holding the voltage level translators disabled by default to ensure that bus contention, excessive currents, or oscillations do not occur during FPGA rails ramp up or down.	SDM_IO0 SDM_IO12	SDM_IO0 SDM_IO9 SDM_IO12	SDM_IO0 SDM_IO9 SDM_IO12
CONF_DONE	The CONF_DONE pin indicates all configuration data has been received.	By default, Altera recommends using the SDM_IO16 pin to implement the CONF_DONE function. If SDM_IO16 is unavailable, the CONF_DONE function can also be implemented using any unused SDM_IO pins.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO6 SDM_IO7 SDM_IO10

**continued...**

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes		
			ASx4	AVSTx8	AVSTx16
		<p>Except for <code>SDM_IO0</code> and <code>SDM_IO16</code>, other <code>SDM_IO</code> pins are required to connect to an external 4.7-kΩ pull-down resistor for the <code>CONF_DONE</code> signal.</p> <p>Connect the <code>CONF_DONE</code> pin to the external configuration controller when configuring using the Avalon streaming interface.</p> <p>You have an option to monitor this signal with an external component if you are using the active serial (AS) x4 configuration scheme.</p>			<code>SDM_IO11</code> <code>SDM_IO12</code> <code>SDM_IO13</code> <code>SDM_IO14</code> <code>SDM_IO15</code> <code>SDM_IO16</code>
<code>INIT_DONE</code>	<p>The <code>INIT_DONE</code> pin indicates the device has entered user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Quartus Prime software.</p> <p>When the <code>INIT_DONE</code> function is enabled, this pin drives high when configuration is completed and the device goes into user mode.</p>	<p>Altera recommends you to use <code>SDM_IO0</code> or <code>SDM_IO16</code> to implement the <code>INIT_DONE</code> function when available as it has an internal weak pull-down for the correct function of <code>INIT_DONE</code> during power up.</p> <p>If <code>SDM_IO0</code> and <code>SDM_IO16</code> are unavailable, <code>SDM_IO5</code> can also be used for the <code>INIT_DONE</code> function when the configuration mode is set to Avalon streaming x8 or Avalon streaming x32 as these modes require an external 4.7-kΩ pull-down resistor.</p> <p>If <code>SDM_IO0</code>, <code>SDM_IO5</code>, and <code>SDM_IO16</code> are unavailable, the <code>INIT_DONE</code> function can also be implemented using any unused <code>SDM_IO</code> pins provided that an external 4.7-kΩ pull-down resistor is provided for the <code>INIT_DONE</code> signal.</p>	<code>SDM_IO0</code> <code>SDM_IO10</code> <code>SDM_IO11</code> <code>SDM_IO12</code> <code>SDM_IO13</code> <code>SDM_IO14</code> <code>SDM_IO16</code>	<code>SDM_IO0</code> <code>SDM_IO5</code> <code>SDM_IO12</code> <code>SDM_IO16</code>	<code>SDM_IO0</code> <code>SDM_IO1</code> <code>SDM_IO2</code> <code>SDM_IO3</code> <code>SDM_IO4</code> <code>SDM_IO6</code> <code>SDM_IO7</code> <code>SDM_IO10</code> <code>SDM_IO11</code> <code>SDM_IO12</code> <code>SDM_IO13</code> <code>SDM_IO14</code> <code>SDM_IO15</code> <code>SDM_IO16</code>
continued...					

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes		
			ASx4	AVSTx8	AVSTx16
CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has received the complete bitstream during configuration via protocol (CvP) core image configuration. When used for this purpose, enable this pin using the Quartus Prime software.	Connect this output pin to an external logic device that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	—
SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Quartus Prime software.	Connect this output pin to an external logic device that monitors the SEU event.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally, this pin generates interrupt to the SDM. The SDM then initiates a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM switches this pin to output and drives a pulse to indicate reset. Once the cold reset procedure is complete, this pin switches back to input.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. If using the HPS_COLD_nRESET functionality of this pin, connect this pin to an external logic device that manages the HPS Cold Reset behavior. External devices must release this signal and allow the pin to float high when not driving it low.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11

continued...

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes		
			ASx4	AVSTx8	AVSTx16
		Do not connect this pin to the reset input of any connected quad serial peripheral interface (quad SPI) devices. If you do not intend to utilize the HPS, do not use this optional SDM signal on this pin.			SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin instructs the device to load factory image, while driving logic low into this pin instructs the device to load the application image.	Connect this input pin to an external logic device that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image becomes the default image of the device, and only switch to factory image if required.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	—	—
nCATTRIP	The catastrophic trip signal, nCATTRIP, is an optional signal that you can assign to any unused SDM_IO pin. If enabled, the nCATTRIP signal always stays high and drives low when the core temperature is greater than the temperature threshold point that you set for your design. When the signal drives low, you must immediately power down the FPGA to avoid permanent damage to the device.	Connect this output pin to an external device that monitors the nCATTRIP event.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16

## Related Information

[Power Management User Guide: Agilex 5 FPGAs and SoCs](#)

## 1.3. Agilex 5 GTS Transceiver Pins

### 1.3.1. GTS Transceiver Power Supply Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 16. GTS Transceiver Power Supply Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCC_HSSI_L1 VCC_HSSI_R4	Power	<p>GTS transceiver digital logic power supply.</p> <ul style="list-style-type: none"> <li>For the devices with speed grade –1V, –2V, –2E, –3V, and –4S, it is 0.8-V.</li> <li>For the devices with speed grade –5S, it is 0.78-V.</li> <li>For the devices with speed grade –6S and –6X, it is 0.75-V.</li> </ul> <p>For more information about the supported pins, refer to the device pin-out file.</p>	<p>Connect VCC_HSSI to low noise switching regulator. Refer to the <i>Power Distribution Network Design Guidelines</i> section in the <i>PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex 5 FPGAs and SoCs</i> for the decoupling capacitor requirement.</p> <p>Do not tie it to GND or leave it floating if unused.</p>
VCCEHT_GTS[L1,R4] [A,B,C,D]	Power	<p>GTS transceiver high-voltage analog power supply pins.</p> <p>For more information about the supported pins, refer to the device pin-out file.</p>	<p>VCCEHT_GTS should share 1.8-V rail with VCCPT through a proper isolation filtering. Refer to <i>PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex 5 FPGAs and SoCs</i> for fitter details and decoupling capacitor requirement.</p> <p>Only selected GTS transceiver banks support power down. Tie to GND for power down only if you do not plan to use it in the future. Refer to the <i>Unused PMA Not Planned for Use in the Future</i> section in the <i>GTS Transceiver PHY User Guide: Agilex 5 FPGAs and SoCs</i> for more details about the GTS transceiver banks that support power down.</p>
VCCERT_GTS[L1,R4] [A,B,C,D]	Power	<p>GTS transceiver analog 1.0-V logic power pins.</p> <p>For more information about the supported pins, refer to the device pin-out file.</p>	<p>Connect VCCERT_GTS to 1.0-V dedicated regulator. Refer to <i>PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex 5 FPGAs and SoCs</i> for decoupling capacitor requirement.</p> <p>Only selected GTS transceiver banks support power down. Tie to GND for power down only if you do not plan to use it in the future. Refer to the <i>Unused PMA Not Planned for Use in the</i></p>

*continued...*

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			<i>Future section in the GTS Transceiver PHY User Guide: Agilex 5 FPGAs and SoCs for more details about the GTS transceiver banks that support power down.</i>

### Related Information

- [Agilex 5 Device Pin-Out Files](#)
- [Power Distribution Network Design Guidelines, PCB Design Guidelines \(HSSI, EMIF, MIPI, True Differential, PDN\) User Guide: Agilex 5 FPGAs and SoCs](#)
- [Unused PMA Not Planned for Use in the Future, GTS Transceiver PHY User Guide: Agilex 5 FPGAs and SoCs](#)



### 1.3.2. GTS Transceiver Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 17. GTS Transceiver Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RCOMP_GTS[L1,R4] [A,B,C,D]_P	Input	External biasing resistors for GTS.	Connect each RCOMP_GTS[L1,R4] [A,B,C,D]_P pin with a 499-Ω resistor ( $\pm 0.1\%$ ) to the RCOMP_GTS[L1,R4] [A,B,C,D]_N pin. In the PCB layout, the trace from this pin to the resistor needs to be routed such that it avoids any aggressor signals. Leave these floating if the entire side of the GTS transceiver banks are unused.
RCOMP_GTS[L1,R4] [A,B,C,D]_N			
REFCLK_GTS[L1,R4] [A,B,C,D]_CH1p	Input/Output	Local reference clock pins for GTS transceiver banks. This pin can be used as an input reference clock pin, or as an output for the CDR recovered clock. This pin is input-only for banks with the CDRCLKOUT pin. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Clock driver must be compatible with input requirement in DC coupling case. Tie to GND if these pins are not used.
REFCLK_GTS[L1,R4] [A,B,C,D]_CH1n			
CDRCLKOUT_GTS[L1,R4] [A,B,C]_CH2p	Output	CDR recovered clock output pins for GTS transceiver banks. This pin is only available in certain banks depending on the device variant. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Leave unused pins floating.
CDRCLKOUT_GTS[L1,R4] [A,B,C]_CH2n			
REFCLK_GTS[L1,R4] [A,B,C,D]_RX_P	Input	Regional reference clock input pins for GTS transceiver banks. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Clock driver must be compatible with input requirement in DC coupling case. Tie to GND if these pins are not used.
REFCLK_GTS[L1,R4] [A,B,C,D]_RX_N			
GTS[L1,R4] [A,B,C,D]_RX_CH[0,1,2,3] p	Input	GTS transceiver input pins. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Tie to GND if these pins are not used.
continued...			

Pin Name	Pin Functions	Pin Description	Connection Guidelines
GTS[L1,R4] [A,B,C,D]_RX_CH[0,1,2,3] ]n			
GTS[L1,R4] [A,B,C,D]_TX_CH[0,1,2,3] ]p	Output	GTS transceiver output pins. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Leave unused pins floating.
GTS[L1,R4] [A,B,C,D]_TX_CH[0,1,2,3] ]n			
APROBE_GTS[L1,R4] [A,B,C,D]_CH[0,1,2,3]	—	—	Leave these pins floating.
APROBE2_GTS[L1,R4] [A,B,C,D]	—	—	Leave these pins floating.

## Related Information

[Agilex 5 Device Pin-Out Files](#)

## 1.4. Agilex 5 Hard Processor System (HPS) Pins

### 1.4.1. HPS Power Supply Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 18. HPS Power Supply Pins**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCL_HPS	Power	VCCL_HPS supplies power to the HPS DSU and periphery circuitry.	For the range of the VCCL_HPS power supply voltage, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> . You must share VCCL_HPS with VCC together. If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS floating or connected to GND.
VCCL_HPS_CORE0_CORE1	Power	Supply power to HPS A55 Core 0 and Core 1.	For the range of the VCCL_HPS_CORE0_CORE1 power supply voltage, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> . VCCL_HPS_CORE0_CORE1 must be sourced from the same regulator with VCCL_HPS. You must share this power with VCC together. You have the option to connect this pin to GND if you do not intend to use the Cortex*-A55 cores.
VCCL_HPS_CORE2	Power	Supply power to the HPS A76 Core 2.	For the range of the VCCL_HPS_CORE2 power supply voltage, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> . VCCL_HPS_CORE2 must be sourced from the same regulator with VCCL_HPS. You must share this power with VCC together. You have the option to connect this pin to GND if you do not intend to use the Cortex-A76 core 2.
VCCL_HPS_CORE3	Power	Supply power to the HPS A76 Core 3.	For the range of the VCCL_HPS_CORE3 power supply voltage, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> .

*continued...*

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			<p>VCCL_HPS_CORE3 must be sourced from the same regulator with VCCL_HPS. You must share this power with VCC together.</p> <p>You have the option to connect this pin to GND if you do not intend to use the Cortex-A76 core 3.</p>
VCCIO_HPS	Power	The HPS dedicated I/Os support 1.8-V voltage level.	<p>Connect these pins to 1.8-V power supply. You have the option to source VCCIO_HPS pins from the same regulator as VCCPT.</p> <p>If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS floating or connected to GND.</p>
VCCPLL1_HPS	Power	Supply analog power to the main HPS PLLs.	<p>Connect these pins to a 1.8-V power supply. You have the option to share VCCPLL1_HPS with the same regulator as VCCPLL_SDM.</p> <p>If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to the HPS power supply. Do not leave the VCCPLL1_HPS floating or connected to GND.</p>
VCCPLL2_HPS	Power	Supply analog power to the peripheral HPS PLLs.	<p>Connect these pins to a 1.8-V power supply. You have the option to share VCCPLL2_HPS with the same regulator as VCCPLL_SDM.</p> <p>If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to the HPS power supply. Do not leave the VCCPLL2_HPS floating or connected to GND.</p>
VCCPLLDIG1_HPS	Power	Digital power supply of the main HPS PLLs.	<p>Connect this to the VCCL_HPS with proper isolation filtering.</p> <p>If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to the HPS power supply. Do not leave the VCCPLLDIG1_HPS floating or connected to GND.</p>
VCCPLLDIG2_HPS	Power	Digital power supply of the peripheral HPS PLLs.	<p>Connect this to the VCCL_HPS with proper isolation filtering.</p> <p>If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to the HPS power supply. Do not leave the VCCPLLDIG2_HPS floating or connected to GND.</p>

## Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)

### 1.4.2. HPS Oscillator Clock Input Pin

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 19. HPS Oscillator Clock Input Pin**

You must provide one input clock source to the HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
HPS_OSC_CLK	Clock input pin that drives the main PLL. Connect a single-ended clock source to this pin. The I/O standard of the clock source must be compatible with VCCIO_HPS. If you do not intend to utilize the HPS, you cannot use the HPS_OSC_CLK.	Input	Select one of the 48 HPS dedicated I/O. For details of the supported frequency, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> .

#### Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)

### 1.4.3. HPS JTAG Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 20. HPS JTAG Pins**

You have the option to connect HPS JTAG pins to the HPS Dedicated I/O using the following assignments.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
JTAG_TCK	HPS JTAG test clock input pin. Connect this pin through a 1-kΩ – 10-kΩ pull-down resistor to GND. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_9

*continued...*

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
	If you do not intend to utilize the HPS, you cannot use the HPS_IOB pins.		
JTAG_TMS	HPS JTAG test mode select input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG. If you do not intend to utilize the HPS, you cannot use the HPS_IOB pins.	Input	HPS_IOB_10
JTAG_TDO	HPS JTAG test data output pin. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG. If you do not intend to utilize the HPS, you cannot use the HPS_IOB pins.	Output	HPS_IOB_11
JTAG_TDI	HPS JTAG test data input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG. If you do not intend to utilize the HPS, you cannot use the HPS_IOB pins.	Input	HPS_IOB_12

#### 1.4.4. HPS GPIO Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 21. HPS GPIO Pins**

There are two GPIO controllers (GPIO0 and GPIO1) for the Agilex 5 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
GPIO0_IO[0..23]	General purpose input output. Ensure that the I/O standard used is compatible with VCCIO_HPS. Supports 1.8 V LVCMOS I/O standard. If you do not intend to utilize the HPS, these pins are in tristate mode with a weak pull-up enabled. Ensure that the weak high state of each pin does not cause issues with external circuitry.	I/O	HPS_IOA_[1..24] HPS_IOB_[1..24]
GPIO1_IO[0..23]			

### 1.4.5. HPS SDMMC Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 22. HPS SDMMC Pins**

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
SDMMC_CLK	SDMMC clock out.	Output	HPS_IOA_3	HPS_IOB_3
SDMMC_CMD	SDMMC command line. Pull this pin high on the board with a weak pull-up resistor. For example, a 10-kΩ to VCCIO_HPS.	I/O	HPS_IOA_8	HPS_IOB_8
SDMMC_DATA0	SDMMC Data 0.	I/O	HPS_IOA_1	HPS_IOB_1
SDMMC_DATA1	SDMMC Data 1.	I/O	HPS_IOA_2	HPS_IOB_2
SDMMC_DATA2	SDMMC Data 2.	I/O	HPS_IOA_6	HPS_IOB_6
SDMMC_DATA3	SDMMC Data 3. When using SD card, there is an existing 50-kΩ pull-up on SDMMC Data Bit 3 which can be disabled in the HPS software by using the SET_CLR_CARD_DETECT (ACMD42) command. This is not applicable to the eMMC flash.	I/O	HPS_IOA_7	HPS_IOB_7
SDMMC_DATA4	SDMMC Data 4.	I/O	HPS_IOA_9	HPS_IOB_9
SDMMC_DATA5	SDMMC Data 5.	I/O	HPS_IOA_10	HPS_IOB_10
SDMMC_DATA6	SDMMC Data 6.	I/O	HPS_IOA_11	HPS_IOB_11
SDMMC_DATA7	SDMMC Data 7.	I/O	HPS_IOA_12	HPS_IOB_12
SDMMC_PWR_ENA	SDMMC Power Enable. Device bus power. Control switch to turn power on or off to the card. Optional.	Output	HPS_IOA_14	HPS_IOB_14
<i>continued...</i>				

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
SDMMC_WRITE_PROTECT	SDMMC Write Protect.	Input	HPS_IOA_5	HPS_IOB_5
SDMMC_DATA_STROBE	SDMMC Data Strobe.	Input	HPS_IOA_16	HPS_IOB_16
SDMMC_PU_PD_DATA2	SDMMC pull-up/pull-down for pin DATA2. Used for 1.8 V operation without a level shifter, and LVSI compatible cards.	Output	HPS_IOA_13	HPS_IOB_13



### 1.4.6. HPS NAND Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 23. HPS NAND Pins**

HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
NAND_ADQ0	NAND Data Bit 0.	I/O	HPS_IOA_1	HPS_IOB_1
NAND_ADQ1	NAND Data Bit 1.	I/O	HPS_IOA_2	HPS_IOB_2
NAND_WE_N	NAND Write Enable. This is an active-low signal.	Output	HPS_IOA_3	HPS_IOB_3
NAND_RE_N	NAND Read Enable. This is an active-low signal.	Output	HPS_IOA_4	HPS_IOB_4
NAND_WP_N	NAND Write Protect. This is an active-low signal.	Output	HPS_IOA_5	HPS_IOB_5
NAND_ADQ2	NAND Data Bit 2	I/O	HPS_IOA_6	HPS_IOB_6
NAND_ADQ3	NAND Data Bit 3	I/O	HPS_IOA_7	HPS_IOB_7
NAND_CLE	NAND Command Latch Enable. This is an active-high signal.	Output	HPS_IOA_8	HPS_IOB_8
NAND_ADQ4	NAND Data Bit 4.	I/O	HPS_IOA_9	HPS_IOB_9
NAND_ADQ5	NAND Data Bit 5.	I/O	HPS_IOA_10	HPS_IOB_10
NAND_ADQ6	NAND Data Bit 6.	I/O	HPS_IOA_11	HPS_IOB_11
NAND_ADQ7	NAND Data Bit 7.	I/O	HPS_IOA_12	HPS_IOB_12
NAND_ALE	NAND Address Latch Enable. This is an active-high signal.	Output	HPS_IOA_13	HPS_IOB_13
NAND_RB_N	NAND Ready/Busy.	Input	HPS_IOA_14	HPS_IOB_14
<i>continued...</i>				

HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
	Connect this pin through a pull-up resistor to VCCIO_HPS. For more information of the pull-up resistor value, refer to the NAND flash specification.			
NAND_CE_N	NAND Chip Enable. This is an active-low signal.	Output	HPS_IOA_15	HPS_IOB_15
NAND_DQS	NAND signal to indicate data valid window.	Output	HPS_IOA_16	HPS_IOB_16
NAND_ADQ8	NAND Data Bit 8.	I/O	HPS_IOA_17	HPS_IOB_17
NAND_ADQ9	NAND Data Bit 9.	I/O	HPS_IOA_18	HPS_IOB_18
NAND_ADQ10	NAND Data Bit 10.	I/O	HPS_IOA_19	HPS_IOB_19
NAND_ADQ11	NAND Data Bit 11.	I/O	HPS_IOA_20	HPS_IOB_20
NAND_ADQ12	NAND Data Bit 12.	I/O	HPS_IOA_21	HPS_IOB_21
NAND_ADQ13	NAND Data Bit 13.	I/O	HPS_IOA_22	HPS_IOB_22
NAND_ADQ14	NAND Data Bit 14.	I/O	HPS_IOA_23	HPS_IOB_23
NAND_ADQ15	NAND Data Bit 15.	I/O	HPS_IOA_24	HPS_IOB_24

### 1.4.7. HPS USB Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 24. HPS USB Pins**

There are two USB controllers (USB0 and USB1) for the Agilex 5 HPS. USB0 supports USB 2.0 and USB1 supports USB 3.1. USB 3.1 pins are for ULPI compatibility only.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB0_CLK	USB0 Clock.	Input	HPS_IOA_1
USB0_STP	USB0 Stop Data.	Output	HPS_IOA_2
USB0_DIR	USB0 Direction.	Input	HPS_IOA_3
USB0_DATA0	USB0 Data Bit 0.	I/O	HPS_IOA_4
USB0_DATA1	USB0 Data Bit 1.	I/O	HPS_IOA_5
USB0_NXT	USB0 Next Data.	Input	HPS_IOA_6
USB0_DATA2	USB0 Data Bit 2.	I/O	HPS_IOA_7
USB0_DATA3	USB0 Data Bit 3.	I/O	HPS_IOA_8
USB0_DATA4	USB0 Data Bit 4.	I/O	HPS_IOA_9
USB0_DATA5	USB0 Data Bit 5.	I/O	HPS_IOA_10
USB0_DATA6	USB0 Data Bit 6.	I/O	HPS_IOA_11
USB0_DATA7	USB0 Data Bit 7.	I/O	HPS_IOA_12
USB1_CLK	USB1 Clock.	Input	HPS_IOA_13
USB1_STP	USB1 Stop Data.	Output	HPS_IOA_14
USB1_DIR	USB1 Direction.	Input	HPS_IOA_15
USB1_DATA0	USB1 Data Bit 0.	I/O	HPS_IOA_16
continued...			

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB1_DATA1	USB1 Data Bit 1.	I/O	HPS_IOA_17
USB1_NXT	USB1 Next Data.	Input	HPS_IOA_18
USB1_DATA2	USB1 Data Bit 2.	I/O	HPS_IOA_19
USB1_DATA3	USB1 Data Bit 3.	I/O	HPS_IOA_20
USB1_DATA4	USB1 Data Bit 4.	I/O	HPS_IOA_21
USB1_DATA5	USB1 Data Bit 5.	I/O	HPS_IOA_22
USB1_DATA6	USB1 Data Bit 6.	I/O	HPS_IOA_23
USB1_DATA7	USB1 Data Bit 7.	I/O	HPS_IOA_24

### 1.4.8. HPS EMAC Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 25. HPS EMAC Pins**

There are three EMAC controllers (EMAC0, EMAC1, and EMAC2) for the Agilex 5 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC0_TX_CLK	EMAC0 Transmit Clock.	Output	HPS_IOA_13
EMAC0_TX_CTL	EMAC0 Transmit Control.	Output	HPS_IOA_14
EMAC0_RX_CLK	EMAC0 Receive Clock.	Input	HPS_IOA_15
EMAC0_RX_CTL	EMAC0 Receive Control.	Input	HPS_IOA_16
EMAC0_TXD0	EMAC0 Transmit Data Bit 0.	Output	HPS_IOA_17
EMAC0_TXD1	EMAC0 Transmit Data Bit 1.	Output	HPS_IOA_18
EMAC0_RXD0	EMAC0 Receive Data Bit 0.	Input	HPS_IOA_19
EMAC0_RXD1	EMAC0 Receive Data Bit 1.	Input	HPS_IOA_20
EMAC0_TXD2	EMAC0 Transmit Data Bit 2.	Output	HPS_IOA_21
EMAC0_TXD3	EMAC0 Transmit Data Bit 3.	Output	HPS_IOA_22
EMAC0_RXD2	EMAC0 Receive Data Bit 2.	Input	HPS_IOA_23
EMAC0_RXD3	EMAC0 Receive Data Bit 3	Input	HPS_IOA_24
EMAC0_PPS0	EMAC0 1PPS signal.	Output	HPS_IOA_1 HPS_IOB_1
EMAC0_PPSTRIG0	EMAC0 1PPS trigger signal.	Input	HPS_IOA_2 HPS_IOB_2
EMAC1_TX_CLK	EMAC1 Transmit Clock.	Output	HPS_IOB_1
EMAC1_TX_CTL	EMAC1 Transmit Control.	Output	HPS_IOB_2

*continued...*

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC1_RX_CLK	EMAC1 Receive Clock.	Input	HPS_IOB_3
EMAC1_RX_CTL	EMAC1 Receive Control.	Input	HPS_IOB_4
EMAC1_TXD0	EMAC1 Transmit Data Bit 0.	Output	HPS_IOB_5
EMAC1_TXD1	EMAC1 Transmit Data Bit 1.	Output	HPS_IOB_6
EMAC1_RXD0	EMAC1 Receive Data Bit 0.	Input	HPS_IOB_7
EMAC1_RXD1	EMAC1 Receive Data Bit 1.	Input	HPS_IOB_8
EMAC1_TXD2	EMAC1 Transmit Data Bit 2.	Output	HPS_IOB_9
EMAC1_TXD3	EMAC1 Transmit Data Bit 3.	Output	HPS_IOB_10
EMAC1_RXD2	EMAC1 Receive Data Bit 2.	Input	HPS_IOB_11
EMAC1_RXD3	EMAC1 Receive Data Bit 3.	Input	HPS_IOB_12
EMAC1_PPS1	EMAC1 1PPS signal.	Output	HPS_IOA_3
EMAC1_PPSTRIG1	EMAC1 1PPS trigger signal.	Input	HPS_IOA_4
EMAC2_TX_CLK	EMAC2 Transmit Clock.	Output	HPS_IOB_13
EMAC2_TX_CTL	EMAC2 Transmit Control.	Output	HPS_IOB_14
EMAC2_RX_CLK	EMAC2 Receive Clock.	Input	HPS_IOB_15
EMAC2_RX_CTL	EMAC2 Receive Control.	Input	HPS_IOB_16
EMAC2_TXD0	EMAC2 Transmit Data Bit 0.	Output	HPS_IOB_17
EMAC2_TXD1	EMAC2 Transmit Data Bit 1.	Output	HPS_IOB_18
EMAC2_RXD0	EMAC2 Receive Data Bit 0.	Input	HPS_IOB_19
EMAC2_RXD1	EMAC2 Receive Data Bit 1.	Input	HPS_IOB_20
EMAC2_TXD2	EMAC2 Transmit Data Bit 2.	Output	HPS_IOB_21
EMAC2_TXD3	EMAC2 Transmit Data Bit 3.	Output	HPS_IOB_22
EMAC2_RXD2	EMAC2 Receive Data Bit 2.	Input	HPS_IOB_23
continued...			

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC2_RXD3	EMAC2 Receive Data Bit 3.	Input	HPS_IOB_24
EMAC2_PPS2	EMAC2 1PPS signal.	Output	HPS_IOA_5 HPS_IOB_5
EMAC2_PPSTRIG2	EMAC2 1PPS trigger signal.	Input	HPS_IOA_6 HPS_IOB_6

### 1.4.9. HPS I2C\_EMAC and MDIO Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

There are three sets of I2C\_EMAC interfaces that can be used as I<sup>2</sup>C interfaces or as the MDIO pins for the EMACs. You must take note that the I2C\_EMAC and MDIO modules must be used with the corresponding EMAC interfaces. For example, you can use either I2C\_EMAC0\_SDA and I2C\_EMAC0\_SCL or MDIO0\_MDIO and MDIO0\_MDC with EMAC0.

The I<sup>2</sup>C protocol requires pull-up resistors to VCCIO\_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7-kΩ.

Typically the MDIO pin requires an external pull-up resistor to VCCIO\_HPS in the range of 1.0-kΩ to 4.7-kΩ.

**Table 26. HPS I2C\_EMAC and MDIO Pins**

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
I2C_EMAC2_SDA	I2C EMAC2 Serial Data.	I/O	HPS_IOA_7	HPS_IOB_9	HPS_IOB_21
I2C_EMAC2_SCL	I2C EMAC2 Serial Clock.	I/O	HPS_IOA_8	HPS_IOB_10	HPS_IOB_22
I2C_EMAC1_SDA	I2C EMAC1 Serial Data.	I/O	HPS_IOA_9	HPS_IOB_19	—
I2C_EMAC1_SCL	I2C EMAC1 Serial Clock.	I/O	HPS_IOA_10	HPS_IOB_20	—
I2C_EMAC0_SDA	I2C EMAC0 Serial Data.	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
I2C_EMAC0_SCL	I2C EMAC0 Serial Clock.	I/O	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24
MDIO0_MDIO	EMAC0 MDIO.	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
MDIO0_MDC	EMAC0 MDC.	Output	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24
MDIO1_MDIO	EMAC1 MDIO.	I/O	HPS_IOA_9	HPS_IOB_19	—
continued...					



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
MDIO1_MDC	EMAC1 MDC.	Output	HPS_IOA_10	HPS_IOB_20	—
MDIO2_MDIO	EMAC2 MDIO.	I/O	HPS_IOA_7	HPS_IOB_9	—
MDIO2_MDC	EMAC2 MDC.	Output	HPS_IOA_8	HPS_IOB_10	—

### 1.4.10. HPS I<sup>2</sup>C Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

In addition to the three I2C\_EMAC controllers, there are two additional I<sup>2</sup>C controllers (I2C0 and I2C1) for dedicated I<sup>2</sup>C usage in the Agilex 5 HPS.

The I<sup>2</sup>C protocol requires pull-up resistors to VCCIO\_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7 kΩ or lower.

**Table 27. HPS I<sup>2</sup>C Pins**

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)			
			Group 1	Group 2	Group 3	Group 4
I2C0_SDA	I2C0 Serial Data.	I/O	HPS_IOA_5	HPS_IOA_23	HPS_IOB_3	—
I2C0_SCL	I2C0 Serial Clock.	I/O	HPS_IOA_6	HPS_IOA_24	HPS_IOB_4	—
I2C1_SDA	I2C1 Serial Data.	I/O	HPS_IOA_3	HPS_IOA_21	HPS_IOB_7	HPS_IOB_13
I2C1_SCL	I2C1 Serial Clock.	I/O	HPS_IOA_4	HPS_IOA_22	HPS_IOB_8	HPS_IOB_14

### 1.4.11. HPS I<sup>3</sup>C Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

There are two I<sup>3</sup>C controllers (I3C0 and I3C1) for dedicated I3C usage in the Agilex 5 HPS.

The I<sup>3</sup>C protocol requires pull-up resistors to `VCCIO_HPS` on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading. Altera recommends using a 1 k $\Omega$  pull-up resistor. Refer to the *I<sup>3</sup>C Controller Design Guidelines and Examples* section in the *Hard Processor System Technical Reference Manual: Agilex 5 SoCs* for more information about the design guidelines.

**Table 28. HPS I<sup>3</sup>C Pins**

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)			
			Group 1	Group 2	Group 3	Group 4
I3C0_SDA	I3C0 Serial Data.	I/O	HPS_IOA_11	HPS_IOA_19	HPS_IOB_7	HPS_IOB_17
I3C0_SCL	I3C0 Serial Clock.	I/O	HPS_IOA_12	HPS_IOA_20	HPS_IOB_8	HPS_IOB_18
I3C0_SDA_PULLUP_EN	I3C0 Enable the pull-up resistor.	Output	—	—	HPS_IOB_1	HPS_IOB_21
I3C1_SDA	I3C1 Serial Data.	I/O	HPS_IOA_9	HPS_IOA_17	HPS_IOB_5	HPS_IOB_15
I3C1_SCL	I3C1 Serial Clock.	I/O	HPS_IOA_10	HPS_IOA_18	HPS_IOB_6	HPS_IOB_16
I3C1_SDA_PULLUP_EN	I3C1 Enable the pull-up resistor.	Output	—	—	HPS_IOB_2	HPS_IOB_22

#### Related Information

[Hard Processor System Technical Reference Manual: Agilex 5 SoCs](#)

### 1.4.12. HPS SPI Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 29. HPS SPI Pins**

There are two SPI Master (SPIM0 and SPIM1) and two SPI Slave (SPIS0 and SPIS1) controllers for the Agilex 5 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIM0_CLK	SPIM0 Clock.	Output	HPS_IOA_5	HPS_IOB_21	HPS_IOB_21
SPIM0_MOSI	SPIM0 Master Out Slave In.	Output	HPS_IOA_6	HPS_IOB_22	HPS_IOB_22
SPIM0_MISO	SPIM0 Master In Slave Out.	Input	HPS_IOA_7	HPS_IOB_19	HPS_IOB_23
SPIM0_SS0_N	SPIM0 Slave Select 0. This is an active-low signal.	Output	HPS_IOA_8	HPS_IOB_20	HPS_IOB_24
SPIM0_SS1_N	SPIM0 Slave Select 1. This is an active-low signal.	Output	HPS_IOA_1	HPS_IOB_18	HPS_IOB_18
SPIM1_CLK	SPIM1 Clock.	Output	HPS_IOA_9	HPS_IOA_21	HPS_IOB_1
SPIM1_MOSI	SPIM1 Master Out Slave In.	Output	HPS_IOA_10	HPS_IOA_22	HPS_IOB_2
SPIM1_MISO	SPIM1 Master In Slave Out.	Input	HPS_IOA_11	HPS_IOA_23	HPS_IOB_3
SPIM1_SS0_N	SPIM1 Slave Select 0. This is an active-low signal.	Output	HPS_IOA_12	HPS_IOA_24	HPS_IOB_4
SPIM1_SS1_N	SPIM1 Slave Select 1. This is an active-low signal.	Output	HPS_IOA_2	HPS_IOA_20	HPS_IOB_5
SPIS0_CLK	SPIS0 Clock.	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_9
SPIS0_MOSI	SPIS0 Master Out Slave In.	Input	HPS_IOA_2	HPS_IOA_22	HPS_IOB_10
SPIS0_MISO	SPIS0 Master In Slave Out.	Output	HPS_IOA_4	HPS_IOA_24	HPS_IOB_12
continued...					

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIS0_SS0_N	SPIS0 Slave Select 0. This is an active-low signal.	Input	HPS_IOA_3	HPS_IOA_23	HPS_IOB_11
SPIS1_CLK	SPIS1 Clock.	Input	HPS_IOA_9	HPS_IOB_5	HPS_IOB_21
SPIS1_MOSI	SPIS1 Master Out Slave In.	Input	HPS_IOA_10	HPS_IOB_6	HPS_IOB_22
SPIS1_MISO	SPIS1 Master In Slave Out.	Output	HPS_IOA_12	HPS_IOB_8	HPS_IOB_24
SPIS1_SS0_N	SPIS1 Slave Select 0. This is an active-low signal.	Input	HPS_IOA_11	HPS_IOB_7	HPS_IOB_23

### 1.4.13. HPS UART Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 30. HPS UART Pins**

There are two UART (UART0 and UART1) controllers for the Agilex 5 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
UART0_CTS_N	UART0 Clear to Send. This is an active-low signal.	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_1
UART0_RTS_N	UART0 Request to Send. This is an active-low signal.	Output	HPS_IOA_2	HPS_IOA_22	HPS_IOB_2
UART0_TX	UART0 Transmit.	Output	HPS_IOA_3	HPS_IOA_23	HPS_IOB_3
UART0_RX	UART0 Receive.	Input	HPS_IOA_4	HPS_IOA_24	HPS_IOB_4
UART1_CTS_N	UART1 Clear to Send. This is an active-low signal.	Input	HPS_IOA_5	HPS_IOB_5	HPS_IOB_17
UART1_RTS_N	UART1 Request to Send. This is an active-low signal.	Output	HPS_IOA_6	HPS_IOB_6	HPS_IOB_18
UART1_TX	UART1 Transmit.	Output	HPS_IOA_7	HPS_IOB_7	HPS_IOB_15
UART1_RX	UART1 Receive.	Input	HPS_IOA_8	HPS_IOB_8	HPS_IOB_16

### 1.4.14. HPS Trace Pins

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

**Table 31. HPS Trace Pins**

You can select up to 16 trace output pins in the Agilex 5 HPS. These pins do not have to be located in the same quadrant.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
Trace_CLK	Trace Clock.	Output	HPS_IOA_20
			HPS_IOB_20
Trace_D0	Trace Data 0.	Output	HPS_IOA_21
			HPS_IOB_21
Trace_D1	Trace Data 1.	Output	HPS_IOA_22
			HPS_IOB_22
Trace_D2	Trace Data 2.	Output	HPS_IOA_23
			HPS_IOB_23
Trace_D3	Trace Data 3.	Output	HPS_IOA_24
			HPS_IOB_24
Trace_D4	Trace Data 4.	Output	HPS_IOA_19
			HPS_IOA_7
			HPS_IOB_19
			HPS_IOB_7
Trace_D5	Trace Data 5.	Output	HPS_IOA_18
			HPS_IOA_6
			HPS_IOB_18
continued...			

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
			HPS_IOB_6
Trace_D6	Trace Data 6.	Output	HPS_IOA_17
			HPS_IOA_5
			HPS_IOB_17
			HPS_IOB_5
Trace_D7	Trace Data 7.	Output	HPS_IOA_16
			HPS_IOA_4
			HPS_IOB_16
			HPS_IOB_4
Trace_D8	Trace Data 8.	Output	HPS_IOA_15
			HPS_IOA_3
			HPS_IOB_15
			HPS_IOB_3
Trace_D9	Trace Data 9.	Output	HPS_IOA_14
			HPS_IOA_2
			HPS_IOB_14
			HPS_IOB_2
Trace_D10	Trace Data 10.	Output	HPS_IOA_13
			HPS_IOA_1
			HPS_IOB_13
			HPS_IOB_1
Trace_D11	Trace Data 11.	Output	HPS_IOA_12
			HPS_IOB_12
Trace_D12	Trace Data 12.	Output	HPS_IOA_11
continued...			



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
			HPS_IOB_11
Trace_D13	Trace Data 13.	Output	HPS_IOA_10
			HPS_IOB_10
Trace_D14	Trace Data 14.	Output	HPS_IOA_9
			HPS_IOB_9
Trace_D15	Trace Data 15.	Output	HPS_IOA_8
			HPS_IOB_8

## 1.5. Power Supply Sharing Guidelines for Agilex 5 Devices

Agilex 5 devices have specific power-up sequence requirements. For more information, refer to the *Power Management User Guide: Agilex 5 FPGAs and SoCs*.

**Note:** Altera recommends you to generate a .pin file from the Quartus Prime Fitter to verify power pin assignment. Altera also recommends using this .pin file to determine if it is safe to power down or ground certain power supplies for your specific design. This step informs you to make the appropriate design choices for unused power supplies for your design.

### Related Information

Power Management User Guide: Agilex 5 FPGAs and SoCs

### 1.5.1. Example 1—Agilex 5 Devices with Speed and Power Grade -1V, -2V, -2E, and -3V

**Table 32. Power Supply Sharing Guidelines for Agilex 5 Devices with Speed and Power Grade -1V, -2V, -2E, and -3V**

Example Requiring 6 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID <sup>(1)</sup> , 0.8	±3%	Switcher <sup>(2)</sup>	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to these power supply pins. Do not leave the VCCL_HPS and VCCPLLDIG1_HPS power supply pins floating or connected to GND.
VCCP						
VCCL_HPS						
VCCL_HPS_CORE0_CORE1						
VCCL_HPS_CORE2						
VCCL_HPS_CORE3						
VCCPLLDIG1_HPS					Filter	

*continued...*

<sup>(1)</sup> For the SmartVID voltage range, refer to the *Agilex 5 FPGAs and SoCs Device Data Sheet*.

<sup>(2)</sup> When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 4 of the *Notes to Agilex 5 Pin Connection Guidelines*.

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCPLLDIG2_HPS						
VCCL_ADC_SDM					Share	
VCC_IO_SDM						
VCCL_SDM	2	0.8	±3%	Switcher <sup>(2)</sup>	Share	Connect the VCCL_SDM to a dedicated 0.8-V power supply. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCC_HSSI						
VCCPLLDIG_SDM					Filter	
VCCERT_GTS	3	1.0	±2.5%	Switcher <sup>(2)</sup> or Linear	Share	Connect to a dedicated 1.0-V power supply. For no transceiver device, move VCCH_SDM together with VCCL_SDM.
VCCH_SDM						
VCCPT	4	1.8	±2.5%	Switcher <sup>(2)</sup>	Share	Connect VCCPT to a dedicated 1.8-V power supply. Connect VCCADC, VCCPLL_SDM, VCCPLL1_HPS, VCCPLL2_HPS, and VCCCEHT_GTS to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Agilex 5 devices.
VCCPT_HVIO						
VCCIO_SDM						
VCCIO_HPS						
VCCFUSEWR_SDM						
VCCPLL1_HPS					Filter	
VCCPLL2_HPS						
VCCADC					Filter	
VCCPLL_SDM						
VCCEHT_GTS					Filter	
VCCRCORE	5	1.2	±5% or ±3% <sup>(3)</sup>	Switcher <sup>(2)</sup>	Share	Connect to a dedicated 1.2-V power supply. If you have LVDS TX signals on the sub-bank of your board, the VCCIO_PIO of this sub-bank is 1.3-V. In this case, you need another VR to support this sub-bank.

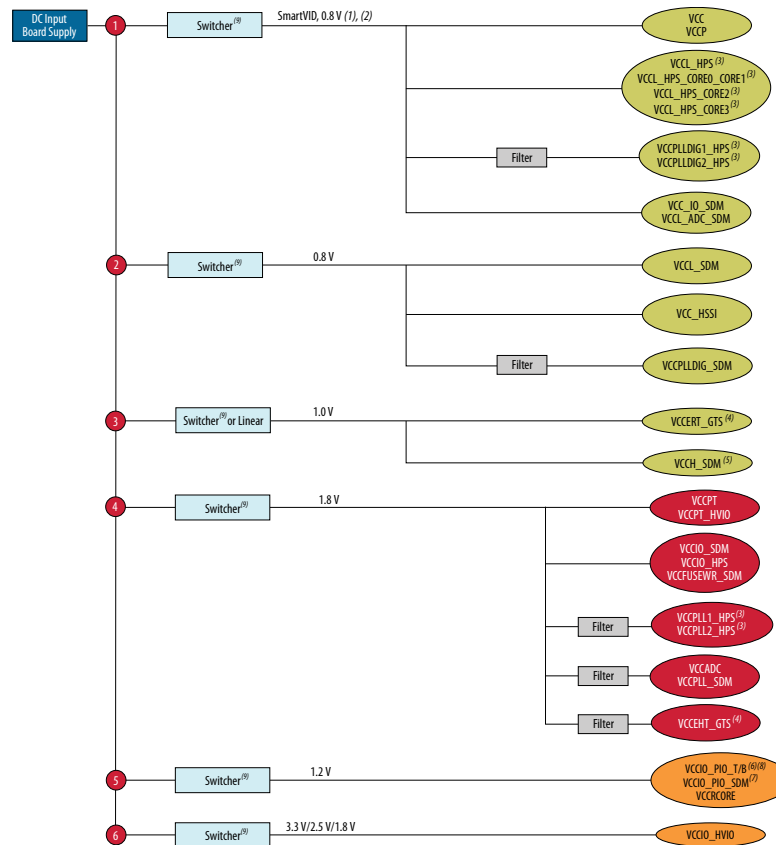
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<sup>(3)</sup> Refer to the *Agilex 5 FPGAs and SoCs Device Data Sheet* for VCCIO\_PIO use cases, to decide the voltage tolerance is ± 3% or ± 5%.

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCIO_PIO_T/B						
VCCIO_PIO_SDM						
VCCIO_HVIO	6	3.3/2.5/1.8	±3%	Switcher <sup>(2)</sup>	Isolate	Connect to a dedicated 3.3-V, 2.5-V, or 1.8-V power supply.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Agilex 5 devices is provided in the following figure.

**Figure 1. Example Power Supply Sharing Guidelines for Agilex 5 Devices with Speed and Power Grade -1V, -2V, -2E, and -3V**



Legend:

● Power Group 1 ● Power Group 2A ● Power Group 2B

Notes:

- (1) When a -V or -E power grade device is used, you must enable the SmartVID connection between the device and VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT\_SCL and PWRMGT\_SDA pin functions.
- (2) When selecting a voltage regulator controller for SmartVID operation, you must choose a controller with the PMBus capability, a feedback node, and a selectable VID format. For example, 4 to 6 bits pattern.
- (3) For the devices without HPS, remove these power rails from the power tree.
- (4) You can power down the GTS power rails if the GTS channels are not used.
- (5) For the devices without GTS transceiver, VCCCH\_SDM is 0.8 V. You can move VCCCH\_SDM together with VCC\_L\_SDM.
- (6) If DDR5 is used in your board, you must have another 1.1-V regulator to support VCCIO\_PIO\_T/B.
- (7) If you use the Avalon streaming x16 mode for FPGA configuration, VCCIO\_PIO\_SDM connect with VCCIO\_PIO\_3AT (1.2 V only for the Avalon streaming x16 mode). If you do not use the Avalon streaming x16 mode, VCCIO\_PIO\_SDM connect with VCCRCORE.
- (8) If you have LVDS Tx signals on the sub-bank on your board, you must have another 1.3-V regulator to support the VCCIO\_PIO\_T/B of this sub-bank.
- (9) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 4 of the Notes to Agilex 5 Pin Connection Guidelines.

## Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)

## 1.5.2. Example 2—Agilex 5 Devices with Speed and Power Grade -4S, -5S, -6S, and -6X

**Table 33. Power Supply Sharing Guidelines for Agilex 5 Devices with Speed and Power Grade 4S, -5S, -6S, and -6X**

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes	
VCC	1	0.8 (-4S) 0.78 (-5S) 0.75 (-6S, -6X)	±3%	Switcher <sup>(4)</sup>	Share	Connect VCC and VCCP to a dedicated 0.8-V, 0.78-V, or 0.75-V power supply. For the power supply voltage level, refer to the <i>Agilex 5 FPGAs and SoCs Device Data Sheet</i> .	
VCCP						Speed and Power Grade	Voltage (V)
VCCL_HPS						-4S	0.8
VCCL_HPS_CORE0_CORE1						-5S	0.78
VCCL_HPS_CORE2						-6S	0.75
VCCL_HPS_CORE3						-6X	0.75
VCCPLLDIG1_HPS					Filter	You have the option to connect VCCL_SDM, VCC_HSSI, VCC_IO_SDM, and VCCL_ADC_SDM to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG1_HPS, VCCPLLDIG2_HPS, and VCCPLLDIG_SDM to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering.  When implementing a filtered supply topology, you must consider the IR drop across the filter.  If you do not intend to utilize the HPS in the Agilex 5 device, you must still provide power to these power supply pins. Do not leave the VCCL_HPS and VCCPLLDIG_HPS power supply pins floating or connected to GND.	
VCCPLLDIG2_HPS							
VCCL_SDM					Share		
VCC_HSSI							
VCC_IO_SDM							
VCCL_ADC_SDM							
VCCPLLDIG_SDM					Filter		
VCCERT_GTS					2	1.0	±2.5%
VCCH_SDM							
continued...							

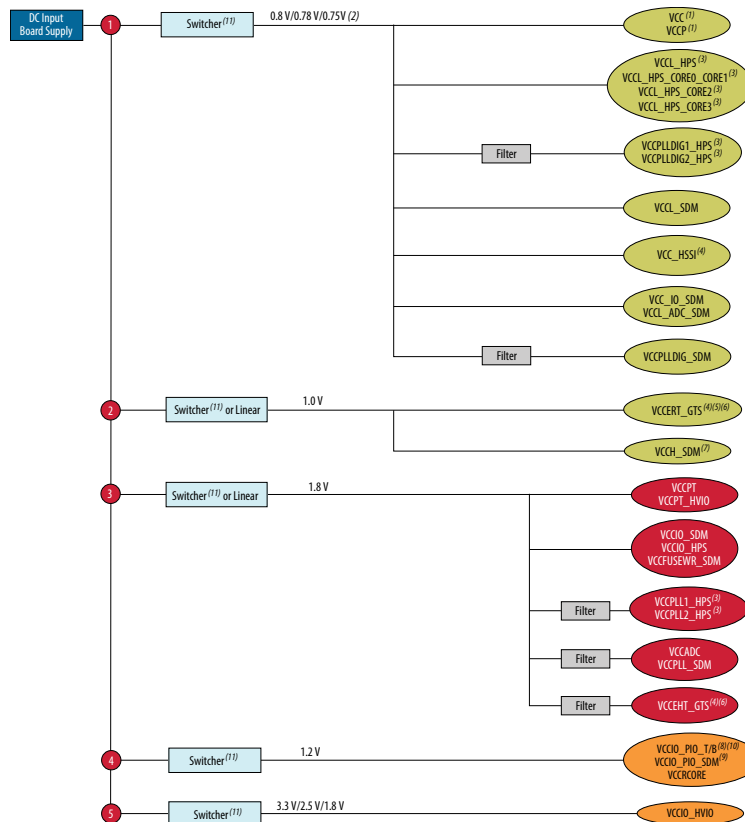
<sup>(4)</sup> When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 4 of the *Notes to Agilex 5 Pin Connection Guidelines*.

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCPT	3	1.8	±2.5%	Switcher <sup>(4)</sup>	Share	<p>Connect VCCPT to a dedicated 1.8-V power supply.</p> <p>Connect VCCADC, VCCPLL_SDM, VCCPLL1_HPS, VCCPLL2_HPS, and VCCEHT_GTS to the same power plane with proper isolation filtering.</p> <p>Depending on the regulator capabilities, you have the option to share this supply with multiple Agilex 5 devices.</p>
VCCPT_HVIO						
VCCIO_SDM						
VCCIO_HPS						
VCCFUSEWR_SDM						
VCCPLL1_HPS					Filter	
VCCPLL2_HPS						
VCCADC					Filter	
VCCPLL_SDM						
VCCEHT_GTS					Filter	
VCCRCORE	4	1.2	±5% or ±3% <sup>(5)</sup>	Switcher <sup>(4)</sup>	Share	<p>Connect to a dedicated 1.2-V power supply. If you have LVDS TX signals on the sub-bank of your board, the VCCIO_PIO of this sub-bank is 1.3 V. In this case, you require another VR to support this sub-bank.</p>
VCCIO_PIO_T/B						
VCCIO_PIO_SDM						
VCCIO_HVIO	5	3.3/2.5/1.8	±3%	Switcher <sup>(4)</sup>	Isolate	<p>Connect to a dedicated 3.3-V, 2.5-V, 1.8-V power supply.</p>

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Agilex 5 devices is provided in the following figure.

<sup>(5)</sup> Refer to the *Agilex 5 FPGAs and SoCs Device Data Sheet* for VCCIO\_PIO use cases, to decide the voltage tolerance is ± 3% or ± 5%.

**Figure 2. Example Power Supply Sharing Guidelines for Agilex 5 Devices with Speed and Power Grade -4S, -5S, -6S, and -6X**



Legend:

● Power Group 1 ● Power Group 2A ● Power Group 2B

Notes:

- (1) When a -S or -X power grade device is used, you must provide VCC/VCCP with a fixed voltage power supply.
- (2) For the range of power supply voltage, refer to the *Agilex 5 FPGAs and SoCs Device Data Sheet*.

Speed and Power Grade	Voltage (V)
-4S	0.8
-5S	0.78
-6S	0.75
-6X	0.75

- (3) For the devices without HPS, remove these power rails from the power tree.
- (4) For the devices without GTS transceiver, remove these power rails from the power tree.
- (5) For the devices without GTS transceiver, remove the regulator from the power tree.
- (6) You can power down the GTS power rails if the GTS channels are not used.
- (7) For the devices without GTS transceiver, VCCH\_SDM can be 0.8 V, 0.78 V, or 0.75 V depending on the speed grade. You have the option to merge VCCH\_SDM with VCC\_L\_SDM.
- (8) If DDR5 is used in your board, you must have an extra 1.1-V regulator to support VCCIO\_PIO\_T/B.
- (9) If you use the Avalon streaming x16 mode for FPGA configuration, VCCIO\_PIO\_SDM connect with VCCIO\_PIO\_3AT (1.2 V only for the Avalon streaming x16 mode). If you do not use the Avalon streaming x16 mode, VCCIO\_PIO\_SDM connect with VCCRCORE.
- (10) If you have LVDS Tx signals on the sub-bank on your board, you must have another 1.3-V regulator to support the VCCIO\_PIO\_T/B of this sub-bank.
- (11) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 4 of the *Notes to Agilex 5 Pin Connection Guidelines*.

## Related Information

[Agilex 5 FPGAs and SoCs Device Data Sheet](#)



## 1.6. Notes to Agilex 5 Pin Connection Guidelines

**Note:** Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. Use the Power and Thermal Calculator to determine the preliminary current requirements for VCC and other power supplies. Use the Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
2. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
3. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express\* (PCIe) protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
4. Low Noise Switching Regulator—defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response. The switching frequency range is not an Altera requirement.
5. There are no dedicated `PR_REQUEST`, `PR_ERROR`, and `PR_DONE` pins. If required, you can use user I/O pins for these functions.
6. The device orientation is die view (bottom of chip view).
7. All I/O pins in a HSIO bank are configured as tri-stated with weak pull-up enabled during device power up (after `VCCIO_PIO` is fully powered up) and device configuration. During device power down, the I/O pin signals are measured between `GND` to `VCCIO_PIO` voltage level when `VCCIO_PIO` is powering down. All valid data transactions should start after the device enters user mode.
8. All I/O pins in a HVIO bank are configured as tri-stated during device power up (after `VCCIO_HVIO` is fully powered up) and device configuration. During device power down, the I/O pin signals are measured between `GND` to `VCCIO_HVIO` voltage level when the `VCCIO_HVIO` are powering down. All valid data transactions should start after the device enters user mode.

9. All dedicated configuration/JTAG, SDM, and SDM optional signal pins are in the undetermined state during device power up and power down. All I/O in the SDM pins are configured as defined in the *General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs* and *LVDS SERDES User Guide: Agilex 5 FPGAs and SoCs* during device configuration.
10. All I/O pins in HPS banks are in the undetermined state during device power up and power down. All I/Os in the HPS pins are configured as the Schmitt trigger input with 20-kΩ weak pull-up enabled after the device is powered up and during HPS or device configuration. All HPS data transaction should start after the device is fully powered up.
11. Input signals of all HSIO, HPS, and SDM I/O pins at any point during power up and power down should not exceed the I/O buffer power supply rail of the bank where the I/O pin resides in. If you use a pin in a GPIO bank with 1.3-V `VCCIO_PIO`, the pin voltage must not exceed the `VCCIO_PIO` rail or 1.2 V, whichever is lower.
12. Input signals of all HVIO pins at any point during power up and power down should not exceed the I/O buffer power supply rail of the bank where I/O resides in.

#### Related Information

- [General-Purpose I/O User Guide: Agilex 5 FPGAs and SoCs](#)
- [LVDS SERDES User Guide: Agilex 5 FPGAs and SoCs](#)

## 1.7. Document Revision History for the Pin Connection Guidelines: Agilex 5 FPGAs and SoCs

Document Version	Changes
2025.11.27	<ul style="list-style-type: none"> <li>Updated the connection guidelines for <code>VCCLSENSE</code> and <code>GNDSENSE</code> in Table: <i>Power Supply Pins</i> for clarity.</li> <li>Removed the guideline enabling <code>INIT_DONE</code> when operating in SmartVID slave mode in Table: <i>SDM Optional Signal Pins</i>.</li> </ul>
2025.08.11	<ul style="list-style-type: none"> <li>Updated <i>Pins Status for Agilex 5 Devices</i>: <ul style="list-style-type: none"> <li>Retitled topic to <i>Pin Connection Guideline Status for Agilex 5 Devices</i>.</li> <li>Added a note about the Agilex 5 pin connection statuses.</li> </ul> </li> <li>Updated and retitled topic <i>Example 1—Agilex 5 Devices with Speed Grade -4S, -5S, -6S, and -6X</i> to <i>Example 1—Agilex 5 Devices with Speed and Power Grade -4S, -5S, -6S, and -6X</i> for clarity.</li> <li>Updated and retitled topic <i>Example 2—Agilex 5 Devices with Speed Grade -4S, -5S, -6S, and -6X</i> to <i>Example 2—Agilex 5 Devices with Speed and Power Grade -4S, -5S, -6S, and -6X</i> for clarity.</li> <li>Updated connection guidelines for <code>VCCL_HPS</code> in Table: <i>HPS Power Supply Pins</i> to state that you must share <code>VCCL_HPS</code> with <code>VCC</code> together.</li> <li>Updated the notes for regulator group 1 in Table: <i>Example 1—Agilex 5 Devices with Speed Grade -4S, -5S, -6S, and -6X</i>.</li> <li>Updated the notes for regulator group 1 in Table: <i>Example 2—Agilex 5 Devices with Speed Grade -4S, -5S, -6S, and -6X</i>.</li> </ul>
continued...	

Document Version	Changes
2025.05.23	<ul style="list-style-type: none"> <li>Updated the connection guidelines for VCCLSENSE and GNDSENSE for Agilex 5 devices of -S and -X speed grades.</li> <li>Updated the connection guidelines for unused HSIO banks and unused pins in an active HSIO bank in the following tables: <ul style="list-style-type: none"> <li>Table: <i>Clock and PLL Pins</i></li> <li>Table: <i>Differential I/O Pins</i></li> <li>Table: <i>External Memory Interface Pins</i></li> </ul> </li> <li>Updated the connection guidelines for VCCEHT_GTS[L1,R4][A,B,C,D] and VCCERT_GTS[L1,R4][A,B,C,D].</li> <li>Removed the notes for I3C0_SDA_PULLUP_EN and I3C1_SDA_PULLUP_EN in Table: <i>HPS I<sup>3</sup>C Pins</i>.</li> </ul>
2024.12.21	<ul style="list-style-type: none"> <li>Updated the connection guidelines for the VREFP_ADC.</li> <li>Made minor editorial edits to the document.</li> </ul>
2024.10.17	<ul style="list-style-type: none"> <li>Updated Table: <i>Differential I/O Pins</i>: <ul style="list-style-type: none"> <li>Updated pin name DIFF_IO_[2][A,B][T,B][1:24][p,n] to DIFF_IO_[2][A,B][T,B][1:24][p,n].</li> <li>Updated pin name DIFF_IO_[3][A,B][T,B][1:24][p,n] to DIFF_IO_[3][A,B][T,B][1:24][p,n].</li> </ul> </li> <li>Updated the VCCIO_PIO connection guidelines for unused HSIO bank and sub-bank in Table: <i>Power Supply Pins</i>.</li> <li>Added new HPS I3C pins in Table: <i>HPS I3C</i>: <ul style="list-style-type: none"> <li>I3C0_SDA_PULLUP_EN</li> <li>I3C1_SDA_PULLUP_EN</li> </ul> </li> <li>Updated the connection guidelines for the AS_nCSO3 pin function of SDM_IO8.</li> <li>Made editorial edits to the connection guidelines of TCK and OSC_CLK_1 in Table: <i>Dedicated Configuration/JTAG Pins</i> for clarity.</li> </ul>
2024.07.08	Updated the pin description and connection guidelines for PIN_PERST_N_CVP_L1[A,B,C,D][0,1] and PIN_PERST_N_R4[A,B,C,D][0,1].
2024.06.12	Updated the connection guidelines for the HPS_COLD_nRESET pin.
2024.04.02	<p>Updated the connection guidelines for the following pins:</p> <ul style="list-style-type: none"> <li>HPS_COLD_nRESET</li> <li>HPS_OSC_CLK</li> <li>JTAG_TCK</li> <li>JTAG_TMS</li> <li>JTAG_TDO</li> <li>JTAG_TDI</li> <li>GPI00_IO[0..23]</li> <li>GPI01_IO[0..23]</li> </ul>
2024.04.01	Initial release.