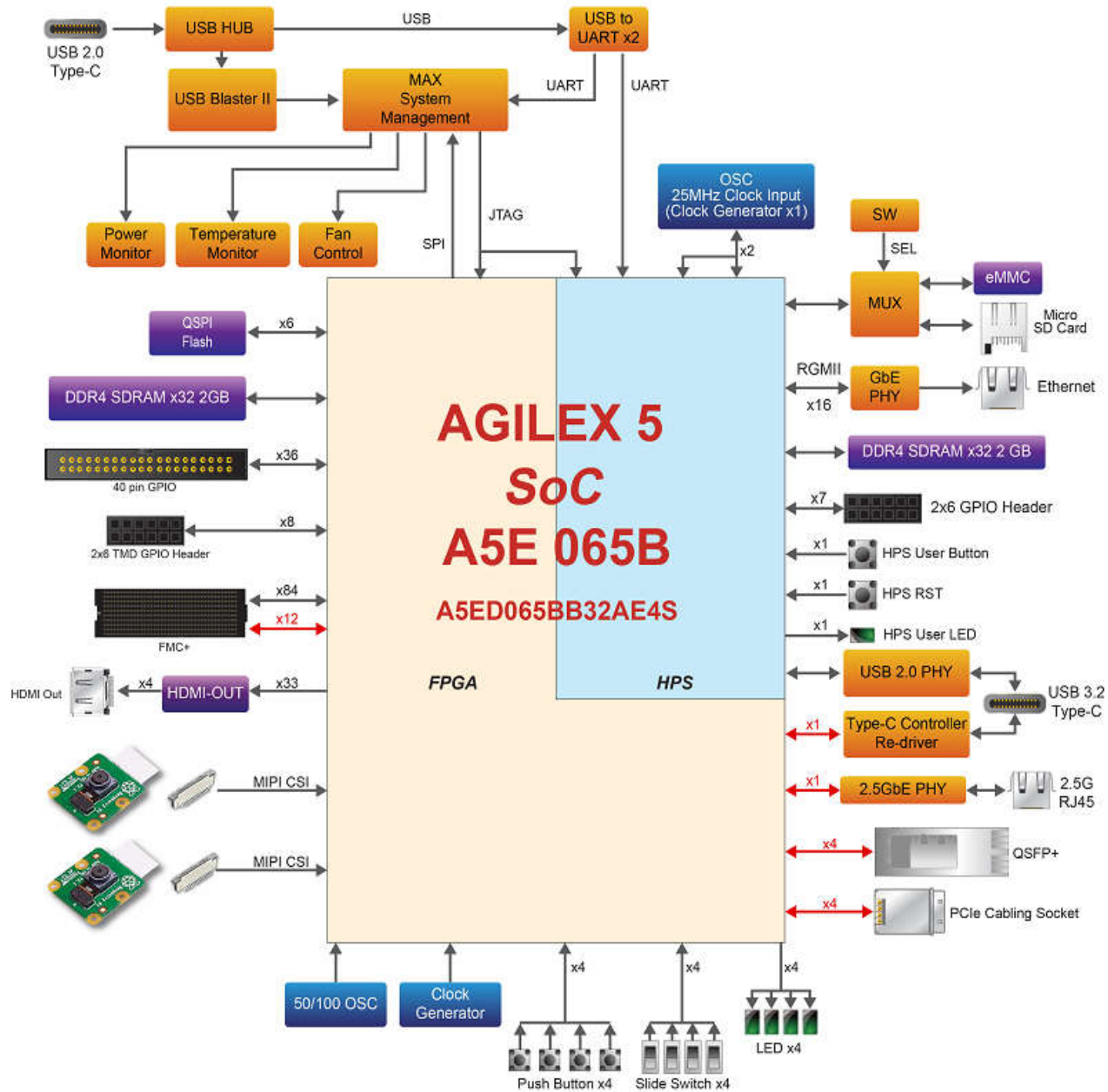
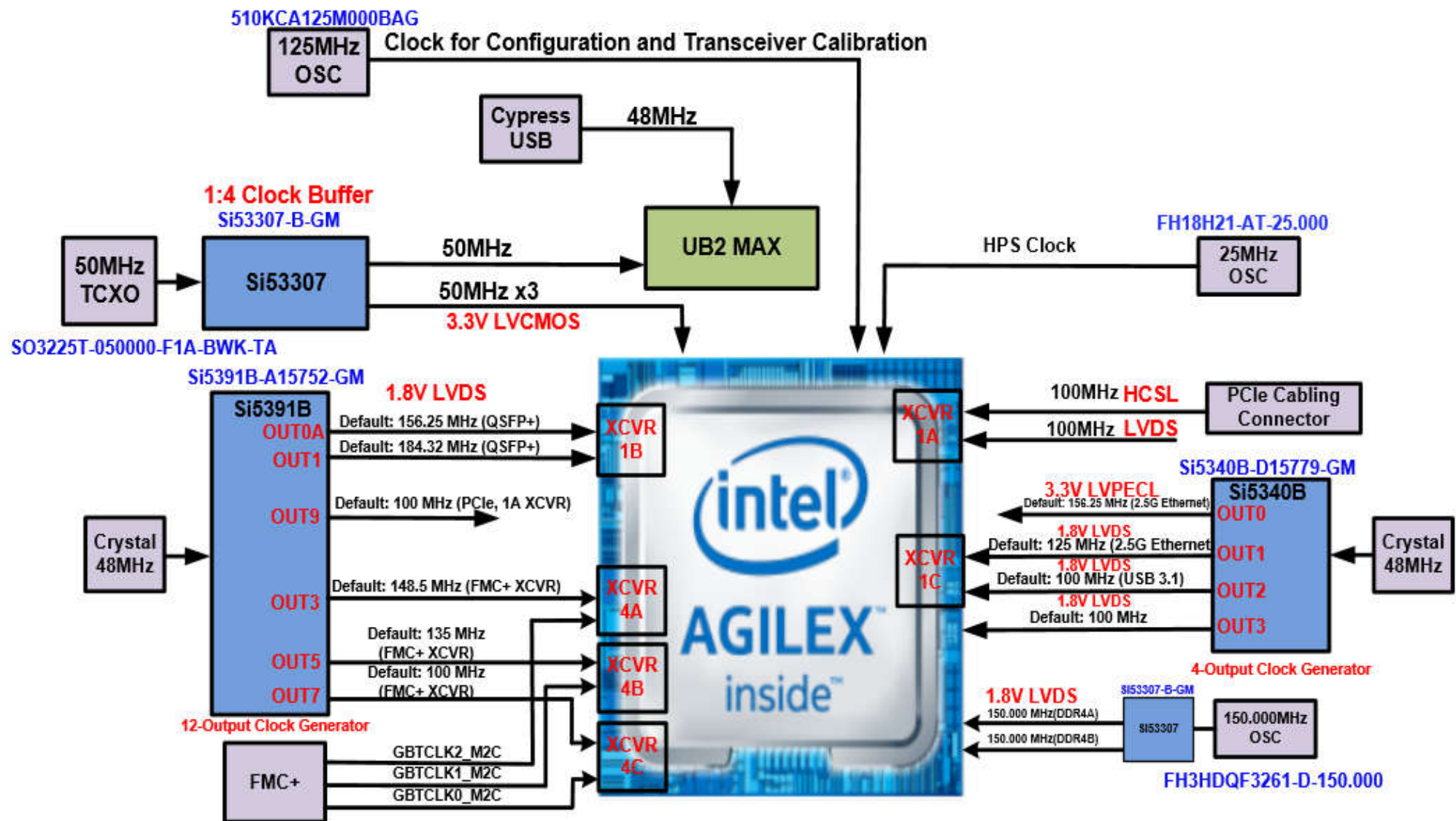


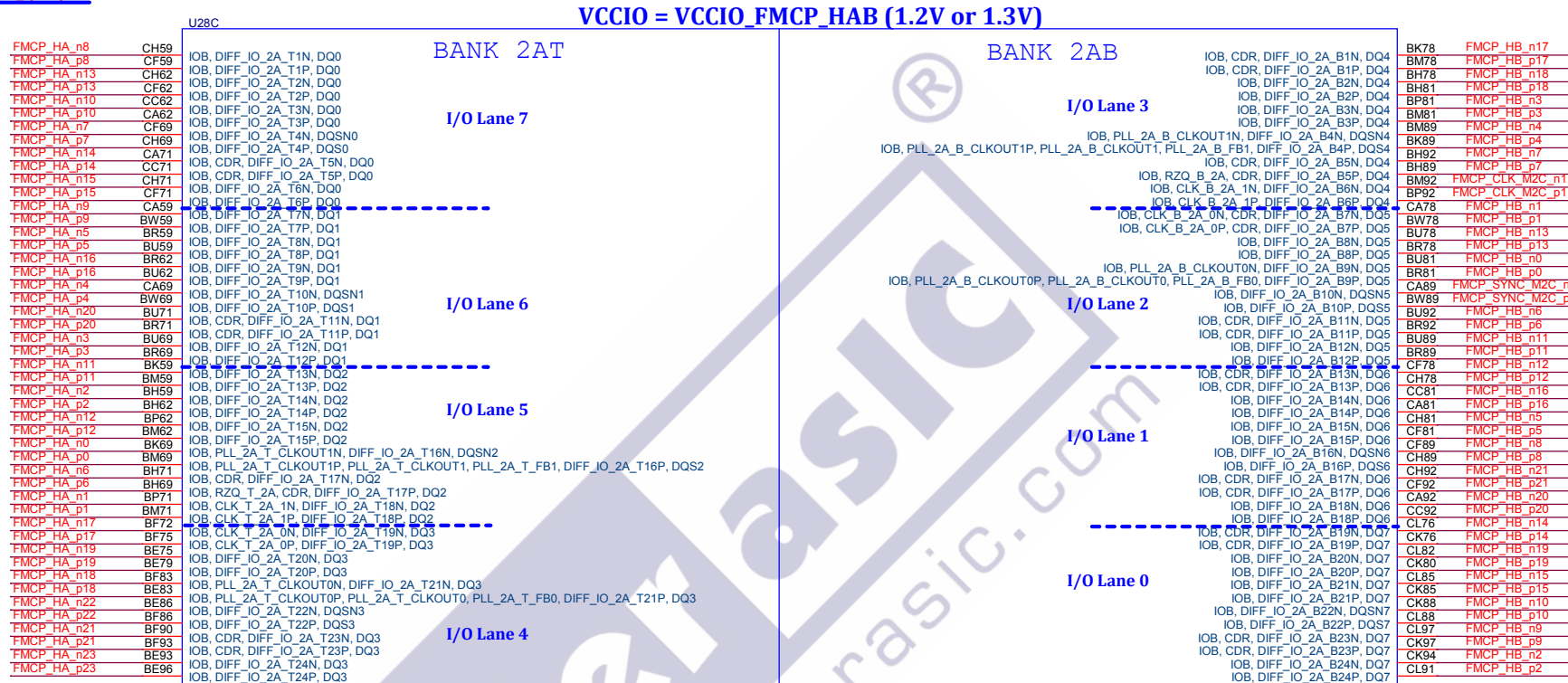
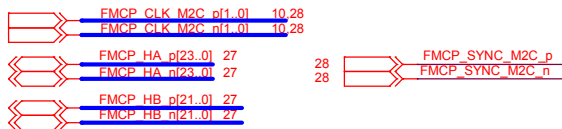
Block Diagram



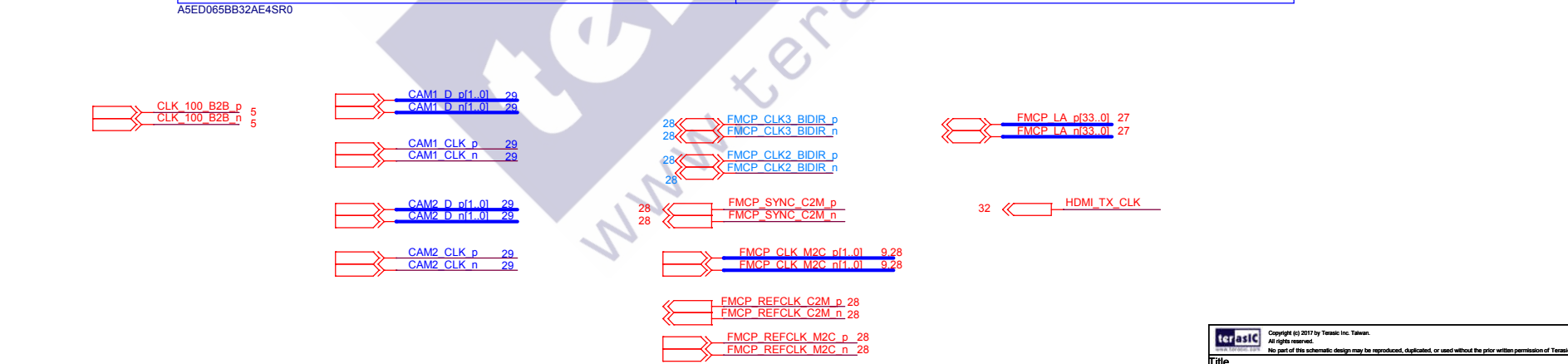
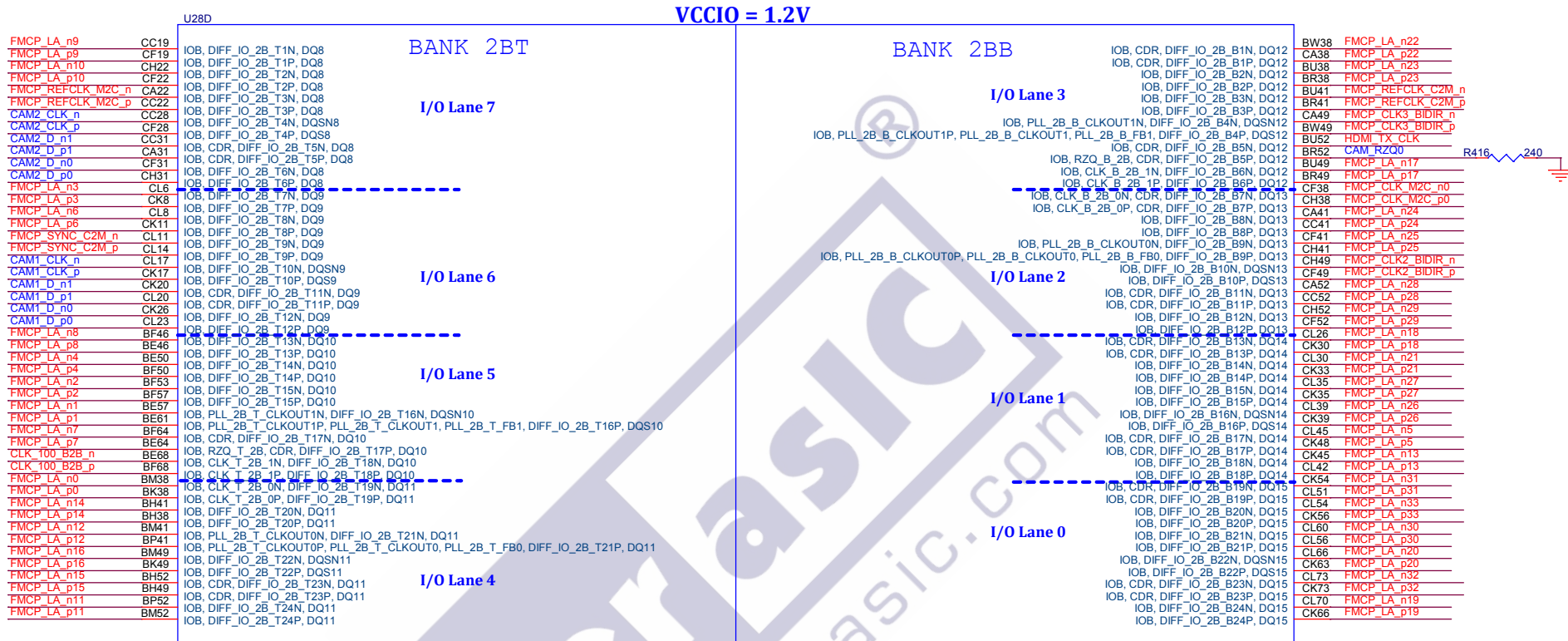
Clock Tree



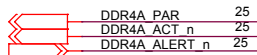
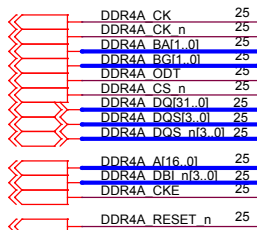
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DDR4-A



RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14

DDR4A_DQ31	D84
DDR4A_DQ29	F84
DDR4A_DQ30	M87
DDR4A_DQ26	K87
DDR4A_DBI_n3	X F87
DDR4A_DQS_n3	D95
DDR4A_DQ33	F95
DDR4A_DQ27	K98
DDR4A_DQ25	M98
DDR4A_DQ28	F98
DDR4A_DQ24	H98
DDR4A_DQ23	P84
DDR4A_DQ22	T84
DDR4A_DQ21	M84
DDR4A_DQ20	K84
DDR4A_DBI_n2	X V87
DDR4A_DQS_n2	M95
DDR4A_DQ32	K95
DDR4A_DQ19	T95
DDR4A_DQ18	P95
DDR4A_DQ17	T98
DDR4A_DQ16	V98
DDR4A_DQ15	Y84
DDR4A_DQ14	Y87
DDR4A_DQ13	Y95
DDR4A_DQ9	Y98
DDR4A_DBI_n1	AC86
DDR4A_DQS_n1	AC90
DDR4A_DQ31	AC93
DDR4A_DQ12	AC96
DDR4A_DQ10	AC100
DDR4A_DQ11	AG104
DDR4A_DQ8	AG100

U28E

BANK 3AT

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

IOB, DIFF_IO_3A_T1N, DQ16
IOB, DIFF_IO_3A_T1P, DQ16
IOB, DIFF_IO_3A_T2N, DQ16
IOB, DIFF_IO_3A_T2P, DQ16
IOB, DIFF_IO_3A_T3N, DQ16
IOB, DIFF_IO_3A_T3P, DQ16, AVST_READY
IOB, DIFF_IO_3A_T4N, DQSN16
IOB, DIFF_IO_3A_T4P, DQS16
IOB, CDR, DIFF_IO_3A_T5N, DQ16
IOB, CDR, DIFF_IO_3A_T5P, DQ16
IOB, DIFF_IO_3A_T6N, DQ16
IOB, DIFF_IO_3A_T6P, DQ16
IOB, DIFF_IO_3A_T7N, DQ17, AVST_DATA10
IOB, DIFF_IO_3A_T7P, DQ17, AVST_DATA9
IOB, DIFF_IO_3A_T8N, DQ17, AVST_DATA8
IOB, DIFF_IO_3A_T8P, DQ17, AVST_VALID
IOB, DIFF_IO_3A_T9N, DQ17, AVST_DATA7
IOB, DIFF_IO_3A_T9P, DQ17, AVST_DATA6
IOB, DIFF_IO_3A_T10N, DQSN17, AVST_DATA5
IOB, DIFF_IO_3A_T10P, DQS17, AVST_DATA4
IOB, CDR, DIFF_IO_3A_T11N, DQ17, AVST_DATA3
IOB, CDR, DIFF_IO_3A_T11P, DQ17, AVST_DATA2
IOB, DIFF_IO_3A_T12N, DQ17, AVST_DATA1
IOB, DIFF_IO_3A_T12P, DQ17, AVST_DATA0
IOB, DIFF_IO_3A_T13N, DQ18
IOB, DIFF_IO_3A_T13P, DQ18
IOB, DIFF_IO_3A_T14N, DQ18
IOB, DIFF_IO_3A_T14P, DQ18
IOB, DIFF_IO_3A_T15N, DQ18
IOB, DIFF_IO_3A_T15P, DQ18
IOB, PLL_3A_T_CLKOUT1N, DIFF_IO_3A_T16N, DQSN18
IOB, PLL_3A_T_CLKOUT1P, PLL_3A_T_CLKOUT1, PLL_3A_T_FB1, DIFF_IO_3A_T16P, DQS18
IOB, CDR, DIFF_IO_3A_T17N, DQ18
IOB, RZQ_T_3A, CDR, DIFF_IO_3A_T17P, DQ18
IOB, CLK_T_3A_1N, DIFF_IO_3A_T18N, DQ18
IOB, CLK_T_3A_1P, DIFF_IO_3A_T18P, DQ18
IOB, CLK_T_3A_0N, DIFF_IO_3A_T19N, DQ19
IOB, CLK_T_3A_0P, DIFF_IO_3A_T19P, DQ19
IOB, DIFF_IO_3A_T20N, DQ19
IOB, DIFF_IO_3A_T20P, DQ19
IOB, PLL_3A_T_CLKOUT0N, DIFF_IO_3A_T21N, DQ19
IOB, PLL_3A_T_CLKOUT0P, PLL_3A_T_CLKOUT0, PLL_3A_T_FB0, DIFF_IO_3A_T21P, DQ19
IOB, DIFF_IO_3A_T22N, DQSN19, AVST_CLK
IOB, DIFF_IO_3A_T22P, DQS19, AVST_DATA15
IOB, CDR, DIFF_IO_3A_T23N, DQ19, AVST_DATA14
IOB, CDR, DIFF_IO_3A_T23P, DQ19, AVST_DATA13
IOB, DIFF_IO_3A_T24N, DQ19, AVST_DATA12
IOB, DIFF_IO_3A_T24P, DQ19, AVST_DATA11

VCCIO = 1.2V

BANK 3AB

I/O Lane 3

I/O Lane 2


I/O Lane 1

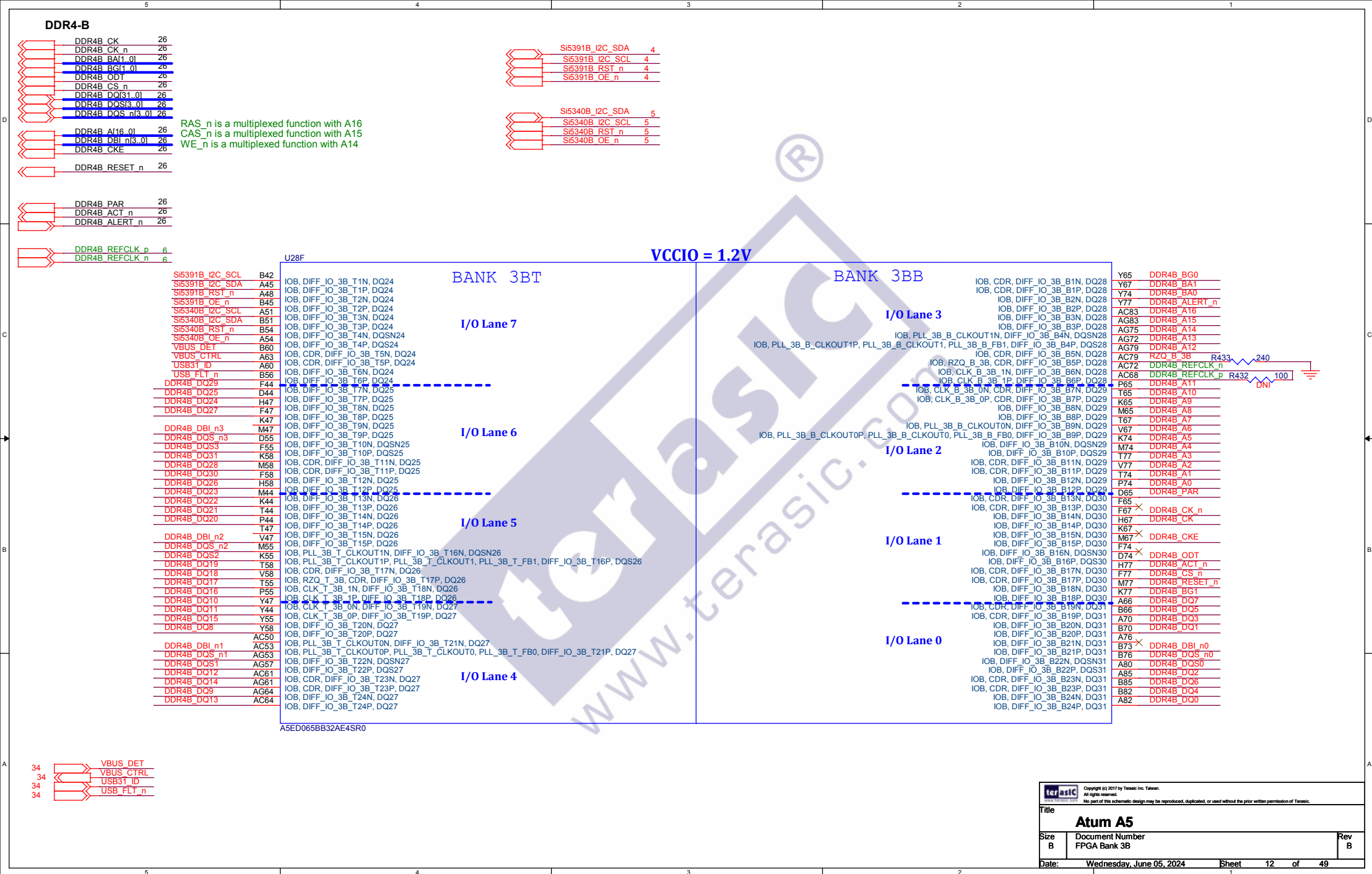
I/O Lane 0

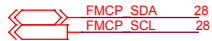
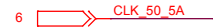
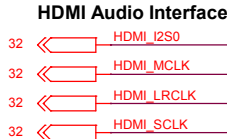
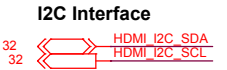
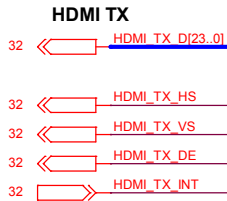
IOB, CDR, DIFF_IO_3A_B1N, DQ20
IOB, CDR, DIFF_IO_3A_B1P, DQ20
IOB, DIFF_IO_3A_B2N, DQ20
IOB, DIFF_IO_3A_B2P, DQ20
IOB, DIFF_IO_3A_B3N, DQ20
IOB, DIFF_IO_3A_B3P, DQ20
IOB, PLL_3A_B_CLKOUT1N, DIFF_IO_3A_B4N, DQSN20
IOB, PLL_3A_B_CLKOUT1P, PLL_3A_B_CLKOUT1, PLL_3A_B_FB1, DIFF_IO_3A_B4P, DQS20
IOB, CDR, DIFF_IO_3A_B5N, DQ20
IOB, RZQ_B_3A, CDR, DIFF_IO_3A_B5P, DQ20
IOB, CLK_B_3A_1N, DIFF_IO_3A_B6N, DQ20
IOB, CLK_B_3A_1P, DIFF_IO_3A_B6P, DQ20
IOB, CLK_B_3A_0N, CDR, DIFF_IO_3A_B7N, DQ21
IOB, CLK_B_3A_0P, CDR, DIFF_IO_3A_B7P, DQ21
IOB, DIFF_IO_3A_B8N, DQ21
IOB, DIFF_IO_3A_B8P, DQ21
IOB, PLL_3A_B_CLKOUT0N, DIFF_IO_3A_B9N, DQ21
IOB, PLL_3A_B_CLKOUT0P, PLL_3A_B_CLKOUT0, PLL_3A_B_FB0, DIFF_IO_3A_B9P, DQ21
IOB, DIFF_IO_3A_B10N, DQSN21
IOB, DIFF_IO_3A_B10P, DQS21
IOB, CDR, DIFF_IO_3A_B11N, DQ21
IOB, CDR, DIFF_IO_3A_B11P, DQ21
IOB, DIFF_IO_3A_B12N, DQ21
IOB, DIFF_IO_3A_B12P, DQ21
IOB, CDR, DIFF_IO_3A_B13N, DQ22
IOB, CDR, DIFF_IO_3A_B13P, DQ22
IOB, DIFF_IO_3A_B14N, DQ22
IOB, DIFF_IO_3A_B14P, DQ22
IOB, DIFF_IO_3A_B15N, DQ22
IOB, DIFF_IO_3A_B15P, DQ22
IOB, DIFF_IO_3A_B16N, DQSN22
IOB, DIFF_IO_3A_B16P, DQS22
IOB, CDR, DIFF_IO_3A_B17N, DQ22
IOB, CDR, DIFF_IO_3A_B17P, DQ22
IOB, DIFF_IO_3A_B18N, DQ22
IOB, DIFF_IO_3A_B18P, DQ22
IOB, CDR, DIFF_IO_3A_B19N, DQ23
IOB, CDR, DIFF_IO_3A_B19P, DQ23
IOB, DIFF_IO_3A_B20N, DQ23
IOB, DIFF_IO_3A_B20P, DQ23
IOB, DIFF_IO_3A_B21N, DQ23
IOB, DIFF_IO_3A_B21P, DQ23
IOB, DIFF_IO_3A_B22N, DQSN23
IOB, DIFF_IO_3A_B22P, DQS23
IOB, CDR, DIFF_IO_3A_B23N, DQ23
IOB, CDR, DIFF_IO_3A_B23P, DQ23
IOB, DIFF_IO_3A_B24N, DQ23
IOB, DIFF_IO_3A_B24P, DQ23

AB105	DDR4A_BG0
Y105	DDR4A_BA1
AB108	DDR4A_BA0
Y108	DDR4A_ALERT_n
AK104	DDR4A_A16
AK107	DDR4A_A15
AB114	DDR4A_A14
Y114	DDR4A_A13
AG111	DDR4A_A12
AK111	RZQ_B_3A_R429
Y117	DDR4A_REFCLK_n
AB117	DDR4A_REFCLK_p
K105	DDR4A_A11
M105	DDR4A_A10
P105	DDR4A_A9
T105	DDR4A_A8
T108	DDR4A_A7
K114	DDR4A_A5
M114	DDR4A_A4
T117	DDR4A_A3
P117	DDR4A_A2
P114	DDR4A_A1
T114	DDR4A_A0
K108	DDR4A_PAR
M108	
F108	DDR4A_CK_n
H108	DDR4A_CK
D105	
F105	DDR4A_CKE
D114	
F114	DDR4A_ODT
M117	DDR4A_ACT_n
K117	DDR4A_CS_n
H117	DDR4A_RESET_n
F117	DDR4A_BG1
A113	DDR4A_DQ7
B113	DDR4A_DQ5
A116	DDR4A_DQ1
B116	DDR4A_DQ3
A122	
B119	DDR4A_DBI_n0
A125	DDR4A_DQS_n0
B122	DDR4A_DQS0
A130	DDR4A_DQ4
B130	DDR4A_DQ2
A128	DDR4A_DQ6
B128	DDR4A_DQ0

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U28G

VCCIO = 3.3V

HDMI_TX_D0	CD134
HDMI_TX_D1	CD135
HDMI_TX_D2	CG134
HDMI_TX_D3	CG135
HDMI_TX_D4	CH132
HDMI_TX_D5	CF132
HDMI_TX_D6	CF128
HDMI_TX_D7	CK134
CLK_50_5A	CH128
HDMI_TX_D8	CL125
HDMI_TX_D9	CF121
HDMI_TX_D10	CF118
HDMI_TX_D11	BU118
HDMI_TX_D12	BR118
HDMI_TX_D13	CA118
HDMI_TX_D14	BW118
HDMI_TX_D15	CL128
HDMI_TX_D16	CL130
HDMI_TX_D17	CK125
HDMI_TX_D18	CK128

HVIO_5A_1, SYSPLLREFCLK_L1A_0, TXCLK1, DATA_CTRL1
HVIO_5A_2, SYSPLLREFCLK_L1A_1, TXCLK2, DATA_CTRL2
HVIO_5A_3, SYSPLLREFCLK_L1B_0, TXCLK3, DATA_CTRL3
HVIO_5A_4, SYSPLLREFCLK_L1B_1, TXCLK4, DATA_CTRL4
HVIO_5A_5, PIN_PERST_N_CVP_L1A_0, TXCLK5, DATA_CTRL5
HVIO_5A_6, PIN_PERST_N_CVP_L1B_0, TXCLK6, DATA_CTRL6
HVIO_5A_7, PIN_PERST_N_CVP_L1C_0, TXCLK7, DATA_CTRL7
HVIO_5A_8, TXCLK8, DATA_CTRL8
HVIO_5A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_5A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_5A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_5A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_5A_13, TXCLK13, DATA_CTRL13
HVIO_5A_14, TXCLK14, DATA_CTRL14
HVIO_5A_15, TXCLK15, DATA_CTRL15
HVIO_5A_16, TXCLK16, DATA_CTRL16
HVIO_5A_17, TXCLK17, DATA_CTRL17
HVIO_5A_18, TXCLK18, DATA_CTRL18
HVIO_5A_19, SYSPLLREFCLK_L1C_0, TXCLK19, DATA_CTRL19
HVIO_5A_20, TXCLK20, DATA_CTRL20

BANK 5A


HVIO_5B_1, SYSPLLREFCLK_L1A_2, TXCLK1, DATA_CTRL1
HVIO_5B_2, SYSPLLREFCLK_L1A_3, TXCLK2, DATA_CTRL2
HVIO_5B_3, SYSPLLREFCLK_L1B_2, TXCLK3, DATA_CTRL3
HVIO_5B_4, SYSPLLREFCLK_L1B_3, TXCLK4, DATA_CTRL4
HVIO_5B_5, PIN_PERST_N_CVP_L1A_1, TXCLK5, DATA_CTRL5
HVIO_5B_6, PIN_PERST_N_CVP_L1B_1, TXCLK6, DATA_CTRL6
HVIO_5B_7, PIN_PERST_N_CVP_L1C_1, TXCLK7, DATA_CTRL7
HVIO_5B_8, TXCLK8, DATA_CTRL8
HVIO_5B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_5B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_5B_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_5B_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_5B_13, TXCLK13, DATA_CTRL13
HVIO_5B_14, TXCLK14, DATA_CTRL14
HVIO_5B_15, TXCLK15, DATA_CTRL15
HVIO_5B_16, TXCLK16, DATA_CTRL16
HVIO_5B_17, TXCLK17, DATA_CTRL17
HVIO_5B_18, TXCLK18, DATA_CTRL18
HVIO_5B_19, SYSPLLREFCLK_L1C_1, TXCLK19, DATA_CTRL19
HVIO_5B_20, TXCLK20, DATA_CTRL20

BANK 5B

BF111, HDMI_TX_D19
BH109, HDMI_TX_D20
BE115, HDMI_TX_D21
BF115, HDMI_TX_D22
BF107, PCIE_PERST_n
BU109, HDMI_TX_D23
BF104, CPU_RESET_n
BR109, HDMI_TX_HS
BE107, HDMI_TX_VS
BK109, HDMI_TX_DE
BE111, HDMI_TX_INT
BM109, HDMI_I2C_SDA
BR112, HDMI_I2C_SCL
BK118, HDMI_I2S0
BM118, HDMI_MCLK
BP112, HDMI_LRCLK
BM112, HDMI_SCLK
BK112, FMCP_SDA
BH118, FMCP_SCL
BF120, LED0

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GPIO

GPIO[35..0] 30

6 CLK_50_6A

SW[3..0] 15 42

FMCP RES0 28

U28H

VCCIO = 3.3V

GPIO3 BU28
GPIO25 BP31
GPIO17 BR28
GPIO4 BR31
GPIO1 BU31
GPIO18 BM28
GPIO8 BW28
GPIO19 BM31
GPIO0 BK31
CLK_50_6A BP22
GPIO20 BK28
GPIO11 BR22
GPIO28 CH12
GPIO10 BU22
GPIO9 BW19
GPIO21 SH28
GPIO13 BM22
GPIO29 CF12
GPIO14 BK19
GPIO27 CF9

HVIO_6A_1, SYSPLLREFCLK_R4A_0, TXCLK1, DATA_CTRL1
HVIO_6A_2, SYSPLLREFCLK_R4A_1, TXCLK2, DATA_CTRL2
HVIO_6A_3, SYSPLLREFCLK_R4B_0, TXCLK3, DATA_CTRL3
HVIO_6A_4, SYSPLLREFCLK_R4B_1, TXCLK4, DATA_CTRL4
HVIO_6A_5, PIN_PERST_N_R4A_0, TXCLK5, DATA_CTRL5
HVIO_6A_6, PIN_PERST_N_R4B_0, TXCLK6, DATA_CTRL6
HVIO_6A_7, PIN_PERST_N_R4C_0, TXCLK7, DATA_CTRL7
HVIO_6A_8, TXCLK8, DATA_CTRL8
HVIO_6A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6A_13, TXCLK13, DATA_CTRL13
HVIO_6A_14, TXCLK14, DATA_CTRL14
HVIO_6A_15, TXCLK15, DATA_CTRL15
HVIO_6A_16, TXCLK16, DATA_CTRL16
HVIO_6A_17, TXCLK17, DATA_CTRL17
HVIO_6A_18, TXCLK18, DATA_CTRL18
HVIO_6A_19, SYSPLLREFCLK_R4C_0, TXCLK19, DATA_CTRL19
HVIO_6A_20, TXCLK20, DATA_CTRL20


BANK 6A

BANK 6B

HVIO_6B_1, SYSPLLREFCLK_R4A_2, TXCLK1, DATA_CTRL1
HVIO_6B_2, SYSPLLREFCLK_R4A_3, TXCLK2, DATA_CTRL2
HVIO_6B_3, SYSPLLREFCLK_R4B_2, TXCLK3, DATA_CTRL3
HVIO_6B_4, SYSPLLREFCLK_R4B_3, TXCLK4, DATA_CTRL4
HVIO_6B_5, PIN_PERST_N_R4A_1, TXCLK5, DATA_CTRL5
HVIO_6B_6, PIN_PERST_N_R4B_1, TXCLK6, DATA_CTRL6
HVIO_6B_7, PIN_PERST_N_R4C_1, TXCLK7, DATA_CTRL7
HVIO_6B_8, TXCLK8, DATA_CTRL8
HVIO_6B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6B_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6B_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6B_13, TXCLK13, DATA_CTRL13
HVIO_6B_14, TXCLK14, DATA_CTRL14
HVIO_6B_15, TXCLK15, DATA_CTRL15
HVIO_6B_16, TXCLK16, DATA_CTRL16
HVIO_6B_17, TXCLK17, DATA_CTRL17
HVIO_6B_18, TXCLK18, DATA_CTRL18
HVIO_6B_19, SYSPLLREFCLK_R4C_1, TXCLK19, DATA_CTRL19
HVIO_6B_20, TXCLK20, DATA_CTRL20

BF21 GPIO30
BE21 GPIO32
BE43 GPIO24
BF40 GPIO23
BE29 GPIO35
BE25 GPIO33
BF32 FMCP RES0
BF36 GPIO22
BF29 GPIO34
BF25 GPIO2
BF16 GPIO31
BH19 GPIO16
BK22 GPIO15
BM19 GPIO12
BU19 GPIO5
BR19 GPIO6
CK2 GPIO28
CJ2 GPIO7
CK4 SW0
CH4 SW1

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TMD Header

6 CLK_50_6C TMD_DI7_01 29

CAM1_GPIO 29
CAM1_I2C_SDA 29
CAM1_I2C_SCL 29

CAM2_GPIO 29
CAM2_I2C_SDA 29
CAM2_I2C_SCL 29

LEDI3_01 13 42

SWI3_01 14 42

BUTTONI3_0K2

TMD_D2 F27
TMD_D3 F24
TMD_D4 H27
TMD_D5 D24
TMD_D6 H18
TMD_D7 D16
TMD_D0 F18
TMD_D1 F15
CLK_50_6C D8
SW2 K8
SW3 F8
BUTTON0 H8
BUTTON1 C2
BUTTON2 D4
BUTTON3 F4
CAM1_GPIO K4
CAM1_I2C_SDA G2
CAM1_I2C_SCL J2
CAM2_GPIO J1
CAM2_I2C_SDA G1

U28I

HVIO_6C_1, TXCLK1, DATA_CTRL1
HVIO_6C_2, TXCLK2, DATA_CTRL2
HVIO_6C_3, TXCLK3, DATA_CTRL3
HVIO_6C_4, TXCLK4, DATA_CTRL4
HVIO_6C_5, TXCLK5, DATA_CTRL5
HVIO_6C_6, TXCLK6, DATA_CTRL6
HVIO_6C_7, TXCLK7, DATA_CTRL7
HVIO_6C_8, TXCLK8, DATA_CTRL8
HVIO_6C_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6C_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6C_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6C_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6C_13, TXCLK13, DATA_CTRL13
HVIO_6C_14, TXCLK14, DATA_CTRL14
HVIO_6C_15, TXCLK15, DATA_CTRL15
HVIO_6C_16, TXCLK16, DATA_CTRL16
HVIO_6C_17, TXCLK17, DATA_CTRL17
HVIO_6C_18, TXCLK18, DATA_CTRL18
HVIO_6C_19, TXCLK19, DATA_CTRL19
HVIO_6C_20, TXCLK20, DATA_CTRL20

BANK 6C

VCCIO = 3.3V

BANK 6D

HVIO_6D_1, TXCLK1, DATA_CTRL1
HVIO_6D_2, TXCLK2, DATA_CTRL2
HVIO_6D_3, TXCLK3, DATA_CTRL3
HVIO_6D_4, TXCLK4, DATA_CTRL4
HVIO_6D_5, TXCLK5, DATA_CTRL5
HVIO_6D_6, TXCLK6, DATA_CTRL6
HVIO_6D_7, TXCLK7, DATA_CTRL7
HVIO_6D_8, TXCLK8, DATA_CTRL8
HVIO_6D_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
HVIO_6D_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
HVIO_6D_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
HVIO_6D_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
HVIO_6D_13, TXCLK13, DATA_CTRL13
HVIO_6D_14, TXCLK14, DATA_CTRL14
HVIO_6D_15, TXCLK15, DATA_CTRL15
HVIO_6D_16, TXCLK16, DATA_CTRL16
HVIO_6D_17, TXCLK17, DATA_CTRL17
HVIO_6D_18, TXCLK18, DATA_CTRL18
HVIO_6D_19, TXCLK19, DATA_CTRL19
HVIO_6D_20, TXCLK20, DATA_CTRL20

FPGA/System MAX SPI

33 ENET_88E2110 RESET_n
33 ENET_88E2110 MDC
33 ENET_88E2110 MDIO
33 ENET_88E2110 INT_n

INFO_SPI_SCLK_7
INFO_SPI_CS_n_7
INFO_SPI_MOSI_7
INFO_SPI_MISO_7

40 PCIE_WAKE_n

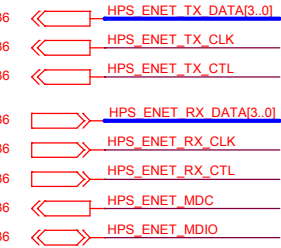
A8 CAM2_I2C_SCL
B4 LED2
A11 LED3
B11 ENET_88E2110 RESET_n
B14 ENET_88E2110 MDC
A14 ENET_88E2110 MDIO
A20 ENET_88E2110 INT_n
A17 INFO_SPI_SCLK
A23 INFO_SPI_CS_n
B20 INFO_SPI_MOSI
B23 INFO_SPI_MISO
B26 QSPF_MOD_SEL_n
B30 QSPF_RST_n
A30 QSPF_SCL
A35 QSPF_SDA
A33 QSPF_LP_MODE
A39 QSPF_INTERRUPT_n
B35 QSPF_MOD_PRS_n
D34 PCIE_WAKE_n
B39 LED1

QSFP+ Control Interface

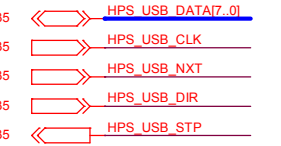
QSFP_MOD_SEL_n 39
QSFP_RST_n 39
QSFP_SCL 39
QSFP_SDA 39
QSFP_LP_MODE 39
QSFP_INTERRUPT_n 39
QSFP_MOD_PRS_n 39

Title		Atum A5	
Size	Document Number	Rev	
B	FPGA Bank 6C - 6D	B	
Date:	Wednesday, June 05, 2024	Sheet	15 of 49

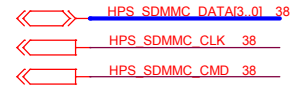
Ethernet PHY Interface (RGMII)



UBS PHY Interface (ULPI)



SD/eMMC Interface



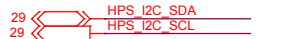
HPS 25MHz Clock



HPS GPIO



HPS I2C Interface



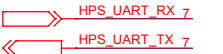
HPS User Button



HPS User LED



UART Interface



HPS_LED	W135
HPS_GPIO4	U135
HPS_UART_TX	W134
HPS_UART_RX	AK115
HPS_I2C_SDA	U134
HPS_I2C_SCL	AL120
HPS_ENET_MDIO	R134
HPS_ENET_MDC	AG115
HPS_GPIO3	N135
HPS_GPIO2	AK120
HPS_GPIO1	N134
HPS_GPIO0	T132
HPS_USB_CLK	P132
HPS_USB_STP	L135
HPS_USB_DIR	J135
HPS_USB_DATA0	AD135
HPS_USB_DATA1	M132
HPS_USB_DATA2	AD134
HPS_USB_DATA3	K132
HPS_USB_DATA4	AG129
HPS_USB_DATA5	J134
HPS_USB_DATA6	AG120
HPS_USB_DATA7	G134
HPS_USB_DATA7	G135

HPS_SDMMC_DATA0	E135
HPS_SDMMC_DATA1	F132
HPS_SDMMC_CLK	D132
HPS_OSC_CLK	AG123
HPS_KEY	B134
HPS_SDMMC_DATA2	AA135
HPS_SDMMC_DATA3	V127
HPS_SDMMC_CMD	AB132
HPS_JTAG_TCK	T127
HPS_JTAG_TMS	T132
HPS_JTAG_TDO	T124
HPS_JTAG_TDI	P124
HPS_ENET_TX_CLK	M127
HPS_ENET_TX_CTL	K127
HPS_ENET_RX_CLK	M124
HPS_ENET_RX_CTL	AB127
HPS_ENET_TX_DATA0	K124
HPS_ENET_TX_DATA1	Y127
HPS_ENET_RX_DATA0	H127
HPS_ENET_RX_DATA1	AB124
HPS_ENET_TX_DATA2	F127
HPS_ENET_TX_DATA3	Y124
HPS_ENET_RX_DATA2	F124
HPS_ENET_RX_DATA3	D124

U28B

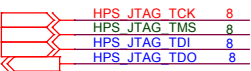
HPS_IOA_1, GPIO0_IO0, SPIM0_SS1_N, SPIS0_CLK, UART0_CTS_N, NAND_ADQ0, SDMMC_DATA0, USB0_CLK, EMAC0_PPS0, TRACE_D10
HPS_IOA_2, GPIO0_IO1, SPIM1_SS1_N, SPIS0_MOSI, UART0_RTS_N, NAND_ADQ1, SDMMC_DATA1, USB0_STP, EMAC0_PPSTRIG0, TRACE_D9
HPS_IOA_3, GPIO0_IO2, SPIS0_SS0_N, UART0_TX, I2C1_SDA, NAND_WE_N, SDMMC_CLK, USB0_DIR, EMAC1_PPS1, TRACE_D8
HPS_IOA_4, GPIO0_IO3, SPIS0_MISO, UART0_RX, I2C1_SCL, NAND_RE_N, USB0_DATA0, EMAC1_PPSTRIG1, TRACE_D7
HPS_IOA_5, GPIO0_IO4, SPIM0_CLK, UART1_CTS_N, I2C0_SDA, NAND_WP_N, SDMMC_WRITE_PROTECT, USB0_DATA1, EMAC2_PPS2, TRACE_D6
HPS_IOA_6, GPIO0_IO5, SPIM0_MOSI, UART1_RTS_N, I2C0_SCL, NAND_ADQ2, SDMMC_DATA2, USB0_NXT, EMAC2_PPSTRIG2, TRACE_D5
HPS_IOA_7, GPIO0_IO6, SPIM0_MISO, MDIO2_MDIO, UART1_TX, I2C_EMAC2_SDA, NAND_ADQ3, SDMMC_DATA3, USB0_DATA2, TRACE_D4
HPS_IOA_8, GPIO0_IO7, SPIM0_SS0_N, MDIO2_MDC, UART1_RX, I2C_EMAC2_SCL, NAND_CLE, SDMMC_CMD, USB0_DATA3, TRACE_D15
HPS_IOA_9, GPIO0_IO8, SPIM1_CLK, SPIS1_CLK, MDIO1_MDIO, I2C_EMAC1_SDA, NAND_ADQ4, SDMMC_DATA4, USB0_DATA4, I3C1_SDA, TRACE_D14
HPS_IOA_10, GPIO0_IO9, SPIM1_MOSI, SPIS1_MOSI, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ5, SDMMC_DATA5, USB0_DATA5, I3C1_SCL, TRACE_D13
HPS_IOA_11, GPIO0_IO10, SPIM1_MISO, SPIS1_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, USB0_DATA6, I3C0_SDA, TRACE_D12
HPS_IOA_12, GPIO0_IO11, SPIM1_SS0_N, SPIS1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, USB0_DATA7, I3C0_SCL, TRACE_D11
HPS_IOA_13, GPIO0_IO12, NAND_ALE, SDMMC_PU_PD_DATA2, USB1_CLK, EMAC0_TX_CLK, TRACE_D10
HPS_IOA_14, GPIO0_IO13, NAND_RB_N, SDMMC_BUS_PWR, USB1_STP, EMAC0_TX_CTL, TRACE_D9
HPS_IOA_15, GPIO0_IO14, NAND_CE_N, USB1_DIR, EMAC0_RX_CLK, TRACE_D8
HPS_IOA_16, GPIO0_IO15, NAND_DQS, SDMMC_DATA_STROBE, USB1_DATA0, EMAC0_RX_CTL, TRACE_D7
HPS_IOA_17, GPIO0_IO16, I3C1_SDA, NAND_ADQ8, USB1_DATA1, EMAC0_TXD0, TRACE_D6
HPS_IOA_18, GPIO0_IO17, I3C1_SCL, NAND_ADQ9, USB1_NXT, EMAC0_TXD1, TRACE_D5
HPS_IOA_19, GPIO0_IO18, I3C0_SDA, NAND_ADQ10, USB1_DATA2, EMAC0_RXD0, TRACE_D4
HPS_IOA_20, GPIO0_IO19, SPIM1_SS1_N, I3C0_SCL, NAND_ADQ11, USB1_DATA3, EMAC0_RXD1, TRACE_CLK
HPS_IOA_21, GPIO0_IO20, SPIM1_CLK, SPIS0_CLK, UART0_CTS_N, I2C1_SDA, NAND_ADQ12, USB1_DATA4, EMAC0_TXD2, TRACE_D0
HPS_IOA_22, GPIO0_IO21, SPIM1_MOSI, SPIS0_MOSI, UART0_RTS_N, I2C1_SCL, NAND_ADQ13, USB1_DATA5, EMAC0_TXD3, TRACE_D1
HPS_IOA_23, GPIO0_IO22, SPIM1_MISO, SPIS0_SS0_N, UART0_TX, I2C0_SDA, NAND_ADQ14, USB1_DATA6, EMAC0_RXD2, TRACE_D2
HPS_IOA_24, GPIO0_IO23, SPIM1_SS0_N, SPIS0_MISO, UART0_RX, I2C0_SCL, NAND_ADQ15, USB1_DATA7, EMAC0_RXD3, TRACE_D3

HPS_IOB_1, GPIO1_IO0, SPIM1_CLK, CM_PLL_CLK0, UART0_CTS_N, EMAC0_PPS0, NAND_ADQ0, SDMMC_DATA0, EMAC1_TX_CLK, TRACE_D10
HPS_IOB_2, GPIO1_IO1, SPIM1_MOSI, CM_PLL_CLK1, UART0_RTS_N, EMAC0_PPSTRIG0, NAND_ADQ1, SDMMC_DATA1, EMAC1_TX_CTL, TRACE_D9
HPS_IOB_3, GPIO1_IO2, SPIM1_MISO, CM_PLL_CLK2, UART0_TX, I2C0_SDA, NAND_WE_N, SDMMC_CLK, EMAC1_RX_CLK, TRACE_D8
HPS_IOB_4, GPIO1_IO3, SPIM1_SS0_N, CM_PLL_CLK3, UART0_RX, I2C0_SCL, NAND_RE_N, EMAC1_RX_CTL, TRACE_D7
HPS_IOB_5, GPIO1_IO4, SPIM1_SS1_N, SPIS1_CLK, UART1_CTS_N, EMAC2_PPS2, NAND_WP_N, SDMMC_WRITE_PROTECT, I3C1_SDA, EMAC1_TXD0, TRACE_D6
HPS_IOB_6, GPIO1_IO5, SPIS1_MOSI, UART1_RTS_N, EMAC2_PPSTRIG2, NAND_ADQ2, SDMMC_DATA2, I3C1_SCL, EMAC1_TXD1, TRACE_D5
HPS_IOB_7, GPIO1_IO6, SPIS1_SS0_N, UART1_TX, I2C1_SDA, NAND_ADQ3, SDMMC_DATA3, I3C0_SDA, EMAC1_RXD0, TRACE_D4
HPS_IOB_8, GPIO1_IO7, SPIS1_MISO, UART1_RX, I2C1_SCL, NAND_CLE, SDMMC_CMD, I3C0_SCL, EMAC1_RXD1, TRACE_D15
HPS_IOB_9, GPIO1_IO8, JTAG_TCK, SPIS0_CLK, MDIO2_MDIO, I2C_EMAC2_SDA, NAND_ADQ4, SDMMC_DATA4, EMAC1_TXD2, TRACE_D14
HPS_IOB_10, GPIO1_IO9, JTAG_TMS, SPIS0_MOSI, MDIO2_MDC, I2C_EMAC2_SCL, NAND_ADQ5, SDMMC_DATA5, EMAC1_TXD3, TRACE_D13
HPS_IOB_11, GPIO1_IO10, JTAG_TDO, SPIS0_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, EMAC1_RXD2, TRACE_D12
HPS_IOB_12, GPIO1_IO11, JTAG_TDI, SPIS0_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, EMAC1_RXD3, TRACE_D11
HPS_IOB_13, GPIO1_IO12, I2C1_SDA, NAND_ALE, SDMMC_PU_PD_DATA2, EMAC2_TX_CLK, TRACE_D10
HPS_IOB_14, GPIO1_IO13, I2C1_SCL, NAND_RB_N, SDMMC_BUS_PWR, EMAC2_TX_CTL, TRACE_D9
HPS_IOB_15, GPIO1_IO14, UART1_TX, NAND_CE_N, I3C1_SDA, EMAC2_RX_CLK, TRACE_D8
HPS_IOB_16, GPIO1_IO15, UART1_RX, NAND_DQS, SDMMC_DATA_STROBE, I3C1_SCL, EMAC2_RX_CTL, TRACE_D7
HPS_IOB_17, GPIO1_IO16, UART1_CTS_N, NAND_ADQ8, I3C0_SDA, EMAC2_TXD0, TRACE_D6
HPS_IOB_18, GPIO1_IO17, SPIM0_SS1_N, UART1_RTS_N, NAND_ADQ9, I3C0_SCL, EMAC2_TXD1, TRACE_D5
HPS_IOB_19, GPIO1_IO18, SPIM0_MISO, MDIO1_MDIO, I2C_EMAC1_SDA, NAND_ADQ10, EMAC2_RXD0, TRACE_D4
HPS_IOB_20, GPIO1_IO19, SPIM0_SS0_N, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ11, EMAC2_RXD1, TRACE_CLK
HPS_IOB_21, GPIO1_IO20, SPIM0_CLK, SPIS1_CLK, I2C_EMAC2_SDA, NAND_ADQ12, EMAC2_TXD2, TRACE_D0
HPS_IOB_22, GPIO1_IO21, SPIM0_MOSI, SPIS1_MOSI, I2C_EMAC2_SCL, NAND_ADQ13, EMAC2_TXD3, TRACE_D1
HPS_IOB_23, GPIO1_IO22, SPIM0_MISO, SPIS1_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ14, EMAC2_RXD2, TRACE_D2
HPS_IOB_24, GPIO1_IO23, SPIM0_SS0_N, SPIS1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ15, EMAC2_RXD3, TRACE_D3

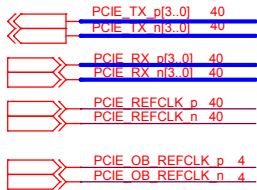
HPS

A5ED065BB32AE4SR0

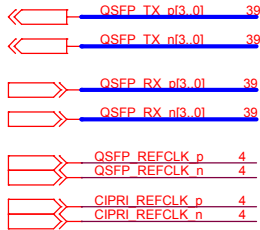
HPS JTAG Interface



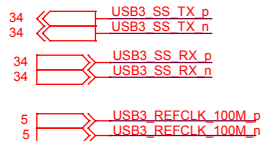
PCle Transceivers



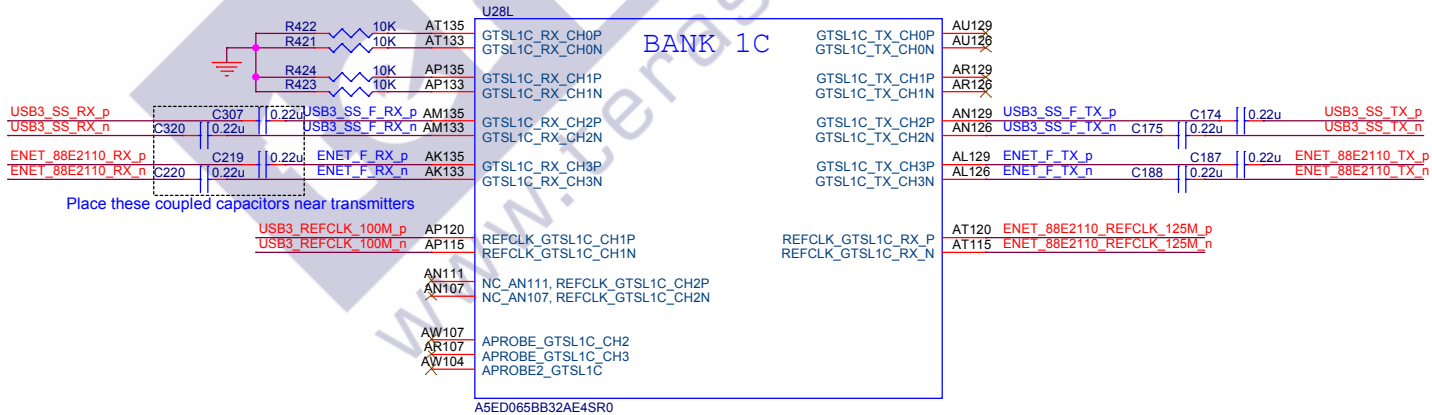
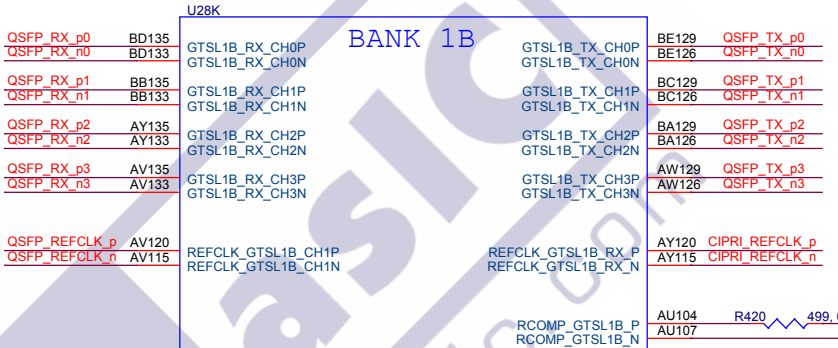
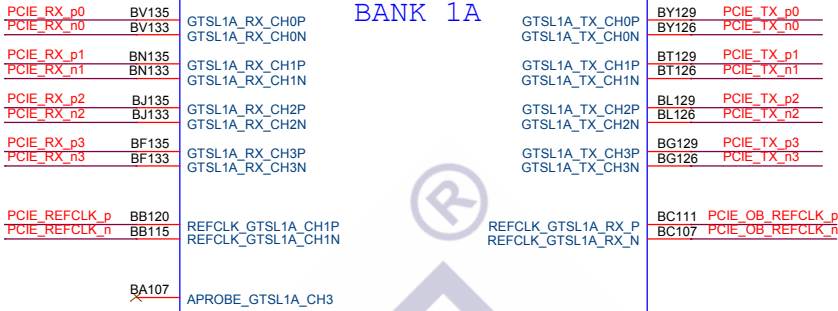
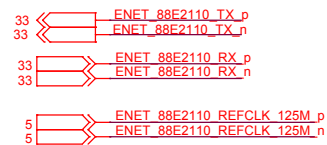
QSFP+ Transceivers



USB 3.1 Transceivers

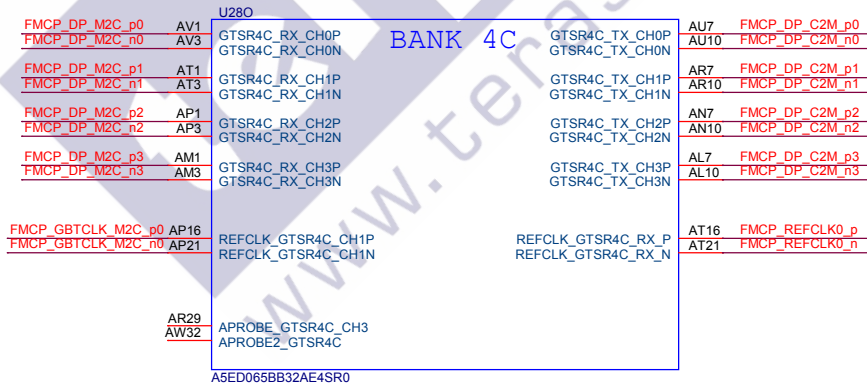
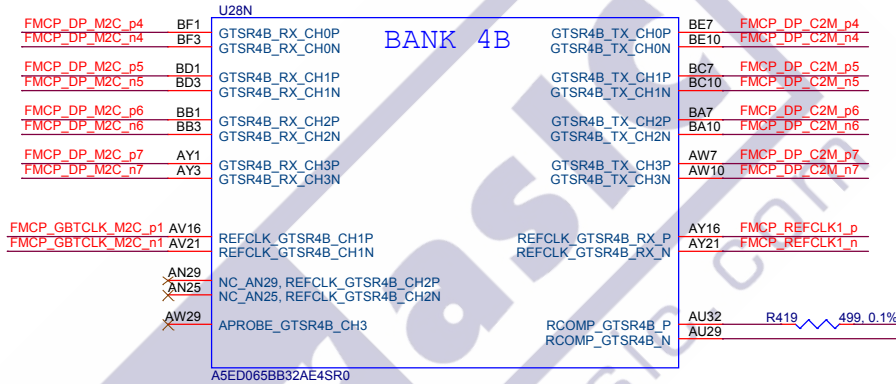
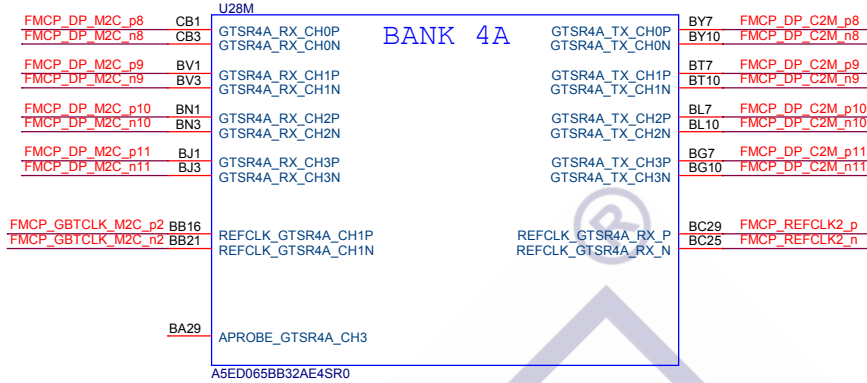
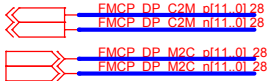


2.5G Ethernet Transceivers



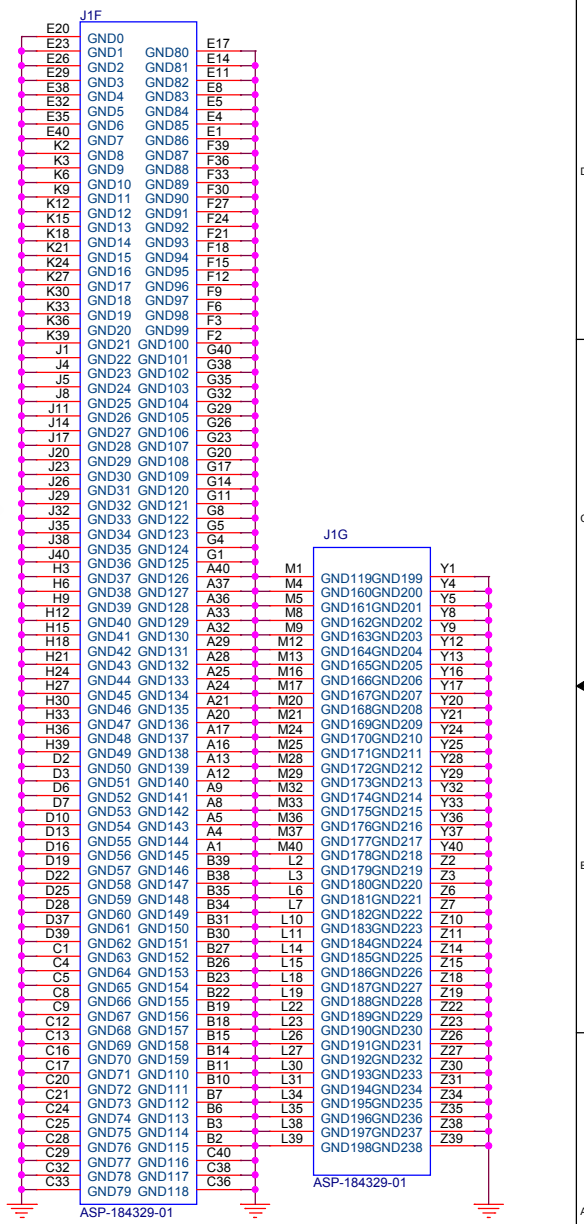
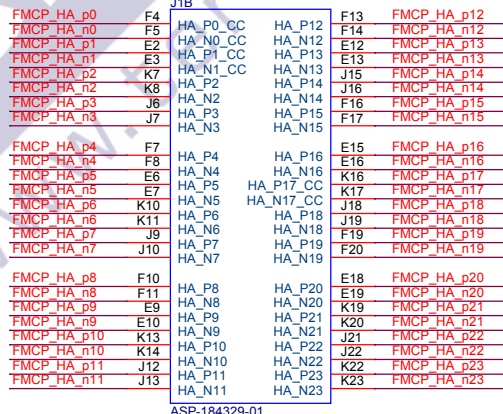
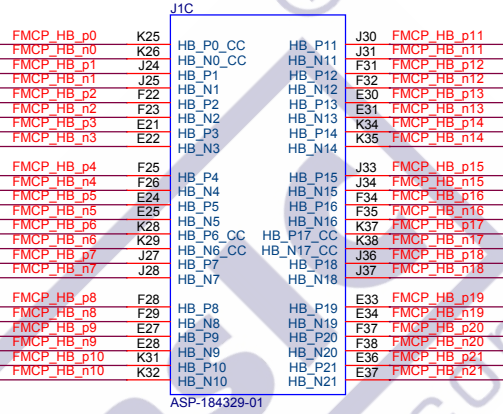
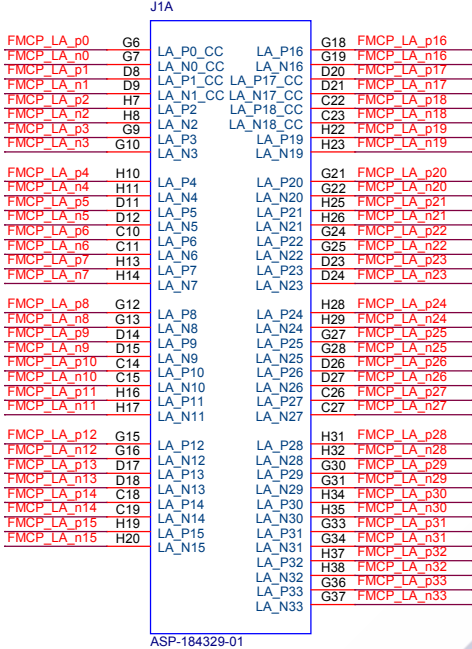
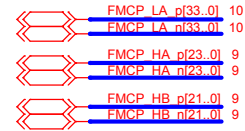
Place these coupled capacitors near transmitters

FMC+ Transceiver



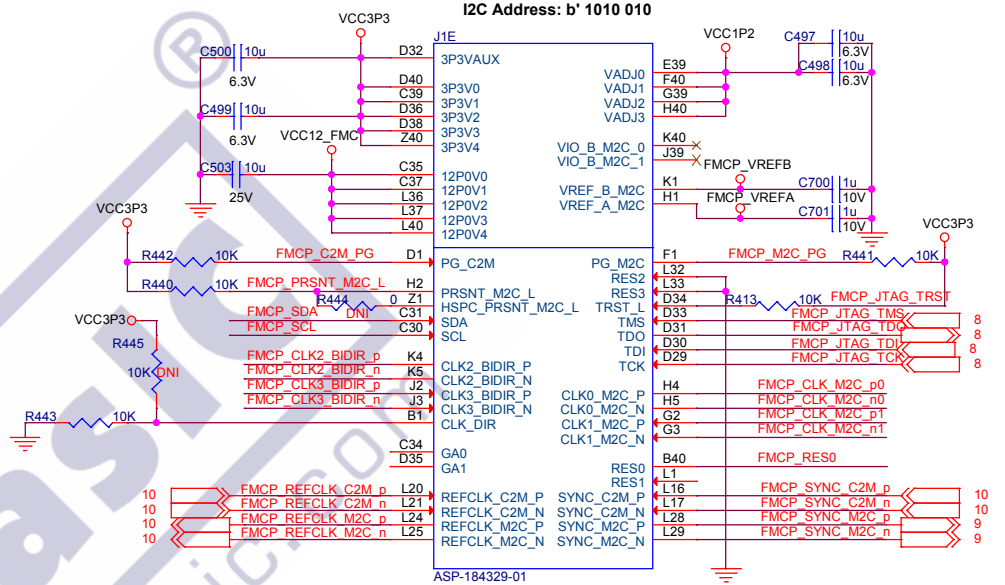
FMC+ PORT INTERFACE(HPC)

FMC+ 1



The diagram illustrates the internal circuitry of the FMCP module. Key components and connections include:

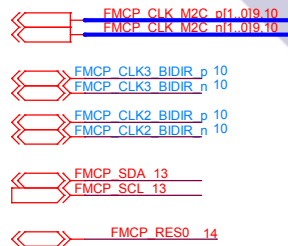
- Power Supply:** A 6.3V supply is connected to capacitors C500 and C499 (both 10uF). A 25V supply is connected to capacitor C503 (10uF).
- Signal Lines:**
 - FMCP_RE (Red)
 - FMCP_CE (Green)
 - FMCP_CU (Blue)
 - FMCP_CL (Yellow)
- Resistors:**
 - R442 (10K) and R440 (10K) are connected between VCC3P3 and the FMCP_RE and FMCP_CE lines, respectively.
 - R445 (10K) is a pull-down resistor connected between VCC3P3 and the FMCP_CU line.
 - R443 (10K) is connected between ground and the FMCP_CL line.
- Other Labels:** VCC3P3, 10u, 6.3V, 25V, 10K, ONI, and various pin numbers (10, 11, 12) are also present.

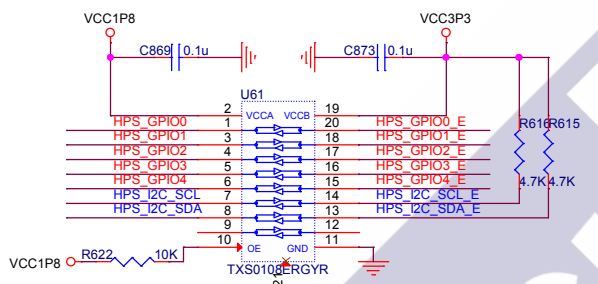
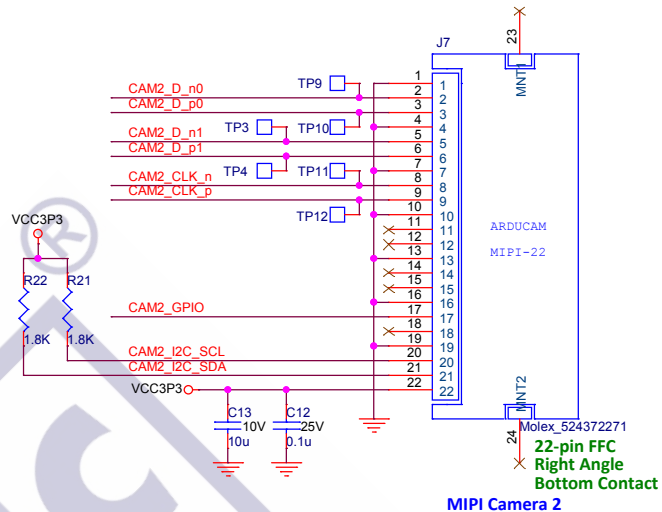
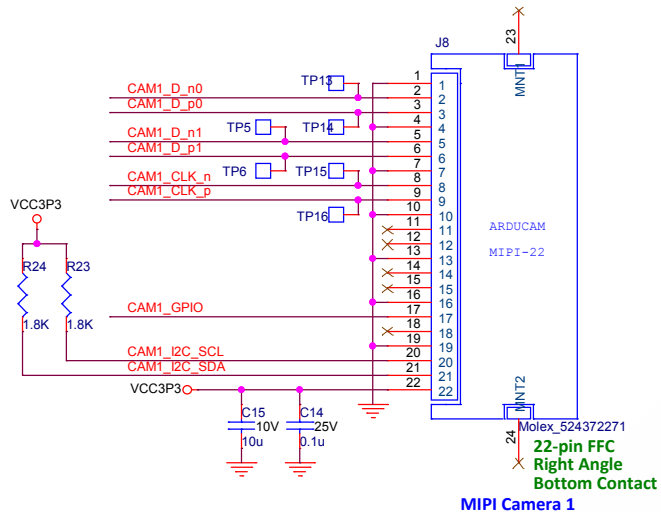
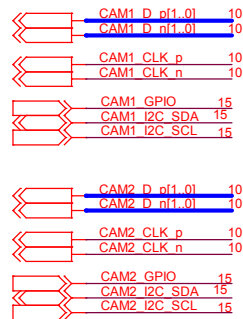


Timing diagram for the FMCP module. The diagram shows the timing relationship between several signals:

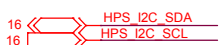
- FMCP_DP_C2M_p[11..0] (18-bit data bus)
- FMCP_DP_C2M_n[11..0] (18-bit data bus)
- FMCP_DP_M2C_p[11..0] (18-bit data bus)
- FMCP_DP_M2C_n[11..0] (18-bit data bus)
- FMCP_GBTCLK_M2C_p[2..0] (3-bit data bus)
- FMCP_GBTCLK_M2C_n[2..0] (3-bit data bus)
- FMCP_PRSENT_M2C_L (1-bit signal)

The diagram illustrates the timing of these signals relative to each other, showing that the data buses are active during specific clock cycles of the GBTCLK signal.

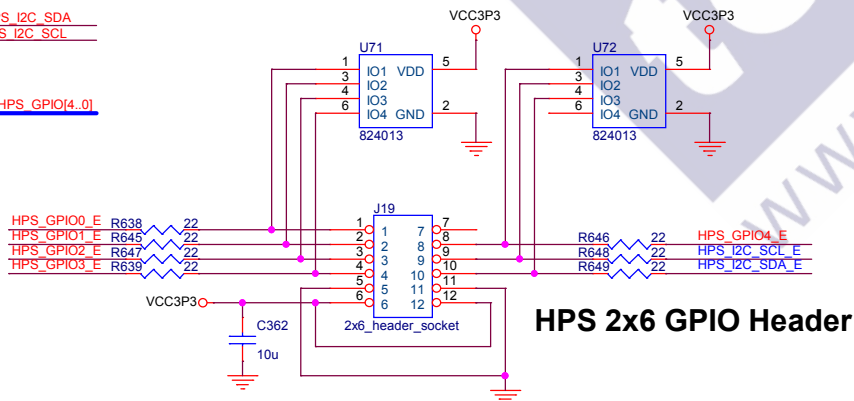




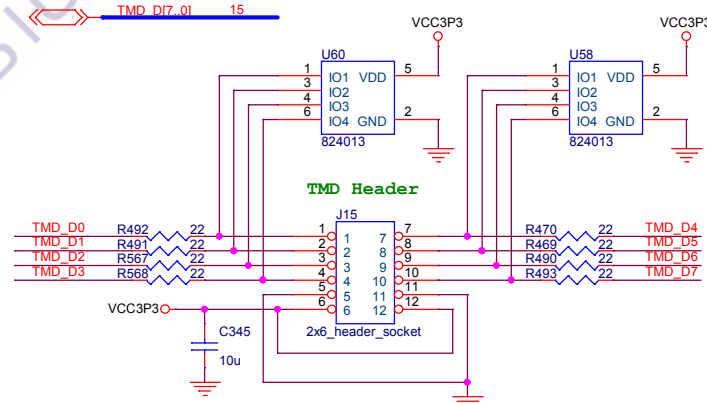
HPS I2C Interface



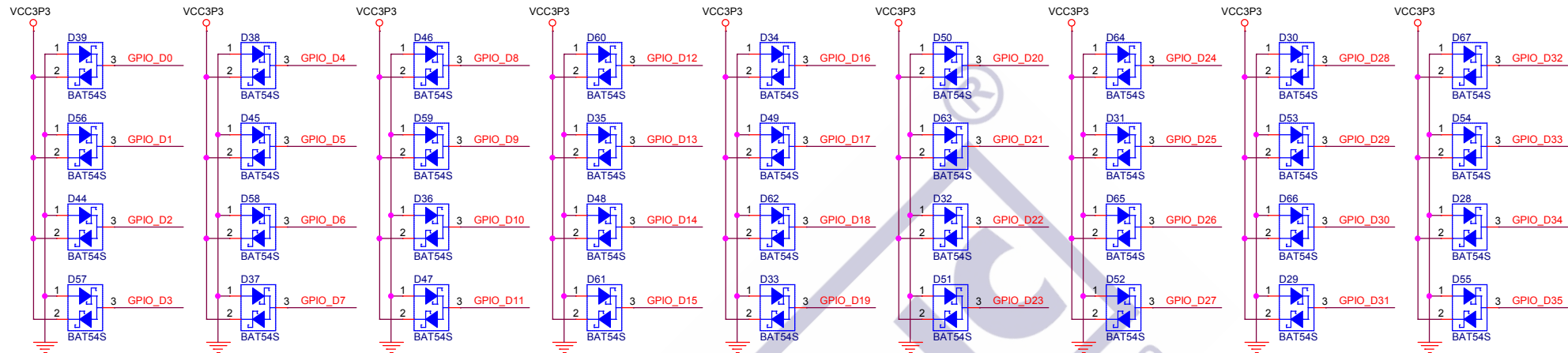
HPS GPIO



TMD 2x6 Header



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GPIO

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