

Dual-Phase 60A, 16V, Scalable Step-Down Regulator with PMBus and AVSBus

MAX20860A

General Description

The MAX20860A is a fully integrated, highly efficient, dual-phase step-down DC-DC switching regulator with PMBus and AVSBus Interfaces. The device operates from 2.7V to 16V input supplies, and the output can be adjusted from 0.4V to 5.8V, delivering up to 60A of load current. The MAX20860A can work with up to two external power stages from 5.0V to 16V input supplies and deliver up to 120A load current.

The switching frequency of the device can be configured from 308kHz to 2MHz, to provide the capability of optimizing the design in terms of size and performance.

MAX20860A utilizes fixed frequency, current-mode control with internal compensation. The IC features selectable advanced modulation scheme (AMS) to provide improved performance during fast load transients. Operation settings and configurable features can be selected by connecting a pin-strap resistors from PGM_ pins to ground or using PMBus commands.

MAX20860A has internal 1.8V LDO outputs to power the gate drives (V_{CC1} and V_{CC2}) and internal circuitry (AVDD and DVDD). The device also has an optional LDO input pin (LDOIN), allowing connection from a 2.5V to 5.5V bias input supply for optimized efficiency.

The IC has multiple protections including positive and negative overcurrent protection, output overvoltage protection and over temperature protection to ensure robust design.

The device is available in 4.25mm x 10mm FC2QFN package. It supports -40°C to +125°C junction temperature operation.

Applications

- Data Center Power
- Communications Equipment
- Networking Equipment
- Servers and Storage
- Point-of-Load Voltage Regulators

[Ordering Information](#) appears at end of data sheet.

Benefits and Features

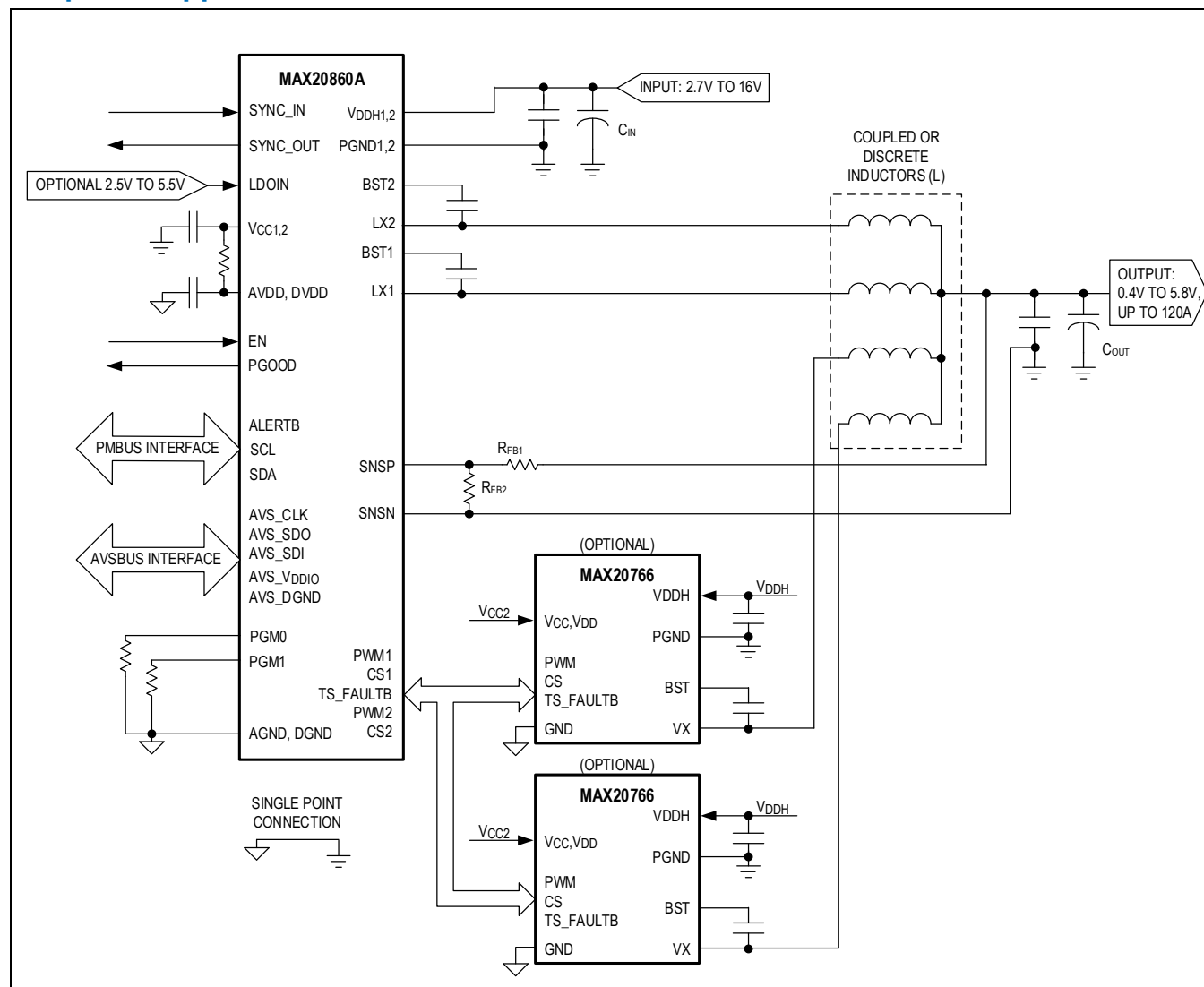
- High Power Density with Low Component Count
 - Dual-Phase Operation
 - Compact 4.25mm x 10mm, 36-pin, FC2QFN Package
 - Internal Compensation
 - Single Supply Operation with Integrated LDO for Bias Generation
- Wide Operating Range
 - Scalable to Up to Four-Phase Operation with External Power Stages
 - 2.7V to 16V Input Voltage Range
 - 0.4V to 5.8V Output Voltage Range
 - 500kHz to 2MHz Configurable Switching Frequency
 - -40°C to +125°C Junction Temperature Range
- Optimized Performance and Efficiency
 - 93%(TBD) Peak Efficiency with VDDH = 12V and $V_{OUT} = 1.2V$
 - High Efficiency with Optional External Bias Input Supply
 - AMS to Improve Load Transient Response
 - Differential Remote Sense
- PMBus and AVSBus Interfaces
 - Adaptive Voltage Scaling of 0.4V to 0.8V Reference Range
 - PMBus Telemetry of Output Current, Output Voltage, Input Voltage and Junction Temperature

| DESCRIPTION | CURRENT RATING* (A) | INPUT VOLTAGE (V) | OUTPUT VOLTAGE (V) |
|-----------------------------------------------------------------|---------------------|-------------------|--------------------|
| Electrical Rating | 60 | 2.7 to 16 | 0.4 to 5.8 |
| Thermal Rating $T_A = 55^\circ\text{C}$, 200LFM air flow | 50 | 12 | 1.8 |
| Thermal Rating $T_A = 85^\circ\text{C}$, no air flow | 50 | 12 | 0.8 |

*Maximum $T_J = 125^\circ\text{C}$. For specific operating conditions, see the Safe Operating Area (SOA) curves in the [Error! Reference source not found.](#) section.

PRELIMINARY

Simplified Application Circuit



PRELIMINARY

Absolute Maximum Ratings

| | |
|-----------------------------------------------|-----------------|
| V _{DDH} _ to PGND_ (Note 1) | -0.3V to +19V |
| LX_ to PGND_ (DC) | -0.3V to +19V |
| LX_ to PGND_ (AC) (Note 2) | -10V to +23V |
| V _{DDH} _ to LX_ (DC) (Note 1) | -0.3V to +19V |
| V _{DDH} _ to LX_ (AC) (Note 2) | -10V to +23V |
| BST_ to PGND_ (DC) | -0.3V to +21.5V |
| BST_ to PGND_ (AC) (Note 2) | -7V to +25.5V |
| BST_ to LX_ | -0.3V to +2.5V |
| PGND_, DGND, AVS_DGND to AGND | -0.3V to +0.3V |
| V _{CC} _ to PGND_ | -0.3V to +2.5 V |
| AVDD to AGND | -0.3V to +2.5V |
| DVDD to DGND | -0.3V to +2.5V |
| LDOIN to AGND | -0.3V to +6V |
| EN, PGOOD, SCL, SDA, ALERTB to AGND | -0.3V to +4V |

| | |
|----------------------------------------------|--------------------|
| SYNC_IN to DGND | -0.3V to +2.5V |
| SYNC_OUT to DGND | -0.3V to DVDD+0.3V |
| SNSP to AGND | -0.3V to AVDD+0.3V |
| SNSN to AGND | -0.3V to +0.3V |
| PGM_ to AGND | -0.3V to AVDD+0.3V |
| TS_FAULTB, PWM_, CS_ to AGND | -0.3V to AVDD+0.3V |
| AVS_V _{DDIO} to AVS_DGND | -0.3V to +2.5V |
| AVS_CLK, AVS_SDI, AVS_SDO to AVS_DGND | -0.3V to +2.5V |
| Peak LX Current | TBDA to TBDA |
| Junction Temperature (T _J) | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Peak Reflow Temperature Lead-Free | +260°C |

Note 1: Input HF capacitors placed not more than 40 mils away from the V_{DDH} pin required to keep inductive voltage spikes within Absolute Maximum limits.

Note 2: AC is limited to 25ns

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

36 FC2QFN

| | |
|---------------------------------------------------------------------------------------------------------------|------------|
| Package Code | F364A10F+1 |
| Outline Number | 21-100573 |
| Land Pattern Number | 90-100208 |
| Thermal Resistance | |
| Junction-to-Ambient (θ _{JA}) | TBD |
| Junction-to-Case Thermal Resistance (θ _{JC}) | TBD |
| Junction-to-Ambient Thermal Resistance (θ _{JA}) on MAX20860ACL2EVKIT# (no heat sink, no airflow) | TBD |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, Refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(See Typical Application Circuit. V_{DDH1} = V_{DDH2} = 12V, V_{LDOIN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. specifications are production tested at T_A = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|------------------|-------------------------------------|-----|-----|-----|-------|
| Input Supply | | | | | | |
| Input Voltage Range | V _{DDH} | | 2.7 | | 16 | V |
| | | Operating with external power stage | 5.0 | | 16 | |

(See Typical Application Circuit. $V_{DDH1} = V_{DDH2} = 12V$, $V_{LDOIN} = 3.3V$, $T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. specifications are production tested at $T_A = +32^{\circ}C$; limits within the operating temperature range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------------|-----------------------|-------------------------------------------------------------------------|------|------|------|-------|
| | | For PMBus Command USER_STORE_ALL | 10.8 | | 16 | |
| Input Supply Current | I_{VDDH} | $V_{LDOIN} = 3.3V$, EN = AGND | | 0.2 | | mA |
| | | $V_{LDOIN} = AGND$, EN = AGND | | 15.2 | | |
| | | | | | | |
| Linear Regulator Input Voltage | V_{LDOIN} | | 2.5 | | 5.5 | V |
| Linear Regulator Input Current | I_{LDOIN} | EN = AGND | | 15 | | mA |
| Internal LDO Regulated Output | V_{CC} | | 1.71 | | 1.95 | V |
| Linear Regulator Current Limit | | $V_{LDOIN} = AGND$ | TBD | | | mA |
| | | $V_{LDOIN} = 3.3V$ | TBD | | | |
| | | $V_{CC} < 1.6V$ | | TBD | | |
| V_{CC} Undervoltage Lockout | V_{CC} | Rising | 1.65 | 1.67 | 1.70 | V |
| V_{CC} Undervoltage Lockout Hysteresis | | | | 55 | | mV |
| AVDD Undervoltage Lockout | AVDD | Rising | 1.65 | 1.67 | 1.70 | V |
| AVDD Undervoltage Lockout Hysteresis | | | | 55 | | mV |
| DVDD Undervoltage Lockout | DVDD | Rising | 1.65 | 1.67 | 1.70 | V |
| DVDD Undervoltage Lockout Hysteresis | | | | 55 | | mV |
| V_{DDH} Undervoltage Lockout | V_{DDH} | Operating without external power stage; rising | 2.4 | 2.5 | 2.6 | V |
| | | Operating with external power stage; rising | 4.55 | 4.75 | 4.90 | |
| | | For PMBus Command USER_STORE_ALL | 10.0 | 10.6 | 10.8 | |
| V_{DDH} Undervoltage Lockout Hysteresis | | Operating without external power stage; rising | | 100 | | mV |
| | | Operating with external power stage; rising | | 300 | | |
| | | For PMBus Command USER_STORE_ALL | | 110 | | |
| V_{DDH} Overvoltage Lockout | V_{DDH} | | 17.3 | 17.8 | 18.3 | V |
| V_{DDH} Overvoltage Lockout Hysteresis | | | | 500 | | mV |
| LDOIN Undervoltage Lockout | V_{LDOIN} | | 2.26 | 2.33 | 2.40 | V |
| LDOIN Undervoltage Lockout Hysteresis | | | | 100 | | mV |
| Output Voltage Range and Accuracy | | | | | | |
| Feedback Voltage Accuracy | $V_{SNSP} - V_{SNSN}$ | $V_{REF} = 0.4V$ to $0.8V$ | -1 | | +1 | % |
| | | $V_{REF} = 0.4V$ to $0.8V$, $T_A = T_J = 0^{\circ}C$ to $+85^{\circ}C$ | -0.6 | | +0.6 | |

PRELIMINARY

(See Typical Application Circuit. $V_{DDH1} = V_{DDH2} = 12V$, $V_{LDOIN} = 3.3V$, $T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. specifications are production tested at $T_A = +32^{\circ}C$; limits within the operating temperature range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------------|-------------------|-----------------------------------------|-------|-----|------|-------|
| Positive Voltage Sense Leakage Current | I _{SNSP} | T _A = T _J = +25°C | | | 1 | μA |
| Negative Voltage Sense Input Range | V _{SNSN} | | -100 | | +100 | mV |
| Negative Voltage Sense Bias Current | I _{SNSN} | | | | 500 | μA |
| Switching Frequency | | | | | | |
| Switching Frequency | f _{SW} | | 308 | | | kHz |
| | | | 400 | | | |
| | | | 444 | | | |
| | | | 500 | | | |
| | | | 571 | | | |
| | | | 667 | | | |
| | | | 800 | | | |
| | | | 1000 | | | |
| | | | 1333 | | | |
| | | | 2000 | | | |
| Switching Frequency Accuracy | | | -10 | | +10 | % |
| Phase Shift Between Two Phases | | | 180 | | | ° |
| Minimum Controllable On-Time | | Inductor valley current ≤ 0A (Note 3) | 50 | | | ns |
| | | Inductor valley current > 0A (Note 3) | 45 | | | |
| Minimum Controllable Off-Time | | | 100 | | | ns |
| Enable and Startup | | | | | | |
| Initialization Time | t _{INIT} | | 2 | | 5 | ms |
| EN Threshold | | Rising | 0.9 | | | V |
| | | Falling | 0.6 | | | |
| EN Filtering Delay | | Rising | 200 | | | μs |
| | | Falling | 2 | | | |
| Soft Startup Slew Rate | | | 1 | | | V/ms |
| | | | 0.5 | | | |
| | | | 0.33 | | | |
| | | | 0.167 | | | |
| Power Good and Fault Protections | | | | | | |
| PGOOD Output Low | | I _{PGOOD} = 3mA | 0.4 | | | V |
| Output Undervoltage (UV) Threshold | | | -16 | -13 | -10 | % |
| Output UV Deglitch Delay | | | 4 | | | μs |

PRELIMINARY

(See Typical Application Circuit. $V_{DDH1} = V_{DDH2} = 12V$, $V_{LDOIN} = 3.3V$, $T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. specifications are production tested at $T_A = +32^{\circ}C$; limits within the operating temperature range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------------------------------------------|--------------------|----------------------------------------------|------|------|------|-------------|
| Output Overvoltage Protection (OVP) Threshold | | | 10 | 13 | 16 | % |
| Output OVP Threshold Deglitch Delay | | | | 2 | | μs |
| Positive Overcurrent Protection (POCP) Threshold | | Per phase, inductor peak current, POCP = 40A | 36 | 40 | 44 | A |
| | | Per phase, inductor peak current, POCP = 35A | 31.5 | 35 | 38.5 | |
| | | Per phase, inductor peak current, POCP = 30A | 27 | 30 | 33 | |
| | | Per phase, inductor peak current, POCP = 25A | 22.5 | 25 | 27.5 | |
| POCP Deglitch Delay | t_{POCP} | | | 51 | | ns |
| Fast Positive Overcurrent Protection (FPOCP) Threshold | | | TBD | TBD | TBD | A |
| Negative Overcurrent Protection (NOCP) Threshold to POCP Threshold Ratio | | | | -83 | | % |
| NOCP Accuracy | | | -20 | | +20 | % |
| BST UVLO Threshold | $V_{BST} - V_{LX}$ | | 1.48 | 1.56 | 1.64 | V |
| BST UVLO Threshold Hysteresis | | | | 52 | | mV |
| Overtemperature Protection (OTP) Rising Threshold | | | | 155 | | $^{\circ}C$ |
| OTP Accuracy | | | | 6 | | % |
| OTP Hysteresis | | | | 20 | | $^{\circ}C$ |
| Hiccup Protection Time | | OVP, POCP or NOCP | | 20 | | ms |
| Synchronization | | | | | | |
| SYNC_IN Pin Input Low | | | | | 0.47 | V |
| SYNC_IN Pin Input High | | | 1.32 | | | V |
| SYNC_IN Input Duty Cycle | | $f_{SW} = 2MHz$ | 10 | | 90 | % |
| Synchronization Lock Frequency Range | | 300kHz to 1MHz | -15 | | +15 | % |
| SYNC_OUT Pin Output Low | | Sinking 3mA | | | 0.5 | V |
| SYNC_OUT Pin Output High | | Sourcing 4mA | 1.31 | | | V |
| External Power Stage Drive Interface (PWM_, CS_ and TS_FAULTB) | | | | | | |
| PWM_ Output | | Logic high, sourcing 4mA | 1.32 | | | V |
| | | Logic low, sinking 3mA | | | 0.5 | |
| Power-Stage Fault Logic-Low Threshold | | With respect to AGND | | 300 | | mV |

(See Typical Application Circuit. $V_{DDH1} = V_{DDH2} = 12V$, $V_{LDOIN} = 3.3V$, $T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. specifications are production tested at $T_A = +32^{\circ}C$; limits within the operating temperature range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------------------------|----------------------|-------------------------------------------------------|-----------------------|-----|-----------------------|------------|
| External Power-Stage Detection Level | | | $0.3 \times AVD_D$ | | $0.7 \times AVD_D$ | V |
| External Power-Stage Detection Time | | Detecting the presence of two external power stages | | | 200 | μs |
| PMBus Interface | | | | | | |
| SCL, SDA Input Logic Low Voltage | | | | | 0.7 | V |
| SCL, SDA Input Logic High Voltage | | | 1.46 | | | V |
| SCL, SDA, ALERTB Logic High Leakage Current | | | | | 1 | μA |
| SDA Output Logic Low | | Sinking 20mA | | | 0.4 | V |
| PMBus Operating Frequency | f_{CLK} | | 100 | | 1000 | kHz |
| SDA Hold Time from SCL | t_{HD_DAT} | (Note 3) | 0 | | | ns |
| SDA Setup Time from SCL | t_{SU_DAT} | (Note 3) | 50 | | | ns |
| SCL High Period | t_{HIGH} | (Note 3) | 0.26 | | | μs |
| SCL Low Period | t_{LOW} | (Note 3) | 0.5 | | | μs |
| AVSBus Interface | | | | | | |
| AVS_ V_{DDIO} Input Voltage Range | V_{DDIO} | | 0.9 | | 1.98 | V |
| AVS_ CLK , AVS_ SDI , Input High Level | V_{IH} | | $0.7 \times V_{DDIO}$ | | | V |
| AVS_ CLK , AVS_ SDI , Input Low Level | V_{IL} | | | | $0.3 \times V_{DDIO}$ | V |
| AVS_ SDO Output High Level | V_{OH} | 10mA sink current | $0.8 \times V_{DDIO}$ | | | V |
| AVS_ SDO Output Low Level | V_{OL} | 10mA source current | | | $0.2 \times V_{DDIO}$ | V |
| AVS_ SDO Weak Pull-Up | R_{PU} | Internal Pull-Up to V_{DDIO} | | 20 | | k Ω |
| Input Leakage Current | | | -10 | | +10 | μA |
| AVS_ CLK Frequency Range | | | 5 | | 50 | MHz |
| Target-to-Controller Data Launch Delay (Transmitter) | t_{LAUNCH_TARGET} | AVS_ CLK crossing V_{IH} to AVS_ SDO transition | | 4 | | ns |
| PMBus/AVSBus Telemetry | | | | | | |
| Reading Update Rate | | Output current | | 1 | | ms |
| | | Output voltage | | 6.5 | | |
| | | Input voltage | | 13 | | |
| | | Junction temperature | | 13 | | |
| System ADC Resolution | | | | 10 | | bits |
| READ_ I_{OUT} Range | | Per phase | 0 | | 40 | A |

(See Typical Application Circuit. $V_{DDH1} = V_{DDH2} = 12V$, $V_{LDOIN} = 3.3V$, $T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. specifications are production tested at $T_A = +32^{\circ}C$; limits within the operating temperature range are guaranteed by design and characterization.)

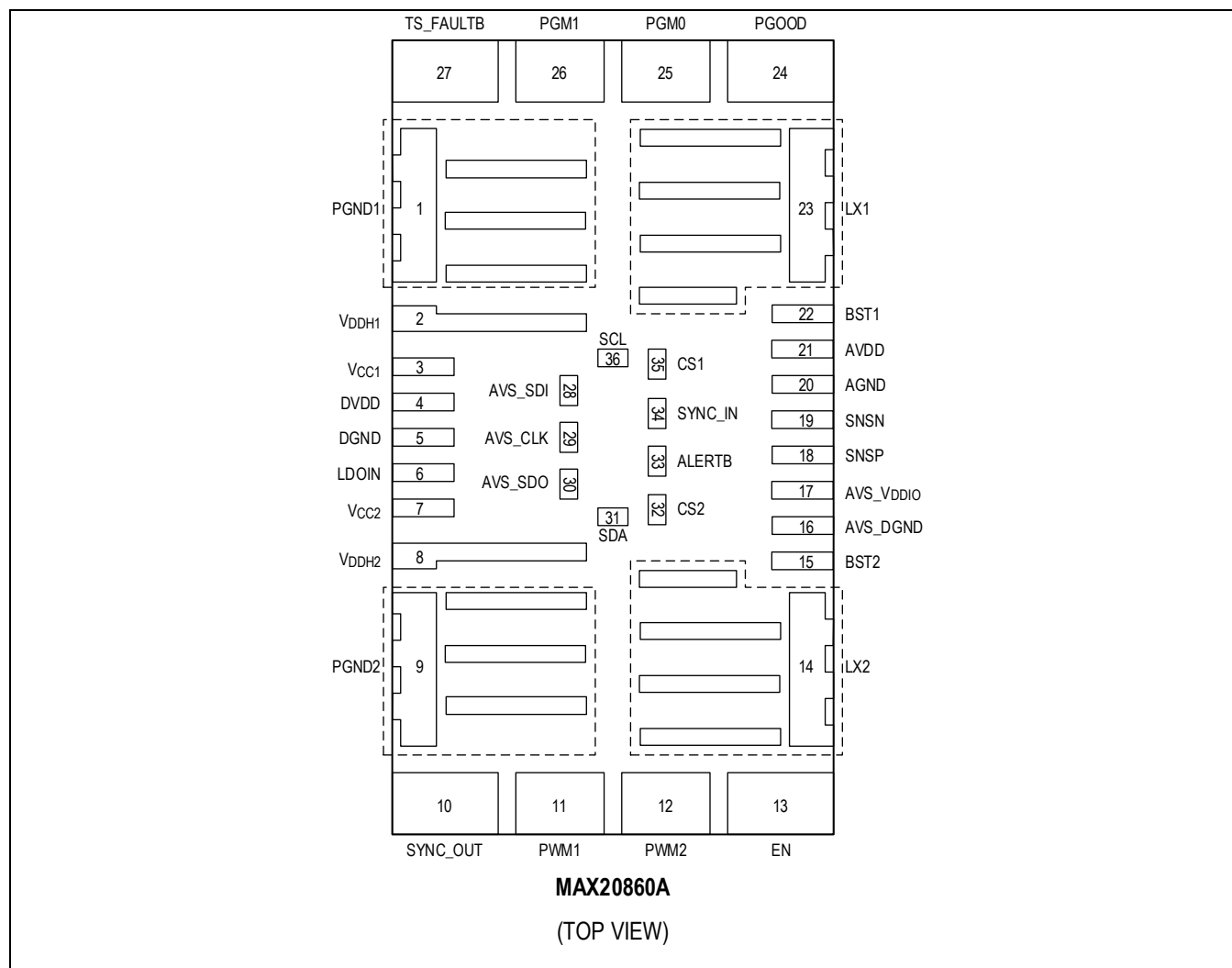
Characterization:

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|--------|-----------------------------|--------------------------|-----|------|-------|
| READ_IOUT Accuracy | | I _{OUT} = 0A | -2.2 | | +2.2 | A |
| | | 0A < I _{OUT} < 60A | -3.6 | | +3.6 | |
| READ_VOUT Range | | | V _{REF} +/- 200 | | | mV |
| READ_VOUT Accuracy | | | -2 | | +2 | % |
| READ_VIN Range | | | 2.3 | | 16 | V |
| READ_VIN Accuracy | | | -3 | | +3 | % |
| READ_TEMPERATURE Range | | | -40 | | 150 | °C |
| READ_TEMPERATURE Accuracy | | | +/-4 | | | °C |
| Programming Pins | | | | | | |
| PGM_ Pin Resistor Range | | | 0.095 | | 115 | kΩ |
| PGM_ Resistor Accuracy | | | -1 | | +1 | % |

Note 3: Guaranteed by design.

Pin Configurations

PRELIMINARY



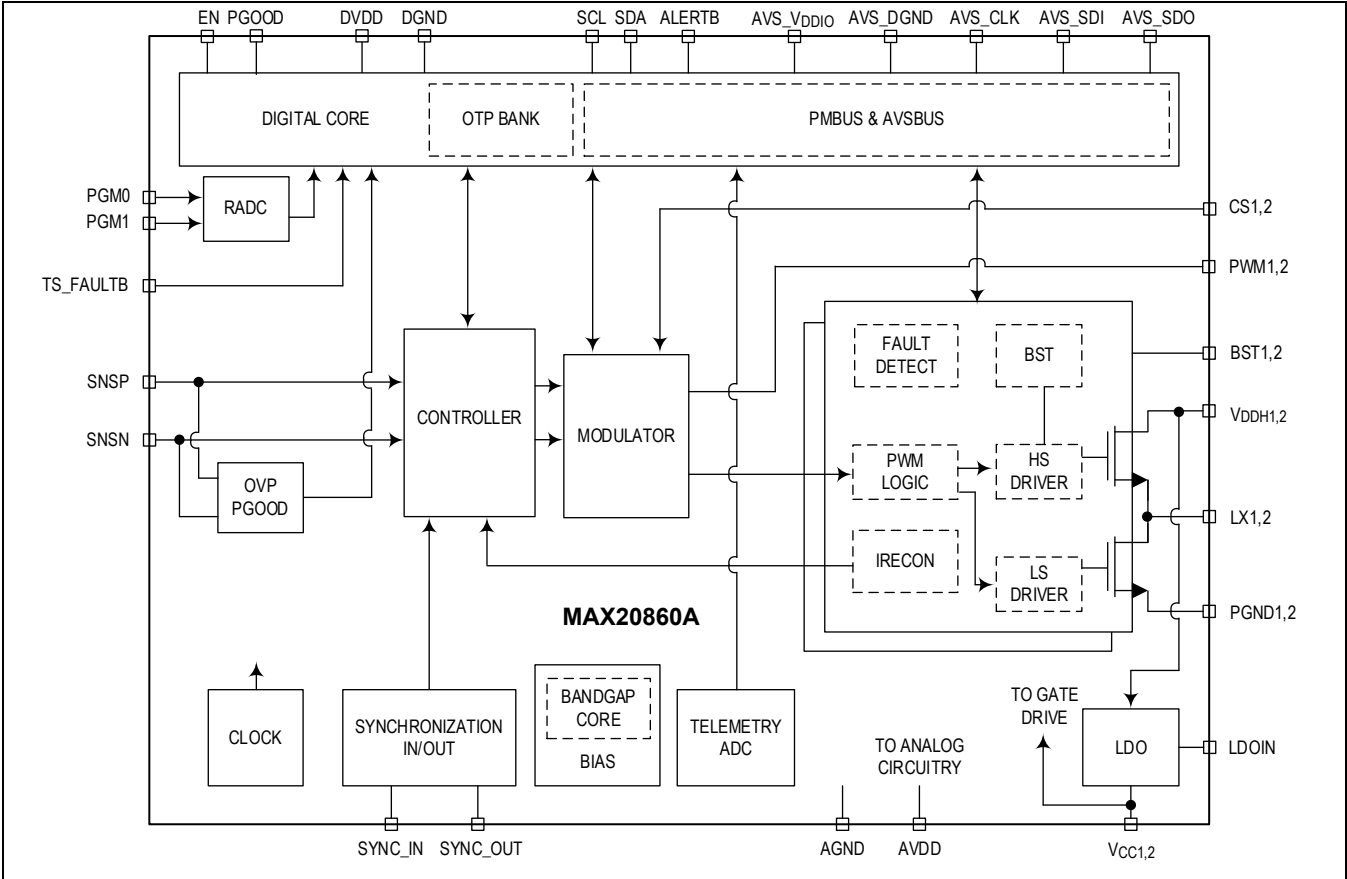
PRELIMINARY

Pin Descriptions

| PIN | NAME | FUNCTION |
|-----|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | PGND1 | Power Ground 1. PGND1 and PGND2 must be connected on the PCB. |
| 2 | V _{DDH1} | Regulator Input Supply 1. V _{DDH1} and V _{DDH2} must be connected on the PCB. |
| 3 | V _{CC1} | Internal 1.8V LDO Output 1. Connect a 4.7μF or greater ceramic capacitor from V _{CC1} to PGND. |
| 4 | DVDD | 1.8V Supply for Digital Circuitry. Connect a 1Ω to 2.2Ω resistor from DVDD to V _{CC1} . Connect a 1μF or greater ceramic capacitor from DVDD to DGND. |
| 5 | DGND | Digital Ground. Connect DGND to AGND on the PCB. |
| 6 | LDOIN | Optional 2.5V to 5.5V LDO Input Supply. Connect this pin to AVDD or GND, or leave this pin floating if unused. |
| 7 | V _{CC2} | Internal 1.8V LDO Output 2. Connect a 4.7μF or greater ceramic capacitor from V _{CC2} to PGND. |
| 8 | V _{DDH2} | Regulator Input Supply 2. V _{DDH1} and V _{DDH2} must be connected on the PCB. |

| | | |
|----|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9 | PGND2 | Power Ground 2. PGND1 and PGND2 must be connected on the PCB. |
| 10 | SYNC_OUT | Synchronization Clock Output. Connect this pin to the downstream regulator SYNC_IN pin or leave this pin floating if unused. |
| 11 | PWM1 | PWM Output for the 3rd Phase External Power Stage. Connect to the external power-stage PWM input or pull to AGND if not used. |
| 12 | PWM2 | Output for the 4th Phase External Power Stage. Connect to the external power-stage PWM input or pull to AGND if not used. |
| 13 | EN | Output Enable. |
| 14 | LX2 | Switching Node 2. Connect LX2 directly to the output inductor. |
| 15 | BST2 | Bootstrap Pin 2. Connect a 0.47μF ceramic capacitor from BST2 to LX2. |
| 16 | AVS_DGND | Digital Ground for AVSBus. Connect AVS_DGND to DGND on the PCB. |
| 17 | AVS_VDDIO | AVSBus Supply Voltage Connection. Connect a 0.1μF or greater ceramic capacitor from AVS_VDDIO to AVS_DGND. |
| 18 | SNSP | Output Voltage Remote Sense Positive Input Pin. Connect SNSP to output voltage at the load. A resistive voltage divider can be inserted between the output and SNSP to regulate the output above the reference voltage. |
| 19 | SNSN | Output Voltage Remote Sense Negative Input. |
| 20 | AGND | Analog Ground. |
| 21 | AVDD | 1.8V Supply for Analog Circuitry. Connect a 1Ω to 2.2Ω resistor from AVDD to V _{CC1} . Connect a 1μF or greater ceramic capacitor from AVDD to AGND. |
| 22 | BST1 | Bootstrap Pin 1. Connect a 0.47μF ceramic capacitor from BST1 to LX1. |
| 23 | LX1 | Switching Node 1. Connect LX1 directly to the output inductor. |
| 24 | PGOOD | Open-Drain Power Good Output. |
| 25 | PGM0 | Program Input. Connect this pin to ground though a programming resistor. |
| 26 | PGM1 | Program Input. Connect this pin to ground though a programming resistor. |
| 27 | TS_FAULTB | External Power-Stage TS_FAULTB Connection. Temperature sense and fault input. Connect a 100pF capacitor to AGND. |
| 28 | AVS_SDI | AVSBus Controller to Target Serial Data Input. |
| 29 | AVS_CLK | AVSBus Controller to Target Clock Input. |
| 30 | AVS_SDO | AVSBus Target to Controller Serial Data Output. |
| 31 | SDA | PMBus Data Input/Output. |
| 32 | CS2 | External Power Stage IC Current-Sensing Input from the 4th Phase. Connect to the external power-stage CS output or pulled to AGND if not used. |
| 33 | ALERTB | PMBus Alert. |
| 34 | SYNC_IN | Synchronization Clock Input. Connect this pin to AGND or leave this pin floating if unused. |
| 35 | CS1 | External Power Stage IC Current-Sensing Input from the 3rd Phase. Connect to the external power-stage CS output or pulled to AGND if not used. |
| 36 | SCL | PMBus Clock Input. |

Block Diagram



PRELIMINARY

Detailed Description

Dual-Phase to Quad-Phase Operations

The MAX20860A is by default configured as a dual-phase 60A converter. When connecting to external power stage(s), The MAX20860A can also support three-phase or quad-phase operations. It is recommended to use MAX20860A compatible external power stages (i.e., MAX20766, MAX16604, etc.). The PWM_, CS_ and TS_FAULTB pins of the MAX20860A are used to communicate PWM signal(s), current sense signal(s), temperature sense signal and fault status between the MAX20860A and the connected external power stage(s).

All operating phases of the MAX20860A are evenly interleaved for reduced input/output voltage ripple and improved load transient performance. Table 1 summarized the phase spacing and firing order for different phase configurations.

Table 1. Phase Configurations

| PHASE CONFIGURATION | PHASE INTERLEAVE | FIRING ORDER |
|---------------------|------------------|----------------------|
| 2-Phase | 180° | LX1, LX2 |
| 3-Phase | 120° | LX1, PWM1, LX2 |
| 4-Phase | 90° | LX1, PWM1, LX2, PWM2 |

Control Architecture

Fixed-Frequency Peak Current Mode Control Loop

The MAX20860A control loop is based on fixed-frequency peak current mode control architecture. A simplified control architecture is shown in Figure 1. The loop contains an error amplifier stage, internal voltage loop compensation network, current sense, internal slope compensation and a PWM modulator that generates the PWM signals to drive high-side and low-side MOSFETs. The reference voltage (V_{REF}) can be adjusted by the PMBus VOUT_COMMAND from 0.4V to 0.8V

with 0.98mV resolution (refer to *UGxxxx: MAX20860A/B PMBus Command Set User Guide*). The default V_{REF} is configured by scenarios selected by PGM1 pin (See *Pin-Strap Programmability*). The difference of V_{REF} and the sensed output voltage is amplified by the first error amplifier. Its output voltage (V_{ERR}) is used as the input of the voltage loop compensation network. The output of the compensation network (V_{COMP}) is fed to a PWM comparator with current sense signal ($V_{ISENSE_}$) and the slope compensation (V_{RAMP}). The output of the PWM comparator is the input of the PWM modulator. The turning on of the high-side MOSFET is aligned with an internal clock. It can either be a fixed-frequency clock or a phase shifted clock if advanced modulation scheme (AMS) is enabled (See *Advanced Modulation Scheme (AMS)*). An active current balance circuit is used to minimize the phase-current imbalance (See *Active Current Balancing*).

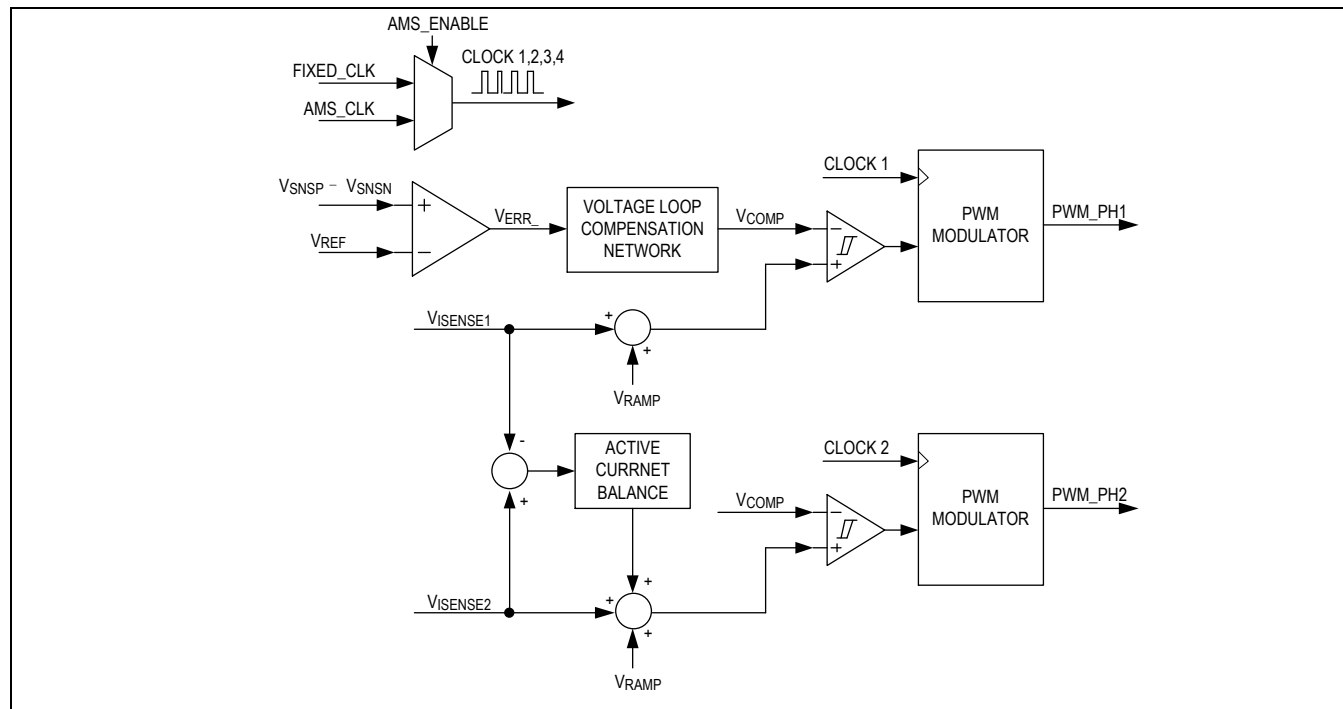


Figure 1. Simplified Control Architecture

Advanced Modulation Scheme (AMS)

The MAX20860A offers a selectable advanced modulation scheme (AMS) to provide improved transient response. AMS provides significant advantage over conventional fixed-frequency PWM schemes. Enabling the AMS feature allows for modulation at both leading and trailing edges, which result a temporary increase or decrease of the switching frequency during large load transients. Figure 2 shows the scheme to include leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows the turn on and off with minimal delay. Since the total inductor current increases very quickly, satisfying the load demand, the current drawn from output capacitors is reduced. With AMS enabled, the control loop phase-margin is boosted which allows extending control loop bandwidth to improve load transient performance. As a result, the output capacitance can be minimized.

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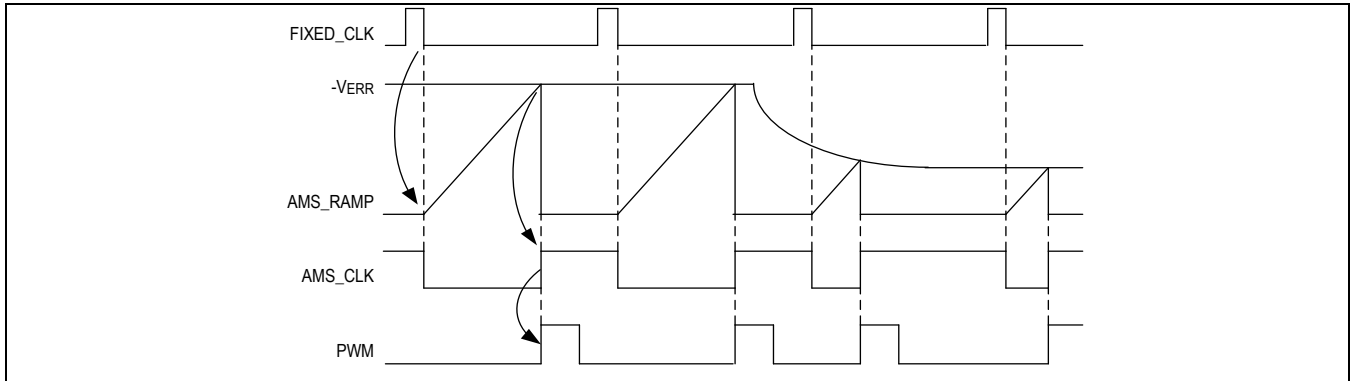


Figure 2. AMS Operation

Active Current Balancing

The MAX20860A operates with active current balancing for enhanced dynamic-current sharing among all phases. This feature maintains the current balance both at steady state and during load transients, even at a load-step frequency close to the switching frequency or its harmonics. The active current-balancing circuit adjusts the individual phase-current control signal in order to minimize the phase-current imbalance.

Synchronization

Synchronizing the switching frequency of multiple units can effectively reduce intermodulation noise and its interference to input current and output voltage. The MAX20860A supports frequency synchronization when a valid external synchronization clock is connected to the SYNC_IN pin. If a valid external synchronization clock is not available or lost during operation, the MAX20860A resumes switching smoothly with its internal clock frequency preset by the PGM1 pin or PMBus command (See [Pin-Strap Programmability](#)). The delay from the rising edge of SYNC_IN and the rising edge of the switch node LX1 can be adjusted with the PMBus INTERLEAVE command (see [PMBus Interface](#)).

The MAX20860A also provides a SYNC_OUT output which has the same frequency as the switching frequency. The SYNC_OUT output can be used as a synchronization clock for the downstream devices. There is a fixed TBD delay from the rising edge of the switch node LX1 and the rising edge of SYNC_OUT.

Internal Linear Regulator

The device contains two internal 1.8V linear regulators (LDO). The 1.8V LDO output voltages V_{CC1} and V_{CC2} are derived from V_{DDH} pins by default. To improve efficiency, an optional 2.5V to 5.5V bias input supply can be applied on the LDOIN pin so that the 1.8V voltages on V_{CC} are converted from the LDOIN pin instead. The optional LDOIN bias input supply can be applied or removed anytime during regulation without affecting operation, as long as the V_{DDH} voltage is present. Once the LDO is in operation and supplied by LDOIN bias supply, it can remain regulation if V_{DDH} voltage is removed from the device.

The 1.8V voltage on V_{CC} pins supply the current to the MOSFET drivers for both internal phases. A decoupling capacitor of at least 4.7 μ F must be connected between V_{CC} and PGND. The AVDD pin of the device requires a 1.8V supply to power the device's internal analog circuitry. A 1 Ω to 2.2 Ω resistor must be connected between AVDD and V_{CC1} . A 1 μ F or greater decoupling capacitor must be used between AVDD and AGND. Similar to AVDD, the DVDD pin of the device also requires a 1.8V supply to power the device's internal digital circuitry. A 1 Ω to 2.2 Ω resistor must also be connected between DVDD and V_{CC1} . A 1 μ F or greater decoupling capacitor must be used between DVDD and DGND. AGND and DGND must be connected on the PCB.

For three-phase and quad-phase operations where external power stages are used, the V_{CC2} of the MAX20860A can be used to supply the bias voltages for the external power stages.

Startup and Shutdown

The startup and shutdown timing is shown in Figure 3. When V_{CC} , AVDD and DVDD voltages are above their rising UVLO threshold, the device goes through an initialization procedure. Configuration settings on PGM_ pins are read. Nonvolatile PMBus memory is loaded. External power stages are detected. Once initialization is complete, the device detects V_{DDH} and EN status. When both are above their rising thresholds, the soft startup begins, and switching is enabled. The output voltage of the enabled output starts to ramp up. The soft startup slew rate is preset by PGM1 resistor

or PMBus. If there are no faults, the open drain PGOOD pin is released from being held low after the soft startup ramp is complete. The device supports smooth startup with output pre-biased.

During operation, if either V_{DDH} or EN falls below their thresholds, switching is stopped immediately. The output voltage is discharged by load current.

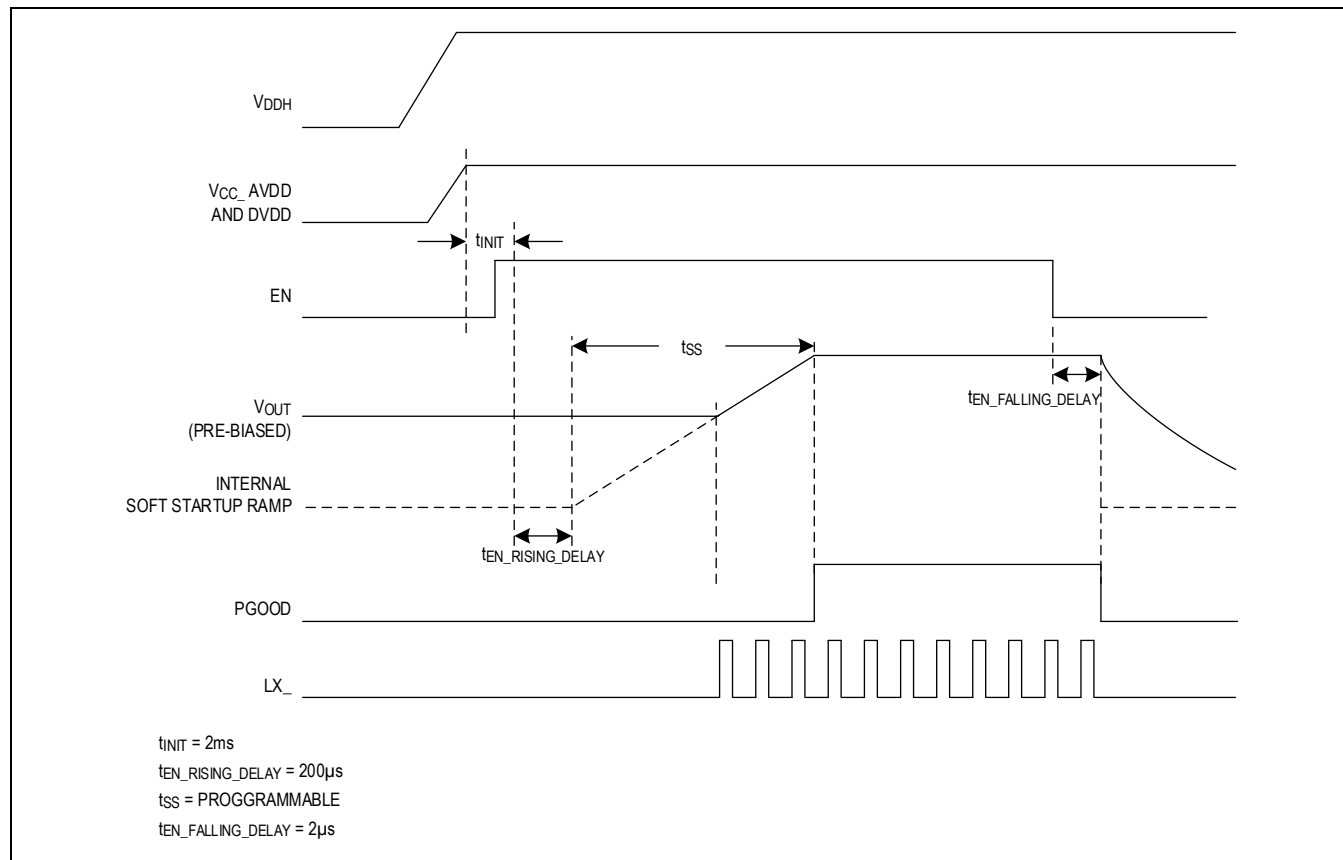


Figure 3. Startup and Shutdown Timing

Fault Handling

Input Undervoltage Lockout (V_{DDH} UVLO)

The MAX20860A internally monitors the V_{DDH} voltage level. When the input supply voltage is below the UVLO threshold, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the UVLO status is cleared. See [Startup and Shutdown](#) for startup sequence.

Output Overvoltage Protection (OVP)

The feedback voltage of $V_{SNSP} - V_{SNSN}$ is monitored for output overvoltage once the soft startup ramp is complete. If the feedback voltage is above the OVP threshold beyond the OVP deglitch filtering delay, the device stops switching and drives PGOOD pin low. The device restarts after 20ms if the OVP status is cleared.

Positive Overcurrent Protection (POCP)

The device's peak current mode control architecture provides inherent current limiting and short circuit protection. The inductor current is continuously monitored while switching. The inductor peak current is limit on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the POCP threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by output voltage. An up-down counter is used to accumulate the number of consecutive POCP events each switching cycle. If the counter exceeds 1024, the device stops switching and drives PGOOD pin low. POCP is a hiccup protection and the device restarts after 20ms.

The MAX20860A offers 4 POCP thresholds (40A, 35A, 30A and 25A per phase), which can be selected by PGM1 pin (see [Pin-Strap Programmability](#)). Due to POCP deglitch delay, for a specific application use case, the actual POCP threshold should be higher depending on the inductor selection (see [Output Inductor Selection](#)).

Besides the current limiting POCP the device also features an FPOCP which is intended to protect extreme overcurrent conditions including inductor short or saturation. The FPOCP has a threshold of 55A per phase. Once the sensed inductor current exceeds the FPOCP threshold, the device stops switching, drives PGOOD pin low and latches the device. It requires cycling power to clear the latched FPOCP fault and resume operation.

Negative Overcurrent Protection (NOCP)

The device also has negative overcurrent protection against inductor valley current. The NOCP threshold is -83% of the POCP threshold. In each switching cycle, once the sensed inductor current exceeds the NOCP threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 180ns time to allow the inductor current to be charged by input voltage. Same as POCP, an up-down counter is used to accumulate the number of consecutive NOCP events. If the counter exceeds 1024, the device stops switching and drives PGOOD pin low. NOCP is a hiccup protection and the device restarts after 20ms.

Overtemperature Protection (OTP) and External Power Stage Fault

The overtemperature protection threshold is 155°C with 20°C hysteresis. The MAX20860A monitors the junction temperature of both internal power trains and optional external power stages. The temperature of external power stages is monitored with the TS_FAULTB pin. If either the internal or external junction temperature reaches OTP threshold during operation, the device stops switching and drives PGOOD pin low. The device restarts after 20ms if the OTP status is cleared.

The external power stage also communicates their faults to the MAX20860A by pulling TS_FAULTB pin low. Once a fault is detected, the device stops switching and drives PGOOD pin low. The device restarts after 20ms if the TS_FAULTB pin is released.

Feedback Pin Open Detection

The MAX20860A supports the SNSP and SNSN pin open detection at startup. If the SNSP pin or SNSN pin is floating for any reason, the regulator does not startup switching. This protection is only active at startup and is disabled in regulation.

Pin-Strap Programmability

The MAX20860A has two program pins (PGM0 and PGM1) to set some of the key configurations of the device. The PGM_ values are read during startup initialization. PGM0 and PGM1 each has 32 detection levels. A pin-strap resistor is connected from PGM_ pin to AGND to select one of the 32 codes. PGM0 is used to select PMBus addresses. PGM1 is used to select the POCP levels and a pre-defined scenario which is defined in Table 4.

Table 2. PGM0 PMBus Address Selection

| PGM0 CODES | R _{PGM0} (Ω) | PMBUS ADDRESS |
|---------------|--------------------------|------------------|
| 0 | 95.3 | 0x10h |
| 1 | 200 | 0x11h |
| 2 | 309 | 0x12h |
| 3 | 422 | 0x13h |
| 4 | 536 | 0x14h |
| 5 | 649 | 0x15h |
| 6 | 768 | 0x16h |
| 7 | 909 | 0x17h |
| 8 | 1050 | 0x18h |
| 9 | 1210 | 0x19h |
| 10 | 1400 | 0x1Ah |
| 11 | 1620 | 0x1Bh |
| 12 | 1870 | 0x1Ch |
| 13 | 2150 | 0x1Dh |
| 14 | 2490 | 0x1Eh |
| 15 | 2870 | 0x1Fh |
| 16 | 3740 | 0x20h |

| | | |
|----|--------|-------|
| 17 | 8060 | 0x21h |
| 18 | 12400 | 0x22h |
| 19 | 16900 | 0x23h |
| 20 | 21500 | 0x24h |
| 21 | 26100 | 0x25h |
| 22 | 30900 | 0x26h |
| 23 | 36500 | 0x27h |
| 24 | 42200 | 0x28h |
| 25 | 48700 | 0x29h |
| 26 | 56200 | 0x2Ah |
| 27 | 64900 | 0x2Bh |
| 28 | 75000 | 0x2Ch |
| 29 | 86600 | 0x2Dh |
| 30 | 100000 | 0x2Eh |
| 31 | 115000 | 0x2Fh |

Table 3. PGM1 POCP and Scenario Selection

| PGM1 CODES | R _{PGM1} (Ω) | POCP (A) | SCENARIO # |
|---------------|--------------------------|----------|------------|
| 0 | 95.3 | 40 | Scenario A |
| 1 | 200 | | Scenario B |
| 2 | 309 | | Scenario C |
| 3 | 422 | | Scenario D |
| 4 | 536 | | Scenario E |
| 5 | 649 | | Scenario F |
| 6 | 768 | | Scenario G |
| 7 | 909 | | Scenario H |
| 8 | 1050 | 35 | Scenario A |
| 9 | 1210 | | Scenario B |
| 10 | 1400 | | Scenario C |
| 11 | 1620 | | Scenario D |
| 12 | 1870 | | Scenario E |
| 13 | 2150 | | Scenario F |
| 14 | 2490 | | Scenario G |
| 15 | 2870 | | Scenario H |
| 16 | 3740 | 30 | Scenario A |
| 17 | 8060 | | Scenario B |
| 18 | 12400 | | Scenario C |
| 19 | 16900 | | Scenario D |
| 20 | 21500 | | Scenario E |
| 21 | 26100 | | Scenario F |
| 22 | 30900 | | Scenario G |
| 23 | 36500 | | Scenario H |
| 24 | 42200 | 25 | Scenario A |
| 25 | 48700 | | Scenario B |
| 26 | 56200 | | Scenario C |
| 27 | 64900 | | Scenario D |
| 28 | 75000 | | Scenario E |
| 29 | 86600 | | Scenario F |
| 30 | 100000 | | Scenario G |
| 31 | 115000 | | Scenario H |

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The MAX20860A has 8 pre-defined scenarios as summarized in Table 4, which can be selected by a pin-strap resistor connected from PGM1 pin to AGND. For each scenario, the Switching Frequency, AMS option, Voltage Loop Gain and some other parameters can be selected. Refer to *Voltage Loop Gain* for information about how to select the voltage loop gain resistance (R_{VGA}) for optimized control loop performance. The configuration settings not offered in these 8 pre-defined scenarios can be selected by PMBus and stored in the device with the STORE_USER_ALL command (see *Nonvolatile PMBus Memory*).

Table 4. Pre-Defined Scenarios (TBD)

| SCENARIO # | V _{REF} AT STARTUP (V) | f _{SW} (kHz) | AMS OPTION | R _{VGA} (kΩ) | SOFT STARTUP SLEW RATE (V/ms) |
|------------|------------------------------------|-----------------------|------------|-----------------------|----------------------------------|
| A | 0.4 | 308 | Disabled | 37.3 | 0.5 |
| B | 0.5 | 308 | Enabled | 44.5 | 0.5 |
| C | 0.5 | 500 | Disabled | 37.3 | 0.5 |
| D | 0.5 | 500 | Enabled | 44.5 | 1 |
| E | 0.5 | 500 | Enabled | 62.3 | 1 |
| F | 0.8 | 800 | Disabled | 37.3 | 1 |
| G | 0.8 | 800 | Enabled | 44.5 | 1 |
| H | 0.8 | 1000 | Enabled | 62.3 | 1 |

PMBus Interface

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language. The MAX20860A supports PMBus interface to communicate with a host device. The device PMBus address is selected by a pin-strap resistor connected from PGM0 pin to AGND (see *Pin-Strap Programmability*). Table 5 shows the supported PMBus commands. For the detailed PMBus command definition and the application note, refer to *UGxxxx: MAX20860A/B PMBus Command Set User Guide*.

Table 5. Supported PMBus Commands

| COMMAND CODE | COMMAND NAME | DESCRIPTION | TYPE | DATA FORMAT | FACTORY VALUE |
|--------------|------------------|-----------------------------------------------------------------------------|-----------|-------------|---------------|
| 0x01 | OPERATION | Output enable/disable. | R/W Byte | Bit field | 0x8A |
| 0x02 | ON_OFF_CONFIG | EN pin & PMBus OPERATION command setting. | R/W Byte | Bit field | 0x1F |
| 0x03 | CLEAR_FAULTS | Clear any fault bits that have been set. | Send Byte | | N/A |
| 0x10 | WRITE_PROTECT | Level of protection provided by the device against accidental changes. | R/W Byte | Bit field | 0x20 |
| 0x15 | STORE_USER_ALL | Store user settings to PMBus nonvolatile memory. | Send Byte | | N/A |
| 0x16 | RESTORE_USER_ALL | Restore to latest user settings stored in the PMBus nonvolatile memory. | Send Byte | | N/A |
| 0x19 | CAPABILITY | Summary of PMBus optional communication protocols supported by this device. | R Byte | Bit field | 0xD4 |
| 0x1B | SMBALERT_MASK | Selectively mask the assertion of the ALERTB output. | R/W Block | Bit field | N/A |
| 0x20 | VOUT_MODE | Output voltage data format and mantissa exponent. | R Byte | Bit field | 0x16 |
| 0x21 | VOUT_COMMAND | Output/feedback voltage setpoint. | R/W Word | ULINEAR16 | Scenario |
| 0x24 | VOUT_MAX | Upper limit of output/feedback voltage setpoint. | R Word | ULINEAR16 | Scenario |

| | | | | | |
|------|------------------------|---------------------------------------------------|----------|-----------|----------------------------------|
| 0x27 | VOUT_TRANSITION_RATE | Transition slew rate for voltage transition. | R/W Word | LINEAR11 | Scenario |
| 0x29 | VOUT_SCALE_LOOP | Feedback voltage divider ratio. | R/W Word | LINEAR11 | N/A |
| 0x2B | VOUT_MIN | Lower limit of output/feedback voltage setpoint. | R Word | ULINEAR16 | Scenario |
| 0x33 | FREQUENCY_SWITCH | Switching frequency. | R/W Word | LINEAR11 | Scenario |
| 0x37 | INTERLEAVE | Phase shift from SYNC_IN to LX1 | R/W Word | Bit field | 0x0180 |
| 0x40 | VOUT_OV_FAULT_LIMIT | Output/feedback overvoltage threshold. | R Word | ULINEAR16 | Scenario |
| 0x41 | VOUT_OV_FAULT_RESPONSE | Output/feedback overvoltage response. | R/W Byte | Bit field | 0xB9 |
| 0x44 | VOUT_UV_FAULT_LIMIT | Output/feedback undervoltage threshold. | R Word | ULINEAR16 | Scenario |
| 0x45 | VOUT_UV_FAULT_RESPONSE | Output/feedback undervoltage response. | R/W Byte | Bit field | 0x39 |
| 0x46 | IOUT_OC_FAULT_LIMIT | Positive overcurrent fault threshold. | R/W Word | LINEAR11 | PGM1 |
| 0x47 | IOUT_OC_FAULT_RESPONSE | Positive overcurrent fault response. | R/W Byte | Bit field | 0xF9 |
| 0x4B | IOUT_UC_FAULT_LIMIT | Negative overcurrent fault threshold. | R Word | LINEAR11 | PGM1 |
| 0x4C | IOUT_UC_FAULT_RESPONSE | Negative overcurrent fault response. | R/W Byte | Bit field | 0xF9 |
| 0x4F | OT_FAULT_LIMIT | Overtemperature fault threshold. | R Word | LINEAR11 | 0xF26C |
| 0x50 | OT_FAULT_RESPONSE | Overtemperature fault response. | R/W Byte | Bit field | 0xF9 |
| 0x51 | OT_WARN_LIMIT | Overtemperature warning threshold. | R/W Word | LINEAR11 | 0xF1F4 |
| 0x55 | VIN_OV_FAULT_LIMIT | Input overvoltage threshold. | R Word | LINEAR11 | 0x00B2 |
| 0x56 | VIN_OV_FAULT_RESPONSE | Input overvoltage response. | R/W Byte | Bit field | 0x39 |
| 0x59 | VIN_UV_FAULT_LIMIT | Input undervoltage threshold. | R Word | LINEAR11 | 0xD853 (Dual-Phase Operation) |
| 0x5A | VIN_UV_FAULT_RESPONSE | Input undervoltage response. | R/W Byte | Bit field | 0xF9 |
| 0x78 | STATUS_BYTE | One byte summary of the unit's fault condition. | R Byte | Bit field | N/A |
| 0x79 | STATUS_WORD | Two bytes summary of the unit's fault condition. | R Word | Bit field | N/A |
| 0x7A | STATUS_VOUT | Output voltage fault and warning status. | R Byte | Bit field | N/A |
| 0x7B | STATUS_IOUT | Output current fault and warning status. | R Byte | Bit field | N/A |
| 0x7C | STATUS_INPUT | Input voltage fault and warning status. | R Byte | Bit field | N/A |
| 0x7D | STATUS_TEMPERATURE | IC junction temperature fault and warning status. | R Byte | Bit field | N/A |
| 0x7E | STATUS_CML | Communication fault and warning status. | R Byte | Bit field | N/A |
| 0x80 | STATUS_MFR_SPECIFIC | Manufacture specific fault and warning status. | R Byte | Bit field | N/A |
| 0x88 | READ_VIN | Input voltage telemetry. | R Word | LINEAR11 | N/A |

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| | | | | | |
|------|-----------------------|---------------------------------------------------------------|-----------|------------------|-------------|
| 0x8B | READ_VOUT | Feedback voltage telemetry. | R Word | ULINEAR16 | N/A |
| 0x8C | READ_IOUT | Output current telemetry. | R Word | LINEAR11 | N/A |
| 0x8D | READ_TEMPERATURE_1 | IC junction temperature telemetry. | R Word | LINEAR11 | N/A |
| 0x8E | READ_TEMPERATURE_2 | External power stage junction temperature telemetry. | R Word | LINEAR11 | N/A |
| 0x98 | PMBUS_REVISION | PMBus revision compliance. | R Byte | Bit field | 0x33 |
| 0xAD | IC_DEVICE_ID | Device root part number. | R Block | ASCII | "MAX20860A" |
| 0xAE | IC_DEVICE_REV | Device revision code. | R Block | ASCII | N/A |
| 0xD4 | RAMP_SLP | Slope compensation options. | R/W Byte | Bit field | Scenario |
| 0xD9 | SLV_FAULT_RESPONSE | External power stage fault response. | R/W Byte | Bit field | 0xC0 |
| 0xDA | LX_FAULT_RESPONSE | Switching node short fault response. | R Byte | Bit field | 0x80 |
| 0xDB | SNRP_FAULT_RESPONSE | Feedback SNSP/SNSN pin open fault response. | R/W Byte | Bit field | 0x80 |
| 0xDD | REMAINING_STORES | Number of remaining units of non-volatile memory | R Byte | Unsigned integer | 0x10 |
| 0xDE | DPLL_FLAGS | Status register of frequency synchronization | R Byte | Bit field | 0x04 |
| 0xE0 | STATUS_MFR_SPECIFIC_2 | Manufacture specific fault and warning status. | R Byte | Bit field | N/A |
| 0xE1 | STATUS_MFR_SPECIFIC_3 | Manufacture specific fault and warning status. | R Byte | Bit field | N/A |
| 0xE7 | RVGA_GAIN | Voltage loop gain resistance options. | R/W Byte | Bit field | Scenario |
| 0xE8 | ZERO_SEL | Voltage loop zero options. | R/W Byte | Bit field | 0x01 |
| 0xE9 | AMS_OPT | Advanced modulation scheme options. | R/W Byte | Bit field | Scenario |
| 0xEA | RESTORE_ADI_ALL | Restore all PMBus commands to the default values at power up. | Send Byte | | N/A |
| 0xF1 | ROCR | ROCR options for current balance | R/W Byte | Bit field | 0x10 |

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Nonvolatile PMBus Memory

The MAX20860A features nonvolatile memory for storage of PMBus command values, which is only guaranteed to retain values correctly when written while V_{DDH} is 10.8V to 16V. STORE_USER_ALL command is used to store user settings to PMBus nonvolatile memory. The stored configurations will override pin-strap settings where appropriate.

The MAX20860A has 16 total storage slots. At any time, the number of remaining storage slots can be determined by reading the REMAINING_STORES command. Refer to [UGxxxx: MAX20860A/B PMBus Command Set User Guide](#) for more information.

AVSBus Interface

The MAX20860A provides a high speed serial interface for Adaptive Voltage Scaling (AVSBus) of up to 50MHz clock frequency. Devices equipped with AVSBus controller capability can use the interface to enable fast V_{OUT} scaling as well as fast telemetry reading. All commands are readable at all times, but they cannot be written to unless the device is set to AVSBus control.

Reference Design Procedure

Output Voltage Sensing

The MAX20860A has a programmable feedback reference voltage (V_{REF}) from 0.4V to 0.8V. The default reference voltage is selected by the pre-defined scenarios ([Table 4](#)).

When the desired output voltage is higher than V_{REF} , it is required to use a resistor divider R_{FB1} and R_{FB2} to sense the output voltage (See *Simplified Application Circuit*). The feedback resistor divider ratio ($VOUT_SCALE_LOOP$) is given by the following equation:

$$VOUT_SCALE_LOOP = \frac{V_{REF}}{V_{OUT}} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

where:

V_{OUT} = Output voltage

V_{REF} = Reference voltage

R_{FB1} = Top divider resistor

R_{FB2} = Bottom divider resistor

The MAX20860A offers four standard $VOUT_SCALE_LOOP$ values which can be selected by PMBus $VOUT_SCALE_LOOP$ command. When one of these four standard ratios are selected, R_{FB1} and R_{FB2} must also be selected properly to match the selected ratio, so that the PMBus $VOUT_COMMAND$ matches 1:1 with the actual output voltage (V_{OUT}). The PMBus $VOUT_COMMAND$ can scale from 0.4V to 2.55V with 0.98mV resolution (refer to *UGxxx: MAX20860A/B PMBus Command Set User Guide*). The standard $VOUT_SCALE_LOOP$, R_{FB1} , R_{FB2} and $VOUT_COMMAND$ ranges are summarized in *Table 6*.

Table 6. Standard Feedback Resistor Divider Ratios

| PMBUS $VOUT_SCALE_LOOP$ | EXAMPLE R_{FB1} / R_{FB2} (E12 VALUES) | EXAMPLE R_{FB1} / R_{FB2} (E96 VALUES) | PMBUS $VOUT_COMMAND$ RANGE |
|------------------------------|---------------------------------------------|---------------------------------------------|--------------------------------|
| 0.3125 | 2.2kΩ / 1.0kΩ | 1.65kΩ / 0.75kΩ | 1.2803V – 2.5596V |
| 0.5000 | Any value $R_{FB1} = R_{FB2}$ | Any value $R_{FB1} = R_{FB2}$ | 0.7998V – 1.5996V |
| 0.6875 | 1.0kΩ / 2.2kΩ | 0.75kΩ / 1.65kΩ | 0.5820V – 1.1641V |
| 1.0000 | Direct remote sense | Direct remote sense | 0.4004V – 0.7998V |

When non-standard feedback resistor divider ratios are used, it is recommended to set PMBus $VOUT_SCALE_LOOP$ to 1.0. In this case the PMBus $VOUT_COMMAND$ sets the feedback reference voltage (V_{REF}) rather than the actual output voltage (V_{OUT}). It is recommended that the value R_{FB2} does not exceed 5kΩ.

Switching Frequency Selection

The MAX20860A offers a wide range of selectable switching frequencies from 308kHz to 2MHz. The selection of switching frequency can be optimized for different applications. Higher switching frequencies are recommended for applications prioritizing solution size, so that the value and size of output LC filter can be reduced. Lower switching frequencies are recommended for applications prioritizing efficiency and thermal dissipation, due to reduced switching losses. It is required that the frequency be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by the following equation:

$$f_{SW(MAX)} = \min \left\{ \frac{V_{OUT}}{t_{ON(MIN)} \times V_{DDH(MAX)}}, \frac{V_{DDH(MIN)} - V_{OUT}}{t_{OFF(MIN)} \times V_{DDH(MIN)}} \right\}$$

where:

$f_{SW(MAX)}$ = Maximum selectable switching frequency

$V_{DDH(MAX)}$ = Maximum input voltage

$V_{DDH(MIN)}$ = Minimum input voltage

$t_{ON(MIN)}$ = Minimum controllable on-time

$t_{OFF(MIN)}$ = Minimum controllable off-time

The MAX20860A internally has a slope compensation applied to the current loop during on-time to guarantee stability and improve noise immunity. To avoid the slope compensation saturating the current loop, it is required that the maximum on-time be limited by:

$$t_{ON(MAX)} = \frac{5pF \left[800mV \times \left(\frac{I_{OUT(MAX)}}{N} + \frac{I_{RIPPLE}}{2} \right) \times \frac{1.6\Omega}{125} \right]}{1.89\mu A}$$

where:

$t_{ON(MAX)}$ = Maximum on-time of the high-side MOSFET

$I_{OUT(MAX)}$ = Maximum load current

N = Number of phases

I_{RIPPLE} = Inductor current ripple peak-to-peak value

The minimum recommended switching frequency is calculated by the following equation:

$$f_{SW(MIN)} = \frac{V_{OUT}}{t_{ON(MAX)} \times V_{DDH(MIN)}}$$

where:

$f_{SW(MIN)}$ = Minimum selectable switching frequency

Due to system noise injection, even at steady state operation, typically the LX_ rising and falling edges would have some random jittering noise. The selection of the switching frequency (f_{SW}) should take into consideration the jittering and be higher than $f_{SW(MIN)}$ and lower than $f_{SW(MAX)}$. To improve the LX_ jittering, it is recommended to use smaller inductor values and lower voltage loop gain, to minimize the noise sensitivity.

Output Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitance needed to maintain transient tolerance. Typically, the output inductor is selected so that the inductor current ripple is 20% to 50% of the maximum load current per-phase for optimized performance. To improve current loop noise immunity, it is recommended that the inductor current ripple is at least 4A. For conventional discrete inductors the recommended inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{I_{RIPPLE} \times f_{SW} \times V_{DDH}}$$

where:

V_{DDH} = Input voltage

I_{RIPPLE} = Inductor current ripple peak-to-peak value

Coupled inductors can be used with the MAX20860A for optimized solution size, efficiency and load transient performance. For coupled inductors driven with duty cycle $\leq 1/N$, the recommended inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}}{I_{RIPPLE} \times f_{SW}} \left(\frac{1}{N} - \frac{V_{OUT}}{V_{DDH}} \right)$$

The inductor should also be selected so that maximum load current delivery can be guaranteed by the selected POCP threshold. The MAX20860A offers 4 POCP thresholds (40A, 35A, 30A and 25A for each phase), which can be selected by PGM1 pin (see [Pin-Strap Programmability](#)). Due to a deglitch delay from POCP comparator tripping to high-side MOSFET turning off, for a specific application use case, the adjusted POCP threshold should take into consideration the inductor value, input voltage and output voltage, which can be calculated by the following equation:

$$POCP_{ADJUST} = POCP + \frac{(V_{DDH} - V_{OUT}) \times t_{POCP}}{L}$$

where:

$POCP_{ADJUST}$ = Adjusted POCP threshold

POCP = POCP level specified in the EC table

t_{POCP} = POCP deglitch delay (51ns typical)

It needs to be verified that the peak inductor current in normal operation does not exceed the minimum adjusted POCP threshold:

$$\frac{I_{OUT(MAX)}}{N} + \frac{I_{RIPPLE}}{2} < POCP_{ADJUST(MIN)}$$

where:

$POCP_{ADJUST(MIN)}$ = Minimum adjusted POCP threshold, calculated with minimum value of the POCP threshold

Table 7 shows some suitable inductor part numbers which are verified on the MAX20860A evaluation kit to offer optimal performance.

Table 7. Recommended Inductors

| COMPANY | TYPE | VALUE (nH) | I_{SAT} (A) | R_{DC} (mΩ) | FOOTPRINT PER PHASE (mm) | HEIGHT (mm) | PART NUMBER |
|---------|----------|------------|---------------|---------------|--------------------------|-------------|-------------------|
| Eaton | Coupled | 100 | 56 | 0.45 | 11.5 × 6.0 | 8.0 | CL1208-x-100TR-R |
| Eaton | Coupled | 50 | 70 | 0.25 | 8.0 × 6.0 | 6.0 | CL0806V1-n-R050-R |
| Eaton | Discrete | 180 | 70 | 0.17 | 10.8 × 8.0 | 8.0 | FP1008R5-R180-R |
| Eaton | Discrete | 220 | 58 | 0.17 | 10.8 × 8.0 | 8.0 | FP1008R5-R220-R |
| Eaton | Discrete | 270 | 44 | 0.17 | 10.8 × 8.0 | 8.0 | FP1008R5-R270-R |
| Würth | Discrete | 330 | 62.5 | 0.165 | 14.0 × 13.0 | 9.0 | 744309033 |
| Würth | Discrete | 470 | 40.5 | 0.165 | 14.0 × 13.0 | 9.0 | 744309047 |

Output Capacitor Selection

One major factor in determining the total required output capacitance is the output voltage ripple. To meet the output voltage ripple requirement, the minimum output capacitance should satisfy the following equation:

$$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \times N \times f_{SW} \times (V_{OUTRIPPLE} - ESR \times I_{RIPPLE})}$$

where:

$V_{OUTRIPPLE}$ = Maximum allowed output voltage ripple

ESR = ESR of output capacitors

The other important factors in determining the total required output capacitance are the maximum allowable output voltage overshoot and undershoot during load transients. For a given loading or unloading current step, the minimum required output capacitance should also satisfy the following equation:

$$C_{OUT} \geq \text{MAX} \left\{ \frac{\left(\frac{\Delta I}{N} + \frac{I_{RIPPLE}}{2} \right)^2 \times L}{2 \times \Delta V_{OUT} \times (V_{DDH} - V_{OUT})}, \frac{\left(\frac{\Delta I}{N} + \frac{I_{RIPPLE}}{2} \right)^2 \times L}{2 \times \Delta V_{OUT} \times V_{OUT}} \right\}$$

where:

C_{OUT} = Output capacitance

ΔI = Loading or unloading current step

ΔV_{OUT} = Maximum allowed output voltage undershoot or overshoot

Input Capacitor Selection

The selection of input capacitance is determined by the requirement of input voltage ripple. The minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \frac{I_{OUT(MAX)} \times V_{OUT}}{N \times f_{SW} \times V_{DDH} \times V_{INPP}}$$

where:

C_{IN} = Input capacitance

V_{INPP} = Peak-to-peak input voltage ripple

Besides the minimum required input capacitance, it is recommended to also place a 0.1μF and a 1μF high frequency decoupling capacitors next to each of the $V_{DDH_}$ pin, to suppress the high frequency switching noises.

Voltage Loop Gain

For stability purpose, it is recommended that the voltage loop bandwidth (BW) be lower than 1/5 of the switching frequency. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The voltage loop BW can be estimated by the following equation:

$$BW = \frac{N \times \frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 4m\Omega \times C_{OUT}}$$

where:

R_{VGA} = The voltage loop gain resistance, which is set by the scenario selected ([Table 4](#))

PCB Layout Guidelines

- For electrical and thermal reasons, the second layer from the top and bottom of the PCB should be reserved for power ground (PGND) planes.
- The input decoupling capacitor should be located the closest to the IC and no more than 40mils from the $V_{DDH_}$ pins.
- The V_{CC} decoupling capacitors should be connected to PGND and placed as close as possible to $V_{CC_}$ pins.
- An analog ground copper polygon or island should be used to connect all analog control-signal grounds. This “quiet” analog ground copper polygon or island should be connected to the PGND through a single connection close to AGND pin. The analog ground can be used as a shield and ground reference for the control signals. The DGND pin should also be connected to this analog ground copper polygon.
- The AVDD decoupling capacitors should be connected to AGND and placed as close as possible to AVDD pin.
- The DVDD decoupling capacitors should be connected to DGND and placed as close as possible to DVDD pin.
- The boost capacitors should be placed as close as possible to $LX_$ and $BST_$ pins, on the same side of the PCB with the IC.
- The feedback resistor-divider and optional external compensation network should be placed close to the IC to minimize the noise injection.
- Output voltage should be sensed with differential remote sense lines routed directly from an output capacitor from the load point, shielded by ground plane and be kept away from switching nodes and the inductors.
- Sensitive signals traces including SCL, SDA, ALERTB, SYNC_IN, SYNC_OUT, PWM_, CS_ and TS_FAULTB should be routed away from the noisy switching nodes and the inductors. It is recommended that these signals are shielded by ground planes.
- The high-speed AVSBus communication lines AVS_CLK, AVS_SDI and AVS_SDO should be routed in parallel to have matched impedance, away from the noisy switching nodes and the inductors. It is recommended that these signals are shielded by ground planes.
- Multiple vias are recommended for all paths that carry high currents and for heat dissipation.
- The input capacitors and output inductors should be placed near the IC and the traces to the components should be kept as short and wide as possible to minimize parasitic inductance and resistance.

Ordering Information

| Part Number | Temp Range | Pin-Package |
|-------------|------------|-------------|
|-------------|------------|-------------|

| | | |
|----------------|-----------------|-----------|
| MAX20860AAFX+ | -40°C to +125°C | 36 FC2QFN |
| MAX20860AAFX+T | -40°C to +125°C | 36 FC2QFN |

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

*Future product – contact factory for availability.

PRELIMINARY

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|------------------|-------------|------------------|
| 0 | 08/23 | Preliminary | — |

PRELIMINARY