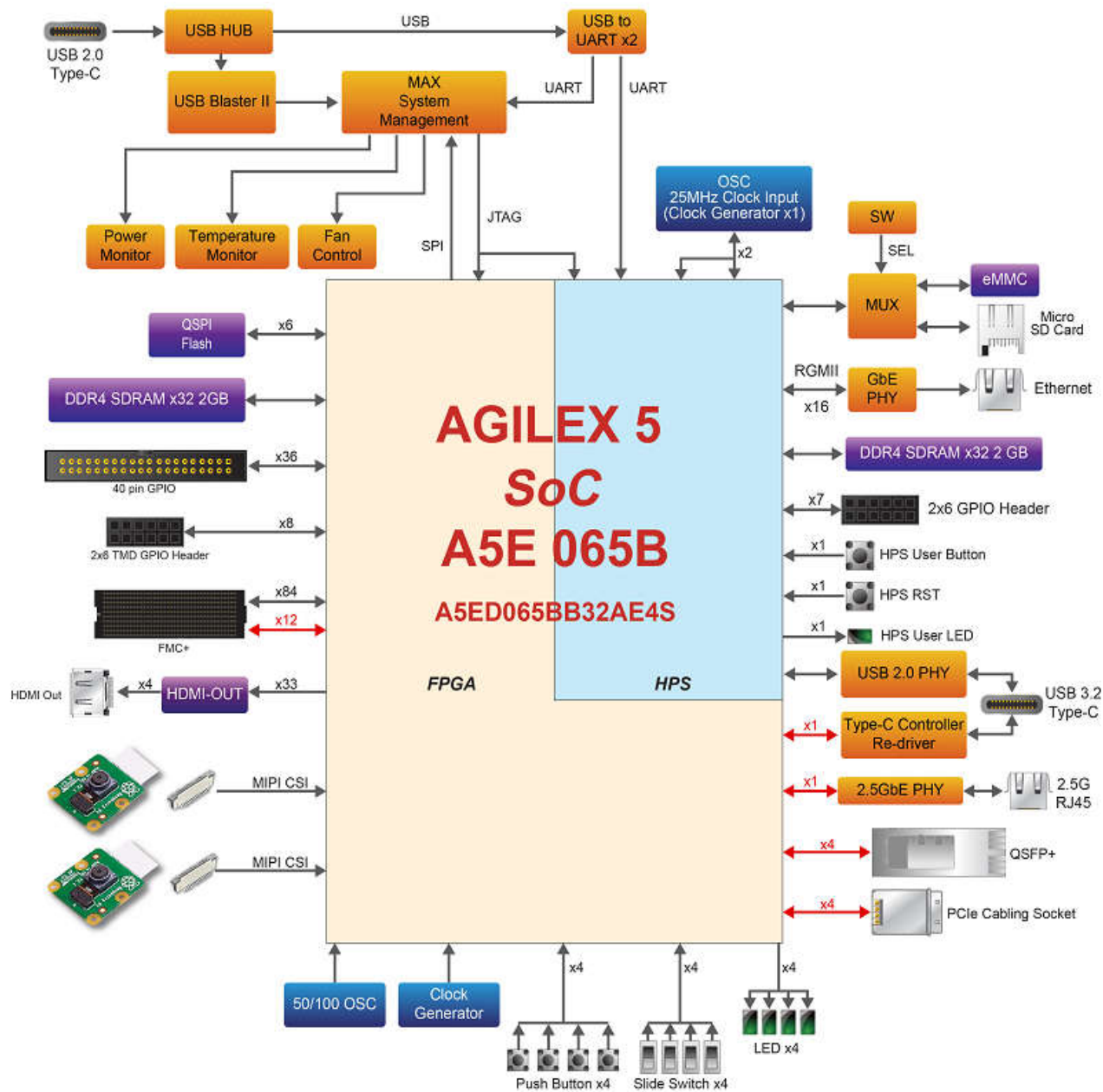
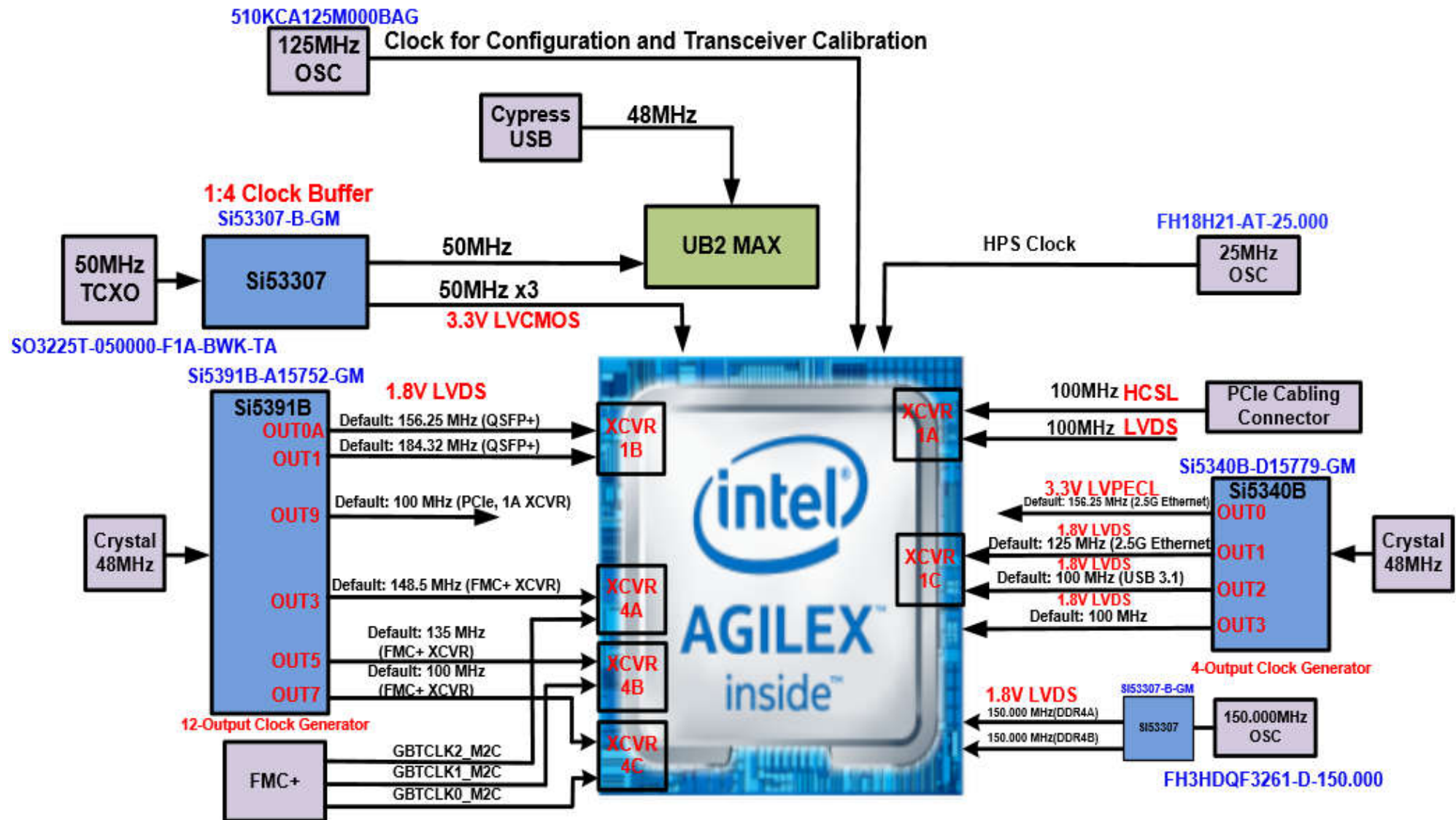


# Block Diagram



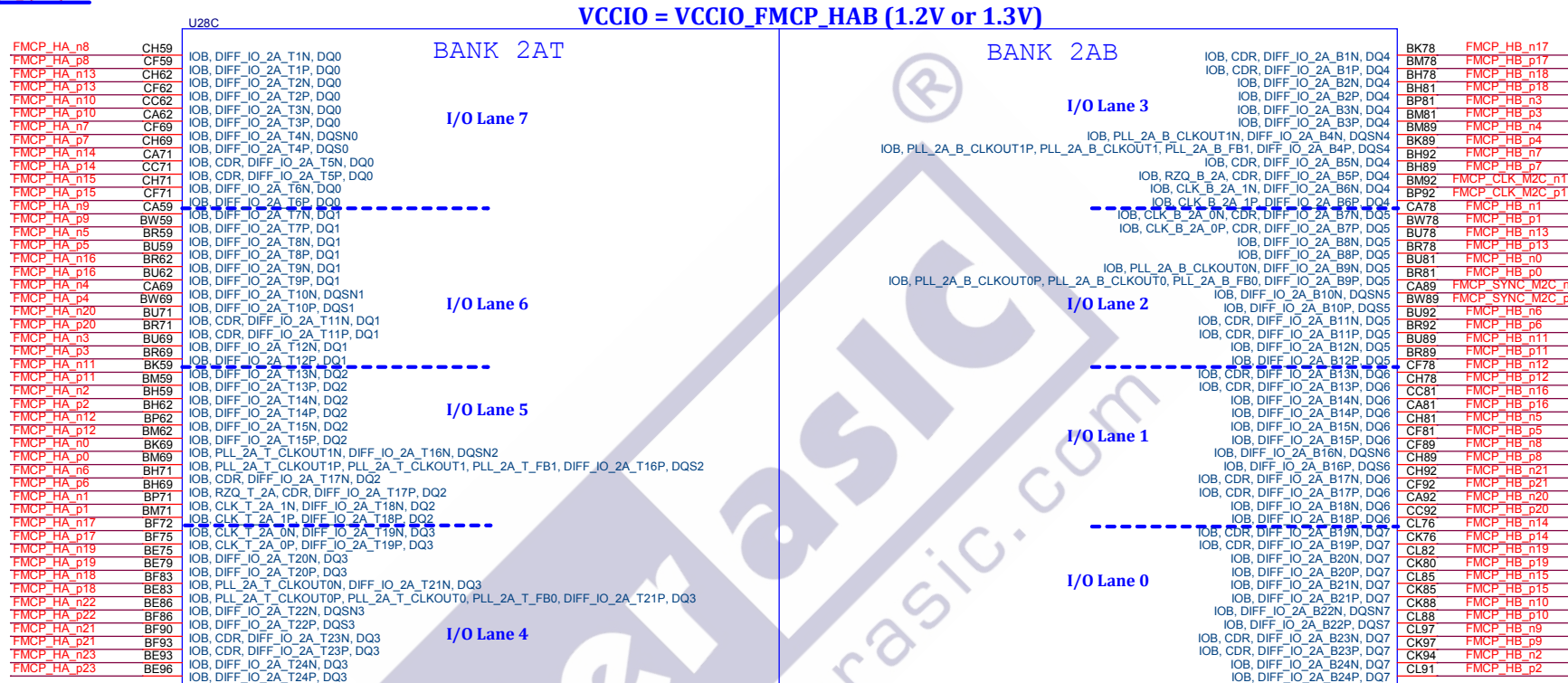
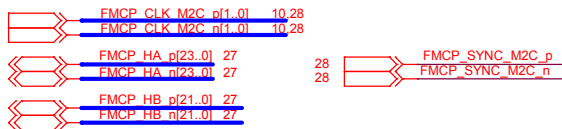


# Clock Tree

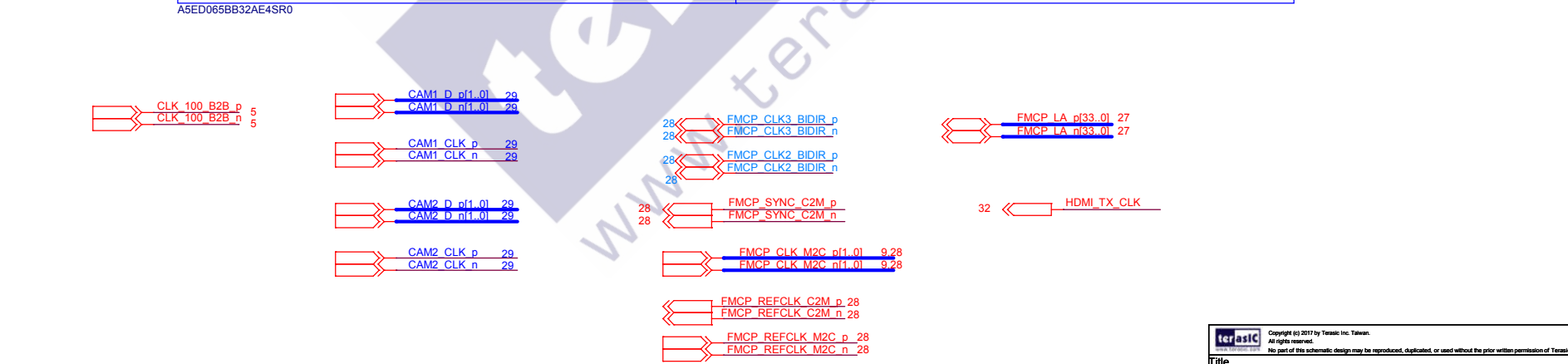
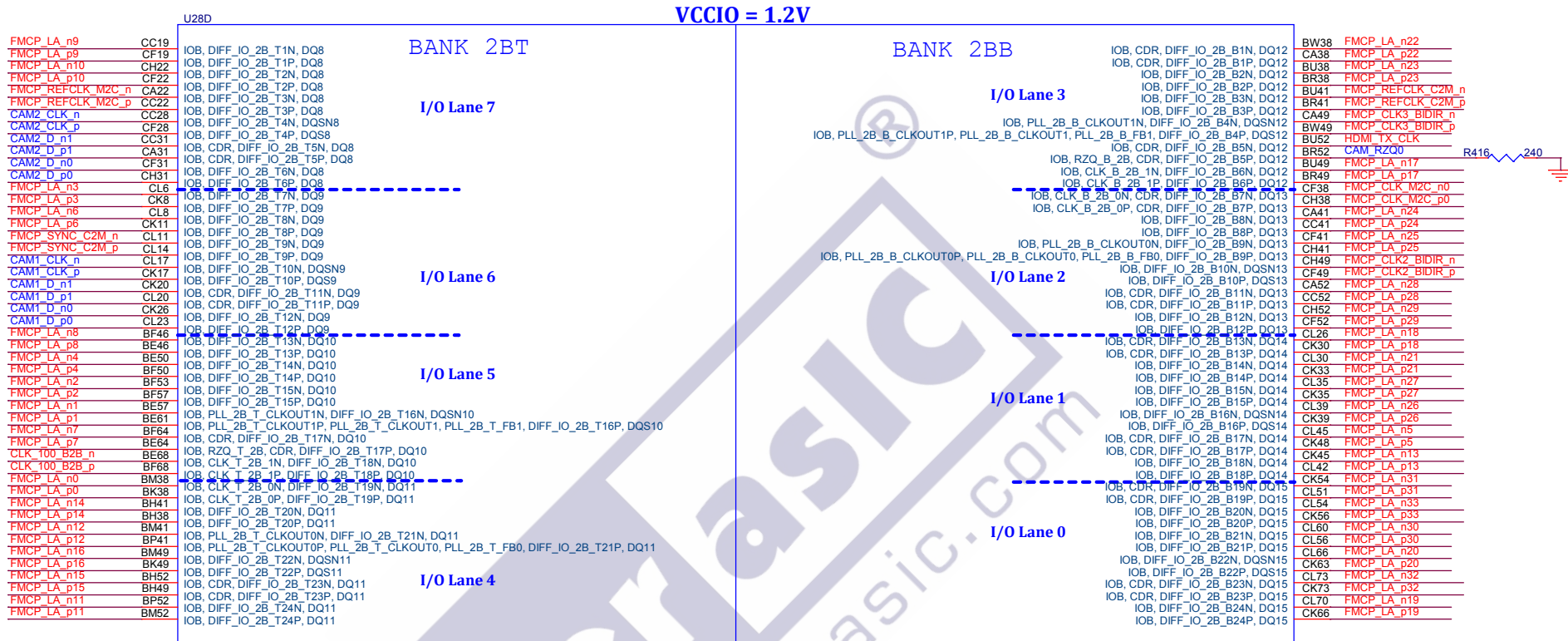


|  |                       |               |
|--|-----------------------|---------------|
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| Title  |                       |               |
| Atum A5  |                       |               |
| Size   | Document Number       | Rev           |
| B  | Clock Tree            | A             |
| Date:  | Monday, June 03, 2024 | Sheet 3 of 49 |



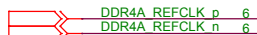
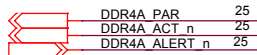
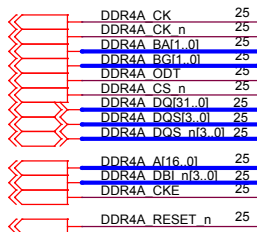








## DDR4-A



RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14

|              |       |
|--------------|-------|
| DDR4A_DQ31   | D84   |
| DDR4A_DQ29   | F84   |
| DDR4A_DQ30   | M87   |
| DDR4A_DQ26   | K87   |
| DDR4A_DBI_n3 | X F87 |
| DDR4A_DQS_n3 | D95   |
| DDR4A_DQ33   | F95   |
| DDR4A_DQ27   | K98   |
| DDR4A_DQ25   | M98   |
| DDR4A_DQ28   | F98   |
| DDR4A_DQ24   | H98   |
| DDR4A_DQ23   | P84   |
| DDR4A_DQ22   | T84   |
| DDR4A_DQ21   | M84   |
| DDR4A_DQ20   | K84   |
| DDR4A_DBI_n2 | X V87 |
| DDR4A_DQS_n2 | M95   |
| DDR4A_DQ32   | K95   |
| DDR4A_DQ19   | T95   |
| DDR4A_DQ18   | P95   |
| DDR4A_DQ17   | T98   |
| DDR4A_DQ16   | V98   |
| DDR4A_DQ15   | Y84   |
| DDR4A_DQ14   | Y87   |
| DDR4A_DQ13   | Y95   |
| DDR4A_DQ9    | Y98   |
| DDR4A_DBI_n1 | AC86  |
| DDR4A_DQS_n1 | AC90  |
| DDR4A_DQ31   | AC93  |
| DDR4A_DQ12   | AC96  |
| DDR4A_DQ10   | AC100 |
| DDR4A_DQ11   | AG104 |
| DDR4A_DQ8    | AG100 |

U28E

## BANK 3AT

I/O Lane 7

I/O Lane 6

I/O Lane 5

I/O Lane 4

IOB, DIFF\_IO\_3A\_T1N, DQ16  
IOB, DIFF\_IO\_3A\_T1P, DQ16  
IOB, DIFF\_IO\_3A\_T2N, DQ16  
IOB, DIFF\_IO\_3A\_T2P, DQ16  
IOB, DIFF\_IO\_3A\_T3N, DQ16  
IOB, DIFF\_IO\_3A\_T3P, DQ16, AVST\_READY  
IOB, DIFF\_IO\_3A\_T4N, DQSN16  
IOB, DIFF\_IO\_3A\_T4P, DQS16  
IOB, CDR, DIFF\_IO\_3A\_T5N, DQ16  
IOB, CDR, DIFF\_IO\_3A\_T5P, DQ16  
IOB, DIFF\_IO\_3A\_T6N, DQ16  
IOB, DIFF\_IO\_3A\_T6P, DQ16  
IOB, DIFF\_IO\_3A\_T7N, DQ17, AVST\_DATA10  
IOB, DIFF\_IO\_3A\_T7P, DQ17, AVST\_DATA9  
IOB, DIFF\_IO\_3A\_T8N, DQ17, AVST\_DATA8  
IOB, DIFF\_IO\_3A\_T8P, DQ17, AVST\_VALID  
IOB, DIFF\_IO\_3A\_T9N, DQ17, AVST\_DATA7  
IOB, DIFF\_IO\_3A\_T9P, DQ17, AVST\_DATA6  
IOB, DIFF\_IO\_3A\_T10N, DQSN17, AVST\_DATA5  
IOB, DIFF\_IO\_3A\_T10P, DQS17, AVST\_DATA4  
IOB, CDR, DIFF\_IO\_3A\_T11N, DQ17, AVST\_DATA3  
IOB, CDR, DIFF\_IO\_3A\_T11P, DQ17, AVST\_DATA2  
IOB, DIFF\_IO\_3A\_T12N, DQ17, AVST\_DATA1  
IOB, DIFF\_IO\_3A\_T12P, DQ17, AVST\_DATA0  
IOB, DIFF\_IO\_3A\_T13N, DQ18  
IOB, DIFF\_IO\_3A\_T13P, DQ18  
IOB, DIFF\_IO\_3A\_T14N, DQ18  
IOB, DIFF\_IO\_3A\_T14P, DQ18  
IOB, DIFF\_IO\_3A\_T15N, DQ18  
IOB, DIFF\_IO\_3A\_T15P, DQ18  
IOB, PLL\_3A\_T\_CLKOUT1N, DIFF\_IO\_3A\_T16N, DQSN18  
IOB, PLL\_3A\_T\_CLKOUT1P, PLL\_3A\_T\_CLKOUT1, PLL\_3A\_T\_FB1, DIFF\_IO\_3A\_T16P, DQS18  
IOB, CDR, DIFF\_IO\_3A\_T17N, DQ18  
IOB, RZQ\_T\_3A, CDR, DIFF\_IO\_3A\_T17P, DQ18  
IOB, CLK\_T\_3A\_1N, DIFF\_IO\_3A\_T18N, DQ18  
IOB, CLK\_T\_3A\_1P, DIFF\_IO\_3A\_T18P, DQ18  
IOB, CLK\_T\_3A\_0N, DIFF\_IO\_3A\_T19N, DQ19  
IOB, CLK\_T\_3A\_0P, DIFF\_IO\_3A\_T19P, DQ19  
IOB, DIFF\_IO\_3A\_T20N, DQ19  
IOB, DIFF\_IO\_3A\_T20P, DQ19  
IOB, PLL\_3A\_T\_CLKOUT0N, DIFF\_IO\_3A\_T21N, DQ19  
IOB, PLL\_3A\_T\_CLKOUT0P, PLL\_3A\_T\_CLKOUT0, PLL\_3A\_T\_FB0, DIFF\_IO\_3A\_T21P, DQ19  
IOB, DIFF\_IO\_3A\_T22N, DQSN19, AVST\_CLK  
IOB, DIFF\_IO\_3A\_T22P, DQS19, AVST\_DATA15  
IOB, CDR, DIFF\_IO\_3A\_T23N, DQ19, AVST\_DATA14  
IOB, CDR, DIFF\_IO\_3A\_T23P, DQ19, AVST\_DATA13  
IOB, DIFF\_IO\_3A\_T24N, DQ19, AVST\_DATA12  
IOB, DIFF\_IO\_3A\_T24P, DQ19, AVST\_DATA11

VCCIO = 1.2V

## BANK 3AB

I/O Lane 3

I/O Lane 2


I/O Lane 1

I/O Lane 0

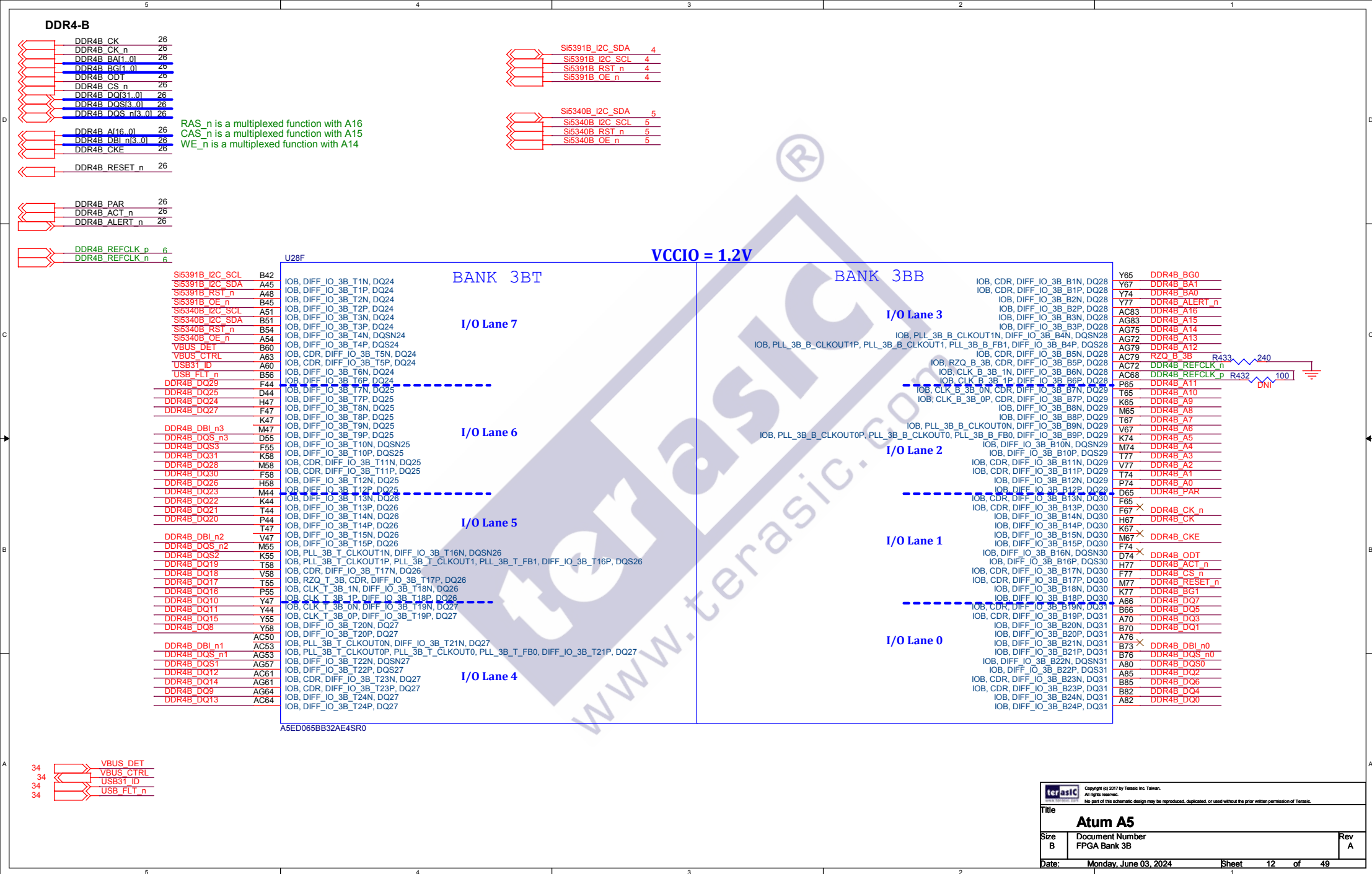
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IOB, DIFF\_IO\_3A\_B2P, DQ20  
IOB, DIFF\_IO\_3A\_B3N, DQ20  
IOB, DIFF\_IO\_3A\_B3P, DQ20  
IOB, PLL\_3A\_B\_CLKOUT1N, DIFF\_IO\_3A\_B4N, DQSN20  
IOB, PLL\_3A\_B\_CLKOUT1P, PLL\_3A\_B\_CLKOUT1, PLL\_3A\_B\_FB1, DIFF\_IO\_3A\_B4P, DQS20  
IOB, CDR, DIFF\_IO\_3A\_B5N, DQ20  
IOB, RZQ\_B\_3A, CDR, DIFF\_IO\_3A\_B5P, DQ20  
IOB, CLK\_B\_3A\_1N, DIFF\_IO\_3A\_B6N, DQ20  
IOB, CLK\_B\_3A\_1P, DIFF\_IO\_3A\_B6P, DQ20  
IOB, CLK\_B\_3A\_0N, CDR, DIFF\_IO\_3A\_B7N, DQ21  
IOB, CLK\_B\_3A\_0P, CDR, DIFF\_IO\_3A\_B7P, DQ21  
IOB, DIFF\_IO\_3A\_B8N, DQ21  
IOB, DIFF\_IO\_3A\_B8P, DQ21  
IOB, PLL\_3A\_B\_CLKOUT0N, DIFF\_IO\_3A\_B9N, DQ21  
IOB, PLL\_3A\_B\_CLKOUT0P, PLL\_3A\_B\_CLKOUT0, PLL\_3A\_B\_FB0, DIFF\_IO\_3A\_B9P, DQ21  
IOB, DIFF\_IO\_3A\_B10N, DQSN21  
IOB, DIFF\_IO\_3A\_B10P, DQS21  
IOB, CDR, DIFF\_IO\_3A\_B11N, DQ21  
IOB, CDR, DIFF\_IO\_3A\_B11P, DQ21  
IOB, DIFF\_IO\_3A\_B12N, DQ21  
IOB, DIFF\_IO\_3A\_B12P, DQ21  
IOB, CDR, DIFF\_IO\_3A\_B13N, DQ22  
IOB, CDR, DIFF\_IO\_3A\_B13P, DQ22  
IOB, DIFF\_IO\_3A\_B14N, DQ22  
IOB, DIFF\_IO\_3A\_B14P, DQ22  
IOB, DIFF\_IO\_3A\_B15N, DQ22  
IOB, DIFF\_IO\_3A\_B15P, DQ22  
IOB, DIFF\_IO\_3A\_B16N, DQSN22  
IOB, DIFF\_IO\_3A\_B16P, DQS22  
IOB, CDR, DIFF\_IO\_3A\_B17N, DQ22  
IOB, CDR, DIFF\_IO\_3A\_B17P, DQ22  
IOB, DIFF\_IO\_3A\_B18N, DQ22  
IOB, DIFF\_IO\_3A\_B18P, DQ22  
IOB, CDR, DIFF\_IO\_3A\_B19N, DQ23  
IOB, CDR, DIFF\_IO\_3A\_B19P, DQ23  
IOB, DIFF\_IO\_3A\_B20N, DQ23  
IOB, DIFF\_IO\_3A\_B20P, DQ23  
IOB, DIFF\_IO\_3A\_B21N, DQ23  
IOB, DIFF\_IO\_3A\_B21P, DQ23  
IOB, DIFF\_IO\_3A\_B22N, DQSN23  
IOB, DIFF\_IO\_3A\_B22P, DQS23  
IOB, CDR, DIFF\_IO\_3A\_B23N, DQ23  
IOB, CDR, DIFF\_IO\_3A\_B23P, DQ23  
IOB, DIFF\_IO\_3A\_B24N, DQ23  
IOB, DIFF\_IO\_3A\_B24P, DQ23

|       |                |
|-------|----------------|
| AB105 | DDR4A_BG0      |
| Y105  | DDR4A_BA1      |
| AB108 | DDR4A_BA0      |
| Y108  | DDR4A_ALERT_n  |
| AK104 | DDR4A_A16      |
| AK107 | DDR4A_A15      |
| AB114 | DDR4A_A14      |
| Y114  | DDR4A_A13      |
| AG111 | DDR4A_A12      |
| AK111 | RZQ_B_3A_R429  |
| Y117  | DDR4A_REFCLK_n |
| AB117 | DDR4A_REFCLK_p |
| K105  | DDR4A_A11      |
| M105  | DDR4A_A10      |
| P105  | DDR4A_A9       |
| T105  | DDR4A_A8       |
| F108  | DDR4A_A7       |
| K114  | DDR4A_A5       |
| M114  | DDR4A_A4       |
| T117  | DDR4A_A3       |
| P117  | DDR4A_A2       |
| V114  | DDR4A_A1       |
| T114  | DDR4A_A0       |
| K108  | DDR4A_PAR      |
| M108  |                |
| F108  | DDR4A_CK_n     |
| H108  | DDR4A_CK       |
| D105  |                |
| F105  | DDR4A_CKE      |
| D114  |                |
| F114  | DDR4A_ODT      |
| M117  | DDR4A_ACT_n    |
| K117  | DDR4A_CS_n     |
| H117  | DDR4A_RESET_n  |
| F117  | DDR4A_BG1      |
| A113  | DDR4A_DQ7      |
| B113  | DDR4A_DQ5      |
| A116  | DDR4A_DQ1      |
| B116  | DDR4A_DQ3      |
| A122  |                |
| B119  | DDR4A_DBI_n0   |
| A125  | DDR4A_DQS_n0   |
| B122  | DDR4A_DQS0     |
| A130  | DDR4A_DQ4      |
| B130  | DDR4A_DQ2      |
| A128  | DDR4A_DQ6      |
| B128  | DDR4A_DQ0      |

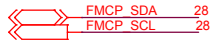
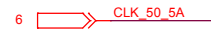
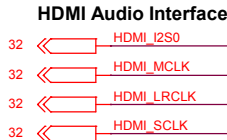
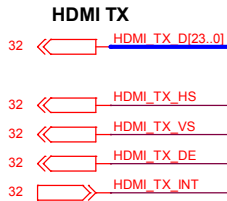
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|--|-----------------------|----------------|
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| Title  |                       |                |
| Atum A5  |                       |                |
| Size   | Document Number       | Rev            |
| B  | FPGA Bank 3A          | A              |
| Date:  | Monday, June 03, 2024 | Sheet 11 of 49 |









U28G

VCCIO = 3.3V

|             |       |
|-------------|-------|
| HDMI_TX_D0  | CD134 |
| HDMI_TX_D1  | CD135 |
| HDMI_TX_D2  | CG134 |
| HDMI_TX_D3  | CG135 |
| HDMI_TX_D4  | CH132 |
| HDMI_TX_D5  | CF132 |
| HDMI_TX_D6  | CF128 |
| HDMI_TX_D7  | CK134 |
| CLK_50_5A   | CH128 |
| HDMI_TX_D8  | CL125 |
| HDMI_TX_D9  | CF121 |
| HDMI_TX_D10 | CF118 |
| HDMI_TX_D11 | BU118 |
| HDMI_TX_D12 | BR118 |
| HDMI_TX_D13 | CA118 |
| HDMI_TX_D14 | BW118 |
| HDMI_TX_D15 | CL128 |
| HDMI_TX_D16 | CL130 |
| HDMI_TX_D17 | CK125 |
| HDMI_TX_D18 | CK128 |

|  |
|--|
| HVIO_5A_1, SYSPLLREFCLK_L1A_0, TXCLK1, DATA_CTRL1          |
| HVIO_5A_2, SYSPLLREFCLK_L1A_1, TXCLK2, DATA_CTRL2          |
| HVIO_5A_3, SYSPLLREFCLK_L1B_0, TXCLK3, DATA_CTRL3          |
| HVIO_5A_4, SYSPLLREFCLK_L1B_1, TXCLK4, DATA_CTRL4          |
| HVIO_5A_5, PIN_PERST_N_CVP_L1A_0, TXCLK5, DATA_CTRL5       |
| HVIO_5A_6, PIN_PERST_N_CVP_L1B_0, TXCLK6, DATA_CTRL6       |
| HVIO_5A_7, PIN_PERST_N_CVP_L1C_0, TXCLK7, DATA_CTRL7       |
| HVIO_5A_8, TXCLK8, DATA_CTRL8                              |
| HVIO_5A_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9          |
| HVIO_5A_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10       |
| HVIO_5A_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11 |
| HVIO_5A_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12 |
| HVIO_5A_13, TXCLK13, DATA_CTRL13                           |
| HVIO_5A_14, TXCLK14, DATA_CTRL14                           |
| HVIO_5A_15, TXCLK15, DATA_CTRL15                           |
| HVIO_5A_16, TXCLK16, DATA_CTRL16                           |
| HVIO_5A_17, TXCLK17, DATA_CTRL17                           |
| HVIO_5A_18, TXCLK18, DATA_CTRL18                           |
| HVIO_5A_19, SYSPLLREFCLK_L1C_0, TXCLK19, DATA_CTRL19       |
| HVIO_5A_20, TXCLK20, DATA_CTRL20                           |

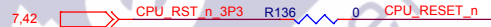
BANK 5A

|  |
|--|
| HVIO_5B_1, SYSPLLREFCLK_L1A_2, TXCLK1, DATA_CTRL1          |
| HVIO_5B_2, SYSPLLREFCLK_L1A_3, TXCLK2, DATA_CTRL2          |
| HVIO_5B_3, SYSPLLREFCLK_L1B_2, TXCLK3, DATA_CTRL3          |
| HVIO_5B_4, SYSPLLREFCLK_L1B_3, TXCLK4, DATA_CTRL4          |
| HVIO_5B_5, PIN_PERST_N_CVP_L1A_1, TXCLK5, DATA_CTRL5       |
| HVIO_5B_6, PIN_PERST_N_CVP_L1B_1, TXCLK6, DATA_CTRL6       |
| HVIO_5B_7, PIN_PERST_N_CVP_L1C_1, TXCLK7, DATA_CTRL7       |
| HVIO_5B_8, TXCLK8, DATA_CTRL8                              |
| HVIO_5B_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9          |
| HVIO_5B_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10       |
| HVIO_5B_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11 |
| HVIO_5B_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12 |
| HVIO_5B_13, TXCLK13, DATA_CTRL13                           |
| HVIO_5B_14, TXCLK14, DATA_CTRL14                           |
| HVIO_5B_15, TXCLK15, DATA_CTRL15                           |
| HVIO_5B_16, TXCLK16, DATA_CTRL16                           |
| HVIO_5B_17, TXCLK17, DATA_CTRL17                           |
| HVIO_5B_18, TXCLK18, DATA_CTRL18                           |
| HVIO_5B_19, SYSPLLREFCLK_L1C_1, TXCLK19, DATA_CTRL19       |
| HVIO_5B_20, TXCLK20, DATA_CTRL20                           |

BANK 5B

|                    |
|--------------------|
| BF111 HDMI_TX_D19  |
| BH109 HDMI_TX_D20  |
| BE115 HDMI_TX_D21  |
| BF115 HDMI_TX_D22  |
| BF107 PCIE_PERST_n |
| BU109 HDMI_TX_D23  |
| BF104 CPU_RESET_n  |
| BR109 HDMI_TX_HS   |
| BE107 HDMI_TX_VS   |
| BK109 HDMI_TX_DE   |
| BE111 HDMI_TX_INT  |
| BM109 HDMI_I2C_SDA |
| BR112 HDMI_I2C_SCL |
| BK118 HDMI_I2S0    |
| BM118 HDMI_MCLK    |
| BP112 HDMI_LRCLK   |
| BM112 HDMI_SCLK    |
| BK112 FMCP_SDA     |
| BH118 FMCP_SCL     |
| BF120 LED0         |

A5ED065BB32AE4SR0





GPIO

GPIO[35..0] 30

6 CLK\_50\_6A

SW[3..0] 15..42

FMCP\_RES0 28

U28H

VCCIO = 3.3V

GPIO3 BU28  
GPIO25 BP31  
GPIO17 BR28  
GPIO4 BR31  
GPIO1 BU31  
GPIO18 BM28  
GPIO8 BW28  
GPIO19 BM31  
GPIO0 BK31  
CLK\_50\_6A BP22  
GPIO20 BK28  
GPIO11 BR22  
GPIO28 CH12  
GPIO10 BU22  
GPIO9 BW19  
GPIO21 SH28  
GPIO13 BM22  
GPIO29 CF12  
GPIO14 BK19  
GPIO27 CF9

HVIO\_6A\_1, SYSPLLREFCLK\_R4A\_0, TXCLK1, DATA\_CTRL1  
HVIO\_6A\_2, SYSPLLREFCLK\_R4A\_1, TXCLK2, DATA\_CTRL2  
HVIO\_6A\_3, SYSPLLREFCLK\_R4B\_0, TXCLK3, DATA\_CTRL3  
HVIO\_6A\_4, SYSPLLREFCLK\_R4B\_1, TXCLK4, DATA\_CTRL4  
HVIO\_6A\_5, PIN\_PERST\_N\_R4A\_0, TXCLK5, DATA\_CTRL5  
HVIO\_6A\_6, PIN\_PERST\_N\_R4B\_0, TXCLK6, DATA\_CTRL6  
HVIO\_6A\_7, PIN\_PERST\_N\_R4C\_0, TXCLK7, DATA\_CTRL7  
HVIO\_6A\_8, TXCLK8, DATA\_CTRL8  
HVIO\_6A\_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA\_CTRL9  
HVIO\_6A\_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA\_CTRL10  
HVIO\_6A\_11, SOURCE\_SYNC\_CLK1, TXCLK11, RXCLK3, DATA\_CTRL11  
HVIO\_6A\_12, SOURCE\_SYNC\_CLK2, TXCLK12, RXCLK4, DATA\_CTRL12  
HVIO\_6A\_13, TXCLK13, DATA\_CTRL13  
HVIO\_6A\_14, TXCLK14, DATA\_CTRL14  
HVIO\_6A\_15, TXCLK15, DATA\_CTRL15  
HVIO\_6A\_16, TXCLK16, DATA\_CTRL16  
HVIO\_6A\_17, TXCLK17, DATA\_CTRL17  
HVIO\_6A\_18, TXCLK18, DATA\_CTRL18  
HVIO\_6A\_19, SYSPLLREFCLK\_R4C\_0, TXCLK19, DATA\_CTRL19  
HVIO\_6A\_20, TXCLK20, DATA\_CTRL20


BANK 6A

HVIO\_6B\_1, SYSPLLREFCLK\_R4A\_2, TXCLK1, DATA\_CTRL1  
HVIO\_6B\_2, SYSPLLREFCLK\_R4A\_3, TXCLK2, DATA\_CTRL2  
HVIO\_6B\_3, SYSPLLREFCLK\_R4B\_2, TXCLK3, DATA\_CTRL3  
HVIO\_6B\_4, SYSPLLREFCLK\_R4B\_3, TXCLK4, DATA\_CTRL4  
HVIO\_6B\_5, PIN\_PERST\_N\_R4A\_1, TXCLK5, DATA\_CTRL5  
HVIO\_6B\_6, PIN\_PERST\_N\_R4B\_1, TXCLK6, DATA\_CTRL6  
HVIO\_6B\_7, PIN\_PERST\_N\_R4C\_1, TXCLK7, DATA\_CTRL7  
HVIO\_6B\_8, TXCLK8, DATA\_CTRL8  
HVIO\_6B\_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA\_CTRL9  
HVIO\_6B\_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA\_CTRL10  
HVIO\_6B\_11, SOURCE\_SYNC\_CLK1, TXCLK11, RXCLK3, DATA\_CTRL11  
HVIO\_6B\_12, SOURCE\_SYNC\_CLK2, TXCLK12, RXCLK4, DATA\_CTRL12  
HVIO\_6B\_13, TXCLK13, DATA\_CTRL13  
HVIO\_6B\_14, TXCLK14, DATA\_CTRL14  
HVIO\_6B\_15, TXCLK15, DATA\_CTRL15  
HVIO\_6B\_16, TXCLK16, DATA\_CTRL16  
HVIO\_6B\_17, TXCLK17, DATA\_CTRL17  
HVIO\_6B\_18, TXCLK18, DATA\_CTRL18  
HVIO\_6B\_19, SYSPLLREFCLK\_R4C\_1, TXCLK19, DATA\_CTRL19  
HVIO\_6B\_20, TXCLK20, DATA\_CTRL20

BANK 6B

BF21 GPIO30  
BE21 GPIO32  
BE43 GPIO24  
BF40 GPIO23  
BE29 GPIO35  
BE25 GPIO33  
BF32 FMCP\_RES0  
BF36 GPIO22  
BF29 GPIO34  
BF25 GPIO2  
BF16 GPIO31  
BH19 GPIO16  
BK22 GPIO15  
BM19 GPIO12  
BU19 GPIO5  
BR19 GPIO6  
CK2 GPIO28  
CJ2 GPIO7  
CK4 SW0  
CH4 SW1

A5ED065BB32AE4SR0

|   |                       |  |                |
|---|-----------------------|--|----------------|
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| Title   |                       |  |                |
| Atum A5   |                       |  |                |
| Size  | Document Number       |  | Rev            |
| B   | FPGA Bank 6A - 6B     |  | A              |
| Date:   | Monday, June 03, 2024 |  | Sheet 14 of 49 |



## TMD Header

6 CLK\_50\_6C

TMD\_DI7\_01 29

CAM1\_GPIO 29  
CAM1\_I2C\_SDA 29  
CAM1\_I2C\_SCL 29CAM2\_GPIO 29  
CAM2\_I2C\_SDA 29  
CAM2\_I2C\_SCL 29

LEDI3\_01 13 42

SWI3\_01 14 42

BUTTONI3\_0W2

TMD\_D2 F27  
TMD\_D3 F24  
TMD\_D4 H27  
TMD\_D5 D24  
TMD\_D6 H18  
TMD\_D7 D16  
TMD\_D0 F18  
TMD\_D1 F15  
CLK\_50\_6C D8  
SW2 K8  
SW3 F8  
BUTTON0 H8  
BUTTON1 C2  
BUTTON2 D4  
BUTTON3 F4  
CAM1\_GPIO K4  
CAM1\_I2C\_SDA G2  
CAM1\_I2C\_SCL J2  
CAM2\_GPIO J1  
CAM2\_I2C\_SDA G1

U28I

HVIO\_6C\_1, TXCLK1, DATA\_CTRL1  
HVIO\_6C\_2, TXCLK2, DATA\_CTRL2  
HVIO\_6C\_3, TXCLK3, DATA\_CTRL3  
HVIO\_6C\_4, TXCLK4, DATA\_CTRL4  
HVIO\_6C\_5, TXCLK5, DATA\_CTRL5  
HVIO\_6C\_6, TXCLK6, DATA\_CTRL6  
HVIO\_6C\_7, TXCLK7, DATA\_CTRL7  
HVIO\_6C\_8, TXCLK8, DATA\_CTRL8  
HVIO\_6C\_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA\_CTRL9  
HVIO\_6C\_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA\_CTRL10  
HVIO\_6C\_11, SOURCE\_SYNC\_CLK1, TXCLK11, RXCLK3, DATA\_CTRL11  
HVIO\_6C\_12, SOURCE\_SYNC\_CLK2, TXCLK12, RXCLK4, DATA\_CTRL12  
HVIO\_6C\_13, TXCLK13, DATA\_CTRL13  
HVIO\_6C\_14, TXCLK14, DATA\_CTRL14  
HVIO\_6C\_15, TXCLK15, DATA\_CTRL15  
HVIO\_6C\_16, TXCLK16, DATA\_CTRL16  
HVIO\_6C\_17, TXCLK17, DATA\_CTRL17  
HVIO\_6C\_18, TXCLK18, DATA\_CTRL18  
HVIO\_6C\_19, TXCLK19, DATA\_CTRL19  
HVIO\_6C\_20, TXCLK20, DATA\_CTRL20

BANK 6C

VCCIO = 3.3V

BANK 6D

## 2.5G Ethernet

33 ENET\_88E2110 RESET\_n  
33 ENET\_88E2110 MDC  
33 ENET\_88E2110 MDIO  
33 ENET\_88E2110 INT\_n

## FPGA/System MAX SPI

INFO\_SPI\_SCLK\_7  
INFO\_SPI\_CS\_n\_7  
INFO\_SPI\_MOSI\_7  
INFO\_SPI\_MISO\_7

40 PCIE\_WAKE\_n

A8 CAM2\_I2C\_SCL  
B4 LED2  
A11 LED3  
B11 ENET\_88E2110\_RESET\_n  
B14 ENET\_88E2110\_MDC  
A14 ENET\_88E2110\_MDIO  
A20 ENET\_88E2110\_INT\_n  
A17 INFO\_SPI\_SCLK  
A23 INFO\_SPI\_CS\_n  
B20 INFO\_SPI\_MOSI  
B23 INFO\_SPI\_MISO  
B26 QSPF\_MOD\_SEL\_n  
B30 QSPF\_RST\_n  
A30 QSPF\_SCL  
A35 QSPF\_SDA  
A33 QSPF\_LP\_MODE  
A39 QSPF\_INTERRUPT\_n  
B35 QSPF\_MOD\_PRS\_n  
D34 PCIE\_WAKE\_n  
B39 LED1

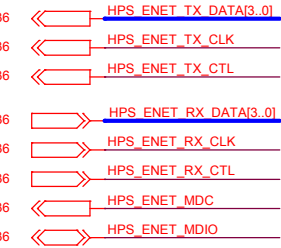
## QSFP+ Control Interface

QSFP\_MOD\_SEL\_n39  
QSFP\_RST\_n 39  
QSFP\_SCL 39  
QSFP\_SDA 39  
QSFP\_LP\_MODE 39  
QSFP\_INTERRUPT\_n 39  
QSFP\_MOD\_PRS\_n39

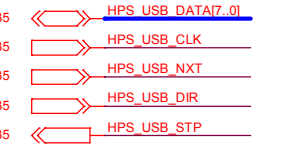
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| Title   |                       |  |                |
| Atum A5 |                       |  |                |
| Size    | Document Number       |  | Rev            |
| B       | FPGA Bank 6C - 6D     |  | A              |
| Date:   | Monday, June 03, 2024 |  | Sheet 15 of 49 |



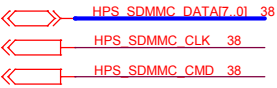
Ethernet PHY Interface (RGMII)



UBS PHY Interface (ULPI)



SD/eMMC Interface



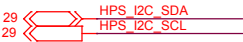
HPS 25MHz Clock



HPS GPIO



HPS I2C Interface



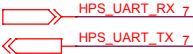
HPS User Button



HPS User LED



UART Interface



|                 |       |
|-----------------|-------|
| HPS_LED         | W135  |
| HPS_GPIO0       | U135  |
| HPS_UART_TX     | W134  |
| HPS_UART_RX     | AK115 |
| HPS_I2C_SDA     | U134  |
| HPS_I2C_SCL     | AL120 |
| HPS_ENET_MDIO   | R134  |
| HPS_ENET_MDC    | AG115 |
| HPS_GPIO2       | N135  |
| HPS_GPIO1       | AK120 |
| HPS_GPIO4       | N134  |
| HPS_USB_CLK     | T132  |
| HPS_USB_STP     | P132  |
| HPS_USB_DIR     | L135  |
| HPS_USB_DATA0   | J135  |
| HPS_USB_DATA1   | AD135 |
| HPS_USB_DATA2   | M132  |
| HPS_USB_DATA3   | AD134 |
| HPS_USB_DATA4   | K132  |
| HPS_USB_DATA5   | AG129 |
| HPS_USB_DATA6   | J134  |
| HPS_USB_DATA7   | AG120 |
| HPS_SDMMC_DATA0 | G134  |
| HPS_SDMMC_DATA1 | G135  |

|                   |       |
|-------------------|-------|
| HPS_SDMMC_DATA0   | E135  |
| HPS_SDMMC_DATA1   | F132  |
| HPS_SDMMC_CLK     | D132  |
| HPS_OSC_CLK       | AG123 |
| HPS_KEY           | B134  |
| HPS_SDMMC_DATA2   | AA135 |
| HPS_SDMMC_DATA3   | V127  |
| HPS_SDMMC_CMD     | AB132 |
| HPS_SDMMC_DATA4   | T127  |
| HPS_SDMMC_DATA5   | T124  |
| HPS_SDMMC_DATA6   | P124  |
| HPS_ENET_TX_CLK   | M127  |
| HPS_ENET_TX_CTL   | K127  |
| HPS_ENET_RX_CLK   | M124  |
| HPS_ENET_RX_CTL   | AB127 |
| HPS_ENET_TX_DATA0 | K124  |
| HPS_ENET_TX_DATA1 | Y127  |
| HPS_ENET_RX_DATA0 | H127  |
| HPS_ENET_RX_DATA1 | AB124 |
| HPS_ENET_TX_DATA2 | F127  |
| HPS_ENET_TX_DATA3 | Y124  |
| HPS_ENET_RX_DATA2 | F124  |
| HPS_ENET_RX_DATA3 | D124  |

U28B

HPS\_IOA\_1, GPIO0\_IO0, SPIM0\_SS1\_N, SPIS0\_CLK, UART0\_CTS\_N, NAND\_ADQ0, SDMMC\_DATA0, USB0\_CLK, EMAC0\_PPS0, TRACE\_D10  
HPS\_IOA\_2, GPIO0\_IO1, SPIM1\_SS1\_N, SPIS0\_MOSI, UART0\_RTS\_N, NAND\_ADQ1, SDMMC\_DATA1, USB0\_STP, EMAC0\_PPSTRIG0, TRACE\_D9  
HPS\_IOA\_3, GPIO0\_IO2, SPIS0\_SS0\_N, UART0\_TX, I2C1\_SDA, NAND\_WE\_N, SDMMC\_CLK, USB0\_DIR, EMAC1\_PPS1, TRACE\_D8  
HPS\_IOA\_4, GPIO0\_IO3, SPIS0\_MISO, UART0\_RX, I2C1\_SCL, NAND\_RE\_N, USB0\_DATA0, EMAC1\_PPSTRIG1, TRACE\_D7  
HPS\_IOA\_5, GPIO0\_IO4, SPIM0\_CLK, UART1\_CTS\_N, I2C0\_SDA, NAND\_WP\_N, SDMMC\_WRITE\_PROTECT, USB0\_DATA1, EMAC2\_PPS2, TRACE\_D6  
HPS\_IOA\_6, GPIO0\_IO5, SPIM0\_MOSI, UART1\_RTS\_N, I2C0\_SCL, NAND\_ADQ2, SDMMC\_DATA2, USB0\_NXT, EMAC2\_PPSTRIG2, TRACE\_D5  
HPS\_IOA\_7, GPIO0\_IO6, SPIM0\_MISO, MDIO2\_MDIO, UART1\_TX, I2C\_EMAC2\_SDA, NAND\_ADQ3, SDMMC\_DATA3, USB0\_DATA2, TRACE\_D4  
HPS\_IOA\_8, GPIO0\_IO7, SPIM0\_SS0\_N, MDIO2\_MDC, UART1\_RX, I2C\_EMAC2\_SCL, NAND\_CLE, SDMMC\_CMD, USB0\_DATA3, TRACE\_D15  
HPS\_IOA\_9, GPIO0\_IO8, SPIM1\_CLK, SPIS1\_CLK, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ4, SDMMC\_DATA4, USB0\_DATA4, I3C1\_SDA, TRACE\_D14  
HPS\_IOA\_10, GPIO0\_IO9, SPIM1\_MOSI, SPIS1\_MOSI, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ5, SDMMC\_DATA5, USB0\_DATA5, I3C1\_SCL, TRACE\_D13  
HPS\_IOA\_11, GPIO0\_IO10, SPIM1\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, SDMMC\_DATA6, USB0\_DATA6, I3C0\_SDA, TRACE\_D12  
HPS\_IOA\_12, GPIO0\_IO11, SPIM1\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ7, SDMMC\_DATA7, USB0\_DATA7, I3C0\_SCL, TRACE\_D11  
HPS\_IOA\_13, GPIO0\_IO12, NAND\_ALE, SDMMC\_PU\_PD\_DATA2, USB1\_CLK, EMAC0\_TX\_CLK, TRACE\_D10  
HPS\_IOA\_14, GPIO0\_IO13, NAND\_RB\_N, SDMMC\_BUS\_PWR, USB1\_STP, EMAC0\_TX\_CTL, TRACE\_D9  
HPS\_IOA\_15, GPIO0\_IO14, NAND\_CE\_N, USB1\_DIR, EMAC0\_RX\_CLK, TRACE\_D8  
HPS\_IOA\_16, GPIO0\_IO15, NAND\_DQS, SDMMC\_DATA\_STROBE, USB1\_DATA0, EMAC0\_RX\_CTL, TRACE\_D7  
HPS\_IOA\_17, GPIO0\_IO16, I3C1\_SDA, NAND\_ADQ8, USB1\_DATA1, EMAC0\_TXD0, TRACE\_D6  
HPS\_IOA\_18, GPIO0\_IO17, I3C1\_SCL, NAND\_ADQ9, USB1\_NXT, EMAC0\_TXD1, TRACE\_D5  
HPS\_IOA\_19, GPIO0\_IO18, I3C0\_SDA, NAND\_ADQ10, USB1\_DATA2, EMAC0\_RXD0, TRACE\_D4  
HPS\_IOA\_20, GPIO0\_IO19, SPIM1\_SS1\_N, I3C0\_SCL, NAND\_ADQ11, USB1\_DATA3, EMAC0\_RXD1, TRACE\_CLK  
HPS\_IOA\_21, GPIO0\_IO20, SPIM1\_CLK, SPIS0\_CLK, UART0\_CTS\_N, I2C1\_SDA, NAND\_ADQ12, USB1\_DATA4, EMAC0\_TXD2, TRACE\_D0  
HPS\_IOA\_22, GPIO0\_IO21, SPIM1\_MOSI, SPIS0\_MOSI, UART0\_RTS\_N, I2C1\_SCL, NAND\_ADQ13, USB1\_DATA5, EMAC0\_TXD3, TRACE\_D1  
HPS\_IOA\_23, GPIO0\_IO22, SPIM1\_MISO, SPIS0\_SS0\_N, UART0\_TX, I2C0\_SDA, NAND\_ADQ14, USB1\_DATA6, EMAC0\_RXD2, TRACE\_D2  
HPS\_IOA\_24, GPIO0\_IO23, SPIM1\_SS0\_N, SPIS0\_MISO, UART0\_RX, I2C0\_SCL, NAND\_ADQ15, USB1\_DATA7, EMAC0\_RXD3, TRACE\_D3

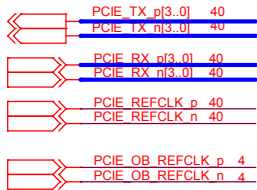
HPS\_IOB\_1, GPIO1\_IO0, SPIM1\_CLK, CM\_PLL\_CLK0, UART0\_CTS\_N, EMAC0\_PPS0, NAND\_ADQ0, SDMMC\_DATA0, EMAC1\_TX\_CLK, TRACE\_D10  
HPS\_IOB\_2, GPIO1\_IO1, SPIM1\_MOSI, CM\_PLL\_CLK1, UART0\_RTS\_N, EMAC0\_PPSTRIG0, NAND\_ADQ1, SDMMC\_DATA1, EMAC1\_TX\_CTL, TRACE\_D9  
HPS\_IOB\_3, GPIO1\_IO2, SPIM1\_MISO, CM\_PLL\_CLK2, UART0\_TX, I2C0\_SDA, NAND\_WE\_N, SDMMC\_CLK, EMAC1\_RX\_CLK, TRACE\_D8  
HPS\_IOB\_4, GPIO1\_IO3, SPIM1\_SS0\_N, CM\_PLL\_CLK3, UART0\_RX, I2C0\_SCL, NAND\_RE\_N, EMAC1\_RX\_CTL, TRACE\_D7  
HPS\_IOB\_5, GPIO1\_IO4, SPIM1\_SS1\_N, SPIS1\_CLK, UART1\_CTS\_N, EMAC2\_PPS2, NAND\_WP\_N, SDMMC\_WRITE\_PROTECT, I3C1\_SDA, EMAC1\_TXD0, TRACE\_D6  
HPS\_IOB\_6, GPIO1\_IO5, SPIS1\_MOSI, UART1\_RTS\_N, EMAC2\_PPSTRIG2, NAND\_ADQ2, SDMMC\_DATA2, I3C1\_SCL, EMAC1\_TXD1, TRACE\_D5  
HPS\_IOB\_7, GPIO1\_IO6, SPIS1\_SS0\_N, UART1\_TX, I2C1\_SDA, NAND\_ADQ3, SDMMC\_DATA3, I3C0\_SDA, EMAC1\_RXD0, TRACE\_D4  
HPS\_IOB\_8, GPIO1\_IO7, SPIS1\_MISO, UART1\_RX, I2C1\_SCL, NAND\_CLE, SDMMC\_CMD, I3C0\_SCL, EMAC1\_RXD1, TRACE\_D15  
HPS\_IOB\_9, GPIO1\_IO8, JTAG\_TCK, SPIS0\_CLK, MDIO2\_MDIO, I2C\_EMAC2\_SDA, NAND\_ADQ4, SDMMC\_DATA4, EMAC1\_TXD2, TRACE\_D14  
HPS\_IOB\_10, GPIO1\_IO9, JTAG\_TMS, SPIS0\_MOSI, MDIO2\_MDC, I2C\_EMAC2\_SCL, NAND\_ADQ5, SDMMC\_DATA5, EMAC1\_TXD3, TRACE\_D13  
HPS\_IOB\_11, GPIO1\_IO10, JTAG\_TDO, SPIS0\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, SDMMC\_DATA6, EMAC1\_RXD2, TRACE\_D12  
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HPS\_IOB\_15, GPIO1\_IO14, UART1\_TX, NAND\_CE\_N, I3C1\_SDA, EMAC2\_RX\_CLK, TRACE\_D8  
HPS\_IOB\_16, GPIO1\_IO15, UART1\_RX, NAND\_DQS, SDMMC\_DATA\_STROBE, I3C1\_SCL, EMAC2\_RX\_CTL, TRACE\_D7  
HPS\_IOB\_17, GPIO1\_IO16, UART1\_CTS\_N, NAND\_ADQ8, I3C0\_SDA, EMAC2\_TXD0, TRACE\_D6  
HPS\_IOB\_18, GPIO1\_IO17, SPIM0\_SS1\_N, UART1\_RTS\_N, NAND\_ADQ9, I3C0\_SCL, EMAC2\_TXD1, TRACE\_D5  
HPS\_IOB\_19, GPIO1\_IO18, SPIM0\_MISO, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ10, EMAC2\_RXD0, TRACE\_D4  
HPS\_IOB\_20, GPIO1\_IO19, SPIM0\_SS0\_N, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ11, EMAC2\_RXD1, TRACE\_CLK  
HPS\_IOB\_21, GPIO1\_IO20, SPIM0\_CLK, SPIS1\_CLK, I2C\_EMAC2\_SDA, NAND\_ADQ12, EMAC2\_TXD2, TRACE\_D0  
HPS\_IOB\_22, GPIO1\_IO21, SPIM0\_MOSI, SPIS1\_MOSI, I2C\_EMAC2\_SCL, NAND\_ADQ13, EMAC2\_TXD3, TRACE\_D1  
HPS\_IOB\_23, GPIO1\_IO22, SPIM0\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ14, EMAC2\_RXD2, TRACE\_D2  
HPS\_IOB\_24, GPIO1\_IO23, SPIM0\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ15, EMAC2\_RXD3, TRACE\_D3

HPS

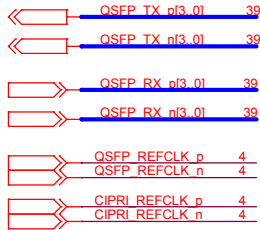
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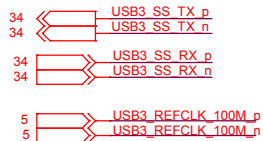
PCle Transceivers



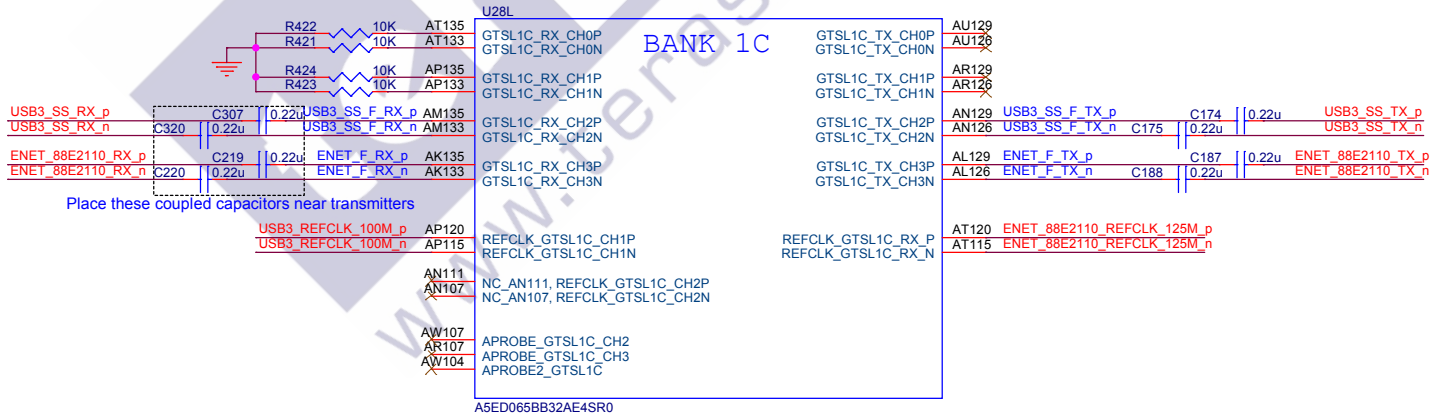
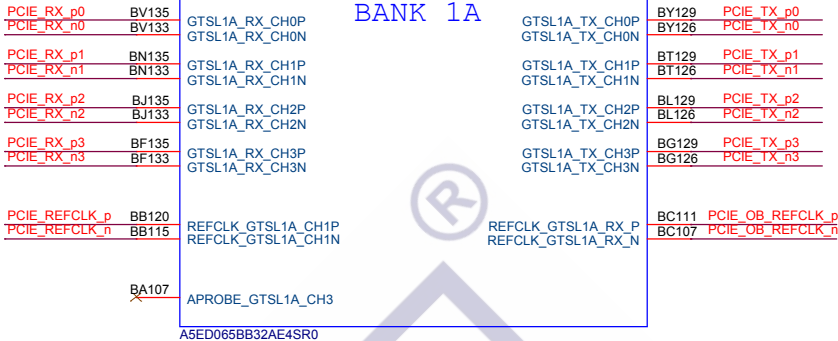
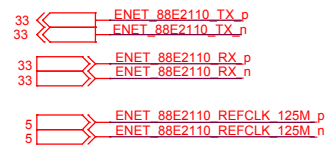
QSFP+ Transceivers



USB 3.1 Transceivers

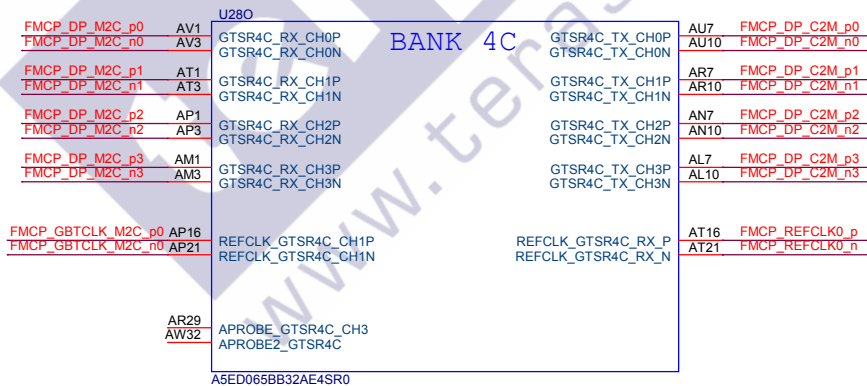
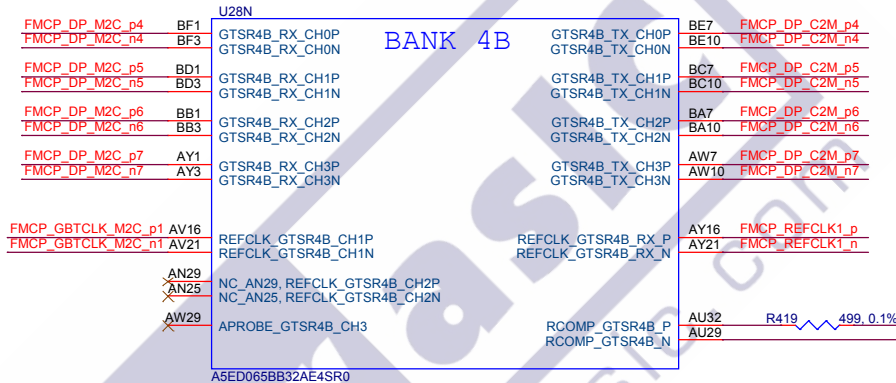
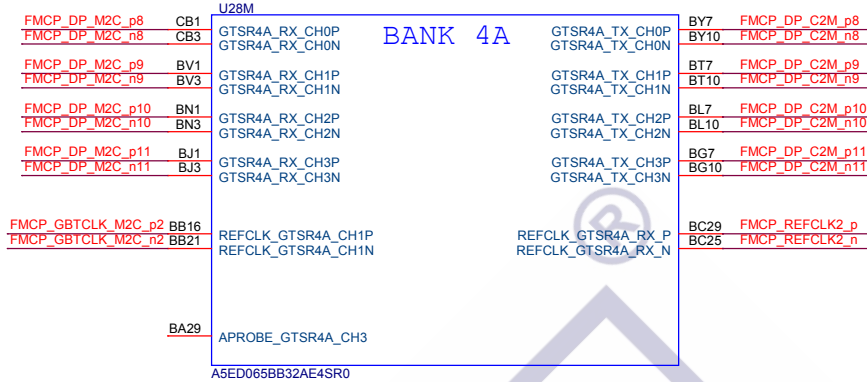
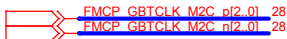
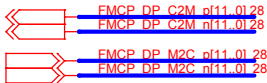


2.5G Ethernet Transceivers





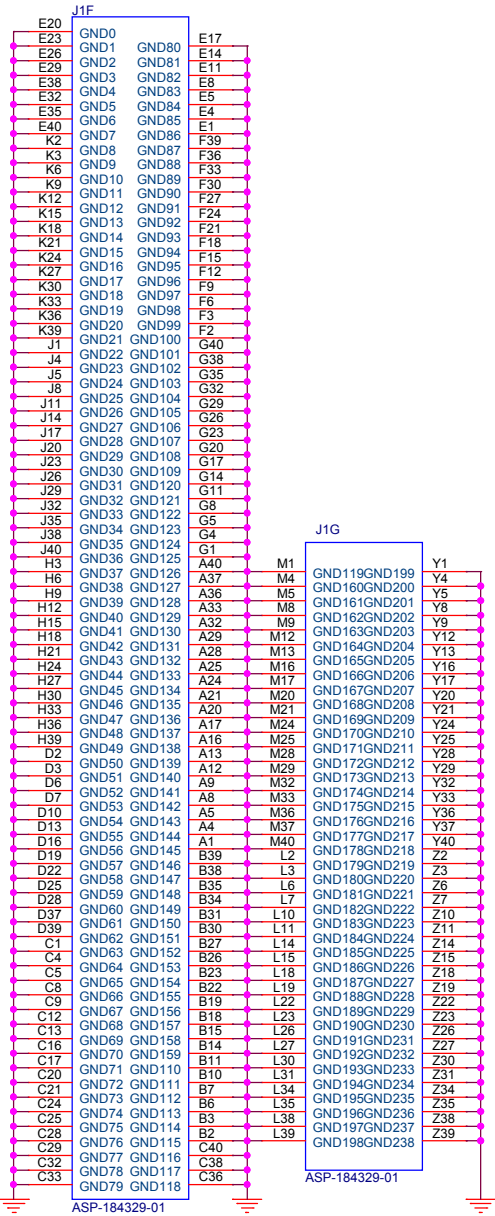
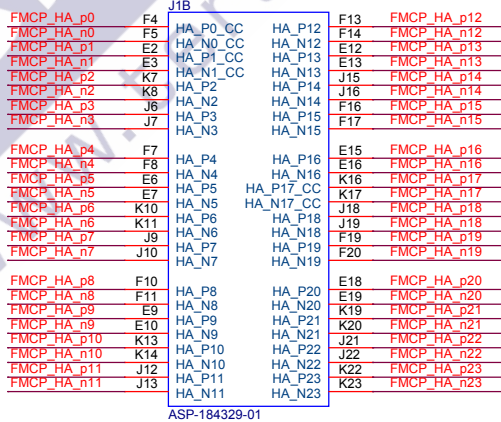
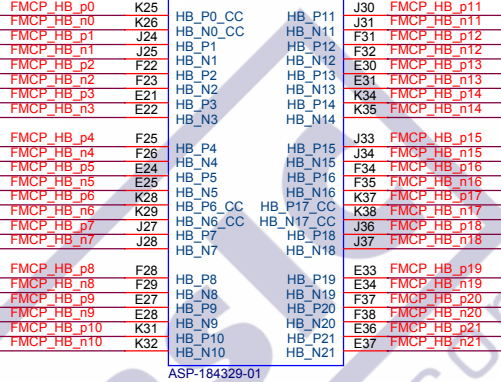
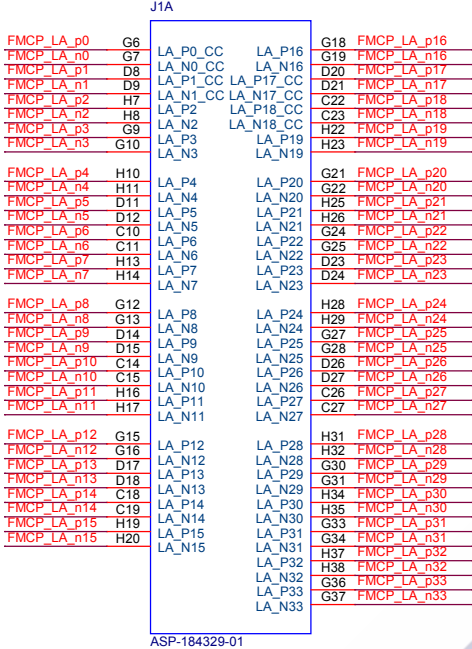
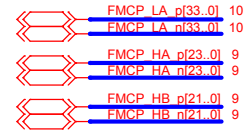
# FMC+ Transceiver



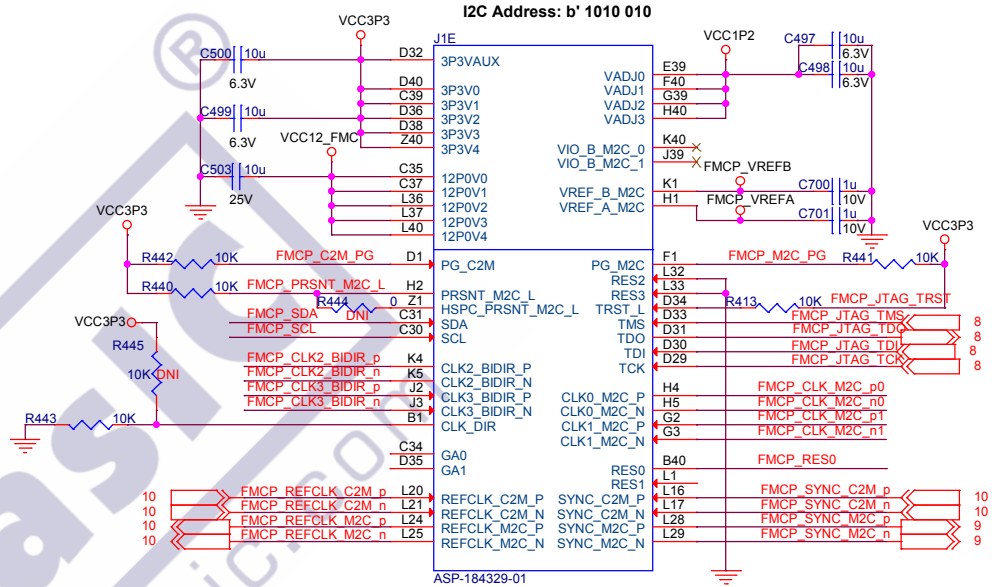


FMC+ PORT INTERFACE(HPC)

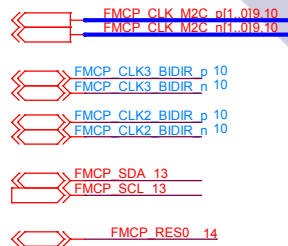
FMC+ 1



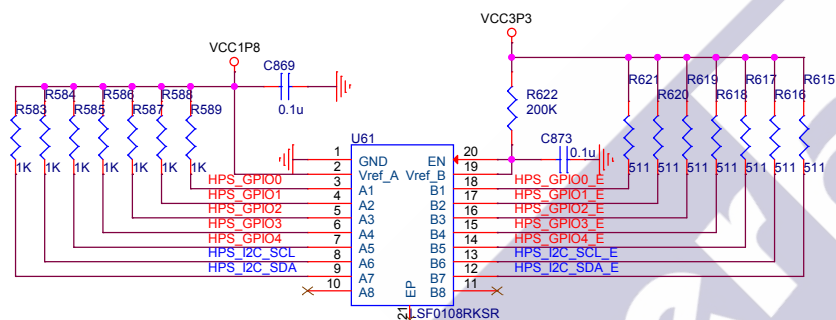
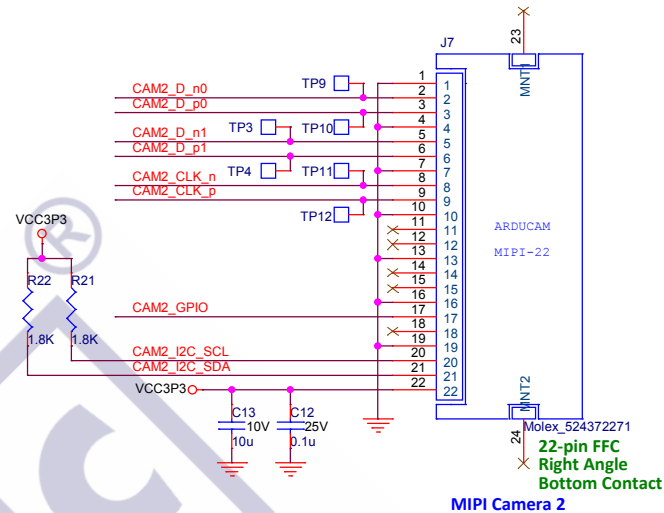
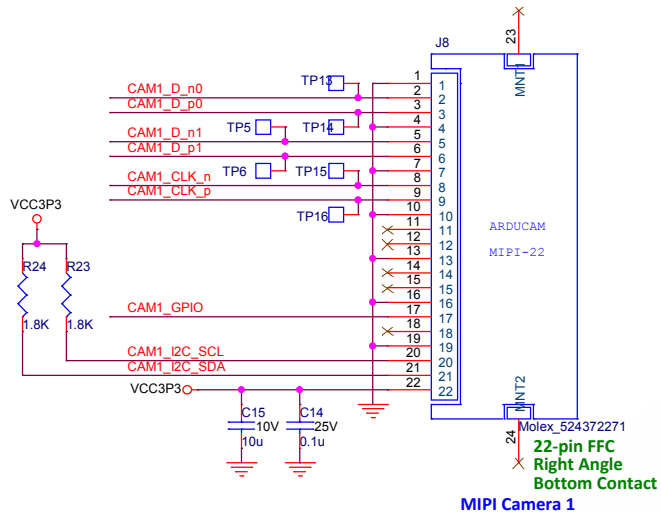
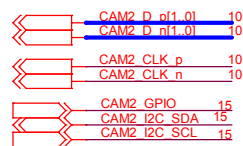
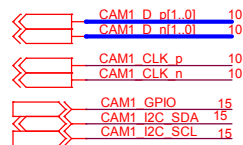




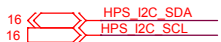
Phylogenetic tree showing relationships between FMCP proteins. The tree is rooted at the bottom left. The FMCP DP C2M p11(1.0) 18 and FMCP DP C2M n1(1.0) 18 are sister taxa. The FMCP DP M2C p11(1.0) 18 and FMCP DP M2C n1(1.0) 18 are sister taxa. The FMCP GBTCLK M2C n12(1.0) 18 and FMCP GBTCLK M2C n12(1.0) 18 are sister taxa. The FMCP PRSNT M2C L 7.44 is a sister taxon to the FMCP GBTCLK M2C n12(1.0) 18 and FMCP GBTCLK M2C n12(1.0) 18.



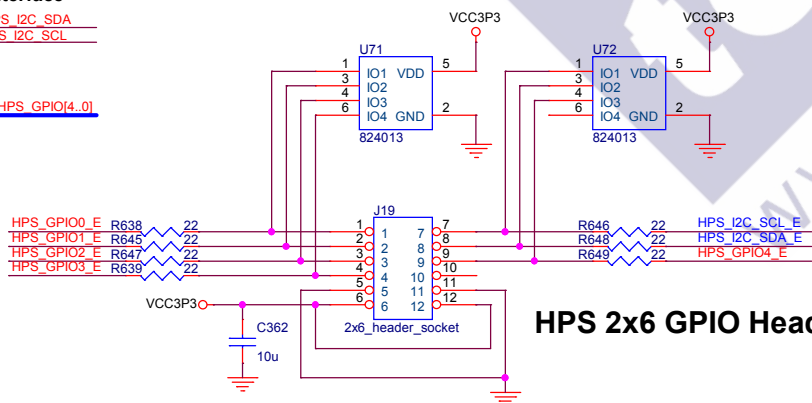




### HPS I2C Interface

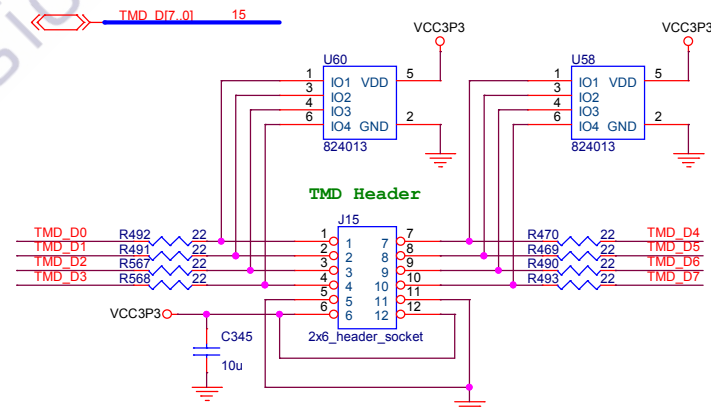



### HPS GPIO



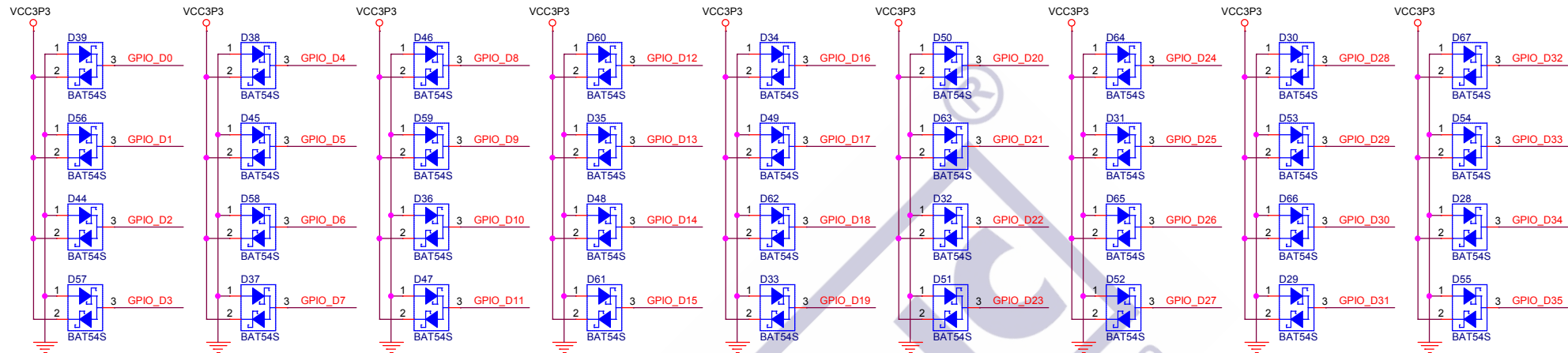
### HPS 2x6 GPIO Header

### TMD 2x6 Header



|   |   |  |          |
|---|---|--|----------|
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| Title   |   |  |          |
| Atum A5   |   |  |          |
| Size  | Document Number                           |  | Rev      |
| B   | MIPI Connectors, TMD Header, HPS 2x6 GPIO |  | A        |
| Date:   | Monday, June 03, 2024                     | Sheet  | 29 of 49 |





GPIO

