



MPM54522

16V, Dual 6A, Single 12A Power Module
With I²C Interface

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPM54522 is a dual 6A power module that integrates a high-efficiency step-down DC/DC converter IC, two inductors, and selected passive components into a single over-molded package.

The two outputs of MPM54522 can be paralleled for up to 12A current. The power module offers active current balancing function that allows equal current sharing of the outputs in parallel operation.

The MPM54522 offers a dedicated programmable low dropout regulator (LDO) with up to 500mA output current to provide ultra-low noise output.

The MPM54522 adopts the Constant On-Time (COT) control scheme that provides fast transient response and minimizes the required output capacitance.

The MPM54522 provides on-chip non-volatile memory (NVM) to store and restore device configurations. Operation parameters, timing and protection thresholds are fully programmable over the I²C bus. MPM54522 offers on-chip current and voltage sensing that allows accurate input/output voltage, output current, and temperature telemetry over the I²C bus.

The MPM54522 is available in an ultra-thin 5x6.5x2.76mm ECLGA package.

FEATURES

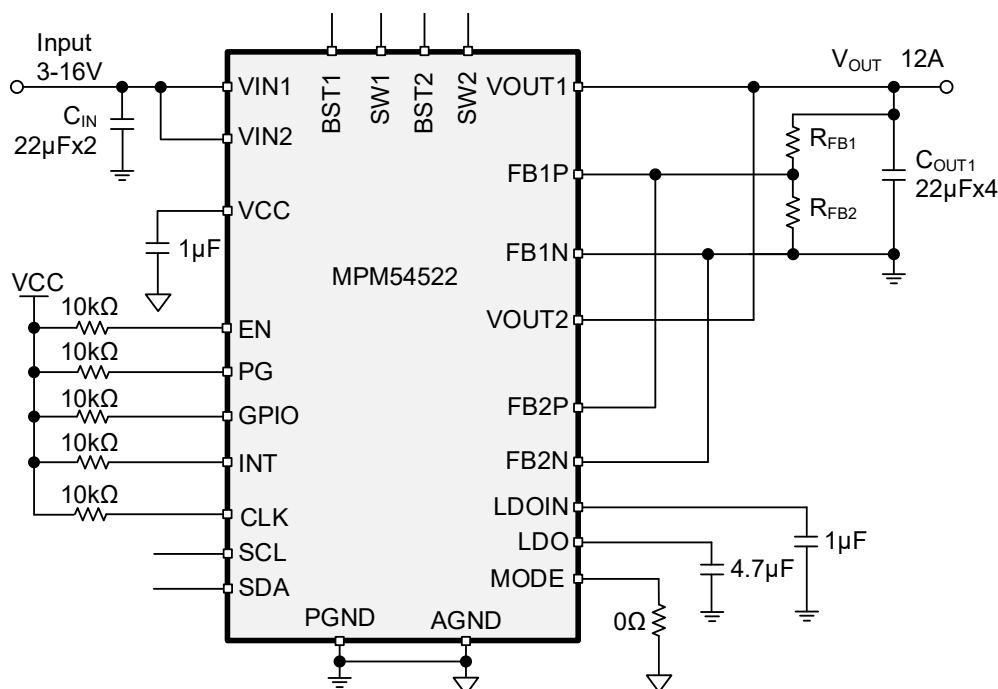
- Wide Input Voltage Range: 3V to 16V
- Dual 6A and Up to 12A for Parallel Operation
- High Efficiency at Light Load in Parallel Operation with Phase Shedding
- MODE Pin for Selection of Output Voltage, Parallel Mode, and Timing by Pin-strapping
- Remote Sense for Both Output Channels
- Programmable 500mA rated LDO with input voltage up to 3.6V
- Programmable Soft-start, Soft-off and Delay with MPS Patented FLEX-Timer Sequence Control
- Programmable Reference Voltage and Slew Rate
- Programmable Switching Frequency: 500kHz, 750kHz, 1MHz, 1.25MHz
- Accurate Output Voltage, Output Current and Junction Temperature Telemetry
- Open-Drain Power Good Indication and General Status Interrupt
- Ultra-thin 5x6.5x2.76mm ECLGA Package

APPLICATIONS

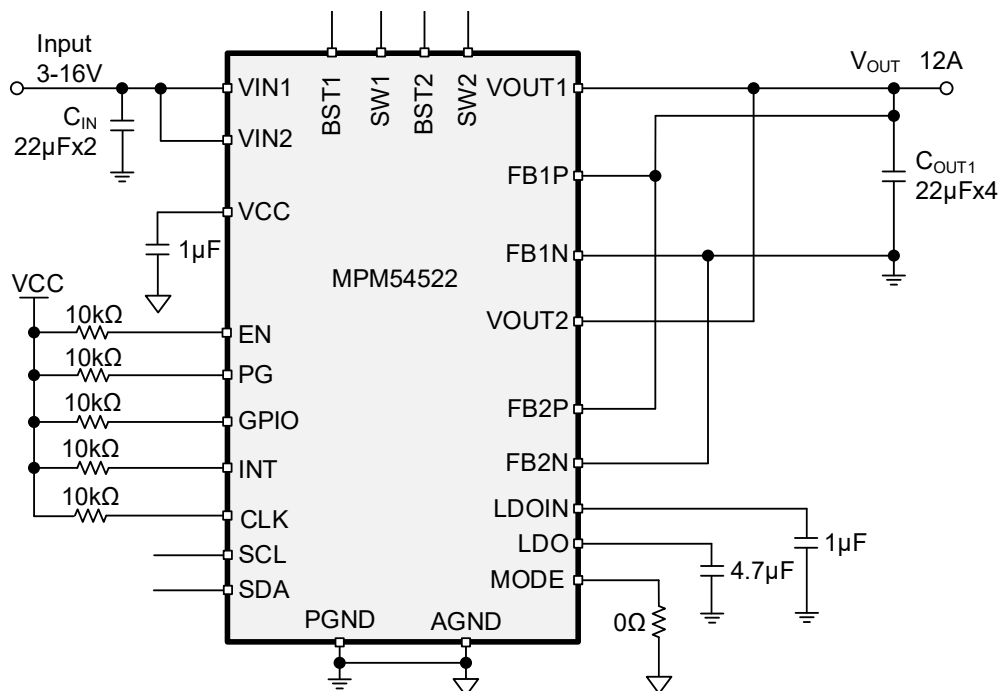
- Storage and Networking
- FPGA and ASIC Power Supply
- Computing and Telecommunication

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

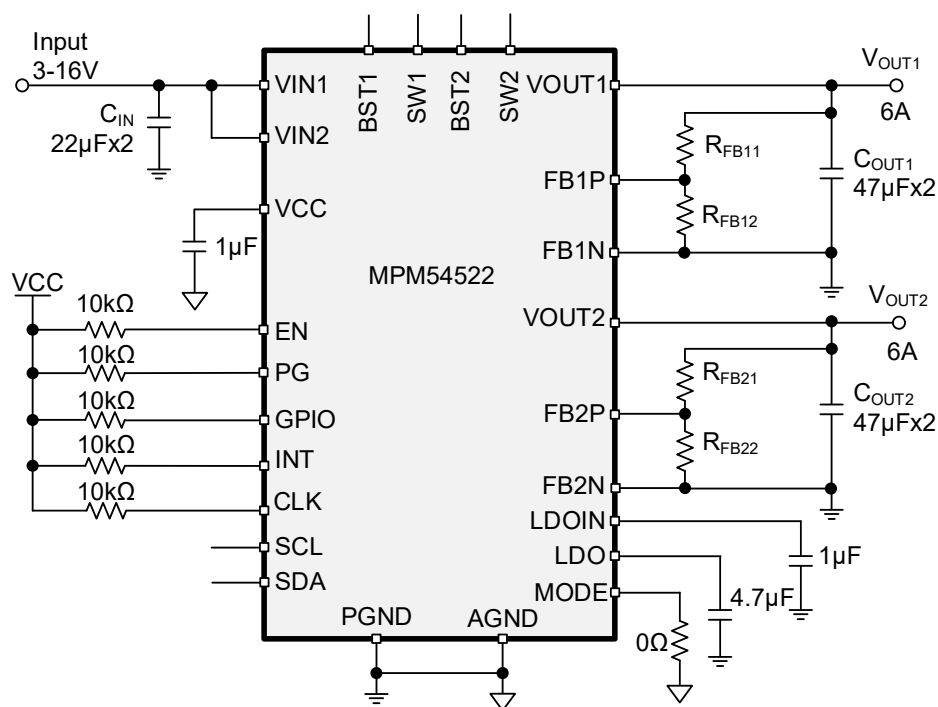
TYPICAL APPLICATION CIRCUIT



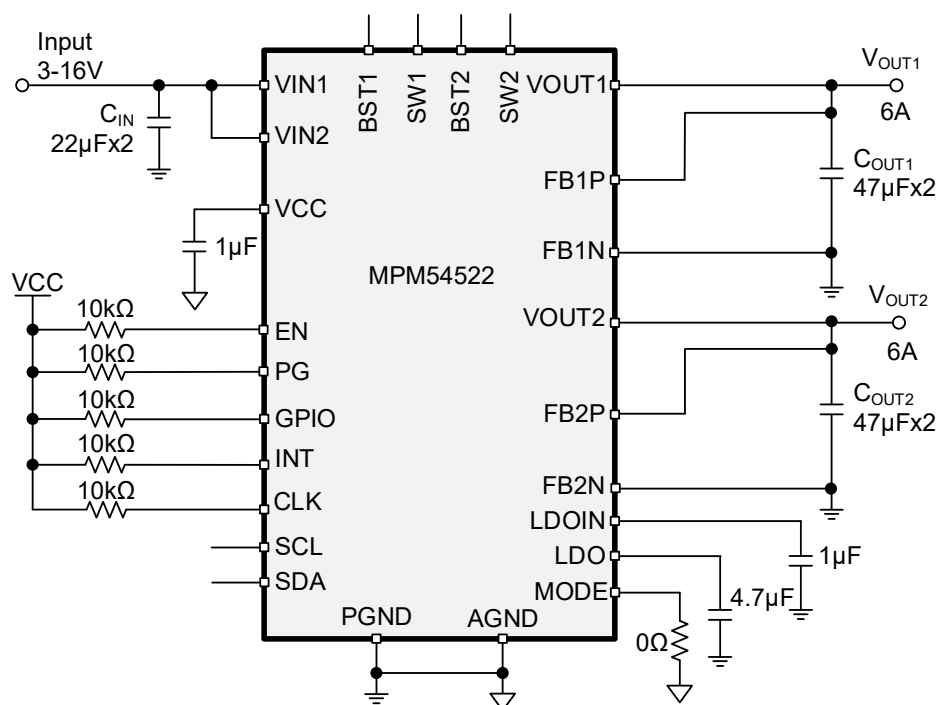
MPM54522 Dual-Phase Operation with External Divider



MPM54522 Dual-Phase Operation with Internal Divider



MPM54522 Dual-Output Operation with External Divider



MPM54522 Dual-Output Operation with Internal Divider

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM54522GPC-xxxx**	ECLGA (5mmx6.5mmx2.76mm)	See Below	3
MPM54522GPC-0000**			

* For Tray, add suffix - T (e.g. MPM54522GPC-xxxx-T).

* For Tape & Reel, add suffix - Z (e.g. MPM54522GPC-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the NVM. The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Please work with MPS FAE to create this unique number. Even if ordering the "0000" code. MPM54522GPC-0000 is the default version.

TOP MARKING

MPSY YWW

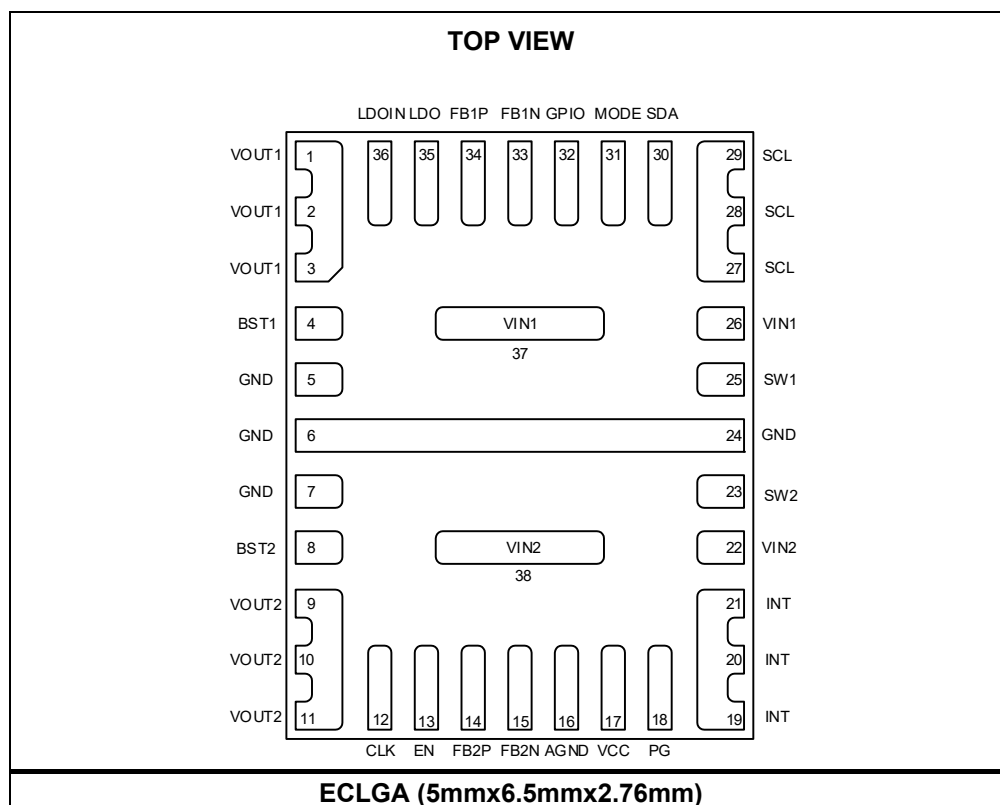
MP54522

LLLLLLL

M

MPS: MPS prefix
YY: Year code
WW: Week code
MP54522: Part number
LLLLLLL: Lot number
M: Module

PACKAGE REFERENCE



PIN FUNCTIONS

Package Pin #	Name	Description
1,2,3	VOUT1	Output of Buck1. Connect this pin with wide PCB trace.
9,10,11	VOUT2	Output of Buck2. Connect this pin with wide PCB trace.
4	BST1	Buck 1 bootstrap. Connect a capacitor between SW1 and BST1 to form a floating supply across the high-side switch driver of Buck 1.
25	SW1	Buck 1 switch output. Float this pin.
5~7,24	PGND	Power ground. PGND requires special consideration during PCB layout. Connect PGND with copper traces and vias.
23	SW2	Buck 2 switch output. Float this pin.
8	BST2	Buck 2 bootstrap. Float this pin
12	CLK	Clock pin for FLEX-Time Control.
13	EN	Enable pin of Buck 1, Buck2, and LDO.
14	FB2P	Positive feedback of buck 2 remote sense.
15	FB2N	Negative feedback of buck 2 remote sense.
16	AGND	Analog ground. Connect AGND to the power ground pin.
17	VCC	Internal 3.6V LDO output. The driver of FETs are powered from the VCC voltage. Decouple VCC with a 1µF ceramic capacitor placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics
18	PG	Power good output, open drain. Pull PG low when any enabled regulator falls below the UV threshold. Pull PG low when all regulators are disabled.
19,20,21	INT	General status interrupt. INT is an open-drain output. The PMIC asserts INT low to communicate any one or more critical event to host. INT remains asserted until the appropriate registers are explicitly cleared or the PMIC is reset.
22,38	VIN2	Supply voltage input of Buck 2. A ceramic capacitor is required to decouple the input rail. Connect VIN2 using a wide PCB trace. VIN1 and VIN2 must be connected to the same bus voltage.
26,37	VIN1	Supply voltage input of Buck 1. A ceramic capacitor is required to decouple the input rail. Connect VIN1 using a wide PCB trace. VIN1 and VIN2 must be connected to the same bus voltage.
27,28,29	SCL	I2C bus clock.
30	SDA	I2C bus data.
31	MODE	MTP selection pin. Connect a resistor to this pin to select MTP configurations of some features. Refer to MODE Determined MTP Map for more details.
32	GPIO	GPIO pin. GPIO pin can be configured into the power up sequence with the regulators or an analog input for the ADC circuit.
33	FB1N	Negative feedback of buck 1 remote sense.
34	FB1P	Positive feedback of buck 1 remote sense.
35	LDO	Output of 500mA LDO.
36	LDOIN	Input of 500mA LDO. The voltage of this pin should be smaller than 3.6V.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{IN})	18V
V_{SW1} , V_{SW2}	-0.3V to $V_{IN}+0.3V$
V_{BST1} , V_{BST2}	$V_{SW1/2} + 4V$
V_{OUT1} , V_{OUT2}	6V
All other pins	-0.3V to 4V
Continuous Power Dissipation ($T_A = +25^{\circ}C$) ⁽²⁾	
ECLGA (5mmx6.5mm)	6.28W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{IN1} , V_{IN2})	3V to 16V
Output voltage (V_{OUT})	0.4V to 5.5V ⁽⁴⁾
Input & output voltage (LDO)	3.6V Max
Output current (LDO)	500mA
Operating junction temp. (T_J)	-40°C to +125°C

Thermal Resistance ⁽⁵⁾⁽⁶⁾⁽⁷⁾⁽⁸⁾ θ_{JA} θ_{JC} θ_{JB}

ECLGA (5mmx6.5mmx2.76mm)

θ_{JA}	19.9°C/W
θ_{JC_top}	0.8°C/W
θ_{JB}	8.1°C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature.
- The device is not guaranteed to function outside of its operating conditions.
- When V_{out} is less than 3.8V, V_{out} can be set from internal divider via I2C; When V_{out} is more than 3.8V, V_{out} need to be set from external divider.
- θ_{JA} is Junction-to-ambient thermal resistance, θ_{JC_top} is Junction-to-case top thermal characterization parameter, θ_{JB} is Junction-to-board thermal characterization parameter.
- The thermal parameter is based on test on MPS evaluation board (T-EVM54522-PC-00A) under no airflow cooling condition in standard enclosure, the board size is 8cm*8cm, 4 layer, of which top and bottom layer Cu thickness is 2Oz.
- Junction-to-case top thermal characterization parameter, θ_{JC_top} , estimates the junction temperature in the real system, based on equation $T_J = \theta_{JC_top} \times P_{loss} + T_{case_top}$, where P_{loss} is the entire loss of module at real application, T_{case_top} is case top temperature
- Junction-to-board thermal characterization parameter, θ_{JB} , estimation the junction temperature in the real system, based on equation $T_J = \theta_{JB} \times P_{loss} + T_{board}$, where P_{loss} is the entire loss of module at real application, T_{board} is board temperature.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C^{(9)}$, typical value is tested at $T_J = +25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN						
VIN UVLO Rising	V_{INUVLO_R}	Registers 0x04 bit[1:0] programmable	2.6	2.75	2.9	V
VIN UVLO Falling	V_{INUVLO_F}			2.6		V
VIN OV Rising Threshold	V_{INOVLO_R}		17	18	19	V
VIN Quiescent Current	I_{Q_PFM}	PFM, No Load		2.8	5	mA
Buck 1, Buck 2						
Switch Leakage	SW_{ILK1}			0	1	μA
Minimum On Time ⁽¹⁰⁾	t_{ON_MIN1}			30		ns
Minimum Off Time ⁽¹⁰⁾	t_{OFF_MIN1}			130		ns
Output Voltage Accuracy	V_{FB1P}	Default output of Buck 1	-1.5%	0.6	+1.5%	V
			-1.5%	0.8	+1.5%	V
			-1.5%	1.2	+1.5%	V
			-1.5%	1.8	+1.5%	V
Output Voltage Accuracy	V_{FB2P}	Default output of Buck 2	-1.5%	0.6	+1.5%	V
			-1.5%	0.8	+1.5%	V
			-1.5%	1.2	+1.5%	V
			-1.5%	1.8	+1.5%	V
Low Side Current Limit (source)	I_{LS_Valley}	Registers 0x04 bit[4:2], 0x09 bit[4:2] programmable		6.5		A
Negative Current Limit	$INOC_P$	Forced PWM/OVP discharge	4.7	6.2	7.7	A
Output Discharge Resistor	$R_{DISCHARGE}$			27		Ω
UV/OV						
Output UV Threshold	V_{UVP_SW1}	Registers 0x05 bit[3:2], 0x0A bit[3:2] programmable	86%	90%	94%	Vref
Output OVP Rising Threshold	V_{OVP1_H}	Registers 0x05 bit[1:0], 0x0A bit[1:0] programmable	109%	113%	117%	VREF
Output OVP Recovery Threshold	V_{OVP1_L}			110%		VREF
Soft Start Time						
Soft Start Time	t_{start}	Registers 0x41[6:4], 0x48[6:4] programmable	1.6	2	2.4	ms
Soft Stop Time	t_{stop}	Registers 0x41[3:2], 0x48[3:2] programmable		0.5		ms
Switching Frequency						
Default Oscillation Frequency	f_{SW}	Registers 0x02 bit[5:4], 0x07 bit[5:4] programmable	800	1000	1200	kHz
LDO						
LDOIN UVLO Rising	V_{LDOIN_R}		2.4	2.6	2.8	V
LDOIN UVLO Hysteresis	V_{LDOIN_HYS}			200		mV
Output Voltage	V_{LDO}	Registers 0x0C programmable	-3%	1.8	3%	V
LDO Load Capability	I_{LIM_LDO}		500			mA

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C^{(9)}$, typical value is tested at $T_J = +25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LDO Voltage Regulation ⁽¹⁰⁾	V_{LDO_RG}	LDOIN = 3.3V, LDO = 1.8V, load = 0~500mA		1		%
EN						
EN Rising Threshold	V_{EN_R}		1	1.2	1.4	V
EN Hysteresis	V_{EN_HYS}			200		mV
MODE Detection						
MODE Sourcing Current	I_{MODE}		11.5	12.8	14.1	uA
MODE Detection Voltage Upper Threshold	V_{MODE_DT0}	MODE0 is detected if $0V < V_{MODE} < V_{MODE_DT0}$			40	mV
	V_{MODE_DT1}	MODE1 is detected if $V_{MODE_DT0} < V_{MODE} < V_{MODE_DT1}$	80		120	mV
	V_{MODE_DT2}	MODE2 is detected if $V_{MODE_DT1} < V_{MODE} < V_{MODE_DT2}$	180		240	mV
	V_{MODE_DT3}	MODE3 is detected if $V_{MODE_DT2} < V_{MODE} < V_{MODE_DT3}$	320		460	mV
	V_{MODE_DT4}	MODE4 is detected if $V_{MODE_DT3} < V_{MODE} < V_{MODE_DT4}$	560		760	mV
	V_{MODE_DT5}	MODE5 is detected if $V_{MODE_DT4} < V_{MODE} < V_{MODE_DT5}$	860		1080	mV
	V_{MODE_DT6}	MODE6 is detected if $V_{MODE_DT5} < V_{MODE} < V_{MODE_DT6}$	1180		1400	mV
	V_{MODE_DT7}	MODE7 is detected if $V_{MODE_DT6} < V_{MODE} < V_{CC}$	1660			mV
PG & INT						
PG, Output Port Sink Current Capability	V_{PG_Sink}	Sink 3mA			0.3	V
INT, Output Port Sink Current Capability	V_{INT_Sink}	Sink 3mA			0.3	V
PG UV rising	$V_{PG_UV_R}$	Registers 0x05 bit[5], 0x0A bit[5] programmable		95%		Vref
PG UV falling	$V_{PG_UV_F}$			92.5%		Vref
PG OV rising	$V_{PG_OV_R}$	Registers 0x05 bit[7:6], 0x0A bit[7:6] programmable		107.5%		Vref
PG OV falling	$V_{PG_OV_F}$			105%		Vref
VCC Regulator						
VCC Voltage	V_{CC}	$I_{CC} = 25mA$		3.6		V
VCC Voltage Regulation	V_{CC_RG}	$I_{CC} = 0-25mA$		1		%
Temperature Protection						
Thermal Shutdown ⁽¹⁰⁾	T_{OTP_R}	Register 0x0F bit[7:5] programmable		150		$^{\circ}C$
Thermal Hysteresis ⁽¹⁰⁾	T_{Hys}			20		$^{\circ}C$
CLK						
CLK logic high	V_{CLK_IH}		1.4			V

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁹⁾, typical value is tested at $T_J = +25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CLK logic low	V_{CLK_IL}				0.4	V
CLK, Output Port Sink Current Capability	V_{CLK_Sink}	Sink 3mA			0.3	V
GPIO						
GPIO, Output Port Sink Current Capability	V_{GPIO_Sink}	Sink 3mA			0.3	V
I²C Interface Specifications ⁽⁹⁾						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.6	V
Output voltage logic low	V_{OUT_L}	Sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				3.4	MHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		200			ns
Data set-up time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$			70		ns
Set-up time for repeated start	$t_{SU.STA}$		160			ns
Hold time for repeated start	$t_{HD.STA}$		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	$t_{SU.STO}$		160			ns
SCL and SDA rising time	t_R		10		300	ns
SCL and SDA falling time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

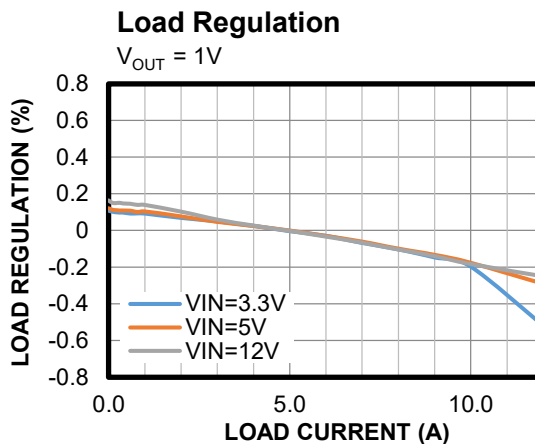
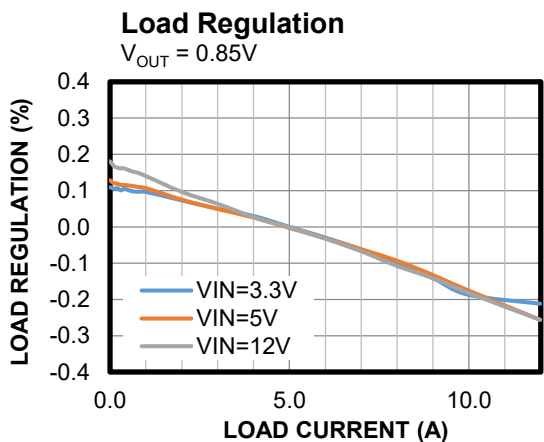
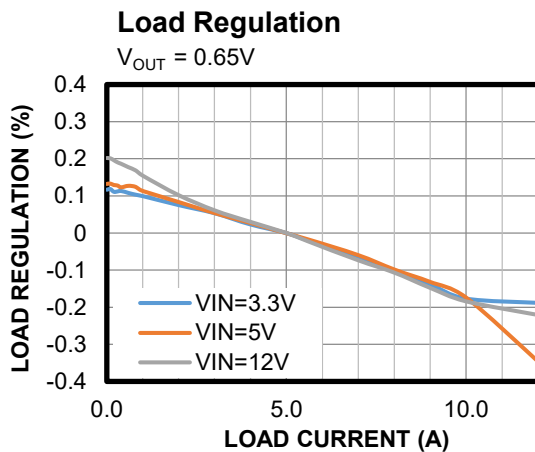
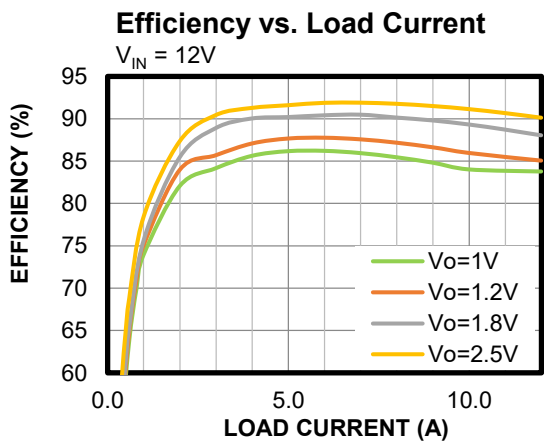
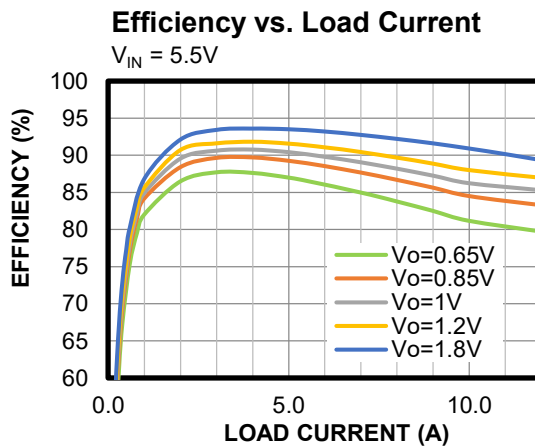
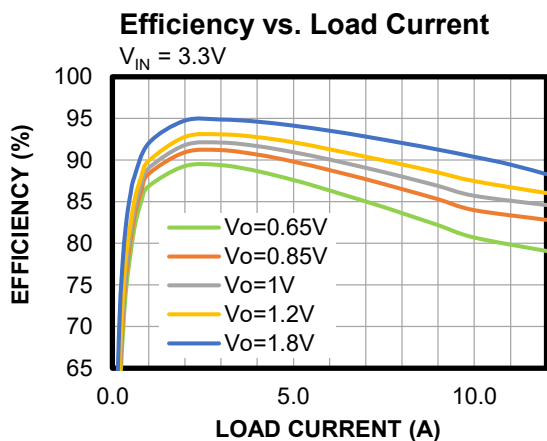
Notes:

9) Not tested in production. Guaranteed by over-temperature correlation.

10) Guarantee by engineering sample characterization

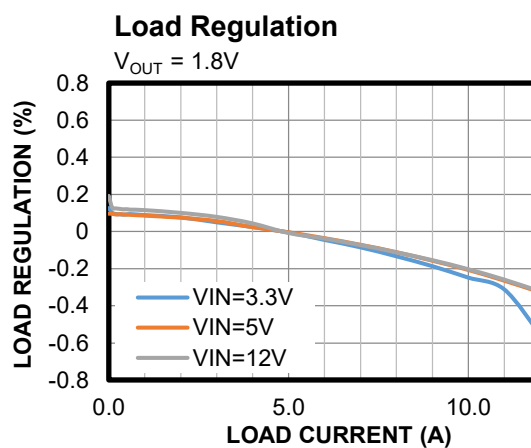
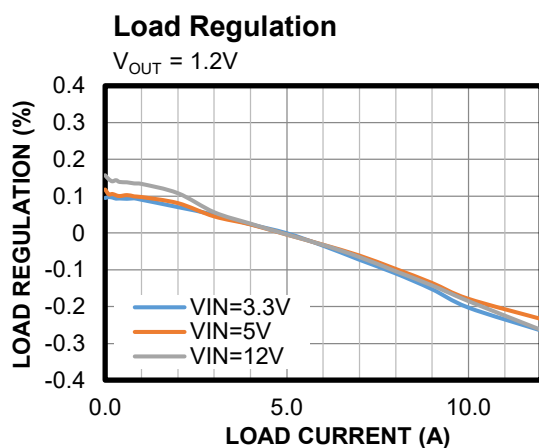
TYPICAL CHARACTERISTICS

Performance curves are test on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 1.2V$, $C_{IN} = 2 \times 22\mu F$, $C_{OUT} = 3 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.



TYPICAL CHARACTERISTICS *(continued)*

Performance curves are test on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 1.2V$, $C_{IN} = 2 \times 22\mu F$, $C_{OUT} = 3 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

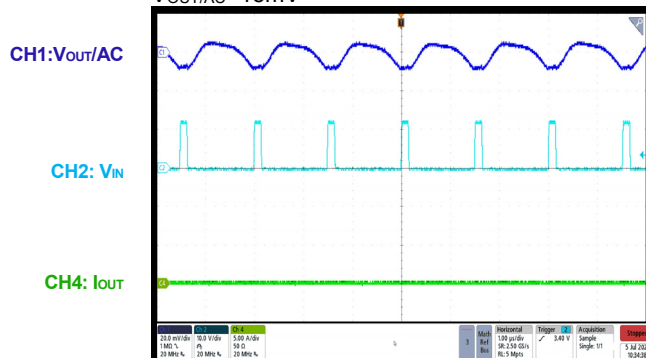


TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves are test on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 1.2V$, $C_{IN} = 2 \times 22\mu F$, $C_{OUT} = 3 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

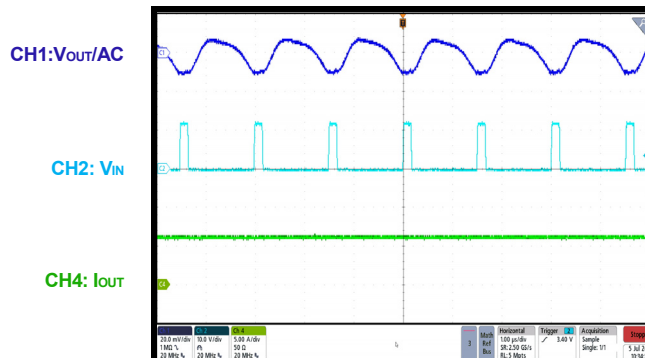
Steady State

$I_{OUT} = 0A$, FSW=750kHz, Independent mode, $V_{OUT/AC} = 15mV$



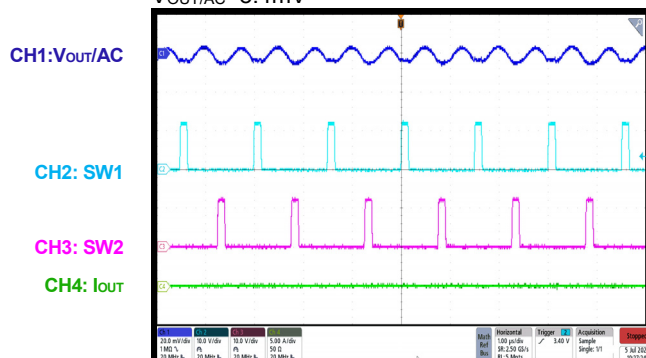
Steady State

$I_{OUT} = 6A$, FSW=750kHz, Independent mode, $V_{OUT/AC} = 18mV$



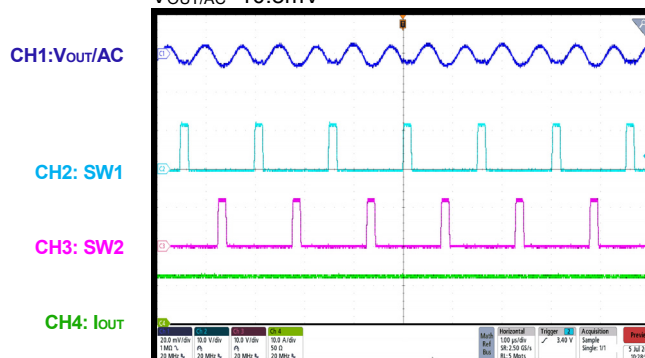
Steady State

$I_{OUT} = 0A$, FSW=750kHz, Paralleled mode, $V_{OUT/AC} = 8.4mV$



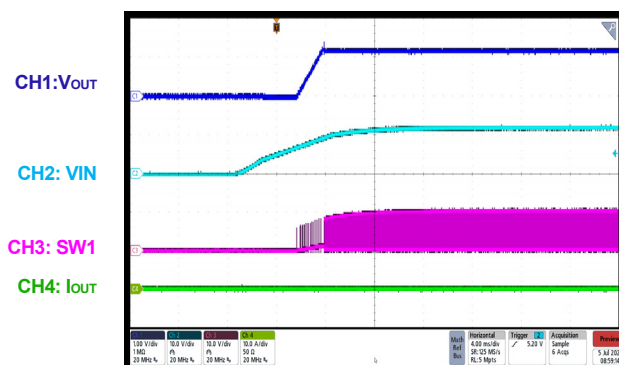
Steady State

$I_{OUT} = 12A$, FSW=750kHz, Paralleled mode, $V_{OUT/AC} = 10.8mV$



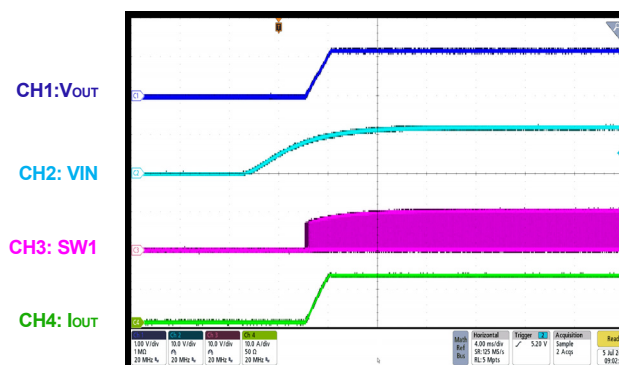
VIN Start-Up

$I_{OUT} = 0A$, Paralleled mode



VIN Start-Up

$I_{OUT} = 12A$, paralleled mode

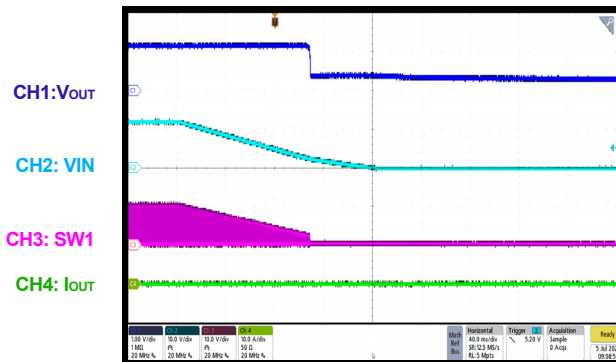


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are test on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 1.2V$, $C_{IN} = 2 \times 22\mu F$, $C_{OUT} = 3 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

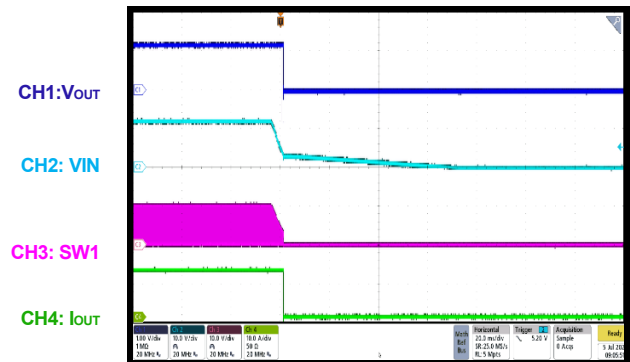
VIN Shut Down

I_{OUT}=0A, Paralleled mode



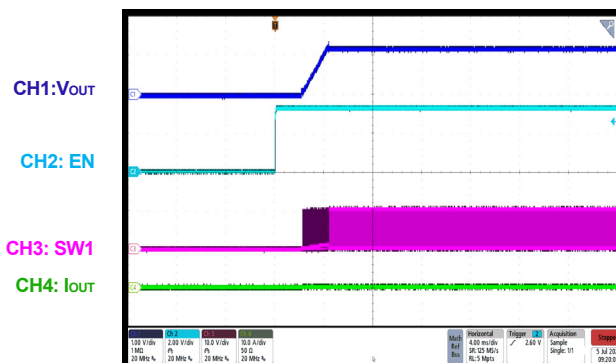
VIN Shut Down

I_{OUT}=12A, Paralleled mode



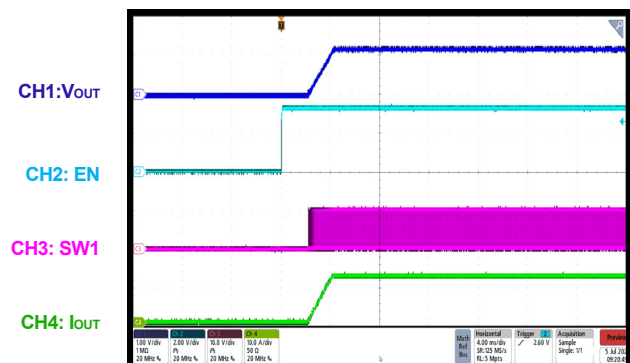
EN Start-Up

I_{OUT}=0A, Paralleled mode



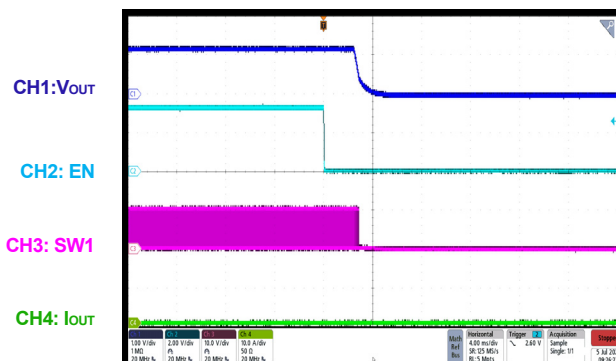
EN Start-Up

I_{OUT}=12A, Paralleled mode



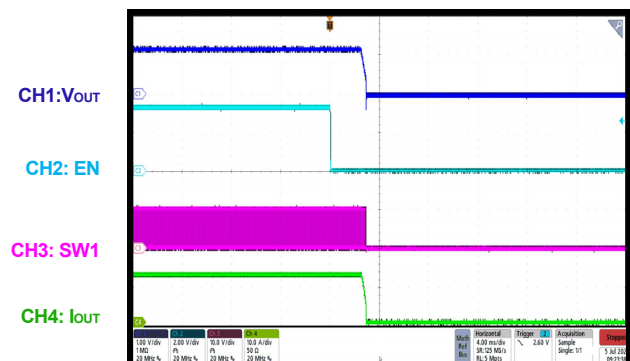
EN Shut Down

I_{OUT}=0A, Paralleled mode



EN Shut Down

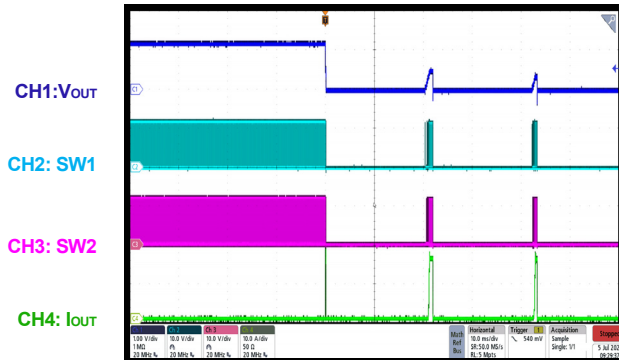
I_{OUT}=12A, Paralleled mode



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

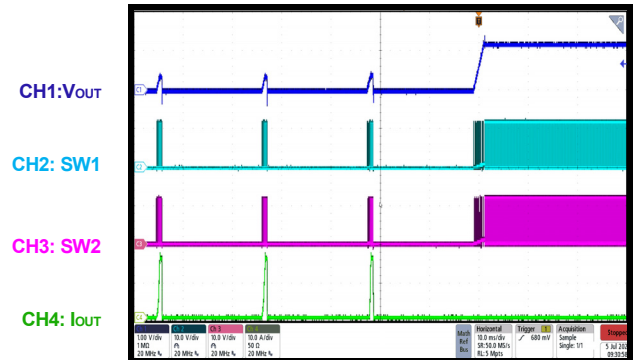
SCP Entry

Paralleled mode



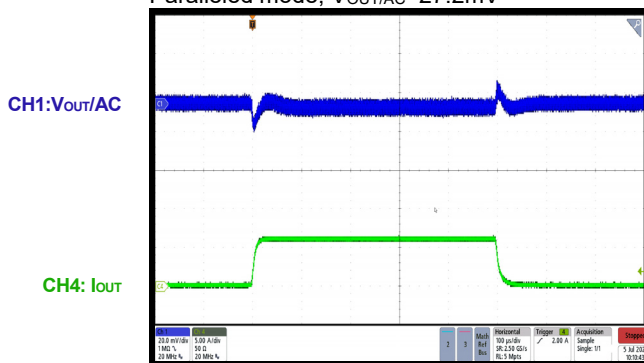
SCP Entry

Paralleled mode



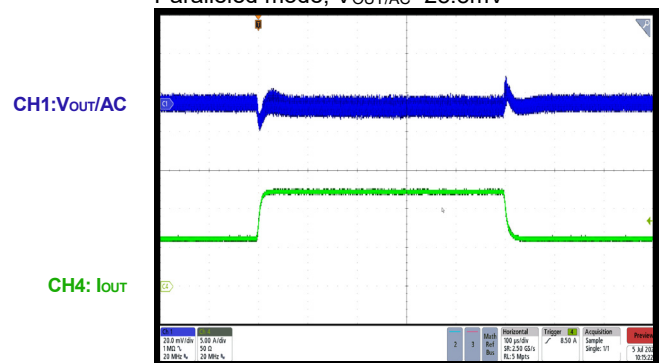
Load Transient

I_{OUT}=0A → 6A, Slew Rate 2.5A/us E-load, Paralleled mode, V_{OUT/AC}=27.2mV



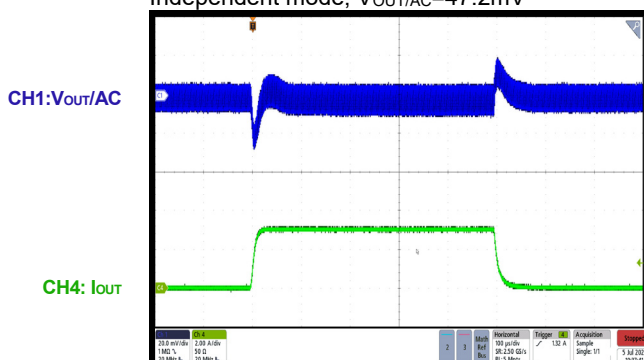
Load Transient

I_{OUT}= 6A→ 12A, Slew Rate = 2.5A/us E-load, Paralleled mode, V_{OUT/AC}=28.8mV



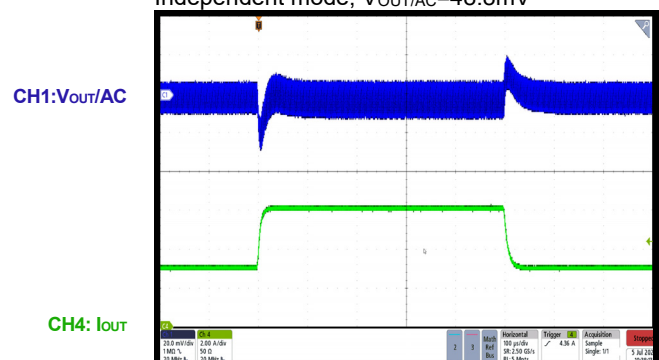
Load Transient

$I_{OUT}=0A \rightarrow 3A$, Slew Rate = $2.5A/\mu s$ E-load,
Independent mode, $V_{OUT/AC}=47.2mV$

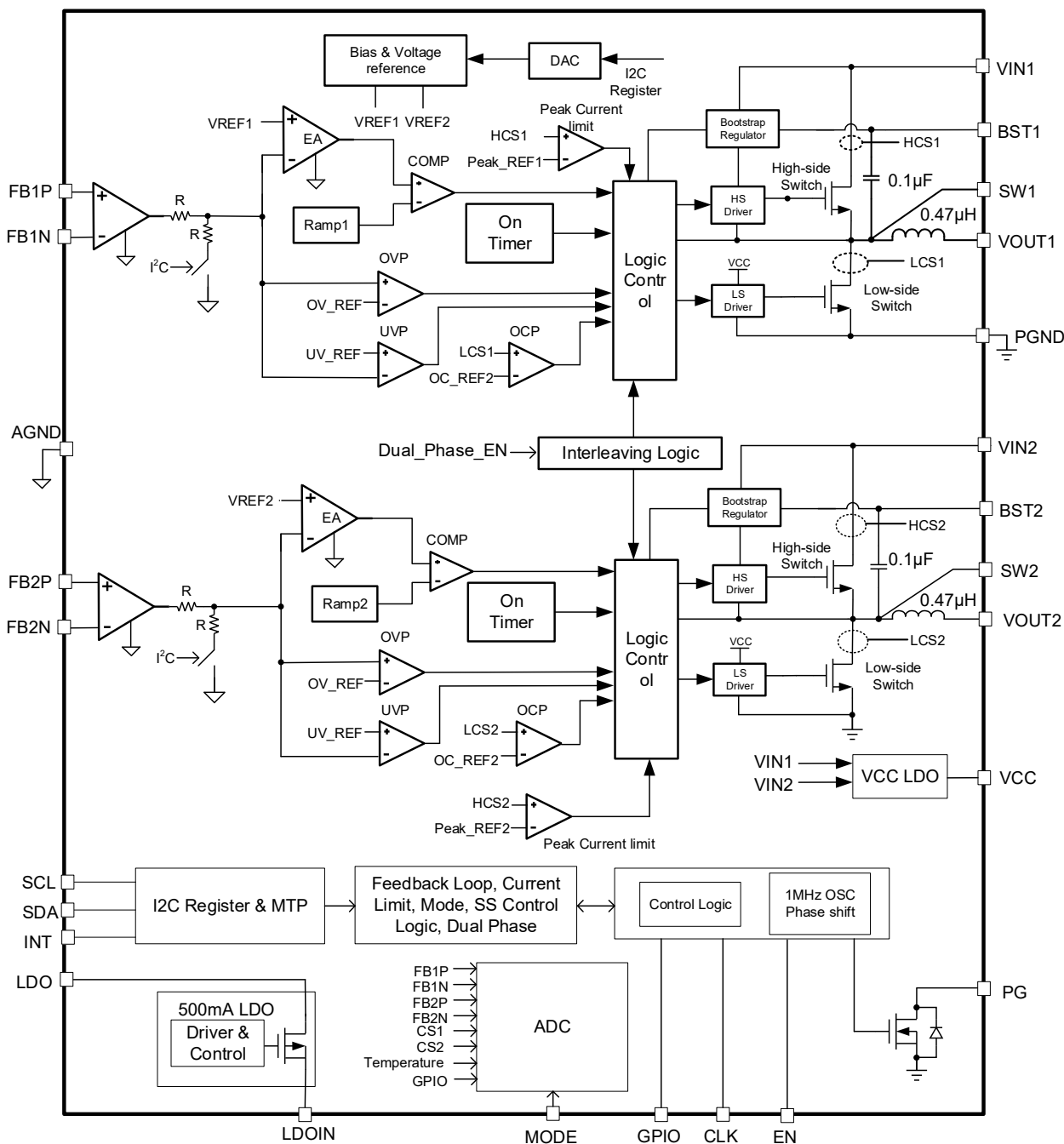


Load Transient

$I_{OUT}=3A \rightarrow 6A$, Slew Rate = $2.5A/\mu s$ E-load,
Independent mode, $V_{OUT/AC}=48.8mV$



FUNCTIONAL BLOCK DIAGRAM



MPM54522 Functional Block Diagram

OPERATION

High Efficiency Buck Regulators

MPM54522 is 2 channel power module. Buck 1 and Buck 2 are synchronous step-down DC/DC converters, which has built-in soft-start, compensation and hiccup current limit protection. Fixed frequency COT control provides fast transient response.

VIN Power Supply

VIN1 is the power supply of Buck 1. VIN2 is power supply of Buck 2. VIN1 to VIN2 are internal connected together and it is recommended to connect VIN1 to VIN2 together during application. When the input voltage is higher than the VIN UVLO rising threshold voltage, the corresponding Buck powers up if all the other startup conditions are met. It shuts down when the input voltage is lower than the VIN UVLO falling threshold voltage.

High Temperature Warning and Thermal Shutdown

The MPM54522 employs high temperature warning and critical temperature shutdown mechanism. MPM54522 monitors the junction temperature of the IC. If the junction temperature exceeds high temperature warning threshold set in Register 0x0F D[4:2], the MPM54522 sets the warning status Register 0x19 D[1]. The MPM54522 continues to operate as normal.

If the MPM54522 temperature goes above the threshold set in Register 0x0F D[7:5], the MPM54522 internally generates Disable command and disables Buck 1, Buck 2, and 500mA LDO, sets the OT status in Register 0x19 D[0], and de-assert PG output signal at the same time.

Soft Start and Soft Stop

MPM54522 employs a soft start and soft stop (SS) mechanism to ensure smooth output during power up and power down. When the part is enabled and the BST voltage reaches its rising threshold, internal DAC will output a Reference Voltage. The output voltage smoothly ramps up with the reference voltage. When the DAC output reaches the final voltage, it will stop at that level. At this point, the soft

start finishes and it enters steady state operation.

When the part is disabled, internal DAC output will ramp down. The output voltage smoothly ramps down with the reference voltage. When the DAC output reaches 300mV (when BUCK1_FB_HALF=1 or BUCK2_FB_HALF=1, the corresponding DAC output reaches 150mV), it will stop at that level. At this point, the soft stop finishes and output will be gradually discharged to 0V by FB1P and FB2P to GND resistance.

The soft-start time and soft-stop time both are programmable by Registers 0x41 and 0x48.

Over-Voltage Protection (OVP)

An output over voltage protection mechanism is implemented to limit the voltages on the MPM54522 output regulators. The MPM54522 actively monitors the output voltage on each enabled regulator.

There are two possibilities where MPM54522 recognizes the over voltage event:

Buck1 output goes above the threshold set in Register 0x05 D[1:0].

Buck2 output goes above the threshold set in Register 0x0A D[1:0].

The fault rail output will go into over voltage protection discharge mode once output voltage is higher than the setting threshold of regulation voltage and lasts more than 2.5μs. In OVP discharge mode, the low-side (LS) FET is turn-on and kept on until the LS current goes to negative current limit, this will discharge the output and try to keep output voltage within the normal range. If output voltage over voltage condition still exists, LS will turn-on again after a fixed delay to repeat the discharge behavior. Part exits this discharge mode when feedback voltage is decreased to threshold of the reference voltage.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MPM54522 has valley current limit control. During LS-FET turn-on state, the inductor current is monitored.

There are two possibilities where MPM54522

recognizes the over current event:

Buck1 inductor current above the valley current limit threshold set in Register 0x04 D[4:2].

Buck2 inductor current above the valley current limit threshold set in Register 0x09 D[4:2].

When the sensed inductor current is higher than the valley current limit threshold, the device enters over-current (OC) protection mode, HS-FET is not allowed to turn-on until inductor current drop to valley current limit. Meanwhile, the output voltage drops until it is below the under voltage (UV) threshold—typically 45% of the reference.

Once UV and OC are both triggered, the MPM54522 enters hiccup mode to periodically restart the related power rail. The hiccup duty cycle is very small to reduce the power dissipation during short circuit condition. During over-current protection, the device tries to recover from over-current fault with hiccup mode. During this period, the chip will disable output power stage, discharge soft-start capacitor and then automatically try to soft-start again. If the over current condition still exists when soft-start elapses, the device repeats this operation. The OCP is non-latch protection.

Active Voltage Position (AVP)

MPM54522 supports AVP by set the AVP_EN bit to 1 via I2C. An internal current-sense circuit produces the I_{droop} current source which is proportion to the internal sensing current. I_{droop} injects to FB pin to produce the feedback voltage with droop voltage. The actual output voltage ($V_{\text{OUT_AVP}}$) can be calculated with equal below:

$$V_{\text{OUT_AVP}} = V_{\text{OUT}} + \text{AVPx_OFFSET} - \text{AVPx_GAIN} \times I_{\text{OUT}} \times \text{FB_FACTOR}$$

Where V_{OUT} is the output voltage when AVP function is disabled. FB_FACTOR is a constant, which is determined by the BUCKx_FB_HALF (See Table 1).

AVPx_GAIN and AVPx_OFFSET can be set in Register 0x1F and Register 0x20 via I2C. And they also can be pre-programmed to MTP Registers 0x5C and 0x5D.

Table 1: FB_FACTOR Selection

BUCKx_FB_HALF*	FB_FACTOR
0	1
1	2

NOTE: *BUCKx_FB_HALF can be programmed by bit[5] of MTP Registers 0x44, 0x4B and bit[7:6] of MODE Registers 0x72, 0x7D, 0x88, 0x93, 0x9E, 0xA9, 0xB4, 0xBF.

Power Good (PG) Signal

The MPM54522 PG pin indicates status of VIN and all enabled output regulators (VOUT1, VOUT2, LDO). The MPM54522 floats PG pin (i.e it is High) when VIN is valid and all enabled output regulator's (VOUT1, VOUT2, LDO) tolerances are maintained as configured in the appropriate register space.

When the output voltages of the power rail VOUTx and LDO are within the power good tolerance threshold, the internal power good register bit PGx will be asserted (High). If the output voltages of the power rail VOUTx and LDO are out of the power good tolerance thresholds, the internal power good register bit PGx will be de-asserted (Low).

The power good status of all the enabled power rails will be used to determine following “AND” logic. If all the enabled rails have high PG status, the PG pin will be high. If one or more enabled rails have low PG status, or all the power rails are disabled, the PG pin will be low.

Interleaving For Dual Phase Operation

When interleaving mode is enabled by setting the Register 0x54 D[7] = “1”, MPM54522 Buck 1/2 operates 2-phase interleaving operation (Dual Phase Mode). The SET signal is triggered by comparing the FB signal and internal REF signal. When SET signal becomes high, only one phase's PWM output becomes high; at the next time of SET becomes high, next phase PWM output becomes high. In this way, automatic interleaving is realized.

When MPM54522 Buck 1 and Buck 2 works in dual phase interleaving operation mode, it senses two phase current and auto tune the buck Ton time to achieve current balance.

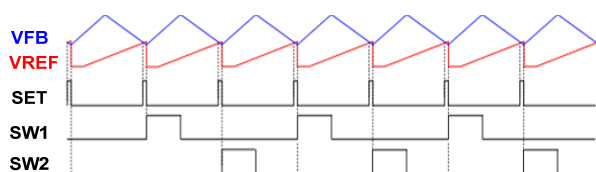


Figure 1: Buck1/2 interleaving for dual phase operation

Analog to Digital Converter (ADC)

The MPM54522 supports analog to digital converter (ADC) to monitor input supply voltages, output voltage regulator voltage (Buck1, Buck2, 500mA LDO,GPIO), and output voltage regulator current (Buck1, Buck2). The Register 0x10 D[7] allows to enable the ADC. The Registers 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18 provide the actual measurement of VOUT1, IOUT1, VOUT2, IOUT2, LDO GPIO, VIN.

MODE Pin Determined MTP Configuration

Some MTP configurations are determined by the resistor connected to MODE pin. 2% or higher accuracy is required for MODE resistor to guarantee correct MODE configuration. These functions are listed in “MODE Determined MTP Register Map” section, and the resistor-CONFIG selections are listed in Table 2.

Table 2: Recommended MODE Determined MTP Configuration Map Selection

MODE Resistor	MODE Determined MTP Configuration
0	MODE0, 0x70-0x7A
7.87kΩ	MODE1, 0x7B-0x85
16.5kΩ	MODE2, 0x86-0x90
30kΩ	MODE3, 0x91-0x9B
51kΩ	MODE4, 0x9C-0xA6
75kΩ	MODE5, 0xA7-0xB1
100kΩ	MODE6, 0xB2-0xBC
No connect or VCC	MODE7, 0xBD-0xC7

After power up, if MODE_EN = 1, the MPM54522 detects MODE pin resistor configuration, and select the corresponding MODEx. Then the MODEx MTP configurations are loaded into the corresponding MTP region registers and then into the I2C region registers.

Otherwise if MODE_EN = 0, the MTP region registers keep the original values, which are loaded into the I2C region registers.

I2C Address Configuration

I2C Address is determined by Register 0x60 D[6:0]. After power up, if MODE_EN = 1, the MPM54522 detects MODE pin resistor configuration, and select the corresponding MODEx. Then the 3 bit register I2C_ADDERSS in MODEx will substitute Register 0x60 D[2:0], the newly constructed 0x60 D[6:0] is current I2C Address.

For example, if we set Register 0x60 D[6:0]=0011000, Register 0x98 D[4:2]=011,when MPM54522 select MODE3 via MODE pin resistor, Register 0x60 D[2:0] will be substituted by 0x98 D[4:2], So the newly Register 0x60 D[6:0]=0011011, which is the current I2C Address.

Interrupt (INT)

INT pin is used to indicate the status of MPM54522. It's specified as an open-drain signal. Interrupts shall be active Low “latched” signal. When any status bit in Register 0x19 and 0x1A is changed to 1, a low level shall be output on INT pin.

The INT pin is held low until both of the following requirements are met:

1. The condition causing the interrupt no longer persists.
2. The register is cleared through I2C write to the clear bit.

All status bits should be latched to ‘1’ (based on their condition occurring). The latch shall remain a ‘1’ until the corresponding clear bit is written with a ‘1’. If an exception bit is cleared, but the condition continues to persist, a new interrupt will be generated (as if it is a new condition).

When the mask register bit is set to 1 (masked), the INT pin will not be low even though the corresponding status bit is triggered and set to 1.

FLEX-Timer Sequence Control

CLK Based Power Sequence Control

This CLK based FLEX-Timer Sequence Control scheme uses “Master-Slave” structure.

As shown in the picture below, the EN pins and CLK pins for all the PMICs are connected

together for the sequence control. The CLK pins should be pulled up to any one of the VCCs via a resistor (typical 10k Ω). One PMIC is configured as the master PMIC (PMIC1 in Figure 3), which generates clock signal output on the CLK pin. Other PMICs are configured as the slave PMICs, which receives the clock signal input on the CLK pin. The power ON/OFF sequence of all the power rails are synchronized by the clock signal.

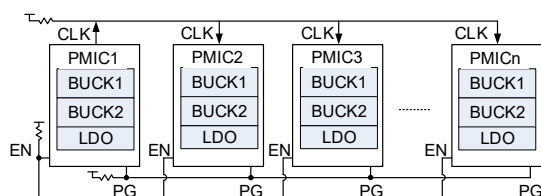


Figure 2: FLEX-Timer Sequence Control connection

When the EN pin is pulled high, the power ON sequence is started, the master PMIC starts generating the clock outputs. The slave PMICs counts the clock signal. For the power rail x in one master/slave PMIC, when the counted clock signal cycle reaches "Power_ON_Delay" (an internal non-volatile memory (NVM) register), the power rail x turns ON. When the master PMIC clock cycle reaches "CLK_Number" (NVM register in master PMIC) and PG goes high (all enabled power rails finish their soft-start process and PG pin is pulled high by an external resistor), the master PMIC stops the clock output, and the power ON sequence finishes. The master PMIC won't stop the clock outputs if the PG pin is float or pulled down.

When the EN pin is pulled low, the power OFF sequence is started, the master PMIC starts generating the clock outputs. The slave PMICs counts the clock signal. For the power rail x in one master/slave PMIC, when the counted clock signal cycle reaches "Power_OFF_Delay" (an internal NVM register), the power rail x turns OFF. When the master PMIC clock cycle reaches "CLK_Number", the master PMIC stops the clock output, and the power OFF sequence finishes.

Clock Pausing Function

For each master/slave PMIC, during the power ON/OFF sequence:

1. If the "CLK_Pause_EN" bit is "1", the master/slave PMIC pulls the CLK pin down during the soft start/stop of any power rails, as shown in Figure 3 and Figure 4. Otherwise if the "CLK_Pausing_EN" bit is "0", the master/slave PMIC does not pull the CLK pin during the soft start/stop of any power rails, as shown in Figure 5 and Figure 6.

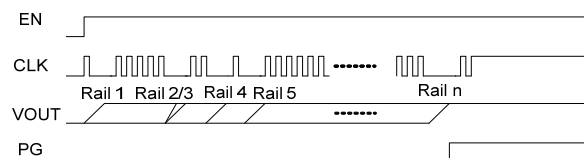


Figure 3: Soft start with CLK pausing

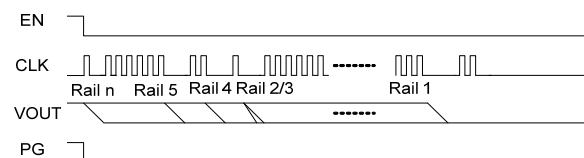


Figure 4: Soft stop with CLK pausing

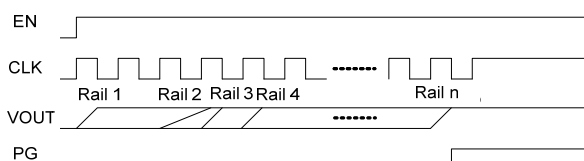


Figure 5: Soft start without CLK pausing

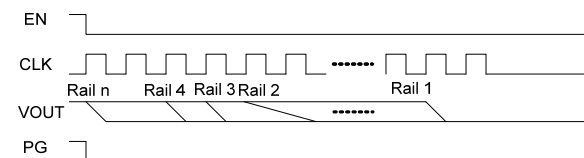


Figure 6: Soft stop without CLK pausing

2. If the "CLK_ON_Error_Pause_EN" bit is "1", the master/slave PMIC pulls the CLK pin down if any error occurs during the soft start of any power rails, as shown in Figure 7. Otherwise if the "CLK_ON_Error_Pause_EN" bit is "0", the master/slave PMIC does not pull the CLK pin even if any error occurs during the soft start of any power rails, as shown in Figure 8.

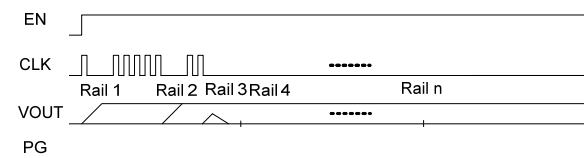


Figure 7: Soft start with CLK pausing during PMIC error

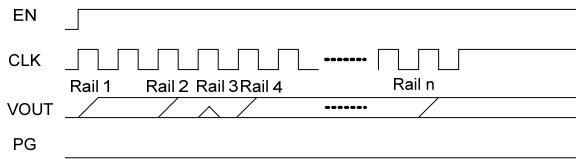


Figure 8: Soft start without CLK pausing during PMIC error

Meanwhile, the master PMIC is generating clock signal as well as monitoring the CLK pin status. When the master PMIC generates clock high (open-drain output) on CLK pin, but the CLK pin keeps low, the CLK pin must be pulled low by one or more master/slave PMIC. The master PMIC pauses the clock signal output, and resumes it until the CLK pin is released or detected high. If the CLK pin is not pulled low for clock pausing, the master PMIC should keep the clock signal output until the power ON/OFF sequence finishes.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MPM54522 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 9).

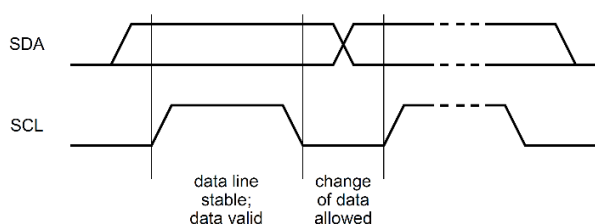


Figure 9: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is HIGH. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

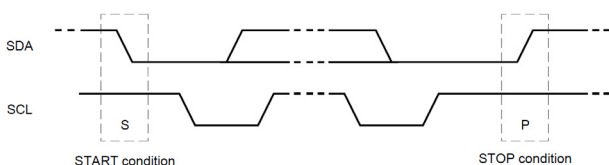


Figure 10: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition, and is considered

to be free again after a minimum of 4.7μs after the stop condition. The bus remains busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 11. After the start condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit data direction bit (R/W). A zero indicates a transmission (write), and a one indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

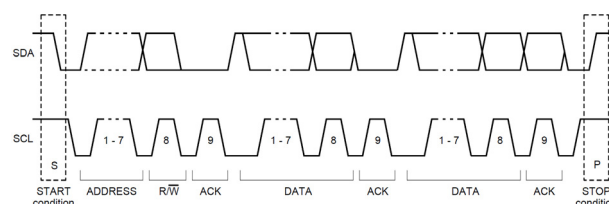


Figure 11: Complete Data Transfer

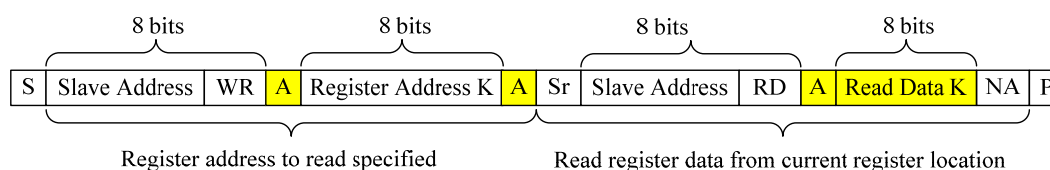
The MPM54522 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPM54522 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPM54522. The MPM54522 performs an update on the falling edge of the LSB byte.

I²C Write and Read Sequence Example



<input type="checkbox"/>	Master to Slave	A = Acknowledge (SDA = LOW)	S = Start Condition	WR Write = 0
<input checked="" type="checkbox"/>	Slave to Master	NA = NOT Acknowledge (SDA = HIGH)	P = Stop Condition	RD Read = 1

I²C Write Example --- Write Single Register



<input type="checkbox"/>	Master to Slave	A = Acknowledge (SDA = LOW)	S = Start Condition	Sr = Repeat Start Condition	WR Write = 0
<input checked="" type="checkbox"/>	Slave to Master	NA = NOT Acknowledge (SDA = HIGH)	P = Stop Condition		RD Read = 1

I²C Read Example --- Read Single Register

Register Attribute Definition

All volatile registers have Base Attributes as defined in Table 3. Some register attributes are further modified with Attribute Modifiers, as defined in Table 4.

Table 3: Register Base Attributes

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Writes have no effect.
Read/Write	RW	This bit can be read or written by host.
Write Only	W	This bit can only be written by host. Read from this bit returns '0'.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return '0' when read. Write has no effect.

Table 4: Register Attribute Modifier

Attribute	Abbreviation	Description
Write '1' Only	1O	This bit can only be set (i.e. write '1') but not reset (i.e. write '0'). Write '0' has no effect.
Protected	P	This bit is protected by the password registers. This bit cannot be written to unless the password code has been written into the password registers.
Persistent	E	This bit is persistent during power cycle.

Table 5: Register Map Breakdown

Register Range	Region	Comments
0x00 - 0x3F	I2C Region	Volatile memory registers
0x40 - 0x6F	MTP Region	Non Volatile Memory These registers require complete power cycle before it takes in effect. Changing these registers under normal operation is considered an illegal operation.
0x70 - 0xCF	MODE Region	Non Volatile Memory These registers are used to configure the default value for some registers in MTP region.

REGISTER DESCRIPTION

I2C Region Register Map

Add (0X)	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	LOCK	R/W	RV							I2C_LOCK_EN
01	BUCK1_CTRL1	R/W	VOUT1_GO_BIT	RV					VOUT1_SLEW_RATE	
02	BUCK1_CTRL2	R/W	BUCK1_PWM/PFM		BUCK1_FSW		RV	VOUT1_SETTING_LOW		
03	BUCK1_CTRL3	R/W	VOUT1_SETTING_HIGH							
04	BUCK1_CTRL4	R/W	VOUT1_DISCH_RG_EN	VOUT1_OVP_EN	RV	BUCK1_OC_TH			RV	
05	BUCK1_CTRL7	R/W	VOUT1_PG_VTH_HIGH		VOUT1_PG_VTH_LOW	RV	VOUT1_UV_VTH		VOUT1_OV_VTH	
06	BUCK2_CTRL1	R/W	VOUT2_GO_BIT	RV					VOUT2_SLEW_RATE	
07	BUCK2_CTRL2	R/W	BUCK2_PWM/PFM		BUCK2_FSW		RV	VOUT2_SETTING_LOW		
08	BUCK2_CTRL3	R/W	VOUT2_SETTING_HIGH							
09	BUCK2_CTRL4	R/W	VOUT2_DISCH_RG_EN	VOUT2_OVP_EN	RV	BUCK2_OC_TH			RV	
0A	BUCK2_CTRL7	R/W	VOUT2_PG_VTH_HIGH		VOUT2_PG_VTH_LOW		VOUT2_UV_VTH		VOUT2_OV_VTH	
0B	LDO_CTRL1	R/W	LDO_GO_BIT	RV			RV		LDO_DISCH_RG	LDO_PG_VTH
0C	LDO_CTRL2	R/W	RV	LDO_SETTING						
0D	SYS_CTRL1	R/W	PMIC_EN	VOUT1_EN	VOUT2_EN	LDO_EN	RV		GPIO_CTRL	
0E	SYS_CTRL3	R/W	VIN_PG_VTH			MASK_PG	RV			
0F	SYS_CTRL4	R/W	OT_TH			OTW_TH			RV	
10	ADC_CTRL1	R/W	ADC_EN	RV					ADC_SAMPLE_FREQ	
11	TEMPERATURE	RO	TEMPERATURE			RV				
12	VOUT1_ADC	RO	VOUT1_ADC							
13	IOUT1_ADC	RO	IOUT1_ADC							
14	VOUT2_ADC	RO	VOUT2_ADC							
15	IOUT2_ADC	RO	IOUT2_ADC							
16	LDO_ADC	RO	LDO_ADC							
17	GPIO_ADC	RO	GPIO_ADC							
18	VIN_ADC	RO	VIN_ADC							
19	FAULT_STATUS	RO	VIN_PG	VOUT1_PG	VOUT2_PG	LDO_PG	RV		OTW	OT
1A	STATUS1	RO	VIN_OV	VIN_UV	VOUT1_OV	VOUT2_OV	VOUT1_UV	VOUT2_UV	VOUT1_OC	VOUT2_OC



1B	MASK1	R/W	VIN_PG_MSK	VOUT1_PG_MSK	VOUT2_PG_MSK	LDO_PG_MSK	RV		OTW_MSK	OT_MSK
1C	MASK2	R/W	VIN_OV_MSK	VIN_UV_MSK	VOUT1_OV_MSK	VOUT2_OV_MSK	VOUT1_UV_MSK	VOUT2_UV_MSK	VOUT1_OC_MSK	VOUT2_OC_MSK
1D	CLEAR1	W1C	VIN_PG_CLEAR	VOUT1_FAULT_CLEAR	VOUT2_FAULT_CLEAR	LDO_FAULT_CLEAR	OTW_CLEAR	OT_CLEAR	RV	ALL_STATUS_CLEAR
1E	CLEAR2	W1C	VIN_OV_CLEAR	VIN_UV_CLEAR	VOUT1_OV_CLEAR	VOUT2_OV_CLEAR	VOUT1_UV_CLEAR	VOUT2_UV_CLEAR	VOUT1_OC_CLEAR	VOUT2_OC_CLEAR
1F	AVP_CTRL1	R/W	AVP1_EN	AVP1_GAIN		AVP1_OFFSET				
20	AVP_CTRL2	R/W	AVP2_EN	AVP2_GAIN		AVP2_OFFSET				
21	STATUS2	RO	VIN_PG_STATUS	VOUT1_PG_STATUS	VOUT2_PG_STATUS	LDO_PG_STATUS	RV		OT_WARNING_STATUS	OT_FAULT_STATUS

MTP Region Register Map

Add (0X)	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
40	LOCK	R/W/ P/E	MTP_REGION_ACCESS_PASSWORD							
41	BUCK1_C TRL1	R/W/ P/E	RV	VOUT1_SOFT_START			VOUT1_SOFT_STOP		VOUT1_SLEW_RATE	
42	BUCK1_C TRL2	R/W/ P/E	BUCK1_PWM/PFM		BUCK1_FSW		RV	VOUT1_SETTING_LOW		
43	BUCK1_C TRL3	R/W/ P/E	VOUT1_SETTING_HIGH							
44	BUCK1_C TRL4	R/W/ P/E	VOUT1_DISC HRG_EN	VOUT1_OV P_EN	BUCK1_FB_HA LF	BUCK1_OC_TH			RV	
45	BUCK1_C TRL5	R/W/ P/E	BUCK1_POWER_On_DELAY							
46	BUCK1_C TRL6	R/W/ P/E	BUCK1_POWER_OFF_DELAY							
47	BUCK1_C TRL7	R/W/ P/E	VOUT1_PG_VTH_HIGH		VOUT1_PG_VT H_LOW	RV	VOUT1_UV_VTH		VOUT1_OV_VTH	
48	BUCK2_C TRL1	R/W/ P/E	RV	VOUT2_SOFT_START			VOUT2_SOFT_STOP		VOUT2_SLEW_RATE	
49	BUCK2_C TRL2	R/W/ P/E	BUCK2_PWM/PFM		BUCK2_FSW		RV	VOUT2_SETTING_LOW		
4A	BUCK2_C TRL3	R/W/ P/E	VOUT2_SETTING_HIGH							
4B	BUCK2_C TRL4	R/W/ P/E	VOUT2_DISC HRG_EN	VOUT2_OV P_EN	BUCK2_FB_HA LF	BUCK2_OC_TH			RV	
4C	BUCK2_C TRL5	R/W/ P/E	BUCK2_POWER_On_DELAY							
4D	BUCK2_C TRL6	R/W/ P/E	BUCK2_POWER_OFF_DELAY							
4E	BUCK2_C TRL7	R/W/ P/E	VOUT2_PG_VTH_HIGH		VOUT2_PG_VT H_LOW	RV	VOUT2_UV_VTH		VOUT2_OV_VTH	
4F	LDO_CTR L1	R/W/ P/E	RV	LDO_SOFT_START			RSVD		LDO_DISCH RG	LDO_PG_V TH
50	LDO_CTR L2	R/W/ P/E	RV	LDO_SETTING						
51	LDO_CTR L3	R/W/ P/E	LDO_POWER_ON_DELAY							
52	LDO_CTR L4	R/W/ P/E	LDO_POWER_OFF_DELAY							
53	SYS_CTR L1	R/W/ P/E	PMIC_EN	VOUT1_EN	VOUT2_EN	LDO_EN	RV		GPIO_CTRL	
54	SYS_CTR L3	R/W/ P/E	SINGLE/DUAL	REV_CODE						
55	SYS_CTR L3	R/W/ P/E	VIN_PG_VTH			MASK_PG	PG_DEL AY_EN	VIN_OVP_ EN	RV	HICCUP
56	SYS_CTR L4	R/W/ P/E	OT_TH			OTW_TH			VIN_UV_SEL	
57	GPIO_CO NFIG	R/W/ P/E	GPIO_POWER_ON_DELAY							
58	GPIO_CO NFIG	R/W/ P/E	GPIO_POWER_OFF_DELAY							
59	ADC_CTR L2	R/W/ P/E	ADC_EN	RV					ADC_SAMPLE_FREQ	
5A	MASK1	R/W/ P/E	VIN_PG_MSK	VOUT1_PG_ MSK	VOUT2_PG_M SK	LDO_PG_ MSK	RV		OTW_MSK	OT_MSK
5B	MASK2	R/W/ P/E	VIN_OV_MSK	VIN_UV_M SK	VOUT1_OV_M SK	VOUT2_OV_ MSK	VOUT1_ UV_MSK	VOUT2_U V_MSK	VOUT1_OC_ MSK	VOUT2_OC_ MSK
5C	AVP_CTR L1	R/W/ P/E	AVP1_EN	AVP1_GAIN		AVP1_OFFSET				



5D	AVP_CTR L2	R/W/ P/E	AVP2_EN	AVP2_GAIN	AVP2_OFFSET			
5E	CLK_CTR L1	R/W/ P/E	CLK_MODE	CLK FREQUENCY		CLK NUMBER		RV
5F	CLK_CTR L2	R/W/ P/E	RV			CLK PAUSE EN	CLK ON ERROR PAUSE EN	RV
60	I2C_CON FIG	R/W/ P/E	MODE_EN	I2C_ADDRESS				
61	MTP CTRL1	R/W/ P/E	MTP_PASSWORD					
62	MTP CTRL2.	R/W/ P/E	RV			MTP_RES TORE	MTP_PROGRAM	
63	RV	R/W/ P/E	RV					
64	ID2	R/W/ P/E	MTP_CODE					

MODE Region Register Map

Add (0X)	R/W	D7	D6	D5	D4	D3	D2	D1	D0
70	RWPE	MODE0 VOUT1 SETTING HIGH							
71	RWPE	MODE0 VOUT2 SETTING HIGH							
72	RWPE	MODE0 BUCK1_FB_HALF	MODE0 BUCK2_FB_HALF	MODE0 VOUT1 SETTING LOW		MODE0 VOUT2 SETTING LOW			
73	RWPE	MODE0 CLK MODE	MODE0 SINGLE/DUAL	RV		MODE0 BUCK1 FSW		MODE0 BUCK2 FSW	
74	RWPE	MODE0 BUCK1 POWER ON DELAY							
75	RWPE	MODE0 BUCK2 POWER ON DELAY							
76	RWPE	MODE0 VOUT1 soft start time			MODE0 VOUT2 soft start time			MODE0 LDO EN	RV
77	RWPE	MODE0 LDO soft start time			MODE0 I2C ADDRESS			MODE0 GPIO CTRL	
78	RWPE	MODE0 LDO SETTING							
79	RWPE	MODE0 LDO POWER ON DELAY							
7A	RWPE	MODE0 GPIO POWER ON DELAY							
7B	RWPE	MODE1 VOUT1 SETTING HIGH							
7C	RWPE	MODE1 VOUT2 SETTING HIGH							
7D	RWPE	MODE1 BUCK1_FB_HALF	MODE1 BUCK2_FB_HALF	MODE1 VOUT1 SETTING LOW		MODE1 VOUT2 SETTING LOW			
7E	RWPE	MODE1 CLK MODE	MODE1 SINGLE/DUAL	RV		MODE1 BUCK1 FSW		MODE1 BUCK2 FSW	
7F	RWPE	MODE1 BUCK1 POWER ON DELAY							
80	RWPE	MODE1 BUCK2 POWER ON DELAY							
81	RWPE	MODE1 VOUT1 soft start time			MODE1 VOUT2 soft start time			MODE1 LDO EN	RV
82	RWPE	MODE1 LDO soft start time			MODE1 I2C ADDRESS			MODE1 GPIO CTRL	
83	RWPE	MODE1 LDO SETTING							
84	RWPE	MODE1 LDO POWER ON DELAY							
85	RWPE	MODE1 GPIO POWER ON DELAY							
86	RWPE	MODE2 VOUT1 SETTING HIGH							
87	RWPE	MODE2 VOUT2 SETTING HIGH							
88	RWPE	MODE2 BUCK1_FB_HALF	MODE2 BUCK2_FB_HALF	MODE2 VOUT1 SETTING LOW		MODE2 VOUT2 SETTING LOW			
89	RWPE	MODE2 CLK MODE	MODE2 SINGLE/DUAL	RV		MODE2 BUCK1 FSW		MODE2 BUCK2 FSW	
8A	RWPE	MODE2 BUCK1 POWER ON DELAY							
8B	RWPE	MODE2 BUCK2 POWER ON DELAY							
8C	RWPE	MODE2 VOUT1 soft start time			MODE2 VOUT2 soft start time			MODE2 LDO EN	RV



8D	RWPE	MODE2 LDO soft start time			MODE2 I2C ADDRESS		MODE2 GPIO CTRL	
8E	RWPE	MODE2 LDO SETTING						
8F	RWPE	MODE2 LDO POWER ON DELAY						
90	RWPE	MODE2 GPIO POWER ON DELAY						
91	RWPE	MODE3 VOUT1 SETTING HIGH						
92	RWPE	MODE3 VOUT2 SETTING HIGH						
93	RWPE	MODE3 BUCK1_FB_HALF	MODE3 BUCK2_FB_HALF	MODE3 VOUT1 SETTING LOW		MODE3 VOUT2 SETTING LOW		
94	RWPE	MODE3 CLK MODE	MODE3 SINGLE/DUAL	RV	MODE3 BUCK1 FSW	MODE3 BUCK2 FSW		
95	RWPE	MODE3 BUCK1 POWER ON DELAY						
96	RWPE	MODE3 BUCK2 POWER ON DELAY						
97	RWPE	MODE3 VOUT1 soft start time			MODE3 VOUT2 soft start time		MODE3 LDO EN	RV
98	RWPE	MODE3 LDO soft start time			MODE3 I2C ADDRESS		MODE3 GPIO CTRL	
99	RWPE	MODE3 LDO SETTING						
9A	RWPE	MODE3 LDO POWER ON DELAY						
9B	RWPE	MODE3 GPIO POWER ON DELAY						
9C	RWPE	MODE4 VOUT1 SETTING HIGH						
9D	RWPE	MODE4 VOUT2 SETTING HIGH						
9E	RWPE	MODE4 BUCK1_FB_HALF	MODE4 BUCK2_FB_HALF	MODE4 VOUT1 SETTING LOW		MODE4 VOUT2 SETTING LOW		
9F	RWPE	MODE4 CLK MODE	MODE4 SINGLE/DUAL	RV	MODE4 BUCK1 FSW	MODE4 BUCK2 FSW		
A0	RWPE	MODE4 BUCK1 POWER ON DELAY						
A1	RWPE	MODE4 BUCK2 POWER ON DELAY						
A2	RWPE	MODE4 VOUT1 soft start time			MODE4 VOUT2 soft start time		MODE4 LDO EN	RV
A3	RWPE	MODE4 LDO soft start time			MODE4 I2C ADDRESS		MODE4 GPIO CTRL	
A4	RWPE	MODE4 LDO SETTING						
A5	RWPE	MODE4 LDO POWER ON DELAY						
A6	RWPE	MODE4 GPIO POWER ON DELAY						
A7	RWPE	MODE5 VOUT1 SETTING HIGH						
A8	RWPE	MODE5 VOUT2 SETTING HIGH						
A9	RWPE	MODE5 BUCK1_FB_HALF	MODE5 BUCK2_FB_HALF	MODE5 VOUT1 SETTING LOW		MODE5 VOUT2 SETTING LOW		
AA	RWPE	MODE5 CLK MODE	MODE5 SINGLE/DUAL	RV	MODE5 BUCK1 FSW	MODE5 BUCK2 FSW		
AB	RWPE	MODE5 BUCK1 POWER ON DELAY						
AC	RWPE	MODE5 BUCK2 POWER ON DELAY						



AD	RWPE	MODE5 VOUT1 soft start time			MODE5 VOUT2 soft start time		MODE5 LDO EN		RV
AE	RWPE	MODE5 LDO soft start time			MODE5 I2C ADDRESS		MODE5 GPIO CTRL		
AF	RWPE	MODE5 LDO SETTING							
B0	RWPE	MODE5 LDO POWER ON DELAY							
B1	RWPE	MODE5 GPIO POWER ON DELAY							
B2	RWPE	MODE6 VOUT1 SETTING HIGH							
B3	RWPE	MODE6 VOUT2 SETTING HIGH							
B4	RWPE	MODE6 BUCK1_FB_HALF	MODE6 BUCK2_FB_HALF	MODE6 VOUT1 SETTING LOW			MODE6 VOUT2 SETTING LOW		
B5	RWPE	MODE6 CLK MODE	MODE6 SINGLE/DUAL	RV		MODE6 BUCK1 FSW		MODE6 BUCK2 FSW	
B6	RWPE	MODE6 BUCK1 POWER ON DELAY							
B7	RWPE	MODE6 BUCK2 POWER ON DELAY							
B8	RWPE	MODE6 VOUT1 soft start time			MODE6 VOUT2 soft start time		MODE6 LDO EN		RV
B9	RWPE	MODE6 LDO soft start time			MODE6 I2C ADDRESS		MODE6 GPIO CTRL		
BA	RWPE	MODE6 LDO SETTING							
BB	RWPE	MODE6 LDO POWER ON DELAY							
BC	RWPE	MODE6 GPIO POWER ON DELAY							
BD	RWPE	MODE7 VOUT1 SETTING HIGH							
BE	RWPE	MODE7 VOUT2 SETTING HIGH							
BF	RWPE	MODE7 BUCK1_FB_HALF	MODE7 BUCK2_FB_HALF	MODE7 VOUT1 SETTING LOW			MODE7 VOUT2 SETTING LOW		
C0	RWPE	MODE7 CLK MODE	MODE7 SINGLE/DUAL	RV		MODE7 BUCK1 FSW		MODE7 BUCK2 FSW	
C1	RWPE	MODE7 BUCK1 POWER ON DELAY							
C2	RWPE	MODE7 BUCK2 POWER ON DELAY							
C3	RWPE	MODE7 VOUT1 soft start time			MODE7 VOUT2 soft start time		MODE7 LDO EN		RV
C4	RWPE	MODE7 LDO soft start time			MODE7 I2C ADDRESS		MODE7 GPIO CTRL		
C5	RWPE	MODE7 LDO SETTING							
C6	RWPE	MODE7 LDO POWER ON DELAY							
C7	RWPE	MODE7 GPIO POWER ON DELAY							

REGISTER DISCRIPTION

I2C Register Region

I2C Registers are volatile memories. These registers directly control PMIC operation.

LOCK (00h)

Format: Unsigned binary

The LOCK command sets the write Lock for I2C Register Region.

Bits	Access	Bit name	Default	Description
D[0]	R/W	I2C_LOCK_EN	1'b 1	Write Lock for I2C Register Region. 0 = Disable write lock 1 = Enable write lock. I2C region writing is not effective when LOCK_EN = 1.

BUCK1_CTRL1 (01h)

Format: Unsigned binary

The BUCK1_CTRL1 command sets GO_BIT and slew rate of VOUT1.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VOUT1_GO_BIT	1'b 0	1'b 0: disable change of VOUT1_SETTING 1: enable change of VOUT1_SETTING on the fly VOUT1_GO_BIT is a self-clear bit. Make the new VOUT1_SETTING configuration first, then set VOUT1_GO_BIT = 1 to start the dynamic voltage scaling. When VOUT1 reaches the new voltage target, VOUT1_GO_BIT will automatically clear.
D[6:2]	R/W	RV	5'b 0000 0	Reserved
D[1:0]	R/W	VOUT1_SLEW_RATE	2'b 00	VOUT1 slew rate during dynamic voltage scaling(no external FB divider resistor) 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK1_CTRL2 (02h)

Format: Unsigned binary

The BUCK1_CTRL2 command sets operation mode and Fsw of VOUT1.

Bits	Access	Bit name	Default	Description
D[7:6]	RW	BUCK1_PFM/PWM	2'b 11	Buck1 Mode Selection 00, 01 = Reserved 2'b 10: COT; DCM (Constant on Time; Discontinuous Current Mode at the light load) 2'b 11: COT; Forced CCM (Constant on Time; Continuous Current Mode)
D[5:4]	RW	BUCK1_FSW	2'b 01	Buck1 Switching Frequency 2'b 00: 500 KHz 2'b 01: 750 KHz 2'b 10: 1000 KHz 2'b 11: 1250 KHz
D[3]	RW	RV	1'b 0	Reserved
D[2:0]	RW	VOUT1_SETTING_LOW	3'b 000 OR MODE DETERMINED	Combined with VOUT_SETTING_HIGH to set VOUT1 voltage.

BUCK1_CTRL3 (03h)
Format: Direct

The BUCK1_CTRL3 command sets VOUT1 voltage.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	VOUT1_SETTING_HIGH	8'b 0011 0010 OR MODE DETERMINED	<p>VOUT_SETTING_HIGH register works together with VOUT_SETTING_LOW register. Adding them up together, the 11-bit register controls the output voltage.</p> <p>VOUT1 setting when BUCK1_FB_HALF = 0: the bits value \leq 001 0010 1100(300d), the setting = 300mV. 001 0010 1100(300d) \leq the bits value \leq 111 1111 1111(2047d) and the bits value are defined equal to X, the setting = X mV, 1mV/step.</p> <p>VOUT1 setting when BUCK1_FB_HALF = 1: the bits value \leq 000 1001 0110(150d), the setting = 300mV. 000 1001 0110(150d) \leq the bits value \leq 111 0110 1100 (1900d) and the bits value are defined equal to X, the setting = 2*X mV, 2mV/step. The bits value \geq 111 0110 1100 (1900d), the setting=3800mV.</p>

BUCK1_CTRL4 (04h)
Format: Unsigned binary

The BUCK1_CTRL4 command sets Enable/Disable of VOUT1 discharge, over voltage protection and over current threshold.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VOUT1_DISCHARGE_EN	1'b 1	<p>Enable bit of Buck1 output passive discharge function. 0 = Disable the passive discharge function; 1 = Enable the passive discharge function</p> <p>If passive discharge function is enabled, when Buck 1 is disabled, a discharging resistor is connected to VOUT1_FB_P pin to discharge VOUT1 until 100mV.</p>
D[6]	R/W	VOUT1_OVP_EN	1'b 1	<p>Enable the Buck1 output active OVP function 0 = output OVP is disabled 1 = output OVP is enabled</p> <p>If output OVP is enabled, Buck1 actively turns on LSFET to discharge VOUT1. Refer to operation for more details.</p>
D[5]	R/W	RV	1'b 0	Reserved.
D[4:2]	R/W	BUCK1_OC_TH	3'b 101	<p>Buck1 Valley Current Limit Threshold selection.</p> <p>3'b 000 = 4.0 A 3'b 001 = 4.5 A 3'b 010 = 5.0 A 3'b 011 = 5.5 A 3'b 100 = 6.0 A 3'b 101 = 6.5 A 3'b 110 = 7.0 A 3'b 111 = 7.5 A</p>
D[1:0]	R/W	RV	2'b 00	Reserved.

BUCK1_CTRL7 (05h)
Format: Unsigned binary

The BUCK1_CTRL7 command sets threshold of VOUT1_PG_HIGH, VOUT1_PG_LOW, VOUT1_UV, VOUT1_OV.

Bits	Access	Bit name	Default	Description
D[7:6]	R/W	VOUT1_PG_VTH_HIGH	2'b 00	VOUT1 High Side Voltage For Power Good Status(no external FB divider resistor) 2'b 00: +5% from VOUT1_SETTING 2'b 01: +7.5% from VOUT1_SETTING 2'b 10: +10% from VOUT1_SETTING 2'b 11: Reserved Hysteresis = 2.5%
D[5]	R/W	VOUT1_PG_VTH_LOW	1'b 0	VOUT1 Threshold Low Side Voltage For Power Good Status 0 = -5% from VOUT1_SETTING 1 = -7.5% from VOUT1_SETTING Hysteresis = 2.5%
D[4]	R/W	RV	1'b 0	Reserved
D[3:2]	R/W	VOUT1_UV_VTH	2'b 00	VOUT1 Threshold For Under Voltage Status 2'b 00: -10% from VOUT1_SETTING 2'b 01: -12.5% from VOUT1_SETTING 2'b 10: Reserved 2'b 11: Reserved Hysteresis = 2.5%
D[1:0]	R/W	VOUT1_OV_VTH	2'b 10	VOUT1 Threshold For Over Voltage Status 2'b 00: +7.5% from VOUT1_SETTING 2'b 01: +10% from VOUT1_SETTING 2'b 10: +12.5% from VOUT1_SETTING 2'b 11: Reserved Hysteresis = 2.5%

BUCK2_CTRL1 (06h)
Format: Unsigned binary

The BUCK2_CTRL1 command sets GO_BIT and slew rate of VOUT2.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VOUT2_GO_BIT	1'b 0	0 = disable change of VOUT2_SETTING 1 = enable change of VOUT2_SETTING on the fly VOUT2_GO_BIT is a self-clear bit. Make the new VOUT2_SETTING configuration first, then set VOUT2_GO_BIT = 1 to start the dynamic voltage scaling. When VOUT2 reaches the new voltage target, VOUT2_GO_BIT will automatically clear.
D[6:2]	R/W	RV	5'b 0000 0	Reserved
D[1:0]	R/W	VOUT2_SLEW_RATE	2'b 00	VOUT2 slew rate during dynamic voltage scaling(no external FB divider resistor) 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK2_CTRL2 (07h)

Format: Unsigned binary

The BUCK2_CTRL2 command sets operation mode and Fsw of VOUT2.

Bits	Access	Bit name	Default	Description
D[7:6]	RW	BUCK2_PFM/PWM	2'b 11	Buck2 Mode Selection 00,01 = Reserved 2'b 10: COT; DCM (Constant on Time; Discontinuous Current Mode) 2'b 11: COT; Forced CCM (Constant on Time; Continuous Current Mode)
D[5:4]	RW	BUCK2_FSW	2'b 01	Buck2 Switching Frequency 2'b 00: 500 KHz 2'b 01: 750 KHz 2'b 10: 1000 KHz 2'b 11: 1250 KHz
D[2:0]	RW	VOUT2_SETTING_LOW	3'b 000 OR MODE DETERMINED	Combined with VOUT_SETTING_HIGH to set VOUT2 voltage.

BUCK2_CTRL3 (08h)

Format: Direct

The BUCK2_CTRL3 command sets VOUT2 voltage.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	VOUT2_SETTING_HIGH	8'b 0011 0010 OR MODE DETERMINED	VOUT_SETTING_HIGH register works together with VOUT_SETTING_LOW register. Adding them up together, the 11-bit register controls the output voltage. VOUT1 setting when BUCK1_FB_HALF = 0: the bits value \leq 001 0010 1100(300d), the setting = 300mV. 001 0010 1100(300d) \leq the bits value \leq 111 1111 1111(2047d) and the bits value are defined equal to X, the setting = X mV, 1mV/step. VOUT1 setting when BUCK1_FB_HALF = 1: the bits value \leq 000 1001 0110(150d), the setting = 300mV. 000 1001 0110(150d) \leq the bits value \leq 111 0110 1100 (1900d) and the bits value are defined equal to X, the setting = 2*X mV, 2mV/step. The bits value \geq 111 0110 1100 (1900d), the setting=3800mV.

BUCK2_CTRL4 (09h)

Format: Unsigned binary

The BUCK2_CTRL4 command sets Enable/Disable of VOUT2 discharge, over voltage protection and over current threshold.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VOUT2_DISCHARGE_EN	1'b 1	Enable bit of Buck1 output passive discharge function. 0 = Disable the passive discharge function; 1 = Enable the passive discharge function If passive discharge function is enabled, when Buck 1 is disabled, a discharging resistor is connected to VOUT2_FB_P pin to discharge VOUT2 until 100mV.

D[6]	R/W	VOUT2_O VP_EN	1'b 1	Enable the Buck1 output active OVP function 0 = output OVP disabled 1 = output OVP enabled If output OVP is enabled, Buck1 actively turns on LSFET to discharge VOUT2. Refer to operation for more details.
D[5]	R/W	RV	1'b 0	Reserved
D[4:2]	R/W	BUCK2 OC TH	3'b 101	Buck2 Valley Current Limit Threshold 3'b 000 = 4.0 A 3'b 001 = 4.5 A 3'b 010 = 5.0 A 3'b 011 = 5.5 A 3'b 100 = 6.0 A 3'b 101 = 6.5 A 3'b 110 = 7.0 A 3'b 111 = 7.5 A

BUCK2_CTRL7 (0Ah)

Format: Unsigned binary

The BUCK2_CTRL7 command sets threshold of VOUT2_PG_HIGH, VOUT2_PG_LOW, VOUT2_UV, VOUT2_OV.

Bits	Access	Bit name	Default	Description
D[7:6]	R/W	VOUT2_P G_VTH_HI GH	2'b 00	VOUT2 High Side Voltage For Power Good Status. 2'b 00: +5% from VOUT2_SETTING 2'b 01: +7.5% from VOUT2_SETTING 2'b 10: +10% from VOUT2_SETTING 2'b 11: Reserved Hysteresis = 2.5%
D[5]	R/W	VOUT2_P G_VTH_LO W	1'b 0	VOUT2 Threshold Low Side Voltage For Power Good Status. 0 = -5% from VOUT2_SETTING 1 = -7.5% from VOUT2_SETTING Hysteresis = 2.5%
D[4]	RW	RV	1'b 0	Reserved
D[3:2]	R/W	VOUT2_UV _VTH	2'b 00	VOUT2 Threshold For Under Voltage Status. 2'b 00: -10% from VOUT2_SETTING 2'b 01: -12.5% from VOUT2_SETTING 2'b 10: Reserved 2'b 11: Reserved Hysteresis = 2.5%
D[1:0]	R/W	VOUT2_O V_VTH	2'b 10	VOUT2 Threshold For Over Voltage Status. 2'b 00: +7.5% from VOUT2_SETTING 2'b 01: +10% from VOUT2_SETTING 2'b 10: +12.5% from VOUT2_SETTING 2'b 11: Reserved Hysteresis = 2.5%

LDO_CTRL1 (0Bh)

Format: Unsigned binary

The LDO_CTRL1 command sets GO_BIT, discharge, PG threshold of LD0.

Bits	Access	Bit name	Default	Description
D[7]	R/W	LDO_GO_ BIT	1'b 0	0 = disable change of LDO_SETTING on the fly. 1 = enable change of LDO_SETTING on the fly.

D[6:2]	RV	RV	5'b 0000 0	Reserved.
D[1]	R/W	LDO_DISC HG	1'b 1	0 = disable LDO discharge 1 = enable LDO discharge
D[0]	R/W	LDO_PG_V TH	1'b 0	LDO Output Threshold Voltage for Power Good Status 0 = -10% from LDO_SETTHING 1 = -15% from LDO_SETTHING Hysteresis = 5%

LDO_CTRL2 (0Ch)

Format: Direct

The LDO_CTRL2 command sets LD0 output.

Bits	Access	Bit name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved
D[6:0]	R/W	LDO_SETT ING	7'b 011 1100 OR MODE DETERMIN ED	LDO output voltage setting: 30mV per LSB from 0.6V to 3.6V All lower setting = Reserved 001 0100: 600 mV 001 0101 = 630 mV ... 111 1111 = 3810 mV All higher setting = Reserved

SYS_CTRL1 (0Dh)

Format: Unsigned binary

The SYS_CTRL1 command sets Enable/Disable of PMIC, VOUT1, VOUT2, LDO and GPIO.

Bits	Access	Bit name	Default	Description
D[7]	R/W	PMIC_EN	1'b 1	0 = Buck1, Buck2, LDO are all disabled 1 = Buck1, Buck2, LDO are all enabled (still need to enable each regulator by I2C setup)
D[6]	R/W	VOUT1_EN	1'b 1	0 = Buck1 Disable 1 = Buck1 Enable
D[5]	R/W	VOUT2_EN	1'b 1	0 = Buck2 Disable 1 = Buck2 Enable
D[4]	R/W	LDO_EN	1'b 0	0 = LDO Disable 1 = LDO Enable
D[3:2]	R/W	RV	2'b 00	Reserved
D[1:0]	R/W	GPIO_CTR L	2'b 10	GPIO open-drain output control. 2'b 00: GPIO output is low. 2'b 01: Reserved 2'b 10: GPIO is part of flex-time control and used as external converter's enable signal. GPIO outputs as an EN signal of external converter and its on/off sequence can be programmed in 0x57 and 0x58 registers. 2'b 11: GPIO output is floating/high.

SYS_CTRL3 (0Eh)

Format: Unsigned binary

The SYS_CTRL3 command sets VIN_PG threshold and PG mask.

Bits	Access	Bit name	Default	Description
D[7:5]	R/W	VIN_PG_V TH	3'b 110	VIN Rising Threshold Voltage for VIN_PG Bit. VIN_PG bit(0x19) is 0(power good) even VIN<VIN PG falling threshold after VIN startup. Then ramp up VIN≥VIN rising threshold, If VIN triggers the VIN PG falling threshold again, VIN_PG bit changes to be 1(power not good). 3'b 000: 9.5 V, same as 001 3'b 001: 9.5 V 3'b 010: 8.5 V 3'b 011: 7.5 V 3'b 100: 6.5 V 101 = 5.5 V 110 = 4.25 V 111 = Reserved Hysteresis = 0.5V
D[4]	R/W	MASK_PG	1'b 0	Mask off the INT pin behavior, but the STATUS register still indicates PG status. 0 = Not Masked 1 = Masked
D[3:0]	R/W	RV	4'b 0000	Reserved

SYS_CTRL4 (0Fh)

Format: Unsigned binary

The SYS_CTRL4 command sets over temperature threshold and over temperature warning threshold.

Bits	Access	Bit name	Default	Description
D[7:5]	R/W	OT_TH	3'b 100	Converter Shutdown Temperature Threshold 3'b 000: 105°C 3'b 001: 115°C 3'b 010: 125°C 3'b 011: 135°C 3'b 100: 145°C 101 = Reserved 110 = Reserved 111 = Reserved Hysteresis = 20°C
D[4:2]	R/W	OTW_TH	3'b 101	Over Temperature Warning Threshold 3'b 000: Reserved 3'b 001: 85°C 3'b 010: 95°C 3'b 011: 105°C 3'b 100: 115°C 3'b 101 = 125°C 3'b 110 = 135°C 111 = Reserved Hysteresis = 20°C
D[1:0]	R/W	RV	2'b 00	Reserved

ADC_CTRL1 (10h)

Format: Unsigned binary

The ADC_CTRL1 command sets ADC_EN and ADC_SAMPLE_FREQ.

Bits	Access	Bit name	Default	Description
D[7]	R/W	ADC_EN	1'b 1	0=Disable ADC 1=Enable ADC

D[6:2]	R/W	RV	5'b 00000	Reserved
D[1:0]	R/W	ADC_SAMPLE_FREQ	2'b 01	The frequency to refresh all the ADC channels 00 = 4kHz 01 = 2kHz 10 = 1kHz 11 = 0.5kHz

TEMPERATURE (11h)

Format: Unsigned binary

The TEMPERATURE command monitors temperature of the IC.

Bits	Access	Bit name	Default	Description
D[7:5]	R/O	TEMPERATURE	3'b 000	PMIC Temperature 000 =< 80°C 001 = 85°C 010 = 95°C 011 = 105°C 100 = 115°C 101 = 125°C 110 = 135°C 111 => 140°C
D[4:0]	R/W	RV	5'b 00000	Reserved

VOUT1_ADC (12h)

Format: Direct

The VOUT1_ADC command monitors VOUT1 voltage.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	VOUT1_ADC	8'b 0000 0000	Buck 1 Output Voltage, LSB=16mV 0000 0000=Undefined 0000 0001=16mV 0000 0010=32mV ... 1111 1110=4064mV 1111 1111 >= 4080mV

IOUT1_ADC (13h)

Format: Direct

The IOUT1_ADC command monitors BUCK1 output current.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	IOUT1_ADC	8'b 0000 0000	Buck 1 Output Current, LSB=50mA 0000 0000= 0 A 0000 0001= 0.05A 0000 0010= 0.1A ... 1111 1110= 12.7 A 1111 1111 = 12.75 A All other encodings are reserved

VOUT2_ADC (14h)

Format: Direct

The VOUT2_ADC command monitors VOUT2 voltage.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	VOUT2_AD C	8'b 0000 0000	Buck 2 Output Voltage, LSB=16mV 0000 0000=Undefined 0000 0001=16mV 0000 0010=32mV ... 1111 1110=4064mV 1111 1111 >= 4080mV

IOUT2_ADC (15h)

Format: Direct

The IOUT2_ADC command monitors BUCK2 output current.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	IOUT2_AD C	8'b 0000 0000	Buck 2 Output Current, LSB=50mA 0000 0000= 0 A 0000 0001= 0.05A 0000 0010= 0.1A ... 1111 1110= 12.7 A 1111 1111 = 12.75 A All other encodings are reserved

LDO_ADC (16h)

Format: Direct

The LDO_ADC command monitors LDO output voltage.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	LDO_ADC	8'b 0000 0000	LDO Output Voltage, LSB=16mV 0000 0000=Undefined 0000 0001=16mV 0000 0010=32mV ... 1111 1110=4064mV 1111 1111 >= 4080mV

GPIO_ADC (17h)

Format: Direct

The GPIO_ADC command monitors GPIO output voltage.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	GPIO_ADC	8'b 0000 0000	LSB = 8 mV 0000 0000 = 0m V 0000 0001 = 8mV ... 1111 1111 = 2040mV

VIN_ADC (18h)
Format: Direct

The VIN_ADC command monitors input voltage.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	VIN_ADC	8'b 0000 0000	Input Voltage, LSB = 64 mV 0000 0000 = 0m V 0000 0001 = 64mV 0000 0010 = 128mV ... 1111 1111 >= 16320mV

FAULT_STATUS (19h)
Format: Direct

FAULT_STATUS command monitors fault status of VIN, VOUT1, VOUT2, LDO, OTW and OT.

Bits	Access	Bit name	Default	Description
D[7]	RO	VIN_PG	1'b 0	VIN Power Good Status. Once VIN OV/UV fault occurs, this bit will be set and latched. The CLEAR1 command 0x1D can reset this bit 0 = Power Good 1 = Power Not Good
D[6]	RO	VOUT1_FAULT	1'b 0	VOUT1 Fault Status. Once VOUT1 fault occurs, this bit will be set and latched. The CLEAR1 command 0x1D can reset this bit 0 = Normal Power On or EN is off 1 = VOUT1 occurs fault when EN is on
D[5]	RO	VOUT2_FAULT	1'b 0	VOUT2 Fault Status. Once VOUT2 fault occurs, this bit will be set and latched. The CLEAR1 command 0x1D can reset this bit 0 = Normal Power On or EN is off 1 = VOUT2 occurs fault when EN is on
D[4]	RO	LDO_FAULT	1'b 0	LDO Fault Status Once LDO fault occurs, this bit will be set and latched. The CLEAR1 command 0x1D can reset this bit 0 = Power Good or EN is off 1 = LDO occurs fault when EN is on
D[3:2]	R/W	RV	2'b 00	Reserved
D[1]	RO	OTW	1'b 0	High Temperature Warning Status Once OVER TEMPERATURE WARNING occurs, this bit will be set and latched. The CLEAR1 command 0x1D can reset this bit 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold

D[0]	RO	OT	1'b 0	Temperature Shutdown Status Once OVER TEMPERATURE FAULT occurs, this bit will be set and latched. The CLEAR1 command 0x1D can reset this bit 0 = No Temperature Shutdown 1 = Temperature Shutdown
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STATUS1 (1Ah)
Format: Direct

STATUS1 command monitors fault status of VIN_OV, VIN_UV, VOUT1_OV, VOUT2_OV, VOUT1_UV, VOUT2_UV, VOUT1_OC, VOUT2_OC.

Bits	Access	Bit name	Default	Description
D[7]	RO	VIN_OV	1'b 0	VIN Over Voltage Status 0 = No Over Voltage 1 = Over Voltage
D[6]	RO	VIN_UV	1'b 0	VIN Under Voltage Status 0 = No Under Voltage 1 = Under Voltage
D[5]	RO	VOUT1_O V	1'b 0	VOUT1 Over Voltage Status 0 = No Over Voltage 1 = Over Voltage
D[4]	RO	VOUT2_O V	1'b 0	VOUT2 Over Voltage Status 0 = No Over Voltage 1 = Over Voltage
D[3]	RO	VOUT1_UV	1'b 0	VOUT1 Under Voltage Status 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
D[2]	RO	VOUT2_UV	1'b 0	VOUT2 Under Voltage Status 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
D[1]	RO	VOUT1_O C	1'b 0	Buck1 Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
D[0]	RO	VOUT2_O C	1'b 0	Buck2 Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event

MASK1 (1Bh)
Format: Unsigned binary

The MASK1 command only can mask off the INT pin behavior, but the STATUS register still indicate each event.

Bits	Access	Bit name	Default	Description
D[7]	RW	VIN_PG_M SK	1'b 0	0 = Do Not Mask 1 = Mask
D[6]	RW	VOUT1_P G_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[5]	RW	VOUT2_P G_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[4]	RW	LDO_PG_ MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[3:2]	RW	RV	2'b 00	Reserved

D[1]	RW	OTW_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[0]	RW	OT_MSK	1'b 0	0 = Do Not Mask 1 = Mask

MASK2 (1Ch)

Format: Unsigned binary

The MASK2 command only can mask off the INT pin behavior, but the STATUS register still indicate each event.

Bits	Access	Bit name	Default	Description
D[7]	RW	VIN_OV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[6]	RW	VIN_UV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[5]	RW	VOUT1_OV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[4]	RW	VOUT2_OV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[3]	RW	VOUT1_UV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[2]	RW	VOUT2_UV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[1]	RW	VOUT1_OC_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[0]	RW	VOUT2_OC_MSK	1'b 0	0 = Do Not Mask 1 = Mask

CLEAR1 (1Dh)

Format: Direct

This CLEAR1 command is used to clear corresponding fault bits that have been set.

Bits	Access	Bit name	Default	Description
D[7]	W1C	VIN_PG_CLEAR	1'b 0	Clear VIN Power Good Status. 1 = Clear
D[6]	W1C	VOUT1_FAULT_CLEAR	1'b 0	Clear 0x19 VOUT1 FAULT Status. 1 = Clear
D[5]	W1C	VOUT2_FAULT_CLEAR	1'b 0	Clear 0x19 VOUT2 FAULT Status. 1 = Clear
D[4]	W1C	LDO_FAULT_CLEAR	1'b 0	Clear 0x19 LDO FAULT Status. 1 = Clear
D[3]	W1C	OTW_CLEAR	1'b 0	Clear High Temperature Warning Status. 1 = Clear
D[2]	W1C	OT_CLEAR	1'b 0	Clear High Temperature Status. 1 = Clear
D[1]	R/W	RV	1'b 0	Reserved
D[0]	W1C	ALL_STATUS_CLEAR	1'b 0	1 = Clear all the status bits

CLEAR1 (1Eh)

Format: Direct

This CLEAR2 command is used to clear corresponding fault bits that have been set.

Bits	Access	Bit name	Default	Description
D[7]	W1C	VIN_OV_C LEAR	1'b 0	Clear VIN Over Voltage Status. 1 = Clear
D[6]	W1C	VIN_UV_C LEAR	1'b 0	Clear VIN Under Voltage Status. 1 = Clear
D[5]	W1C	VOUT1_O V_CLEAR	1'b 0	Clear VOUT1 Over Voltage Status 1 = Clear
D[4]	W1C	VOUT2_O V_CLEAR	1'b 0	Clear VOUT2 Over Voltage Status. 1 = Clear
D[3]	W1C	VOUT1_UV _CLEAR	1'b 0	Clear VOUT1 Under Voltage Status 1 = Clear
D[2]	W1C	VOUT2_UV _CLEAR	1'b 0	Clear VOUT2 Under Voltage Status. 1 = Clear
D[1]	W1C	VOUT1_O C_CLEAR	1'b 0	Clear Buck1 Output Current Limiter Warning Status. 1 = Clear
D[0]	W1C	VOUT2_O C_CLEAR	1'b 0	Clear Buck2 Output Current Limiter Warning Status. 1 = Clear

AVP_CTRL1 (1Fh)

Format: Unsigned binary

This AVP_CTRL1 command is used to set AVP function of BUCK1.

Bits	Access	Bit name	Default	Description
D[7]	R/W	AVP1_EN	1'b 0	Enable bit of Buck 1 AVP function. 0 = Disable the AVP function 1 = Enable the AVP function
D[6:5]	R/W	AVP1_GAIN	2'b 00	Set the AVP Gain. 00 = 2mV/A 01 = 4mV/A 10 = 6mV/A 11 = 8mV/A
D[4:0]	R/W	AVP1_OFFS ET	5'b 0000 1	Set the DC offset voltage to the output voltage command value when AVP is enabled. From -30mV to 30mV, 2mV per step. x_0000 = 0mV 0_0001 = 2mV ... 0_1111 = 30mV 1_0001 = -2mV ... 1_1111 = -30mV

AVP_CTRL2 (20h)

Format: Unsigned binary

This AVP_CTRL2 command is used to set AVP function of BUCK2.

Bits	Access	Bit name	Default	Description
D[7]	R/W	AVP2_EN	1'b 0	Enable bit of Buck 2 AVP function. In Dual phase single output Mode, AVP2 function is invalid. 0 = Disable the AVP function 1 = Enable the AVP function

D[6:5]	R/W	AVP2_GAIN	2'b 00	Set the AVP Gain. In Dual phase single output Mode, AVP2 function is invalid. 00 = 2mV/A 01 = 4mV/A 10 = 6mV/A 11 = 8mV/A
D[4:0]	R/W	AVP2_OFFSET	5'b 0000 1	Set the DC offset voltage to the output voltage command value when AVP is enabled. From -30mV to 30mV, 2mV per step x_0000 = 0mV 0_0001 = 2mV ... 0_1111 = 30mV 1_0001 = -2mV ... 1_1111 = -30mV

STATUS2 (21h)

Format: Direct

STATUS2 command monitors status of VIN_PG, VOUT1_PG, VOUT2_PG, LDO_PG OT_WARING and OT_FAULT.

Bits	Access	Bit name	Default	Description
D[7]	R	VIN_PG_STATUS	1'b 0	VIN Power Good Status. Active Bit. Do Not Require Clear. 0 = Normal Power On 1 = VIN Fault Occurs
D[6]	R	VOUT1_PG_STATUS	1'b 0	VOUT1 Power Good Status. Active Bit. Do Not Require Clear. 0 = Normal Power On 1 = VOUT1 Is Not On The Target
D[5]	R	VOUT2_PG_STATUS	1'b 0	VOUT2 Power Good Status. Active Bit. Do Not Require Clear. 0 = Normal Power On 1 = VOUT2 Is Not On The Target
D[4]	R	LDO_PG_STATUS	1'b 0	LDO Power Good Status. Active Bit. Do Not Require Clear. 0 = Normal Power On 1 = LDO Voltage Is Not On The Target
D[3:2]	R	RV	2'b 00	Reserved.
D[1]	R	OT_WARING_STATUS	1'b 0	Over Temperature Waring Status. Active Bit. Do Not Require Clear. 0 = Normal Power On 1 = Over Temperature Waring
D[0]	R	OT_FAULT_STATUS	1'b 0	Over Temperature Fault Status. Active Bit. Do Not Require Clear. 0 = Normal Power On 1 = Over Temperature Fault

MTP Register Region

The MTP region registers are non-volatile memories. Most registers are the shadow of I2C region registers. MTP registers do not directly control Converter operation. At VIN power ON, the setting is copied from MTP registers to I2C registers.

LOCK (40h)

Format: Direct

LOCK command sets MTP REGION ACCESS PASSWORD.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	MTP REGION ACCESS PASSWOR D	8'b 0000 0000	Correct Password has to be present to access MTP Register Region and MODE Register Region. Please contact FAE for password.

BUCK1_CTRL1 (41h)

Default Setting for Register 0x01. No direct control on Converter operation except for SOFT START and SOFT STOP.

Bits	Access	Bit name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved
D[6:4]	R/W	VOUT1_S OFT_STAR T	3'b 001 OR MODE DETERMIN ED	Buck1 Soft Start Time After Enable. Output is between 0% and 100% of VOUT. 3'b 000: 1 ms 3'b 001: 2 ms 3'b 010: 4 ms 3'b 011: 6ms 3'b 100: 8ms 101 = 10ms 110 = 12ms 111 = 14ms
D[3:2]	R/W	VOUT1_S OFT_STOP	2'b 00	Buck1 Soft Stop Time After Enable. Output is between 0% and 100% of VOUT. 2'b 00: 0.5 ms 2'b 01: 1 ms 2'b 10: 2 ms 2'b 11: 4 ms
D[1:0]	R/W	VOUT1_SL EW_RATE	2'b 00	VOUT1 slew rate during dynamic voltage scaling(no external FB divider resistor) 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK1_CTRL2 (42h)

Default setting for Register 0x02. No direct control on Converter operation.

In dual phase single output mode, the BUCK2_FSW, BUCK2_PFM/PWM, VOUT2 setting are masked in internal, they are determined by BUCK1 corresponding setting.

In single phase dual output mode, recommend to set BUCK1_FSW and BUCK2_FSW the same frequency.

Bits	Access	Bit name	Default	Description
D[7:6]	RW	BUCK1_PFM/PWM	2'b 11	Buck1 Mode Selection 00,01 = Reserved 2'b 10: COT; DCM (Constant on Time; Discontinuous Current Mode at the light load) 2'b 11: COT; Forced CCM (Constant on Time; Continuous Current Mode)
D[5:4]	RW	BUCK1_FSW	2'b 01	Buck1 Switching Frequency 2'b 00: 500 KHz 2'b 01: 750 KHz 2'b 10: 1000 KHz 2'b 11: 1250 KHz
D[3]	RW	RV	1'b 0	Reserved
D[2:0]	RW	VOUT1_SETTING_LOW	3'b 000 OR MODE DETERMINED	Combined with VOUT_SETTING_HIGH to set VOUT1 voltage.

BUCK1_CTRL3 (43h)

Default setting for Register 0x03. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	VOUT1_SETTING_HIGH	8'b 0011 0010 OR MODE DETERMINED	VOUT_SETTING_HIGH register works together with VOUT_SETTING_LOW register. Adding them up together, the 11-bit register controls the output voltage. VOUT1 setting when BUCK1_FB_HALF = 0: the bits value \leq 001 0010 1100(300d), the setting = 300mV. 001 0010 1100(300d) \leq the bits value \leq 111 1111 1111(2047d) and the bits value are defined equal to X, the setting = X mV, 1mV/step. VOUT1 setting when BUCK1_FB_HALF = 1: the bits value \leq 000 1001 0110(150d), the setting = 300mV. 000 1001 0110(150d) \leq the bits value \leq 111 0110 1100 (1900d) and the bits value are defined equal to X, the setting = 2*X mV, 2mV/step. The bits value \geq 111 0110 1100 (1900d), the setting=3800mV.

BUCK1_CTRL4 (44h)

Default setting for Register 0x04. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VOUT1_DISCHG_EN	1'b 1	Enable bit of Buck1 output passive discharge function. 0 = Disable the passive discharge function; 1 = Enable the passive discharge function If passive discharge function is enabled, when Buck 1 is disabled, a discharging resistor is connected to VOUT1_FB_P pin to discharge VOUT1 until 100mV.
D[6]	R/W	VOUT1_OVP_EN	1'b 1	Enable the Buck1 output active OVP function 0 = output OVP disabled 1 = output OVP enabled If output OVP is enabled, Buck1 actively turns on LSFET to discharge VOUT1. Refer to operation for more details.

D[5]	R/W	BUCK1_FB_HALF	1'b 0	Enable the Buck1 internal FB 1/2 divider 0 = no internal FB divider 1 = internal 1/2 FB divider is enabled
D[4:2]	R/W	BUCK1_OC_TH	3'b 101	Buck1 Valley Current Limit Threshold 3'b 000 = 4.0 A 3'b 001 = 4.5 A 3'b 010 = 5.0 A 3'b 011 = 5.5 A 3'b 100 = 6.0 A 3'b 101 = 6.5 A 3'b 110 = 7.0 A 3'b 111 = 7.5 A
D[1:0]	R/W	RV	2'b 00	Reserved

BUCK1_CTRL5 (45h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	BUCK1_POWER_ON_DELAY	8'b 0000 0100 OR MODE DETERMINED	Buck1 Soft Start When Counting This Number Of CLK Pulses: 0000 0000 = 0 0000 0001 = 1 0000 0010 = 2 0000 0011 = 3 0110 0100 = 100 0110 0101 = 102 0110 0110 = 104 1001 0110 = 200 1001 0111 = 204 1001 1000 = 208 1100 1000 = 400 1100 1001 = 408 1100 1010 = 416 1110 0001 = 600 1110 0010 = 616 1110 0011 = 632 1111 1010 = 1000 1111 1011 = 1024 1111 1100 ~ 1111 1111 = Reserved

BUCK1_CTRL6 (46h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	BUCK1_POWER_OF_DELAY	8'b 0000 0100	Buck1 Soft Stop When Counting This Number Of CLK Pulses: 0000 0000 = 0 0000 0001 = 1 0000 0010 = 2 0000 0011 = 3 0110 0100 = 100 0110 0101 = 102 0110 0110 = 104 1001 0110 = 200 1001 0111 = 204 1001 1000 = 208 1100 1000 = 400 1100 1001 = 408 1100 1010 = 416 1110 0001 = 600 1110 0010 = 616 1110 0011 = 632 1111 1010 = 1000 1111 1011 = 1024 1111 1100 ~ 1111 1111 = Reserved

BUCK1_CTRL7 (47h)

Default setting for Register 0x05. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:6]	R/W	VOUT1_PG_VTH_HIGH	2'b 00	VOUT1 High Side Voltage For Power Good Status 2'b 00: +5% from VOUT1_SETTING 2'b 01: +7.5% from VOUT1_SETTING 2'b 10: +10% from VOUT1_SETTING 2'b 11: Reserved Hysteresis = 2.5%
D[5]	R/W	VOUT1_PG_VTH_LOW	1'b 0	VOUT1 Threshold Low Side Voltage For Power Good Status 0 = -5% from VOUT1_SETTING 1 = -7.5% from VOUT1_SETTING Hysteresis = 2.5%
D[4]	R/W	RV	1'b 0	Reserved
D[3:2]	R/W	VOUT1_UV_VTH	2'b 00	VOUT1 Threshold For Under Voltage Status 2'b 00: -10% from VOUT1_SETTING 2'b 01: -12.5% from VOUT1_SETTING 2'b 10: Reserved 2'b 11: Reserved Hysteresis = 2.5%

D[1:0]	R/W	VOUT1_O V_VTH	2'b 10	VOUT1 Threshold For Over Voltage Status 2'b 00: +7.5% from VOUT1_SETTING 2'b 01: +10% from VOUT1_SETTING 2'b 10: +12.5% from VOUT1_SETTING 2'b 11: Reserved Hysteresis = 2.5%
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BUCK2_CTRL1 (48h)

Default setting for Register 0x06. No direct control on Converter operation except for SOFT START and SOFT STOP.

Bits	Access	Bit name	Default	Description
D[7]	R/W	RV	1'b0	Reserved
D[6:4]	R/W	VOUT2_S OFT_STAR T	3'b 001 OR MODE DETERMIN ED	Buck2 Soft Start Time After Enable. Output is between 0% and 100% of VOUT. 3'b 000: 1 ms 3'b 001: 2 ms 3'b 010: 4 ms 3'b 011: 6ms 3'b 100: 8ms 101 = 10ms 110 = 12ms 111 = 14ms
D[3:2]	R/W	VOUT2_S OFT_STOP	2'b 00	Buck2 Soft Stop Time After Enable. Output is between 0% and 100% of VOUT. 2'b 00: 0.5 ms 2'b 01: 1 ms 2'b 10: 2 ms 2'b 11: 4 ms
D[1:0]	R/W	VOUT2_SL EW_RATE	2'b 00	VOUT2 slew rate during dynamic voltage scaling(no external FB divider resistor) 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK2_CTRL2 (49h)

Default setting for Register 0x07. No direct control on Converter operation.

In dual phase single output mode, the BUCK2_FSW, BUCK2_PFM/PWM, VOUT2 setting are masked in internal, they are determined by BUCK1 corresponding setting.

In single phase dual output mode, recommend to set BUCK1_FSW and BUCK2_FSW the same frequency.

Bits	Access	Bit name	Default	Description
D[7:6]	RW	BUCK2_PFM/PWM	2'b 11	Buck2 Mode Selection 00,01 = Reserved 2'b 10: COT; DCM (Constant on Time; Discontinuous Current Mode) 2'b 11: COT; Forced CCM (Constant on Time; Continuous Current Mode)
D[5:4]	RW	BUCK2_FSW	2'b 01	Buck2 Switching Frequency. 2'b 00: 500 KHz 2'b 01: 750 KHz 2'b 10: 1000 KHz 2'b 11: 1250 KHz

D[3]	RW	RV	1'b 0	Reserved
D[2:0]	RW	VOUT2_SETTING_LOW	3'b 000 or MODE determined	Combined with VOUT_SETTING_HIGH to set VOUT2 voltage.

BUCK2_CTRL3 (4Ah)

Default setting for Register 0x08. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	VOUT2_SETTING_HIGH	8'b 0011 0010 OR MODE DETERMINED	<p>VOUT_SETTING_HIGH register works together with VOUT_SETTING_LOW register. Adding them up together, the 11-bit register controls the output voltage.</p> <p>VOUT1 setting when BUCK1_FB_HALF = 0: the bits value \leq 001 0010 1100(300d), the setting = 300mV. 001 0010 1100(300d) \leq the bits value \leq 111 1111 1111(2047d) and the bits value are defined equal to X, the setting = X mV, 1mV/step.</p> <p>VOUT1 setting when BUCK1_FB_HALF = 1: the bits value \leq 000 1001 0110(150d), the setting = 300mV. 000 1001 0110(150d) \leq the bits value \leq 111 0110 1100 (1900d) and the bits value are defined equal to X, the setting = 2*X mV, 2mV/step. The bits value \geq 111 0110 1100 (1900d), the setting=3800mV.</p>

BUCK2_CTRL4 (4Bh)

Default setting for Register 0x09. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VOUT2_DISCHG_EN	1'b 1	<p>Enable bit of Buck2 output passive discharge function. 0 = Disable the passive discharge function; 1 = Enable the passive discharge function</p> <p>If passive discharge function is enabled, when Buck 1 is disabled, a discharging resistor is connected to VOUT2_FB_P pin to discharge VOUT2 until 100mV.</p>
D[6]	R/W	VOUT2_OVP_EN	1'b 1	<p>Enable the Buck2 output active OVP function 0 = output OVP disabled 1 = output OVP enabled</p> <p>If output OVP is enabled, Buck1 actively turns on LSFET to discharge VOUT2. Refer to operation for more details.</p>
D[5]	R/W	BUCK2_FB_HALF	1'b 0	<p>Enable the Buck2 internal FB 1/2 divider 0 = no internal FB divider 1 = internal 1/2 FB divider is enabled</p>
D[4:2]	R/W	BUCK2_OCTH	3'b 101	<p>Buck2 Valley Current Limit Threshold 3'b 000 = 4.0 A 3'b 001 = 4.5 A 3'b 010 = 5.0 A 3'b 011 = 5.5 A 3'b 100 = 6.0 A 3'b 101 = 6.5 A 3'b 110 = 7.0 A 3'b 111 = 7.5 A</p>

BUCK2_CTRL5 (4Ch)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	BUCK2_POWER_ON_DELAY	8'b 0000 0100 OR MODE DETERMINED	Buck2 Soft Start When Counting This Number Of CLK Pulses: 0000 0000 = 0 0000 0001 = 1 0000 0010 = 2 0000 0011 = 3 0110 0100 = 100 0110 0101 = 102 0110 0110 = 104 1001 0110 = 200 1001 0111 = 204 1001 1000 = 208 1100 1000 = 400 1100 1001 = 408 1100 1010 = 416 1110 0001 = 600 1110 0010 = 616 1110 0011 = 632 1111 1010 = 1000 1111 1011 = 1024 1111 1100 ~ 1111 1111 = Reserved

BUCK2_CTRL6 (4Dh)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	BUCK2_POWER_OFF_DELAY	8'b 0000 0100	Buck2 Soft Stop When Counting This Number Of CLK Pulses: 0000 0000 = 0 0000 0001 = 1 0000 0010 = 2 0000 0011 = 3 0110 0100 = 100 0110 0101 = 102 0110 0110 = 104 1001 0110 = 200 1001 0111 = 204 1001 1000 = 208 1100 1000 = 400 1100 1001 = 408 1100 1010 = 416 1110 0001 = 600 1110 0010 = 616 1110 0011 = 632 1111 1010 = 1000 1111 1011 = 1024 1111 1100 ~ 1111 1111 = Reserved

BUCK2_CTRL7 (4Eh)

Default setting for Register 0x0A. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:6]	R/W	VOUT2_P G_VTH_HI GH	2'b 00	VOUT2 High Side Voltage For Power Good Status 2'b 00: +5% from VOUT2_SETTING 2'b 01: +7.5% from VOUT2_SETTING 10 = +10% from VOUT2_SETTING 2'b 11: Reserved Hysteresis = 2.5%
D[5]	R/W	VOUT2_P G_VTH_LO W	1'b 0	VOUT2 Threshold Low Side Voltage For Power Good Status 0 = -5% from VOUT2_SETTING 1 = -7.5% from VOUT2_SETTING Hysteresis = 2.5%
D[4]	R/W	RV	1'b 0	Reserved
D[3:2]	R/W	VOUT2_UV _VTH	2'b 00	VOUT2 Threshold For Under Voltage Status 2'b 00: -10% from VOUT2_SETTING 2'b 01: -12.5% from VOUT2_SETTING 2'b 10: Reserved 2'b 11: Reserved Hysteresis = 2.5%
D[1:0]	R/W	VOUT2_O V_VTH	2'b 10	VOUT2 Threshold For Over Voltage Status 2'b 00: +7.5% from VOUT2_SETTING 2'b 01: +10% from VOUT2_SETTING 2'b 10: +12.5% from VOUT2_SETTING 2'b 11: Reserved Hysteresis = 2.5%

LDO_CTRL1 (4Fh)

Default setting for Register 0x0B. No direct control on Converter operation expect for SOFT START.

Bits	Access	Bit name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved
D[6:4]	R/W	LDO_SOFT _START	3'b 001 OR MODE DETERMIN ED	LDO Soft Start Time After Enable. Output is between 0% and 100% of VOUT. 3'b 000: 1 ms 3'b 001: 2 ms 3'b 010: 4 ms 3'b 011: 6ms 3'b 100: 8ms 101 = 10ms 110 = 12ms 111 = 14ms
D[3:2]	RV	RV	2'b 00	Reserved
D[1]	R/W	LDO_DISC HG	1'b 1	0 = disable LDO discharge 1 = enable LDO discharge
D[0]	R/W	LDO_PG_V TH	1'b 0	LDO Output Threshold Voltage for Power Good Status 0 = -10% from LDO_SETTING 1 = -15% from LDO_SETTING Hysteresis = 5%

LDO_CTRL2 (50h)

Default setting for Register 0x0C. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved
D[6:0]	R/W	LDO_SETT ING	7'b 011 1100 OR MODE DETERMIN ED	LDO output voltage setting: 30mV per LSB from 0.6V to 3.6V All lower setting = Reserved 001 0100 = 600 mV 001 0101 = 630 mV ... 111 1000 = 3600 mV All higher setting = Reserved

LDO_CTRL3 (51h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	LDO_POW ER_ON_D ELAY	8'b 0000 0000 OR MODE DETERMIN ED	LDO Soft Start When Counting This Number Of CLK Pulses: 0000 0000 = 0 0000 0001 = 1 0000 0010 = 2 0000 0011 = 3 0110 0100 = 100 0110 0101 = 102 0110 0110 = 104 1001 0110 = 200 1001 0111 = 204 1001 1000 = 208 1100 1000 = 400 1100 1001 = 408 1100 1010 = 416 1110 0001 = 600 1110 0010 = 616 1110 0011 = 632 1111 1010 = 1000 1111 1011 = 1024 1111 1100 ~ 1111 1111 = Reserved

LDO_CTRL4 (52h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	LDO_POWER_OFF_DELAY	8'b 0000 0000	<p>LDO Soft Stop When Counting This Number Of CLK Pulses:</p> <p>0000 0000 = 0</p> <p>0000 0001 = 1</p> <p>0000 0010 = 2</p> <p>0000 0011 = 3</p> <p>.....</p> <p>0110 0100 = 100</p> <p>0110 0101 = 102</p> <p>0110 0110 = 104</p> <p>.....</p> <p>1001 0110 = 200</p> <p>1001 0111 = 204</p> <p>1001 1000 = 208</p> <p>.....</p> <p>1100 1000 = 400</p> <p>1100 1001 = 408</p> <p>1100 1010 = 416</p> <p>.....</p> <p>1110 0001 = 600</p> <p>1110 0010 = 616</p> <p>1110 0011 = 632</p> <p>.....</p> <p>1111 1010 = 1000</p> <p>1111 1011 = 1024</p> <p>1111 1100 ~ 1111 1111 = Reserved</p>

SYS_CTRL1 (53h)

Default setting for Register 0x0D. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	CONVERTER_EN	1'b 1	<p>0 = Buck1, Buck2, LDO are all disabled</p> <p>1 = Buck1, Buck2, LDO are all enabled (still need to enable each regulator)</p>
D[6]	R/W	VOUT1_EN	1'b 1	<p>0 = Buck1 Disable</p> <p>1 = Buck1 Enable</p>
D[5]	R/W	VOUT2_EN	1'b 1	<p>0 = Buck2 Disable</p> <p>1 = Buck2 Enable</p>
D[4]	R/W	LDO_EN	1'b 0	<p>0 = LDO Disable</p> <p>1 = LDO Enable</p>
D[3:2]	R/W	RV	2'b 00	Reserved
D[1:0]	R/W	GPIO_CTRL	2'b 10	<p>GPIO open-drain output or analog input control.</p> <p>2'b 00: GPIO output is low.</p> <p>2'b 01: Reserved</p> <p>10 = GPIO is part of flex-time control and used as external converter's enable signal. GPIO outputs as an EN signal of external converter and its on/off sequence can be programmed in 0x57 and 0x58 registers.</p> <p>2'b 11: GPIO output is floating/high.</p>

SYS_CTRL3 (54h)

Default setting for Register 0x0D. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	SINGLE/DUAL	1'b 1 OR MODE DETERMINED	Buck1/2 Operate in Single phase dual output/Dual phase single output 0 = Single phase dual output 1 = Dual phase single output
D[6:0]	R/W	RV	0000000	Reserved

SYS_CTRL3 (55h)

Default setting for Register 0x0E. No direct control on Converter operation except for PROTECT_MODE.

Bits	Access	Bit name	Default	Description
D[7:5]	R/W	VIN_PG_VTH	3'b 110	VIN Rising Threshold Voltage for VIN_PG Bit. VIN_PG bit(0x19) is 0(power good) even VIN<VIN PG falling threshold after VIN startup. Then ramp up VIN \geq VIN rising threshold, If VIN triggers the VIN PG falling threshold again, VIN_PG bit changes to be 1(power not good). 3'b 000: 9.5 V, same as 001. 3'b 001: 9.5 V 3'b 010: 8.5 V 3'b 011: 7.5 V 3'b 100: 6.5 V 101 = 5.5 V 110 = 4.25 V 111 = Reserved Hysteresis = 0.5V
D[4]	R/W	MASK_PG	1'b 0	Mask PG Pin Output 0 = Not Masked 1 = Masked
D[3]	R/W	PG_DELAY_EN	1'b 0	0 = no delay on PG 1 = 100 μ s on PG
D[2]	R/W	VIN_OVP_EN	1'b 1	0 = Enable VIN OVP 1 = Disable VIN OVP
D[1]	R/W	RV	1'b 0	Reserved
D[0]	R/W	PROTECT_MODE	1'b 1	Protection Mode Selection for Buck Converters 0 = Latch-off mode 1 = Hiccup mode

SYS_CTRL4 (56h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:5]	R/W	OT_TH	3'b 100	Converter Shutdown Temperature Threshold 3'b 000: 105°C 3'b 001: 115°C 3'b 010: 125°C 3'b 011: 135°C 3'b 100: 145°C 101 = Reserved 110 = Reserved 111 = Reserved Hysteresis = 20°C

D[4:2]	R/W	OTW_TH	3'b 110	Over Temperature Warning Threshold 3'b 000: Reserved 3'b 001: 85°C 3'b 010: 95°C 3'b 011: 105°C 3'b 100: 115°C 3'b 101: 125°C 3'b 110 = 135°C 3'b 111 = Reserved Hysteresis = 20°C
D[1:0]	R/W	VIN_UV_S EL	2'b 00	Buck VIN UVLO Rising Threshold 2'b 00: Default value in EC table 2'b 01: 2.9V 2'b 10: 4V 2'b 11: 6V

GPIO_CONFIG (57h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	GPIO_POWER_ON_DELAY	8'b 0000 0000 OR MODE DETERMINED	If GPIO_CTL = 10 GPIO Goes High When Counting This Number Of CLK Pulses: 0000 0000 = 0 0000 0001 = 1 0000 0010 = 2 0000 0011 = 3 0110 0100 = 100 0110 0101 = 102 0110 0110 = 104 1001 0110 = 200 1001 0111 = 204 1001 1000 = 208 1100 1000 = 400 1100 1001 = 408 1100 1010 = 416 1110 0001 = 600 1110 0010 = 616 1110 0011 = 632 1111 1010 = 1000 1111 1011 = 1024 1111 1100 ~ 1111 1111 = Reserved

GPIO_CONFIG (58h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	GPIO_POWER_OFF_DELAY	8'b 0000 0000 OR MODE DETERMINED	If GPIO_CTL = 10 GPIO Goes Low When Counting This Number Of CLK Pulses: 0000 0000 = 0 0000 0001 = 1 0000 0010 = 2 0000 0011 = 3 0110 0100 = 100 0110 0101 = 102 0110 0110 = 104 1001 0110 = 200 1001 0111 = 204 1001 1000 = 208 1100 1000 = 400 1100 1001 = 408 1100 1010 = 416 1110 0001 = 600 1110 0010 = 616 1110 0011 = 632 1111 1010 = 1000 1111 1011 = 1024 1111 1100 ~ 1111 1111 = Reserved

ADC_CTRL2 (59h)

The ADC_CTRL2 command sets ADC enable and sample frequency.

Bits	Access	Bit name	Default	Description
D[7]	R/W	ADC_EN	1'b 1	0 = Disable ADC 1 = Enable ADC
D[6:2]	R/W	RV	5'b 00000	Reserved.
D[1:0]	R/W	ADC_SAMPLE_FREQ	2'b 01	The frequency to refresh all the ADC channels 00 = 4kHz 01 = 2kHz 10 = 1kHz 11 = 0.5kHz

MASK1 (5Ah)

Default setting for Register 0x1B. No direct control on Converter operation.

This register can mask off the INT pin behavior, but the STATUS register still indicate each event.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VIN_PG_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[6]	R/W	VOUT1_PG_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[5]	R/W	VOUT2_PG_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[4]	R/W	LDO_PG_MSK	1'b 0	0 = Do Not Mask 1 = Mask

D[3:2]	R/W	RV	2'b 00	Reserved
D[1]	R/W	OTW_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[0]	R/W	OT_MSK	1'b 0	0 = Do Not Mask 1 = Mask

MASK1 (5Bh)

Default setting for Register 0x1C. No direct control on Converter operation.

This register can mask off the INT pin behavior, but the STATUS register still indicate each event.

Bits	Access	Bit name	Default	Description
D[7]	R/W	VIN_OV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[6]	R/W	VIN_UV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[5]	R/W	VOUT1_OV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[4]	R/W	VOUT2_OV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[3]	R/W	VOUT1_UV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[2]	R/W	VOUT2_UV_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[1]	R/W	VOUT1_OC_MSK	1'b 0	0 = Do Not Mask 1 = Mask
D[0]	R/W	VOUT2_OC_MSK	1'b 0	0 = Do Not Mask 1 = Mask

AVP_CTRL1 (5Ch)

Default setting for Register 0x1F. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	AVP1_EN	1'b 0	Enable bit of Buck 1 AVP function 0 = Disable the AVP function 1 = Enable the AVP function
D[6:5]	R/W	AVP1_GAIN	2'b 00	Set the AVP Gain. 2'b 00: 3mV/A 2'b 01: 5.5mV/A 2'b 10: Reserved 2'b 11: Reserved
D[4:0]	R/W	AVP1_OFFSET	5'b 0000 1	Set the DC offset voltage to the output voltage command value when AVP is enabled. From -30mV to 30mV, 2mV per step x_0000 = 0mV 0_0001 = 2mV ... 0_1111 = 30mV 1_0001 = -2mV ... 1_1111 = -30mV

AVP_CTRL1 (5Dh)

Default setting for Register 0x20. No direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	AVP2_EN	1'b 0	Enable bit of Buck 2 AVP function 0 = Disable the AVP function 1 = Enable the AVP function
D[6:5]	R/W	AVP2_GAIN	2'b 00	Set the AVP Gain. 2'b 00: 3mV/A 2'b 01: 5.5mV/A 2'b 10: Reserved 2'b 11: Reserved
D[4:0]	R/W	AVP2_OFFSET	5'b 0000 1	Set the DC offset voltage to the output voltage command value when AVP is enabled. From -30mV to 30mV, 2mV per step x_0000 = 0mV 0_0001 = 2mV ... 0_1111 = 30mV 1_0001 = -2mV ... 1_1111 = -30mV

CLK_CTRL1 (5Eh)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	CLK_MODE	1'b 1 OR MODE DETERMINED	Master/Slave Configuration For Power Sequence 0 = Slave Converter 1 = Master Converter
D[6:4]	RW	CLK_FREQUENCY	3'b 100	CLK Pin Clock Frequency Configuration 3'b 000: 100Hz 3'b 001: 200Hz 3'b 010: 500Hz 3'b 011: 1KHz 3'b 100: 2KHz 101 = 5KHz 110 = 10KHz 111 = 20KHz
D[3:1]	RW	CLK_NUMBER	3'b 001	CLK Pin Max Clock Output Number Configuration. If the PG pin is pulled up, and the max POWER_ON_DELAY or max POWER_ON_DELAY CLK number of the enabled power rails is less than the CLK_NUMBER, CLK outputs CLK_NUMBER clocks during EN on/off. If the power on/off delay CLK number is more than CLK_NUMBER, CLK continues outputting clocks until on/off sequence is done. If the PG pin float or lower than 2.3V, CLK doesn't stop outputting clocks until the EN off Vin<UVLO. Note: enable or disable power channel through I2C, the CLK keeps high. 3'b 000: 8 3'b 001: 16 3'b 010: 32 3'b 011: 64 3'b 100: 128 3'b 101: 256 3'b 110: 512 3'b 111: 1024
D[0]	R/W	RV	1'b 0	Reserved

CLK_CTRL2 (5Fh)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:3]	R/W	RV	5'b 0000 0	Reserved
D[2]	RW	CLK PAUSE EN	1'b 0	Enable/Disable the Pausing Feature Of The CLK Clock Output 0 = Disable, Converter Does Not Pull Low the CLK Pin During Soft Start/Soft Stop 1 = Enable, Converter Pull Low the CLK Pin During Soft Start/Stop
D[1]	RW	CLK ON ERROR PAUSE EN	1'b 0	Enable/Disable the Pausing Feature When Error Happens During Soft Start 0 = Disable, Converter Does Not Pull Low the CLK Pin if Error Happens During Soft Start 1 = Enable, Converter Pull Low the CLK Pin if Error Happens During Soft Start
D[0]	R/W	RV	1'b 0	Reserved

I2C_CONFIG (60h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7]	R/W	MODE_EN	1'b 1	MODE Enable control. 0 = MODE is disabled, the MODE determined MTP registers keep the original value as the default value 1 = MODE is enabled, the MODE determined MTP registers load the default value based on MODE selection
D[6:0]	R/W	I2C_ADDR ESS	7'b 000 0000	I2C 7-bit Address

MTP_CTRL1 (61h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	WO	MTP PASSWORD	-	Password for MTP programming.

MTP_CTRL1 (62h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:2]	R/W	RV	6'b 0000 00	Reserved
D[1]	R/W	MTP_PROGRAM	1'b 0	MTP Programming Control Write "1" to this bit to start MTP program. Note: write 0xc8 to 0x61 register before programming.
D[0]	R/W	MTP_RESTORE	1'b 0	MTP Restore Control Write "1" to this bit to restore all registers value to MTP registers' value.

ID2 (64h)

Direct control on Converter operation.

Bits	Access	Bit name	Default	Description
D[7:0]	R/W	MTP_SUFFIX	8'b 0000 0000	MTP Suffix Code MPS defines this register.

MODE Region Registers

When MODE_EN = 1, some of the MTP region registers load default value from MODE region registers depending on the MODE pin resistance.

For the following register settings, their configuration will be copied from corresponding registers in 0x70 – 0xC7. There are 8 sets of configuration settings listed in MODE0 – MODE7 for each of the following bits, and MODE resistor determines which MODEx is selected, based on the table below.

Table 6 Registers Selected According to MODE0 – MODE7

COMMAND CODE(0X)	COMMAND NAME	TAPE	D7	D6	D5	D4	D3	D2	D1	D0
41	BUCK1_CT RL1	R/W		VOUT1_SOFT_START						
42	BUCK1_CT RL2	R/W			BUCK1_FSW			VOUT1_SETTING_LOW		
43	BUCK1_CT RL3	R/W	VOUT1_SETTING_HIGH							
44	BUCK1_CT RL4	R/W			BUCK1_F B_HALF					
45	BUCK1_CT RL5	R/W	BUCK1_POWER_ON_DELAY							
48	BUCK2_CT RL1	R/W		VOUT2_SOFT_START						
49	BUCK2_CT RL2	R/W			BUCK2_FSW			VOUT2_SETTING_LOW		
4A	BUCK2_CT RL3	R/W	VOUT2_SETTING_HIGH							
4B	BUCK2_CT RL4	R/W			BUCK2_F B_HALF					
4C	BUCK2_CT RL5	R/W	BUCK2_POWER_ON_DELAY							
4F	LDO_CTRL 1	R/W		LDO_SOFT_START						
50	LDO_CTRL 2	R/W		LDO_SETTING						
51	LDO_CTRL 3	R/W	LDO_POWER_ON_DELAY							
53	SYS_CTRL 1	R/W				LDO_EN			GPIO_CTRL	
54	SYS_CTRL 3	R/W	SINGLE/D UAL							
57	GPIO_CON FIG	R/W	GPIO_POWER_ON_DELAY							
5E	CLK_CTRL 1	R/W	CLK_MOD E							
60	I2C_CONFI G	R/W		I2C_ADDRESS						

MODE Region Register Description

BIT NAME	Description
MODEx VOUT1 SETTING	Default value for register 0x43 VOUT1_SETTING_HIGH and register 0x42[2:0] VOUT1_SETTING_LOW
MODEx VOUT2 SETTING	Default value for register 0x4A VOUT2_SETTING_HIGH and register 0x49[2:0] VOUT2_SETTING_LOW
MODEx BUCK1_FB_HALF	Default value for register 0x44[5] BUCK1_FB_HALF
MODEx BUCK2_FB_HALF	Default value for register 0x4B[5] BUCK2_FB_HALF
MODEx BUCK1 FSW	Default value for register 0x42[5:4] BUCK1_FSW
MODEx BUCK2 FSW	Default value for register 0x49[5:4] BUCK2_FSW
MODEx CLK MODE	Default value for register 0x5E[7] CLK_MODE
MODEx SINGLE/DUAL	Default value for register 0x54[7] SINGLE/DUAL
MODEx BUCK1 POWER ON DELAY	Default value for register 0x45 BUCK1_POWER_ON_DELAY
MODEx BUCK2 POWER ON DELAY	Default value for register 0x4C BUCK2_POWER_ON_DELAY



MODEx VOUT1 SOFT START TIME	Default value for register 0x41[6:4] VOUT1_SOFT_START
MODEx VOUT2 SOFT START TIME	Default value for register 0x48[6:4] VOUT2_SOFT_START
MODEx LDO EN	Default value for register 0x53[4] LDO_EN
MODEx LDO SOFT START TIME	Default value for register 0x4F[6:4] LDO_SOFT_START
MODEx I2C ADDRESS	Default value for the last three digits of I2C_ADDRESS 0x60[2:0]
MODEx GPIO CTRL	Default value for register 0x53[1:0] GPIO_CTRL
MODEx LDO SETTING	Default value for register 0x50 LDO_SETTING
MODEx LDO POWER ON DELAY	Default value for register 0x51 LDO_POWER_ON_DELAY
MODEx GPIO POWER ON DELAY	Default value for register 0x57 GPIO_POWER_ON_DELAY

Note:

MODEx represents MODE0 – MODE7.

APPLICATION INFORMATION

Setting the Output Voltage

When using external resistor divider, set the VOUTx_setting to a proper value and BUCKx_FB_HALF = 0, the feedback resistor (R_{FB1}) cannot be too large or too small considering the trade-off for stability and dynamics. There is no strict requirement for the feedback resistor. R_{FB2} can be calculated by

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{V_{FB}} - 1}$$

V_{FB} is generated by the internal DAC which can be adjusted from 0.4V to 2V. For default code 0000, take V_{FB}=0.6V for example, the recommended resistor values for common output voltages is shown in table below.

Resistor Values for Common Output Voltages

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	20 (1%)	30 (1%)
1.2	20 (1%)	20 (1%)
1.8	20 (1%)	10 (1%)
2.5	20 (1%)	6.32 (1%)
3.3	20 (1%)	4.42 (1%)
5	20(1%)	2.73(1%)

However, when BUCKx_FB_HALF = 1, remove RFB2, and RFB1, connect VO directly with FBxP pin by Kelvin connection. When using internal resistor divider, the maximum Vout can only be set to 3.8V.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor is to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22μF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case condition occurs at V_{IN} = 2V_{OUT}, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Step-Down Regulator

Output Capacitor

The output capacitor for step-down regulator maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where L₁ is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

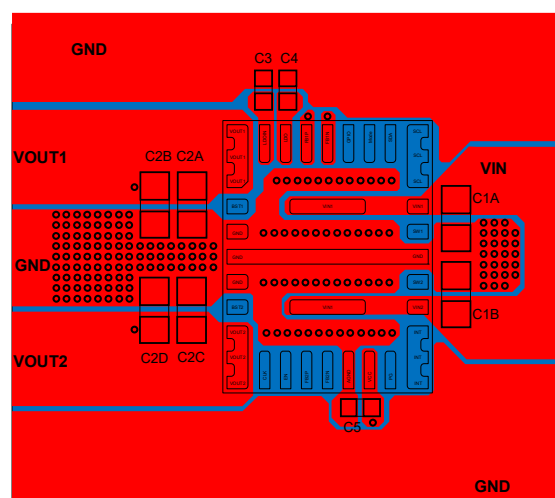
The characteristics of the output capacitor also affect the stability of the regulation.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation, especially for the high switching frequency converter. If the layout is not done carefully, the regulator could show poor line or load regulation or stability issues. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the input capacitor and output capacitor close to VIN, VOUT, and PGND.
2. Place the ceramic capacitor, especially the small package size (0402) bypass capacitor as close to the VOUT and PGND pins as possible to minimize high-frequency noise.
3. Place the VCC decoupling capacitor close to VCC and AGND.
4. Keep the FB resistor divider as closely as possible to FB.
5. Connect FBxP and FBxN with VOUT and GND via Kelvin connection.
6. It is recommended to use 4-layer PCB.

■ Top Layer ■ Bottom Layer ○ Via



MTP CONFIGURATION

Table 6: 0000 Suffix Code Configuration

ITEMS	BUCK1	BUCK2	LDO
MTP			
Switching Mode	FCCM	FCCM	
VOUT Slew Rate	0.5mV/μs	0.5mV/μs	
VOUT discharge	ENABLE	ENABLE	ENABLE
VOUT OVP	ENABLE	ENABLE	
Valley Current Limit	6.5A	6.5A	
Buck Power OFF Delay	4 CLK cycles	4 CLK cycles	4 CLK cycles
VOUT PG Threshold High	5%	5%	-10%
VOUT PG Threshold Low	-5%	-5%	
VOUT OV Threshold	12.50%	12.50%	
VOUT UV Threshold	-10%	-10%	
PG Delay	0μs		
VIN OVP	ENABLE		
Protection motion	Hiccup		
Over Temperature Threshold	145°C		
Over Temperature Warning Threshold	135°C		
ADC	ENABLE		
ADC Sample rate	2kHz		
Active Voltage Positioning(AVP)	DISBALE		
AVP Gain	2mV/A		
AVP Offset	0mV		
CLK Frequency	2kHz		
CLK Number	16		
MODE Control	ENABLE MODE determine MTP registers		
LOT code	00		
MTP code	00		

Mode0	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	400 mV	FB Voltage=	400 mV	
	CLK Mode	Master Mode				
	Working Mode	Dual Phase				
	Switching Frequency	750kHz		750kHz		
	Buck Power ON Delay	4 CLK cycles		4 CLK cycles		4 CLK cycles
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	0				
	GPIO_CTRL	GPIO is a flex-time control and used as external converter's enable signal				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				
Mode1	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	600 mV	FB Voltage=	600 mV	
	CLK Mode	Master Mode				
	Working Mode	Dual Phase				
	Switching Frequency	1000kHz		1000kHz		
	Buck Power ON Delay	4 CLK cycles		4 CLK cycles		4 CLK cycles
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	1				
	GPIO_CTRL	GPIO is Low				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				

Mode2	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	400 mV	FB Voltage=	400 mV	
	CLK Mode	Master Mode				
	Working Mode	Single Phase				
	Switching Frequency	750kHz		750kHz		
	Buck Power ON Delay	4 CLK cycles		4 CLK cycles		
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	2				
	GPIO_CTRL	GPIO is Low				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				
Mode3	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	600 mV	FB Voltage=	600 mV	
	CLK Mode	Master Mode				
	Working Mode	Single Phase				
	Switching Frequency	1000kHz		1000kHz		
	Buck Power ON Delay	4 CLK cycles		4 CLK cycles		
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	3				
	GPIO_CTRL	GPIO is Low				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				

Mode4	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	600 mV	FB Voltage=	600 mV	
	CLK Mode	Master Mode				
	Working Mode	Single Phase				
	Switching Frequency	750kHz		1000kHz		
	Buck Power ON Delay	4 CLK cycles		4 CLK cycles		
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	4				
	GPIO_CTRL	GPIO is Low				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				
Mode5	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	600 mV	FB Voltage=	600 mV	
	CLK Mode	Master Mode				
	Working Mode	Single Phase				
	Switching Frequency	1000kHz		750kHz		
	Buck Power ON Delay	4 CLK cycles		4 CLK cycles		
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	5				
	GPIO_CTRL	GPIO is Low				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				

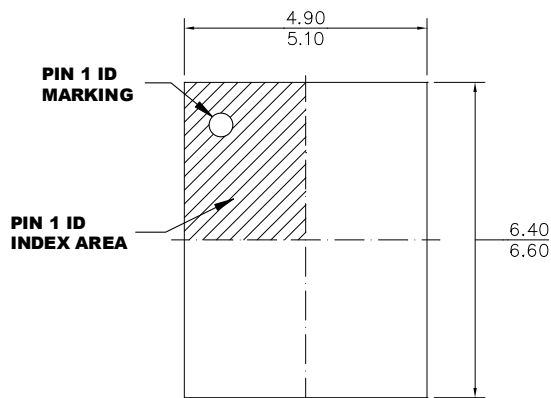
Mode6	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	400 mV	FB Voltage=	400 mV	
	CLK Mode	Master Mode				
	Working Mode	Single Phase				
	Switching Frequency	750kHz		750kHz		
	Buck Power ON Delay	2 CLK cycles		12 CLK cycles		
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	6				
	GPIO_CTRL	GPIO is Low				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				
Mode7	LDO_EN					DISABLE
		External Divider		External Divider		
	Voltage Setting	FB Voltage=	400 mV	FB Voltage=	400 mV	
	CLK Mode	Master Mode				
	Working Mode	Single Phase				
	Switching Frequency	1000kHz		1000kHz		
	Buck Power ON Delay	2 CLK cycles		12 CLK cycles		
	VOUT_SOFTSTART_TIME	2ms		2ms		
	LDO_SOFTSTART_TIME					
	I2C address	7				
	GPIO_CTRL	GPIO is Low				
	LDO_SETTING					
	LDO Power ON Delay					
	GPIO Power ON Delay	0 CLK cycles				

Table 7: 0000 Suffix Code Register Value

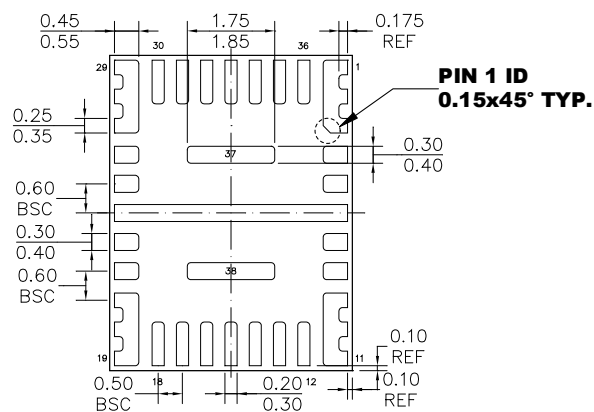
Register	Hex Value	Register	Hex Value	Register	Hex Value
0x41	10h	0x79	0h	0xA1	4h
0x42	D0h	0x7A	4h	0xA2	24h
0x43	32h	0x7B	4Bh	0xA3	10h
0x44	D4h	0x7C	4Bh	0xA4	3Ch
0x45	4h	0x7D	0h	0xA5	0h
0x46	4h	0x7E	CAh	0xA6	4h
0x47	2h	0x7F	4h	0xA7	4Bh
0x48	10h	0x80	4h	0xA8	4Bh
0x49	D0h	0x81	24h	0xA9	0h
0x4A	32h	0x82	24h	0xAA	89h
0x4B	D4h	0x83	3Ch	0xAB	4h
0x4C	4h	0x84	0h	0xAC	4h
0x4D	4h	0x85	4h	0xAD	24h
0x4E	2h	0x86	32h	0xAE	14h
0x4F	12h	0x87	32h	0xAF	3Ch
0x50	3Ch	0x88	0h	0xB0	0h
0x51	0h	0x89	85h	0xB1	4h
0x52	0h	0x8A	4h	0xB2	32h
0x53	E2h	0x8B	4h	0xB3	32h
0x54	80h	0x8C	24h	0xB4	0h
0x55	C5h	0x8D	8h	0xB5	85h
0x56	98h	0x8E	3Ch	0xB6	0h
0x57	4h	0x8F	0h	0xB7	4h
0x58	0h	0x90	4h	0xB8	24h
0x59	81h	0x91	4Bh	0xB9	18h
0x5C	1h	0x92	4Bh	0xBA	3Ch
0x5D	1h	0x93	0h	0xBB	0h
0x5E	C2h	0x94	8Ah	0xBC	4h
0x5F	0h	0x95	4h	0xBD	32h
0x60	80h	0x96	4h	0xBE	32h
0x64	0h	0x97	24h	0xBF	0h
0x70	32h	0x98	2Ch	0xC0	8Ah
0x71	32h	0x99	7Dh	0xC1	4h
0x72	0h	0x9A	0h	0xC2	4h
0x73	C5h	0x9B	4h	0xC3	24h
0x74	4h	0x9C	4Bh	0xC4	1Ch
0x75	4h	0x9D	4Bh	0xC5	3Ch
0x76	24h	0x9E	0h	0xC6	0h
0x77	22h	0x9F	86h	0xC7	4h
0x78	3Ch	0xA0	4h		

PACKAGE INFORMATION

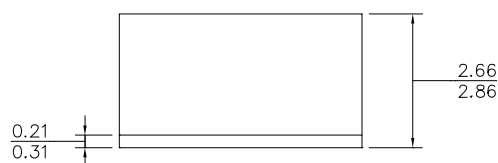
ECLGA (5mmx6.5mmx2.76mm)



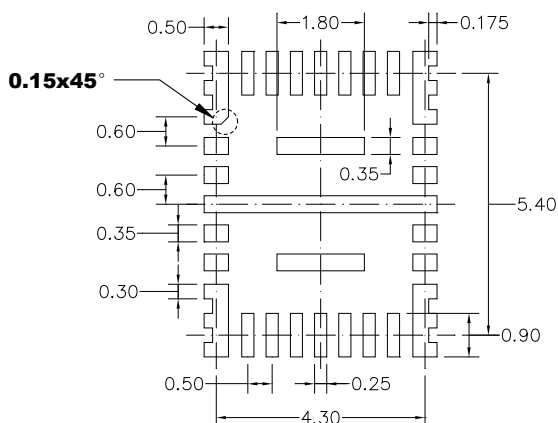
TOP VIEW



BOTTOM VIEW



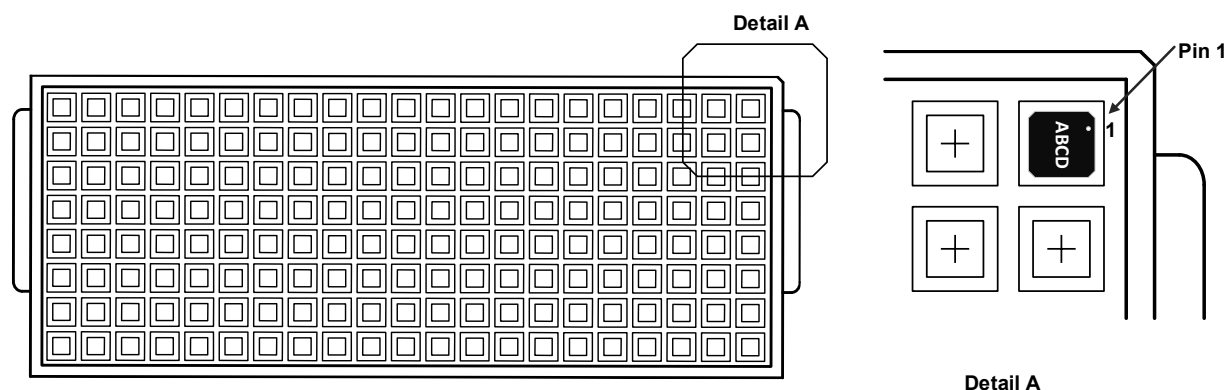
SIDE VIEW



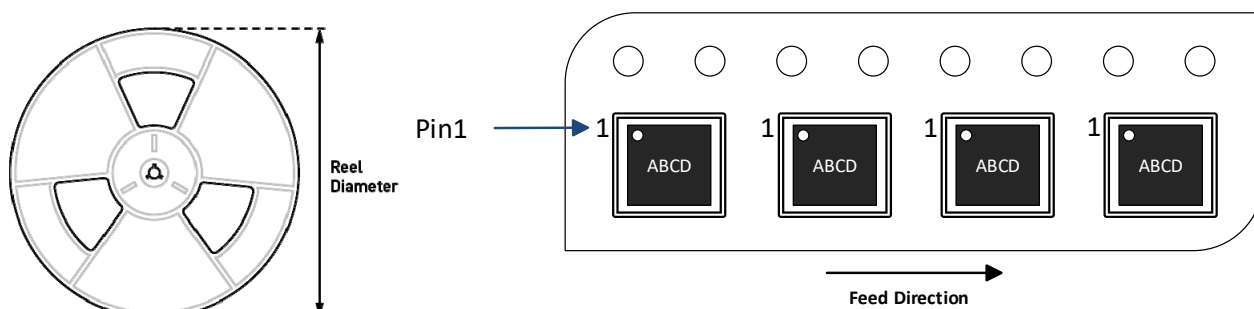
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-303.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION


Note:

This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width and height.


Note:

This is a schematic diagram of Reel. Different packages correspond to different reels with different length, width and height.

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM54522GPB- xxx-T	CELGA (5mmx6.5mmx2.76mm)	N/A	N/A	392	N/A	N/A	N/A
MPM54522GPB- xxx-Z	CELGA (5mmx6.5mmx2.76mm)	1000	N/A	N/A	13 in.	16 mm	8 mm

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